用于CEPC内层顶点探测器的高计数率CMOS像素探测器芯片研制

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On behalf of the CEPC MOST2 Vertex detector design team

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Outline

- Project introduction and TaichuPix chip overview
- Small-scale prototypes design and test results
- Full-scale prototype design and preliminary test
- Summary & Outlook

CEPC Vertex detector requirements

Circular Electron Positron Collider (CEPC) proposed as a Higgs factory.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

  ➔ Impact parameter resolution,

$$\sigma_{r\emptyset} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$

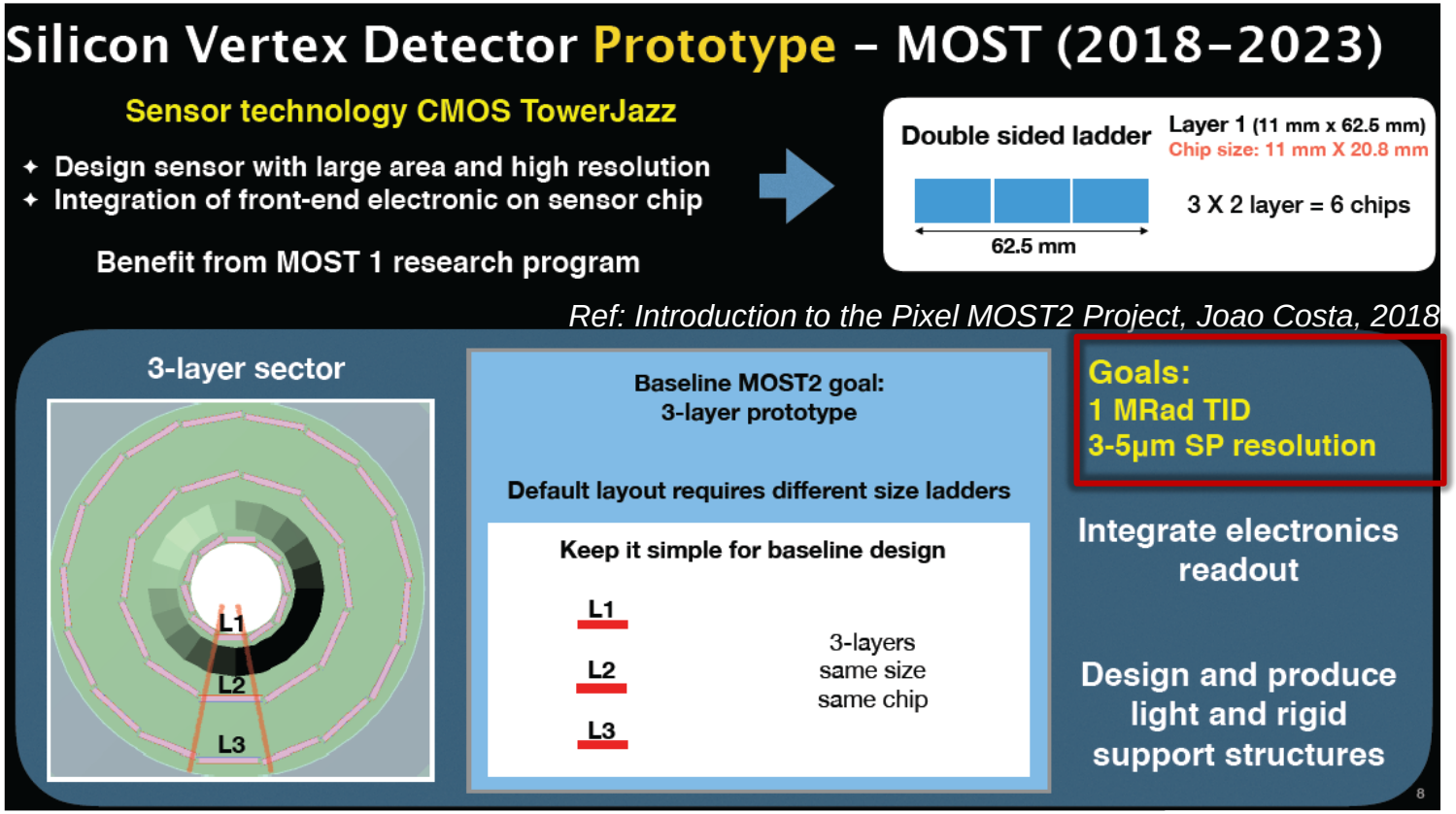
Physics driven requirements		Running constraints	Sensor specifications	
$\sigma_{s.p.}$	2.8 μm		Small pixel	~16 μm
Material budget	0.15% X_0/layer		Thinning to	50 μm
		Air cooling	low power	50 mW/cm²
r of Inner most layer	16 mm	beam-related background	fast readout	~1 μs
		radiation damage	radiation tolerance	≤3.4 Mrad/ year
				≤6.2×10¹² n_{eq}/ (cm² year)

Baseline design parameters for CEPC vertex detector

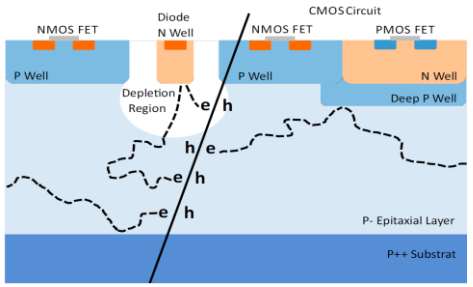
	R (mm)	$\lvert z \rvert$ (mm)	$\lvert \cos\theta \rvert$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

MOST2 project requirements on pixel chip



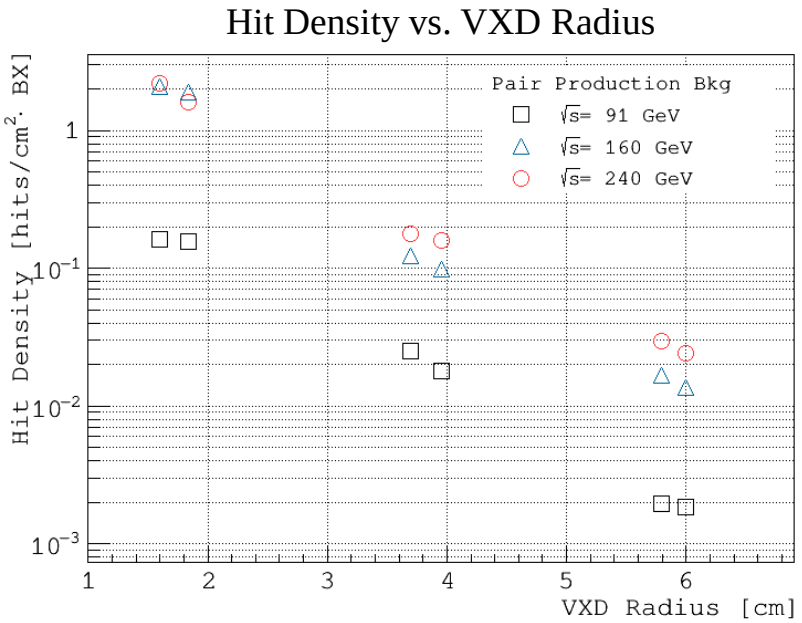
- **Motivation for TaichuPix chip design**
  - Large-scale & full functionality pixel chip
  - Fit to be assembled on ladders with backend Elec. & DAQ



CMOS pixel sensor

Main specs of the full scale chip for high rate vertex detector

- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: **25 ns**
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm

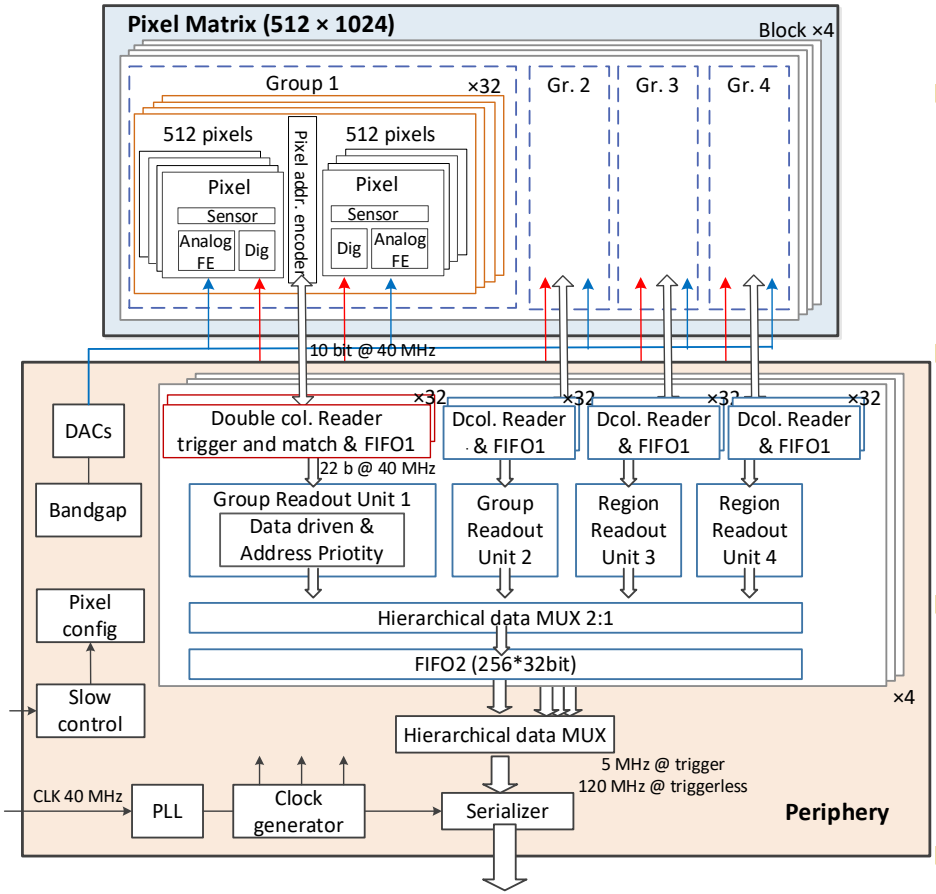


Ref: CEPC Conceptual Design Report, Volume II

For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Date rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	< 500 ns --for 98% efficiency	Chip size	~1.4 cm×2.56 cm

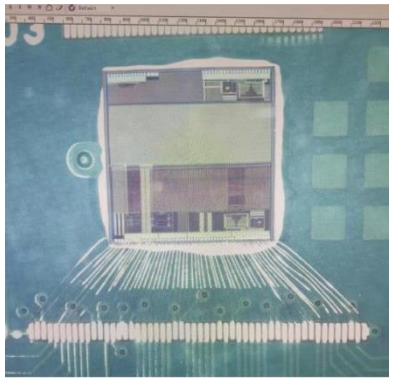
TaichuPix architecture

Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype

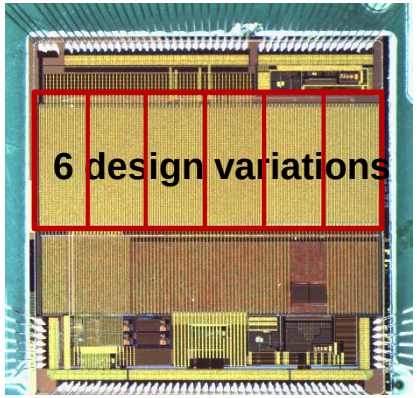


- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - **Time stamp added at EOC**
  - **Readout time**: **50 ns** for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 4.48 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

TaichuPix small prototypes overview



TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

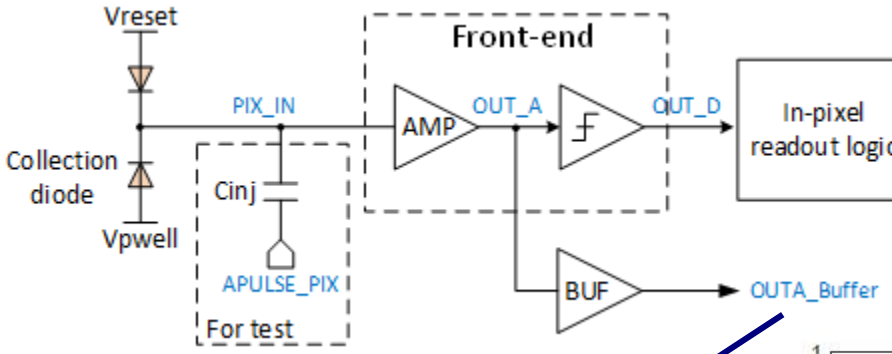


TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

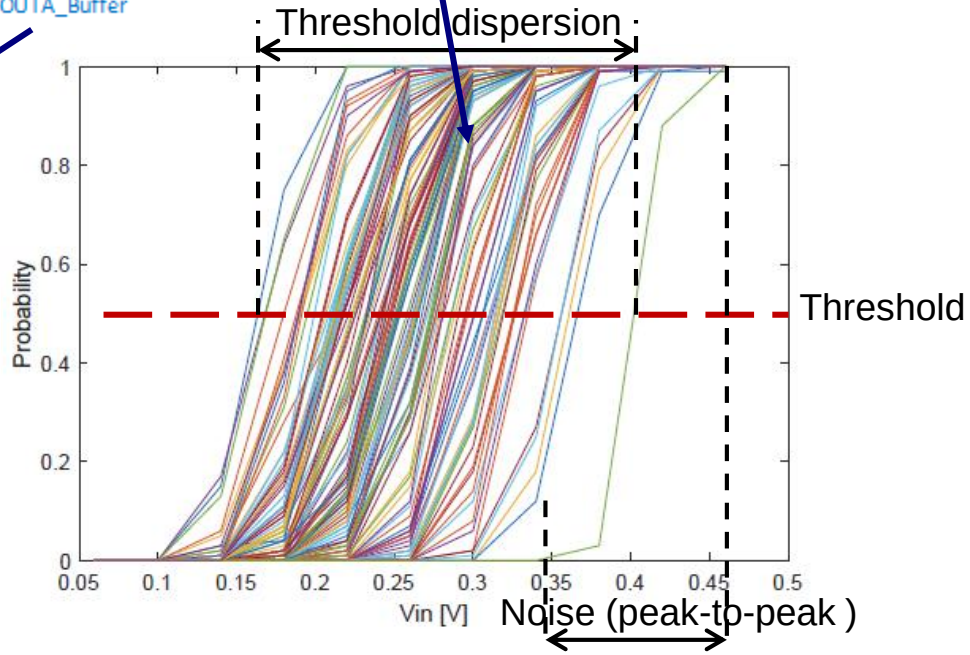
- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06
- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

Electrical test

- **Electrical performance verified by injecting external voltage pulses into pixel front-end**



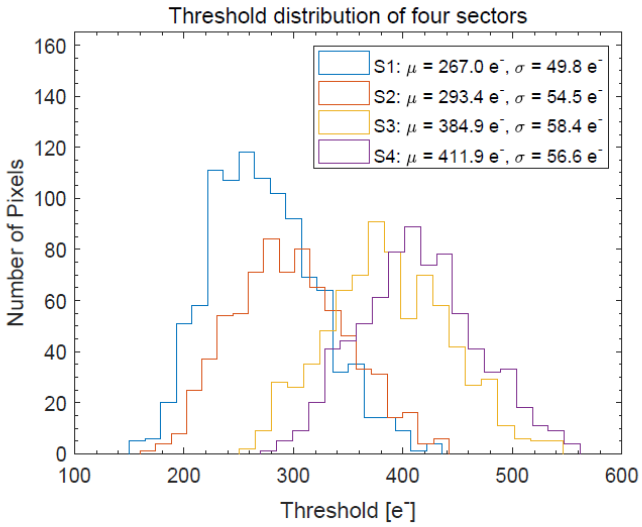
Analog output of a pixel @ Vin = 0.9 V

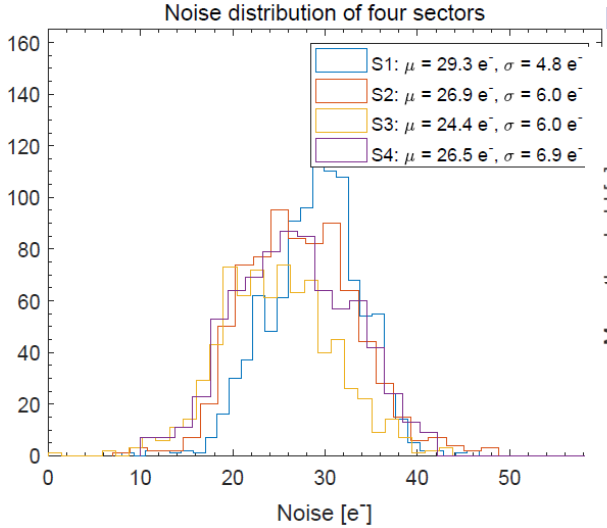


Measured “S-curve” for 128 pixels

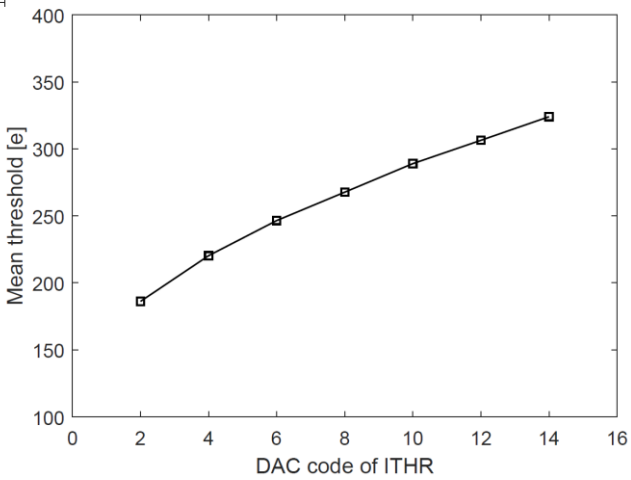
Performance of threshold and noise of TaichuPix2

- Pixel array includes 4 sectors with different transistor parameters/layout for analog front-end, S1 chosen for the full-scale design.
- Threshold can be tuned by changing ‘ITHR’ (a global current bias)





Mean threshold of Sector1 vs. ITHR setting

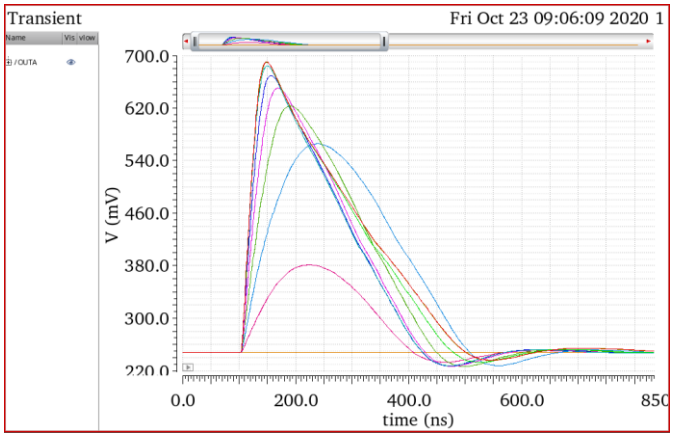


Chip4	Threshold Mean (e^-)	Threshold rms (e^-)	Temporal noise (e^-)	Total equivalent noise (e^-)
S1	267.0	49.8	29.3	57.8
S2	293.4	54.5	26.9	60.8
S3	384.9	58.4	24.4	63.3
S4	411.9	56.6	26.5	62.5

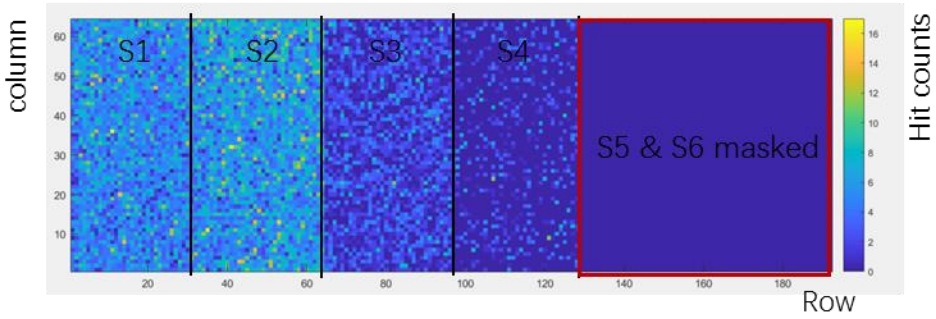
Functionality of complete signal chain of TaichuPix2

- **Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was firstly proved with an X-ray source and a laser source.**

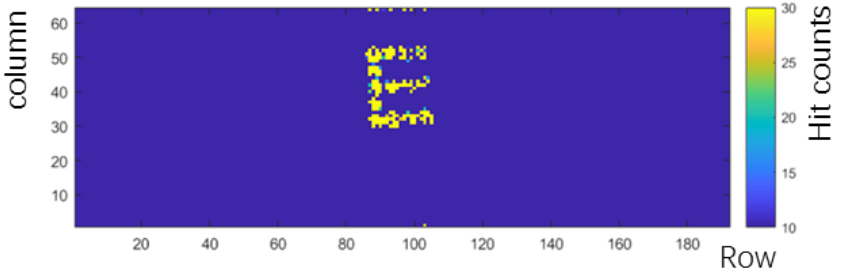
TaichuPix2 response to **X-ray** tube (cutting energy @ 6keV)



Simulated analog output with different input signal



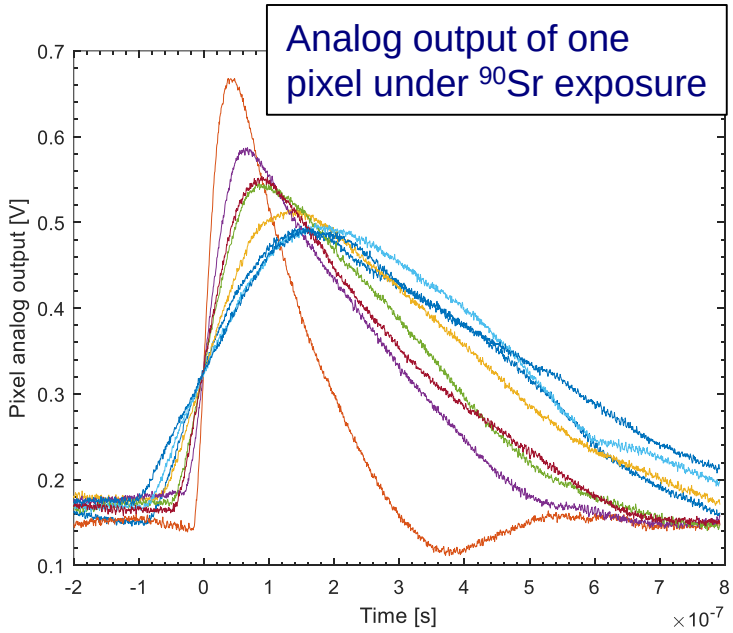
Hit map of the TaichuPix-2 under X-ray from the X-tube voltage of 8 kV for 5 min.

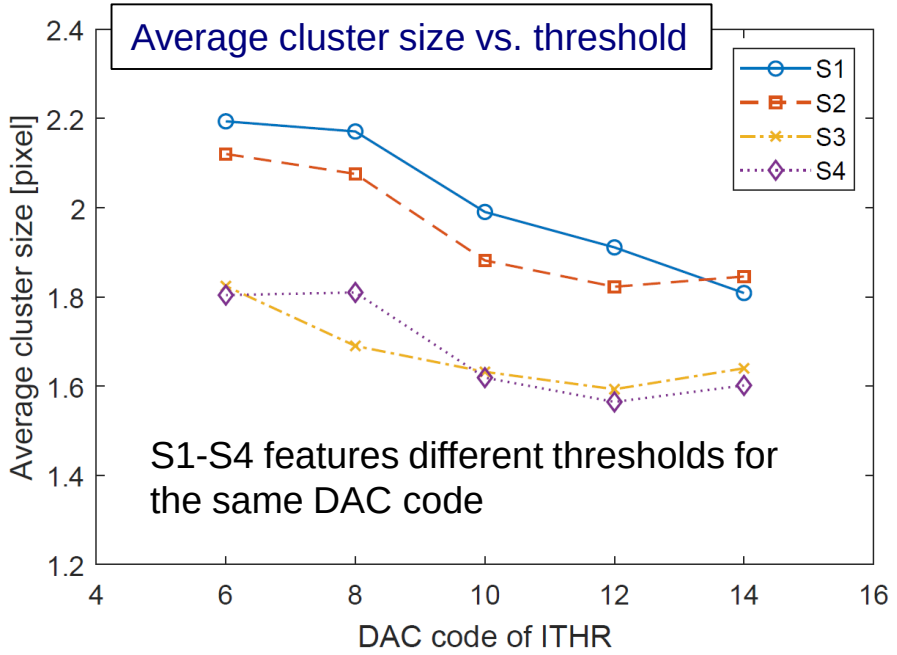


Letter imaging obtained with a 1064 nm laser spot scanning on the TaichuPix-2

TaichuPix2 test with ^{90}Sr

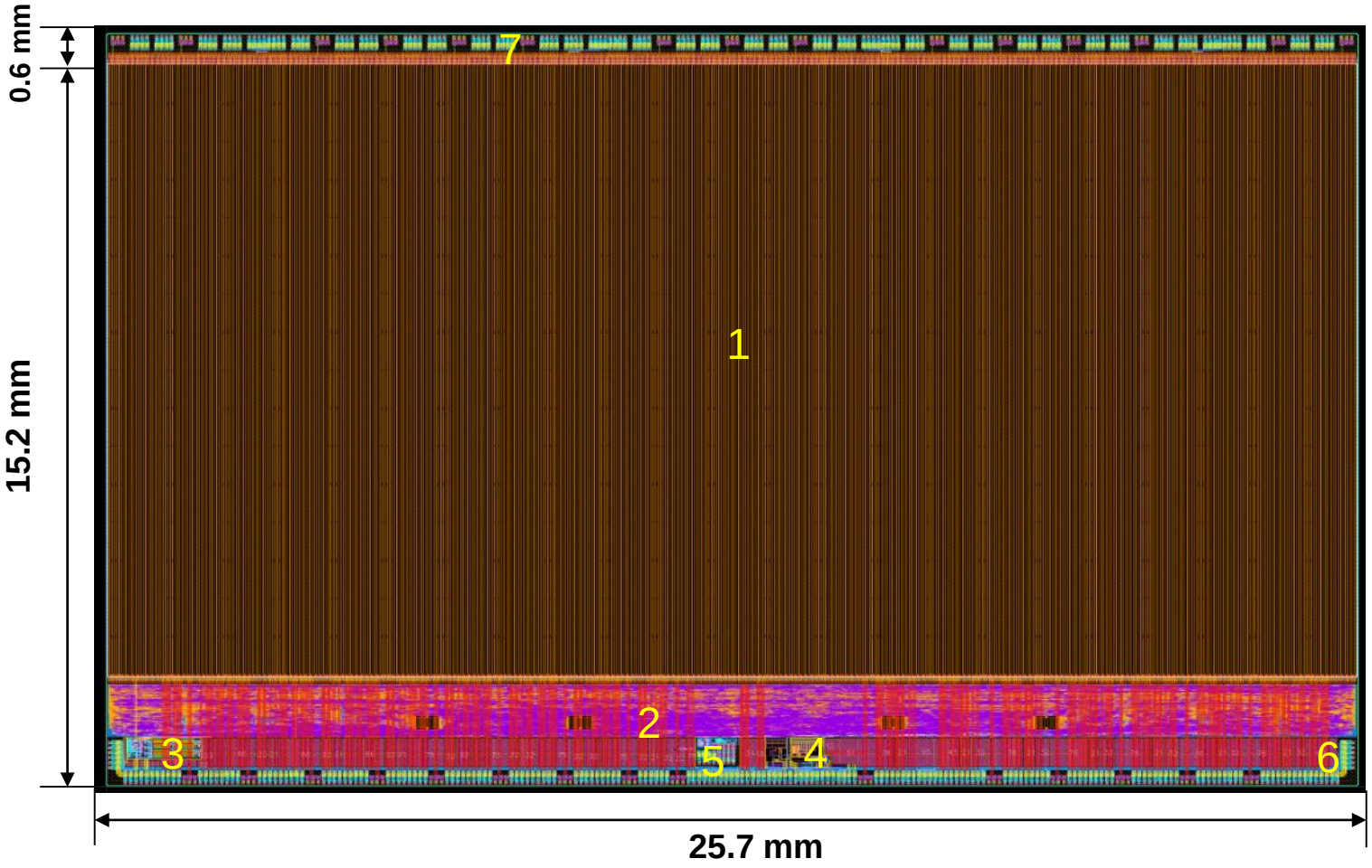
- **TC2 exposure to ^{90}Sr source at different threshold setting (ITHR)**





- Shape and amplitude of analog signal as expected, but peaking time and pulse length larger than simulation.
- Average cluster size decreases with threshold as expected
- **Average cluster size for S1-S4 less than 3 as expected**
  - **Indicates the estimated maximum hit rate (36 MHz/cm^2) reasonable**
  - **Cluster size >1, benefits the spatial resolution (better than $pitch/\sqrt{12}$ = 7.2 μm)**

Overview of the large-scale prototype —— TCPX3



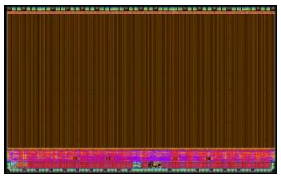
1. Pixel array 1024*512
2. Periphery
3. DAC & Bias generation
4. Data interface
5. LDO (test blocks)
6. Chip inter-connection features
7. Scribe-able top power connection features

- Process: 180 nm CMOS Imaging Sensor process (7 metal layers)
- Pixel cell copied exactly from MPW + scaled logic with new layout
  Periphery + debugged/improved blocks + enhanced power network

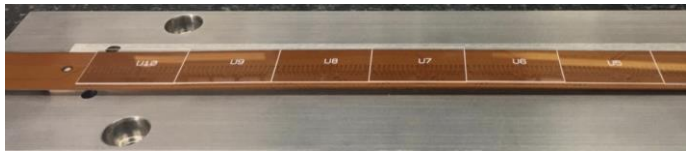
Ladder readout design

- **Detector ladder required for detector assembly**
  - Sensor chips, readout electronics, mechanical support, etc.

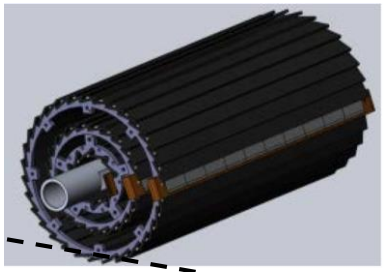
CMOS imaging sensor prototype

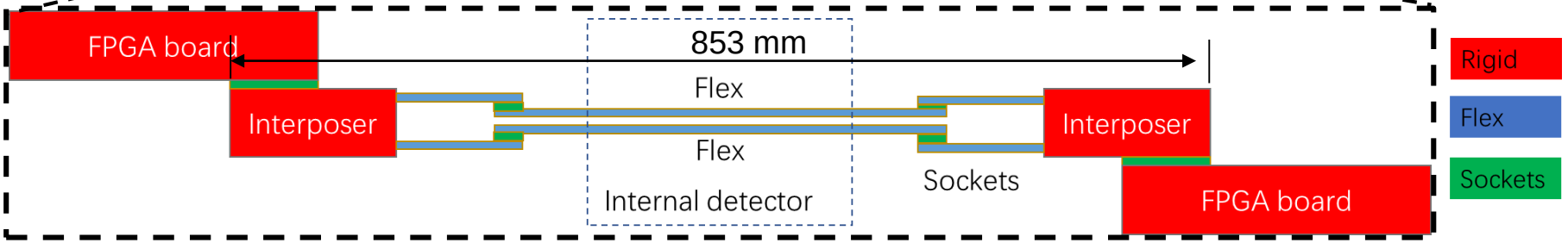


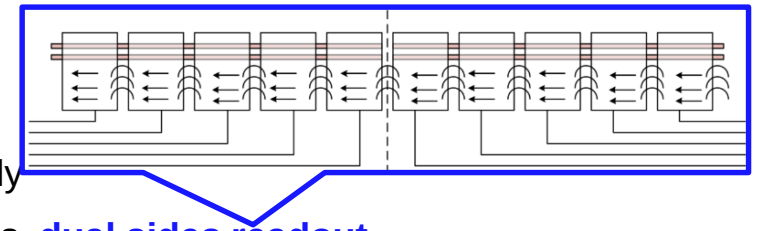
Detector module (ladder) prototype



Full size vertex detector Prototype



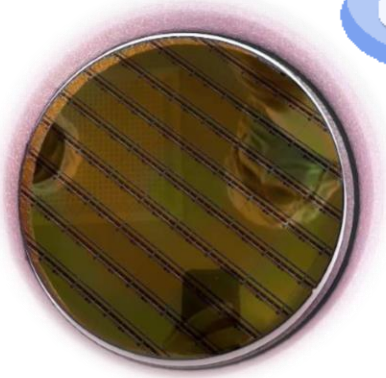




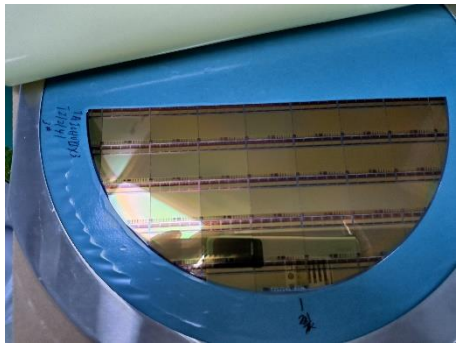
- **Ladder readout structure**
  - Containing 3 boards for easier production & assembly
    - Flex board：Assembled with 10 TaichuPix chips, **dual sides readout**
    - Interposer board：FMC mezzanine rigid and flex board, in production
    - FPGA board：FMC carrier board, available in the lab

Large-scale TaichuPix chip

- **6 TaichuPix-3 wafers arrived at IHEP in July**
  - **One wafer thinned down to 150 μm and diced**
    - Single die size ~25.7 mm × 15.9 mm
    - Next step: thinned down to the final target thickness ~100 μm for ladder assembly

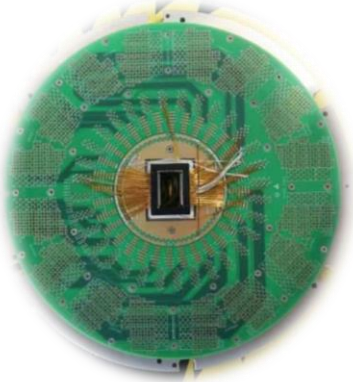


8-inch wafer



Wafer after thinning and dicing

Thickness after thinning

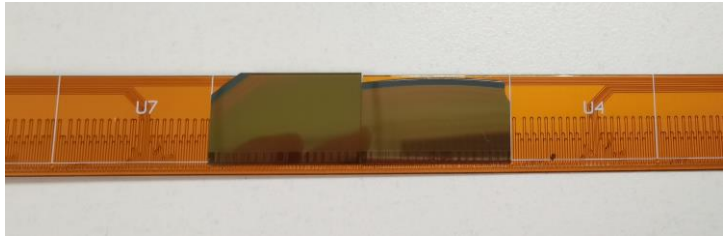


TaichuPix-3 chip on probe card

  - **3 wafers sent to do wafer test on probe-station**

    → chip selecting & yield evaluation

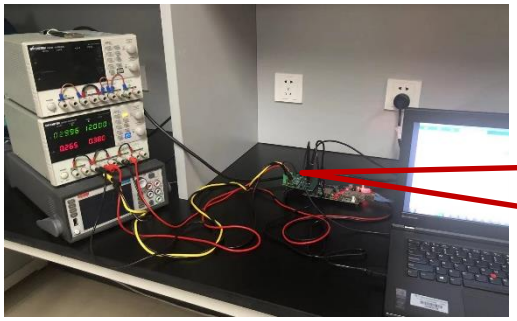
  - **Ladder assembly study under way**
    - First version of flex board produced
    - Jig tool design, assembly tool & process experiments

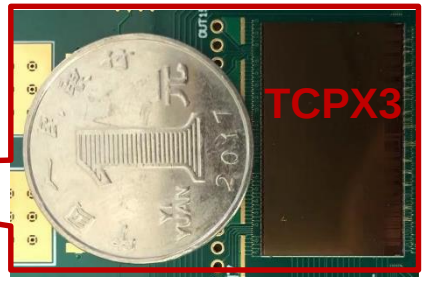


Dummy chip glued to the flex board

Preliminary TaichuPix-3 testing

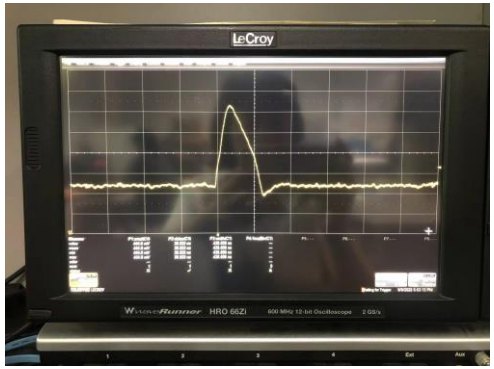
- **Single chip test in progress**
  - Chip bonded on the test board
  - Test system built, preliminary debugging finished





TaichuPix-3 chip vs. coin

- **Preliminary test result**
  - Pixel analog responds normal to an injected voltage
  - Functionality of primary circuit normal
    - Pixel analog + pixel digital + periphery readout + data interface



Analog output of a pixel @ Vin = 1.1 V

	Data valid	Time stamp	Column	Row	Pattern
2	1	57	63	1023	0
3	1	57	63	1021	0
4	1	57	63	1020	0
5	1	57	63	1019	0
6	1	57	63	1018	0
7	1	57	63	1017	0
8	1	57	63	1016	0
9	1	57	63	1023	0
10	1	57	63	1014	0
11	1	57	63	1013	0
12	1	57	63	1012	0
13	1	57	63	1011	0
14	1	57	63	1010	0
15	1	57	63	1009	0
16	1	57	63	1008	0

Digital output data with test input to pixels of col.63

Summary & Outlook

- **Two small-scale TaichuPix chips were developed to perform initial R&D**
  - Pixel pitch 25 μm, readout time 50 ns/pixel
  - Full signal chain & functionality verified with both electrical & radioactive test
- **The first full scale prototype have been fabricated**
  - Die size ~25.7 mm × 15.9 mm, will be assembled on a ladder for a silicon vertex detector prototype
  - Preliminary single chip test proves major functionality normal

- **Outlook**
  - Detailed test on TaichuPix-3
  - Ladder assembly with TaichuPix-3 chips
  - 6 double-sided ladder expected available in November
  - Beam test @ DESY planned in December

Thank you very much for your attention!