Development of HVCMOS-based silicon tracker for CEPC

中国物理学会高能物理分会
HIGH ENERGY PHYSICS BRANCH OF CPS

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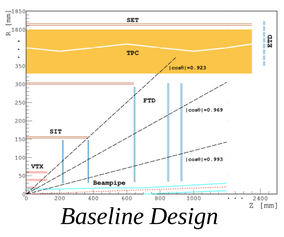
1.Abstract

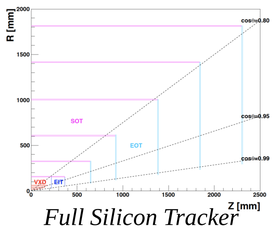
The CEPC physics programs unanimously rely on a high-resolution, fine-pitch, low-material and fast-readout tracking system with a large-area coverage. CEPC has an average bunch spacing of 0.68μs for the Higgs factory operation and 25ns for the Z factory operation with a high luminosity(peak luminosity for Z ~$10^{36}cm^{-2}s^{-1}$). In order to overcome these challenges, It's necessary to use large area monolithic pixel sensor silicon . This technology has been developing fast. The High Voltage Metal-Oxide-Semiconductor(HVCMOS) technology is a promising candidate. Latest development based on ATLASPix3 sensor prototypes will be reported, including efforts to characterising the sensor performance in beamtest using electron beam at DESY.

2.Introduction

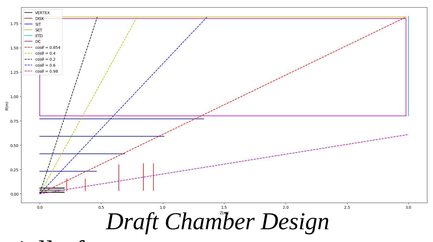
Si Tracker for CEPC



Baseline Design



Full Silicon Tracker



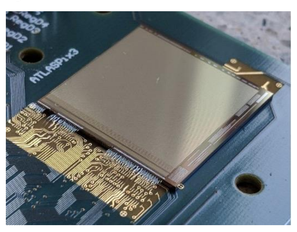
Draft Chamber Design

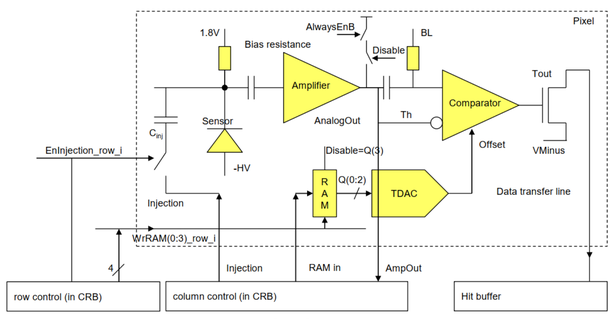
CEPC requires a high-resolution and low-material tracking system especially for momentum measurement ($\sigma_{1/pt} = 2 \times 10^{-5} \oplus \frac{1\times10^{-3}}{p\sin^{3/2}\theta}\ GeV^{-1}$). The three figures above are potential designs for CEPC. Without doubt, CEPC tracker will use large area silicon. Over 70m^2 for silicon + TPC/DC designs, about 140m^2 for full silicon design. HVCMOS is an economical and effective candidate.

Sensor technology

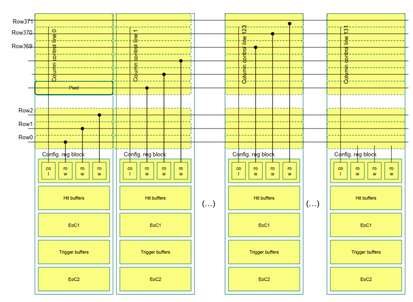
R&D is carried so far with ATLASPix3, a High-Voltage CMOS pixel sensor designed by KIT

- 180nm HVCMOS technology of TSI
- Pixel size 50 × 150 μm^2(or smaller)
- 132 columns × 372 rows (20.2 × 21 mm^2 chip size)
- Material budget for tracker layers: ~0.65% (TPC/Si)/, ~1% (Full Si) X0 / layer
- Binary with ToT(Time over Threshold) information(time bin size 25ns)
- Triggerless(1.6 Gbps with 8b/10b coding) /triggered(1.28 Gbps with 64b/66b coding) readout possible





Pixel schematic



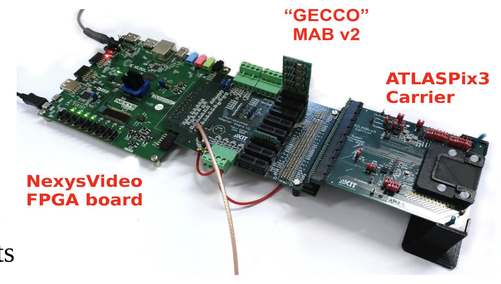
Block scheme of the pixel matrix and column circuits

3.Test Modules

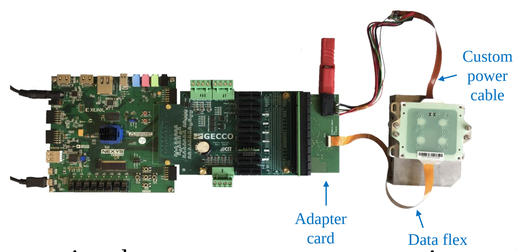
Single chip module

Tuning and readout for single chip

- GEneric Configuration and COntrol System - designed at KIT, produced in China
- LFP-FMC connection to Nexys FPGA, PCIe x16 to DUT, allows extensive tests
- Carrier board for ATLASPix3 single-chip, produced in China



Quad module



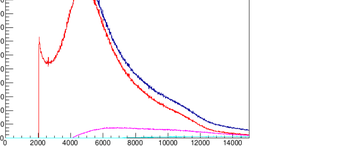
Four chips sharing services by common power connections and configuration lines for large area application

- Data flex and power cables designed by INFN Milano, under verification
- Adapter card for connecting to GECCO

Telescope module

Readout up to four chips. When use triggerless mode : each sensor provides hits and time stamps.
The telescope can be used as a simple tracker

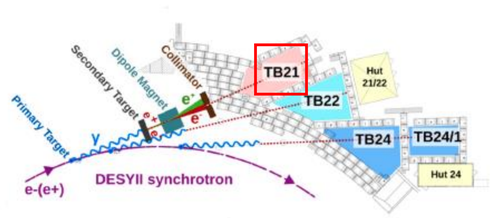
- KIT produced telescope cards carrying 4 sensors with ~2.5 cm spacing



3.Beamtest @ DESY

Experimental setup

- Device: two ATLAS Pix V3.1 telescopes + Quad Module
- Time of test: 4th - 10th Apr, 2022
- Team members from KIT, Lancaster, Bristol, Milano, RAL, IHEP
- Time Alignment: Reset the time stamps and hit count; Send out a check pulse
- Time drift correction: Time drift 1 ms/s - 2 ms/s on average
- UDP, USB readout



Test beam area

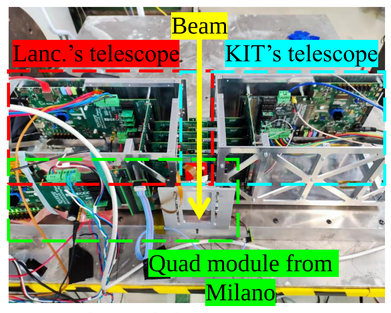
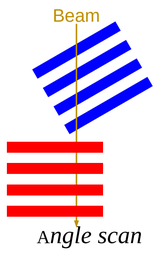


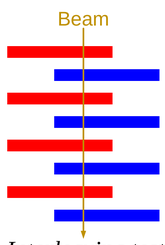
Photo of the beamtest setup

Test programmes

- Energy scan
  - Different beam energy: 6 GeV, 5.6 GeV, 5 GeV, 4 GeV, 2 GeV, 1.4 GeV, 1 GeV
  - To measure the patch scattering with different energy
- Angle scan
  - Different orientations of the telescopes: 0°, 11°, 20.5°, 28°, 40.5°, 45°, 86.5°
  - To measure long track and clusters, also the charge sharing when hitting on the pixel edge and corner
- High Voltage scan
  - -48.6 V, -30 V, -20 V, -15 V, -10 V, -8 V, -6 V, -4 V, -2 V, 0 V
  - To measure the resolution difference against noise on chip due to the high voltage
- Interleaving test
  - Interleave 8 layers from 2 telescopes
  - To investigate track reconstruction between the 2 telescopes



Angle scan

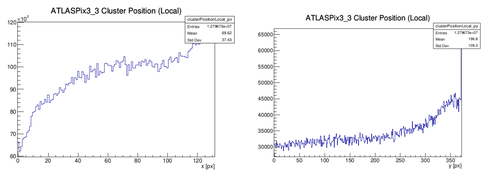


Interleaving test

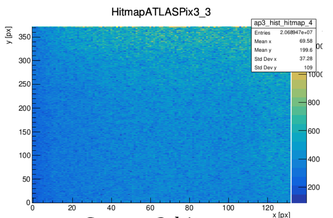
Preliminary Results

- Hits position
  - Raw hit position from one run without masks or noise threshold shows noisy pixels at the edge
  - The beam is not centered, so the hitmap is sparse on the left and dense on the right
  - Hit position histograms correspond to hitmap

- Hits position

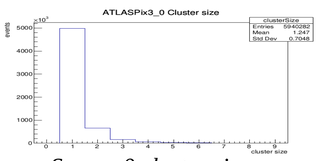


Sensor 3 hits distribution



Sensor 3 hit map

- Cluster width
  - Cluster algorithm has no minimum seed value
  - Similar distribution on all 4 layers
  - 1-pixel clusters dominate

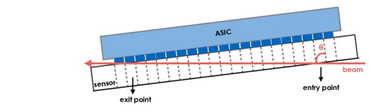


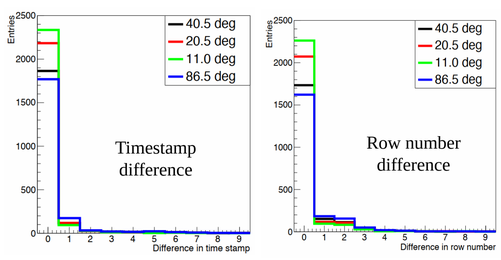
Sensor 0 cluster size

- Cluster charge
  - Time-Over-Threshold calibration gives Landau disctribution of cluster charge with MPV around 5000e
  - Large plateau under study

blue: total; red: 1 pixel; pink: 2 pixels ; cyan: 3 pixels

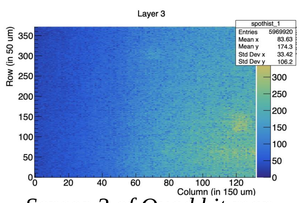
- Track angle



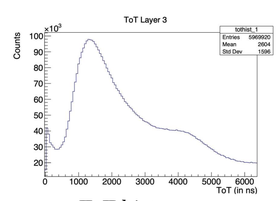


- Expected longer clusters, with same time stamp, same column and long rows or vice versa
- Timestamp difference result: maybe due to time walk
- Row number difference in a single event with same timestamp shows the longer cluster
- Tendency for longer clusters at high angle

- Quad module
  - Pixel map: sample of 10^7 hits
    chip 3 ~370 hits/s
    chip 4 ~250 hits/s
  - ToT histogram is similar with the Telescope's



Sensor 3 of Quad hit map



ToT histogram

◆ A lot of data is waiting to be analyzed