Study of the Single-Event Effect on the SALT Chip

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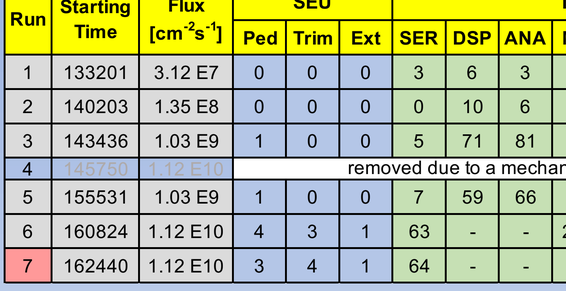
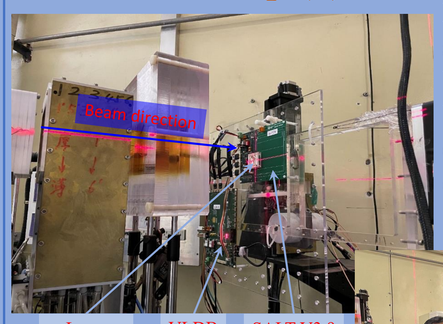
Introduction

- **UT**(Upstream Tracker) is a new silicon tracker in LHCb upgrade to replace the old tracker TT.
- It has 4 layers, each layer consists of 16/18 staves, and each stave consists of 14/16 hybrids.
- **SALT** (Silicon ASIC for LHCb Tracker) is the front end readout ASIC of the UT system.



Test Beam Setup (1)



Main equipment
a) 1 SALT board + 1 VLDB board
b) 1 LinuxPC
c) 1 MiniDAQ
d) 1 Raspberry Pi3 computer

The Features of Beam	
Size	2.0×2.0cm²
Energy	100MeV
Flux	3×10^{7}–$10^{10} p/cm^2/s$
Uniformity	90%

Run	Starting Time	Flux [cm⁻²s⁻¹]	SEU			TMR						
			Ped	Trim	Ext	SER	DSP	ANA	MIS	TFC	MEM	GLB
1	133201	3.12 E7	0	0	0	3	6	3	0	4	0	28
2	140203	1.35 E8	0	0	0	0	10	6	4	5	0	59
3	143436	1.03 E9	1	0	0	5	71	81	17	25	7	-
4	145750	1.12 E10	removed due to a mechanical issue									
5	155531	1.03 E9	1	0	0	7	59	66	17	38	2	-
6	160824	1.12 E10	4	3	1	63	-	-	214	-	56	-
7	162440	1.12 E10	3	4	1	64	-	-	x	-	51	-

- Calibration with a Faraday cup was performed for each intensity value.
- A run lasts 600s. Total 7 runs were taken. In the last run the Kill Mask was disabled, to test ADC readout.
- The total fluence for SEU test is 1.48×10^{13} cm^{-2}, 45.5% with KillMask disabled.

Register configuration & Rate of SEUs

- SALT V3.9 was configured to a normal running condition.
- All TrimDAC, Pedestal, KillMask & InjectMask were set to 0×AA. In the last run KillMask = 0×00, so as to read out ADC value from all channels.

Address	Number	Value	Function
206-285	128	0×AA	TrimDAC
115-194	128	0×AA	Pedestal
105-114	16	0×AA	Kill Mask
307-316	16	0×AA	Inject Mask
205	1	0×AA	Global TrimDac
286-287	2	0×AA	TestChan TrimDAC

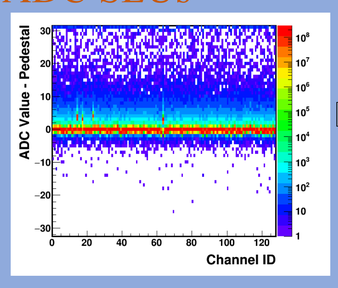
- Here are all SEUs in the Configuration Registers.

Run	Regi	Vset	Vnew	Nbit	Ch
3	154	AA	00	4	3F
5	190	AA	8A	1	7B
6	26F	AA	8A	1	69
	144	AA	08	3	2F
	14F	AA	A0	2	3A
	26D	AA	A2	1	67
	214	AA	A2	1	0E
	14D	AA	00	4	38
	11E	AA	00	4	09
	114	AA	00	4	-
7	245	AA	88	2	3F
	217	AA	8A	1	11
	130	AA	00	4	1B
	182	AA	02	3	6D
	214	AA	80	3	0E
	204	0C	08	1	-
	21D	AA	82	2	17
	172	AA	00	4	5D

Chronological order

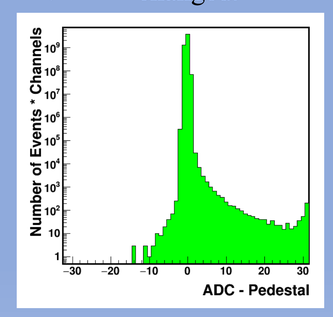
- The SEU rate of the per channel TrimDAC register.
  a) Total 7 register changes ⇒ cross section = 4.7×10^{-13} cm^2.
  b) SEU rate in the UT innermost region = 2.8×10^{-6} Hz.
  c) SEU rate if the whole UT uses SALT V3.9 = **1.2 / hour** TrimDAC changes.
- Pedestal register SEU rate ⇒ **1.6 / hour** Pedestal changes.

ADC SEUs



Flux = 1.12×10^{10} cm^{-2}s^{-1}

~140 M NZS events, remove channels **14,17,23,& 63** that TrimDAC registers changed.



ADC – Ped	Rate
> +7	4.8×10^{-7}
> +5	8.1×10^{-7}
> +3	1.7×10^{-6}
< –3	3.5×10^{-8}
< –5	9.1×10^{-9}
< –7	4.2×10^{-9}

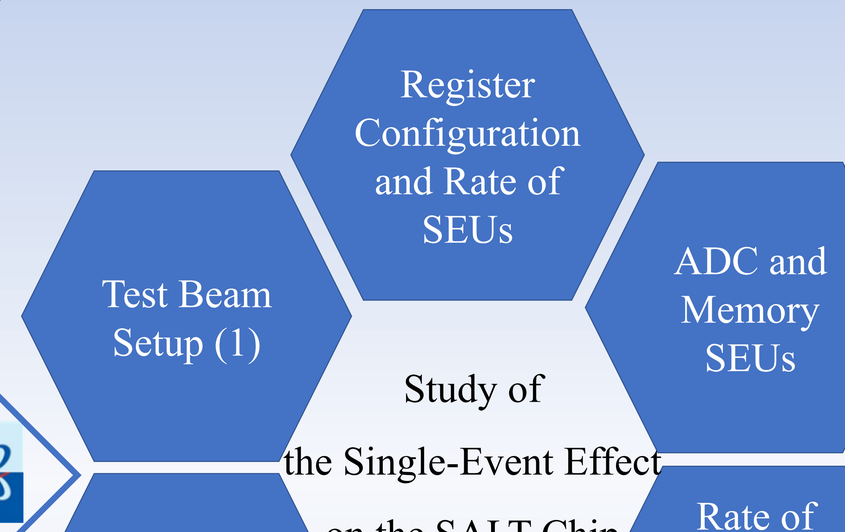
Memory SEUs

163043	
Expected	Readout
3D2 0F0	3D2 0F0
452 0F0	452 0F0
5D2 0F0	5D2 0F0
6D2 0F0	6D2 0F0
752 0F0	652 0F0
852 0F0	852 0F0
9D2 0F0	9D2 0F0
AD2 0F0	AD2 0F0
B52 0F0	B52 0F0
CD2 0F0	CD2 0F0
0111→0110	

163314	
Expected	Readout
452 5D2	452 5D2
6D2 752	6D2 752
852 9D2	852 9D2
AD2 B52	AD2 B52
CD2 D52	CD2 D56
E52 FD2	E52 FD2
0D2 152	0D2 152
252 0F0	252 0F0
3D2 0F0	3D2 0F0
452 0F0	452 0F0
0010→0110	

- The system is stable enough that we are able to check the memory SEU.
- 2 memory SEUs are observed. One has a bit change of "1→0". The other has a "0→1".
- We are curious about the result of memory SEU, so we did another beam test at Dongguan to check more about memory SEU. This will be covered in the following section.

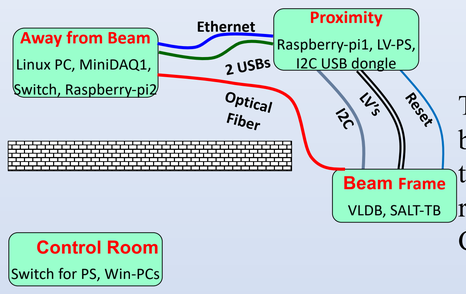
Register SEU Test @CIAE



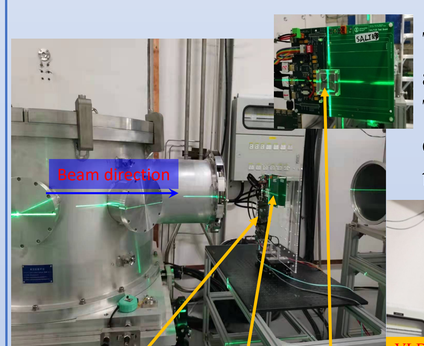
Motivation of radiation test

- SALT V3.5 is vulnerable to radiation in its TrimDAC and Pedestal registers.
  This was first observed at the MGH radiation test on Aug 4th, 2019. It was further confirmed at the PSI radiation test on Nov 3rd, 2019.
- After careful studies, a possible solution was found and implemented in a new design release, SALT V3.9. It needs to be validated in the test.
- **SALT V3.9 was also tested twice.**
  The first was at the **CIAE**(China Institute of Atomic Energy) on Dec 31, 2020.
  The second was at the **CSNS**(China Spallation Neutron Source) from Oct 18 to 25, 2021.

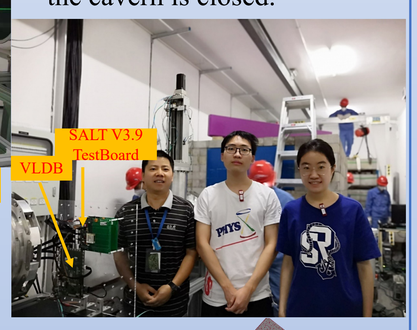
Test Beam Setup (2)



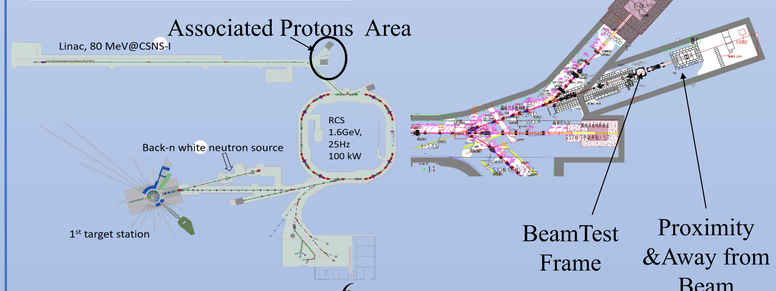
The two layouts are basically similar, except that the latter adds an extra raspberry-pi to reset the CCPC of the MiniDAQ.



The same board that was used at CIAE is tested at CSNS. The 2nd board failed and could not be corrected once the cavern is closed.



The Features of Beam	
Size	2.0×2.0cm²
Energy	80MeV
Flux	$3.4\times10^{9} p/cm^2/s$
Uniformity	90%



Memory SEU Test @CSNS

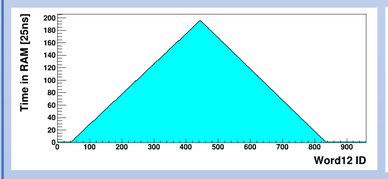
Two Configuration Modes & Calculation Model

- SALT V3.9 was set to a special mode that the ADC value is constant 0x15.

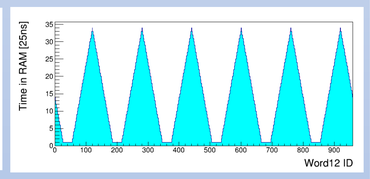
Address	Number	Value	Function
100	1	0x55	ADC use constant value 0x15
103	1	0x40	Output NZS after pedestal subtraction
206-285	128	0x80	TrimDac
115-194	128	0x00	Pedestal
105-114	16	0x00	Kill Mask
307-316	16	0x00	Inject Mask

- In order to calculate the rate of SEUs occurring **during memory** or **data transfer**, we planned two different configurations, difference between which is the time of data in the memory~6 times.

DAQ Configuration:
❑MEP size of N × 480 BXs.
❑TFC sequence= 6*(1 NZS + 79 HeaderOnly). Average time in memory: 81.4*25ns
TFC sequence= (1 NZS + 79 HeaderOnly).Average time in memory: 14.4*25ns



Memory-dominated Mode



Transfer-dominated Mode

- During the process of fetching data, the beam flux was maintained at $3.4\times10^{9} p/cm^2/s$. There are 10 and 7 SEUs observed in the two modes respectively.
- Model

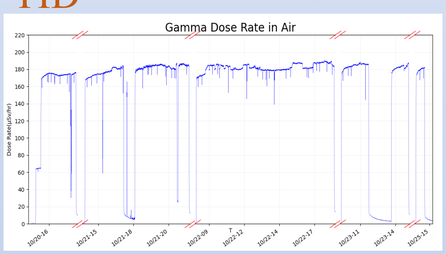
$$N^{RAM} \propto T\times \sigma_{RAM} \times fluence \qquad N_1 = N_1^{RAM} + N_1^{Trans}$$
$$N^{Trans} \propto \sigma_{Trans} \times fluence \qquad N_2 = N_2^{RAM} + N_2^{Trans}$$

Rate of Memory SEUs

The cross section of data during transfer is much larger(~100 times) than that in memory. Take the cross section of **data transfer as the total cross section**.

- The SEU rate of the per channel in data transfer:
  a) cross section $\sigma_{total} = 5.9\times10^{-14} cm^2$.
  b) SEU rate in the UT innermost region = 3.5×10^{-7}Hz
  c) SEU rate if the whole UT uses SALT V3.9 = **3.7 / Day** Data transfer SEUs.

TID



a) @CSNS, fluence: 2.92×10^{14} cm^{-2}, TID~277Mrad
b) @CIAE, fluence: 1.48×10^{13} cm^{-2}, TID~14Mrad
c) ASIC works after the TID ~ 291 Mrad

Special Events

22_092326			
Excepted		Readout	
152	0F0	152	0F0
252	0F0	252	0F0
3D2	0F0	3D2	0F0
452	0F0	452	0F0
5D2	0F0	5D2	000
6D2	0F0	000	6D2
752	0F0	752	0F0
852	0F0	852	0F0
9D2	0F0	9D2	0F0
AD2	0F0	AD2	0F0
B52	0F0	B52	0F0

23_101352			
Excepted		Readout	
555	555	555	555
555	555	555	555
555	B52	555	AD2
CD2	D52	B52	CD2
E52	FD2	D52	E52
0D2	152	FD2	0D2
252	3D2	152	252
452	5D2	3D2	452
6D2	752	5D2	6D2
852	9D2	752	852
AD2	B52	9D2	AD2

- The 1st event was that 000000 were inserted in the middle of the data.
- The 2nd event was that BXID was one less count. Until the next BxReset, the data get right.

Acknowledgements

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