

# Plan for an upgrade Upstream Tracker at LHCb Upgrade II

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## Introduction

LHCb starts data-taking at  $L=2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$  in 2022 with upgraded detector. Upstream Tracker (UT) is located just upstream of the magnet and covers the full detector acceptance.

- Provide **fast track reconstruction** to speed up trigger decision
- Reduce **ghost rate** in long tracks
- Improve **momentum resolution**

But with  $L = 1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  in Upgrade II after 2032, it can not cope with the **data rate** and the **high occupancy** (up to  $\sim 10\%$ ) would significantly compromise the UT performance.

The proposed design for the upgraded UT detector is discussed using **CMOS MAPS technology** and give results from preliminary performance studies, together with an R&D plan.

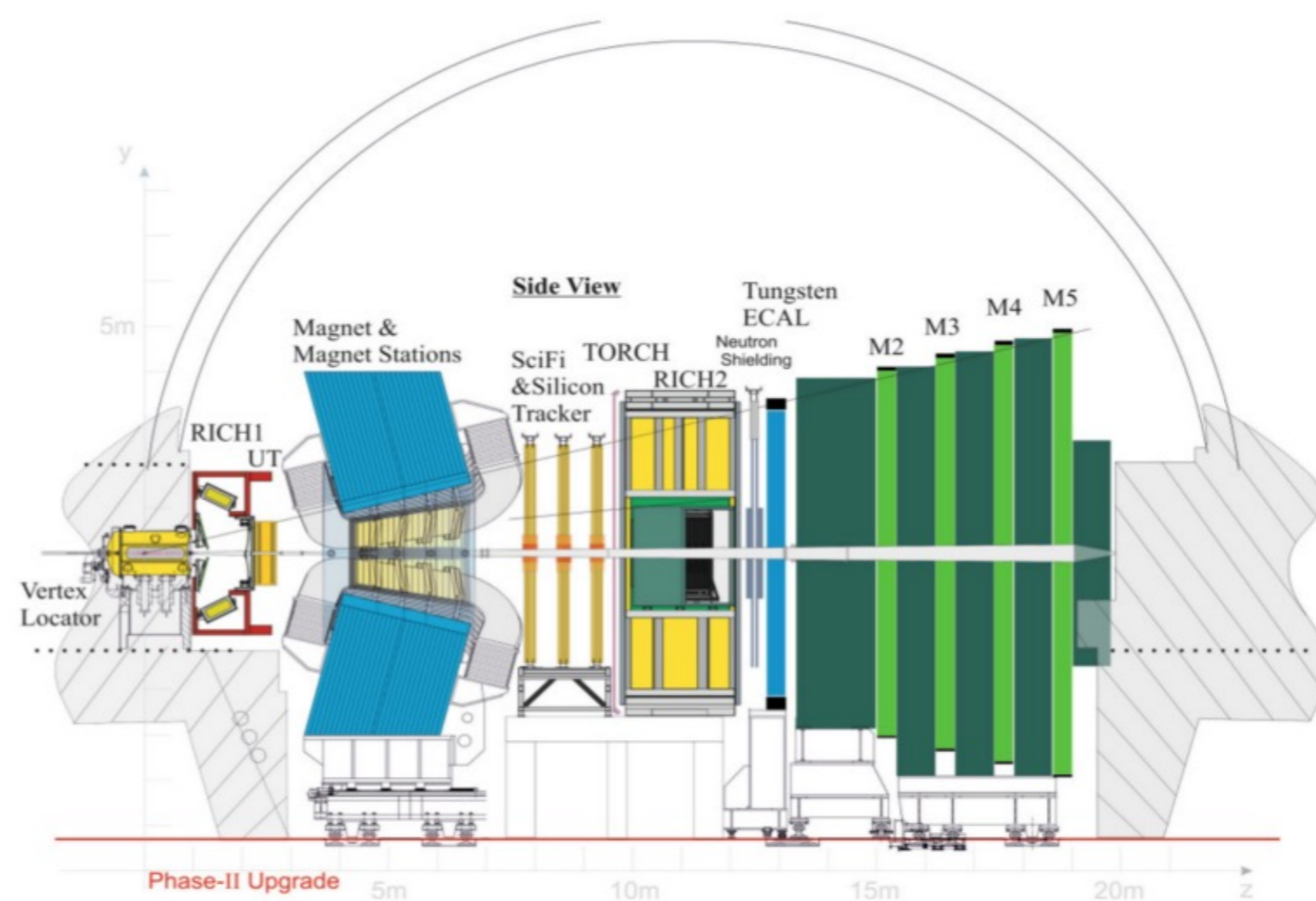


Fig. 1: LHCb Detector at Upgrade II

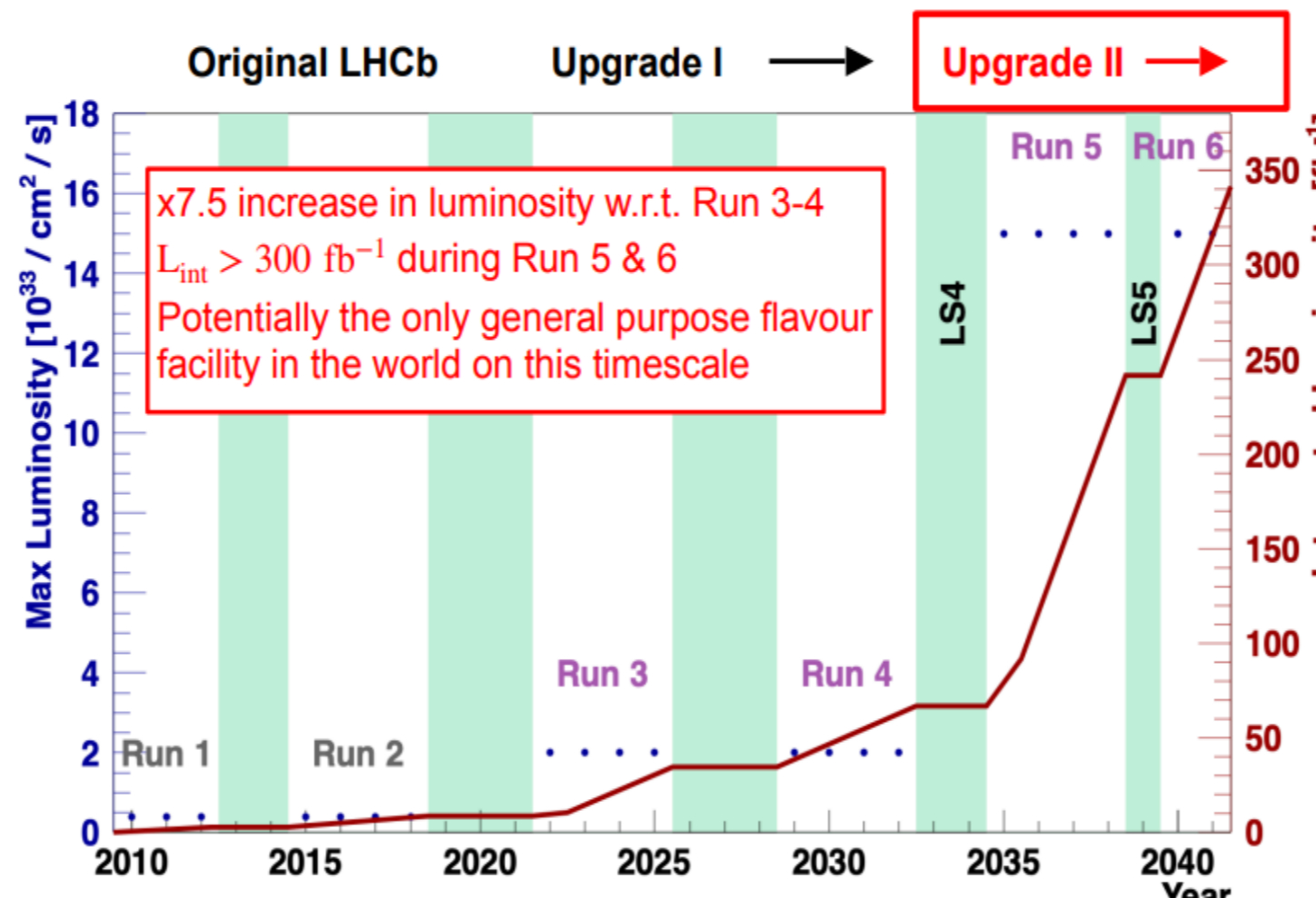


Fig. 2: Upgrade II timeline

## Hit Density Simulation

Performance studies are based on simulation samples generated in Upgrade II conditions using the available Run 3 UT material and design in Geant4.

The two relevant occupancy related quantities for the future UT design are the **mean and maximum hit density per bunch crossing**, respectively.

Figure 3 shows the average hit densities per bunch crossings in p-p and Pb-Pb collisions.

- In p-p running conditions, the average density is **5.9 hits/cm<sup>2</sup>/BX** in colliding bunch crossings, or 4.0 hits/cm<sup>2</sup>/BX in all bunch crossings, while it is **2.9 hits/cm<sup>2</sup>/BX** for colliding Pb-Pb bunch crossings.
- The maximum hit density in a central Pb-Pb events can reach  $\sim$  **52.5 hits/cm<sup>2</sup>**, much larger than in p-p collisions.
- For a pixel size of  $50 \times 150 \mu\text{m}^2$ , the corresponding occupancy rate is  $3.9 \times 10^{-3}$ .

## Silicon Sensor Technology

The ongoing R&D studies indicate that **Depleted Monolithic Active Pixel Sensors** (DMAPS) can be considered as very strong candidates for UT. Other technologies such as LGADs, that add timing capability, are optional choices.

To achieve substantial depletion in the sensing volume and improve the speed and radiation tolerance of the detector, DMAPS implementations follow two different approaches, namely large fill-factor or high-voltage (**HVCMOS**) and low fill-factor or low-voltage (**LVC MOS**).

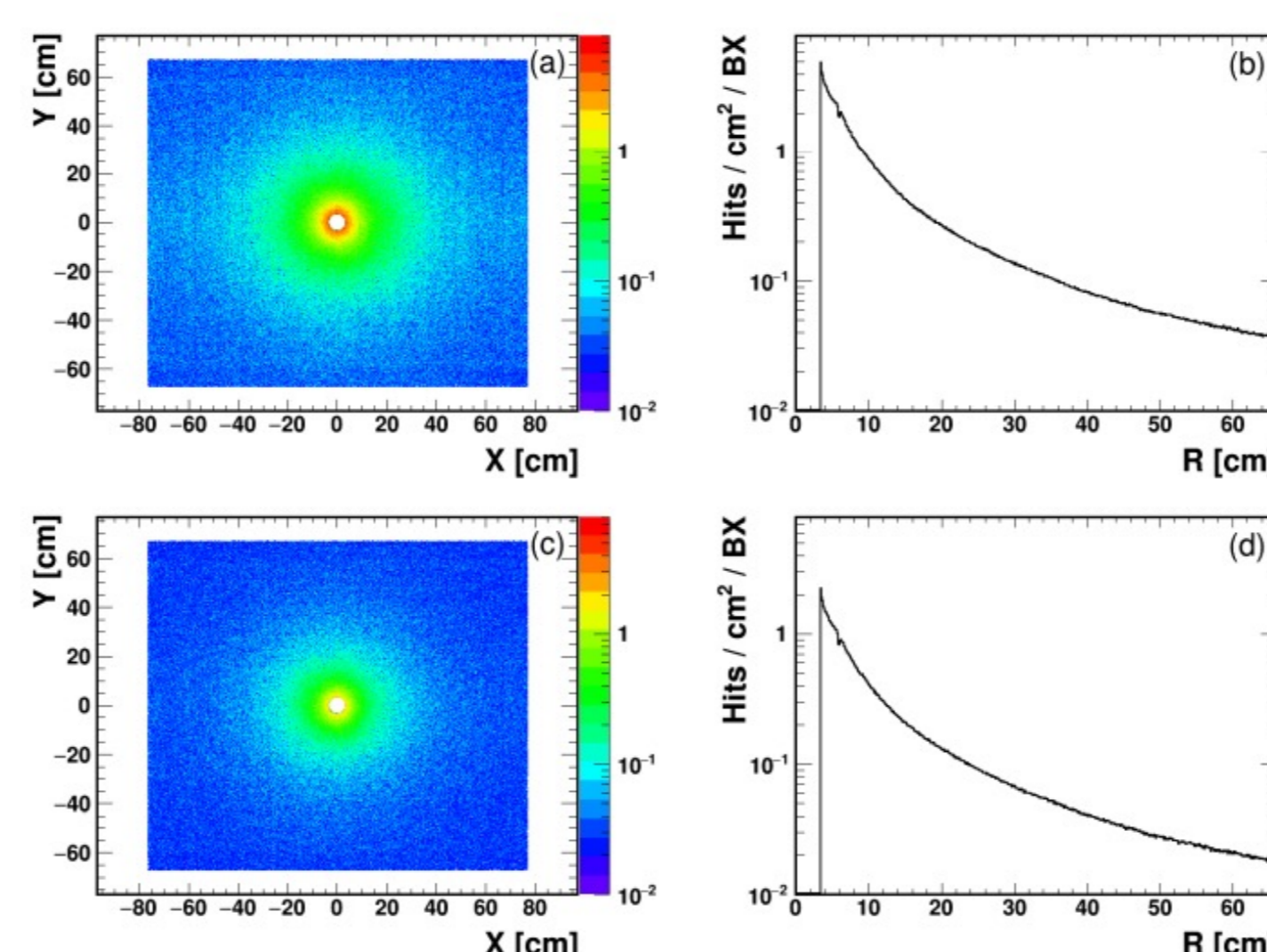


Fig. 3: The mean UT hit density per BX at the first plane per beam-beam colliding bunch in (a and b) the p-p programme, and (c and d) the Pb-Pb programme. All four plots use the same scale for direct comparison. The colour map of the 2-D plots are also shown.

## Consideration on Electronics Design

The UT has a significantly high occupancy, with the hottest chip requiring a data rate of about 9.0 Gbps. In total, **the UT has a data rate of about 6.8 Tbps**.

Fig. 4 shows an illustrative plan, based on simulation studies at the peak luminosity, of how many IpGBT readout links (e-links) will be required on the chips in different regions of the detector.

- The e-links of IpGBT can be set to **1.28, 0.64, or 0.32 Gbps** bandwidth.
- The hottest chip needs at least **8 e-links of 1.28 Gbps** for event data.
- In the outer regions of each plane, **one link of 0.32 Gbps** bandwidth is sufficient. Thus dual-modules can be constructed for 28 sensor chips that share a single IpGBT.
- In total, about **1888 event data IpGBTs** are deployed. An extra **1312 IpGBTs** are used for fast and slow control.

## Detector Layout

**A four-plane detector based on HVCMOS is proposed.** Layout using other MAPS technology like LVC MOS is similar.

A potential detector layout is illustrated in Fig. 5. The basic element from which the overall detector plane is constructed is the stave, which is composed of modules containing the MAPS chips.

- **Fourteen chips in a 7 × 2 array** are interconnected to a flex circuit to form a module.
- The common **HL-LHC radiation tolerant ASIC** for data, timing, trigger and control applications, known as the IpGBT, will be utilized for data concentration and transmission.
- **A total of 36 modules** are mounted alternately on both sides of a supporting bare stave, **in total 12 staves**.
- The inner staves differ in design, with their innermost modules consisting of only  $5 \times 2$  sensor chips each due to the beam hole.

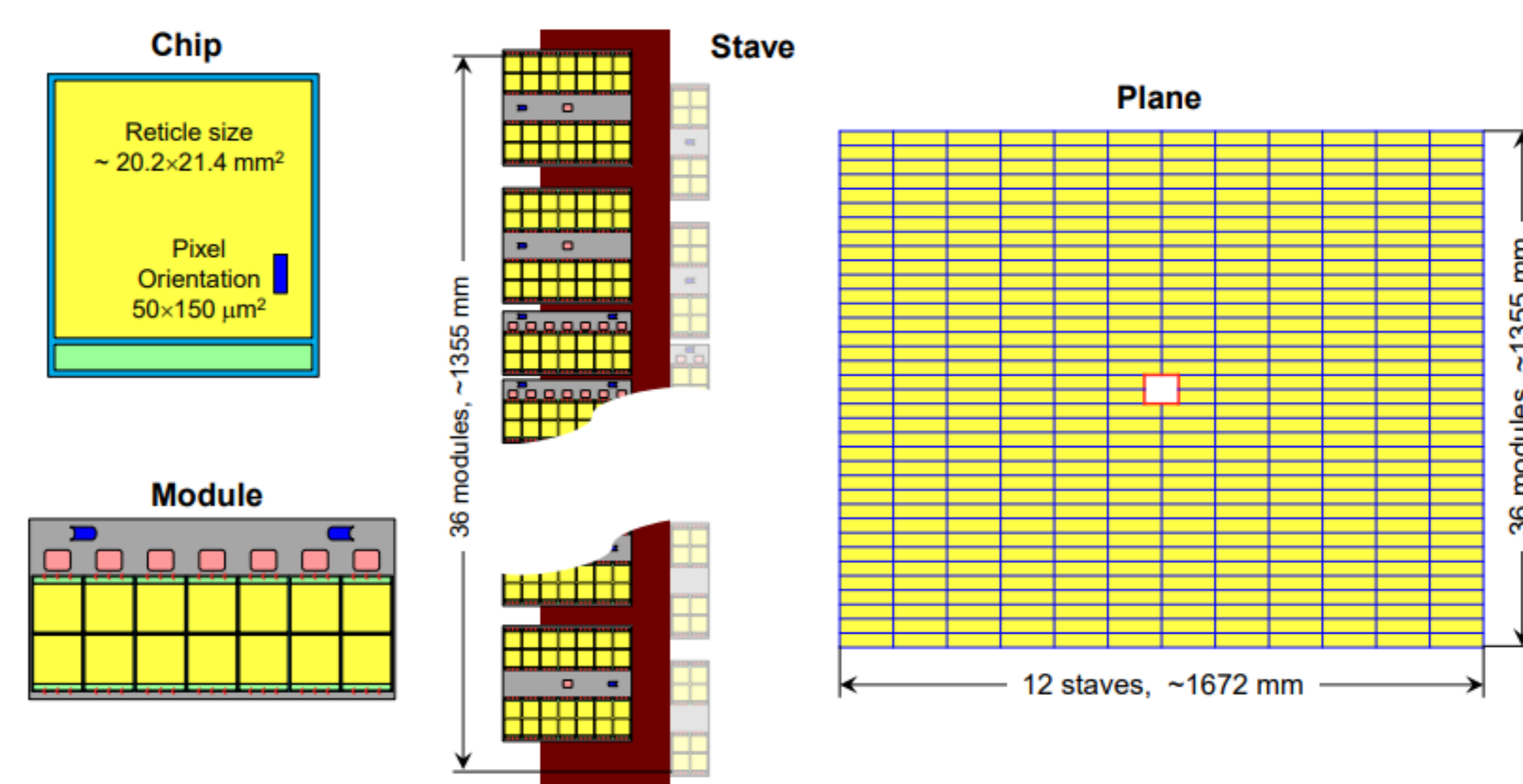


Fig. 5: A possible configuration for the Upgrade II UT detector.

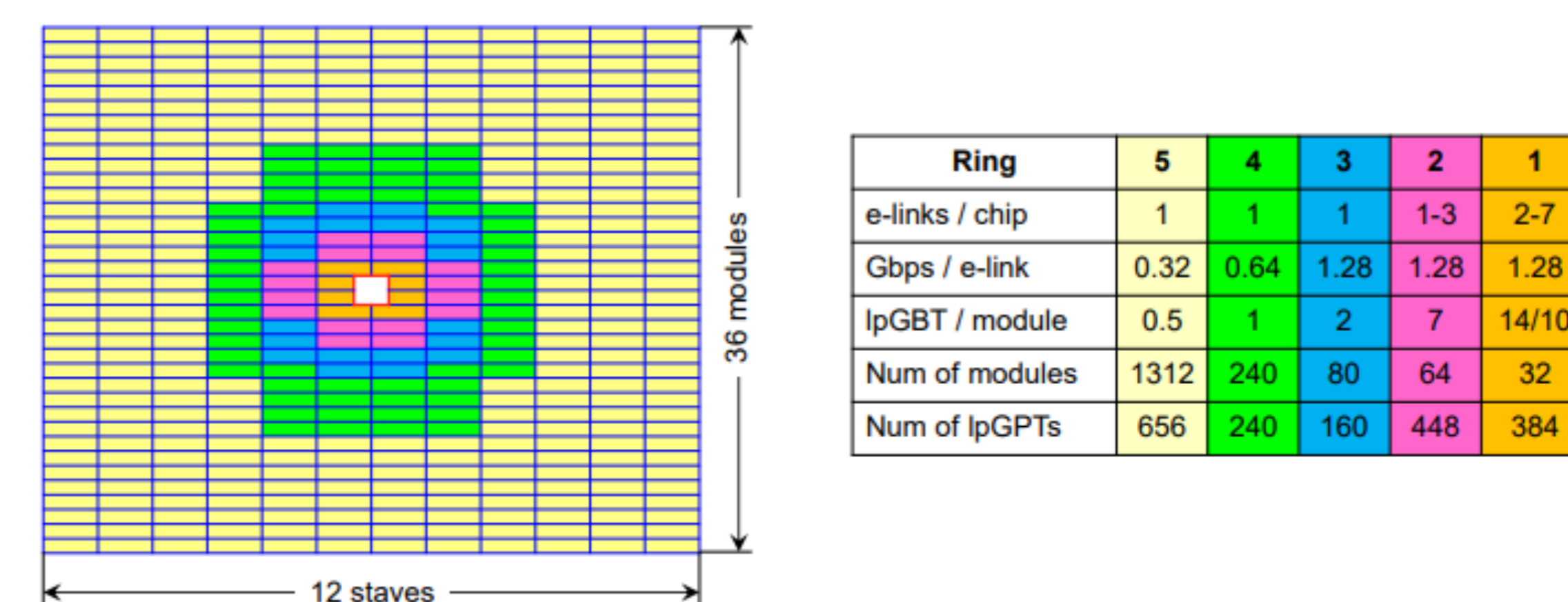


Fig. 4: The IpGBT allocation and configuration plan. Only IpGBTs for event data are listed

## Optimisation Plan

A strong R&D programme on the technology will be pursued over the next period. In parallel, detailed studies are ongoing to **define many aspects of the design**, which include:

- The impact of the VELO-UT momentum resolution on the tracking, especially at low-pT together with the Magnet Stations.
- Assessment of the detector acceptance (especially in the x direction) with respect to the tracking at low momentum associated to the Magnet Stations.
- Optimization of the number and layout of planes
- Assessment of the material budget and multiple scattering requirements.
- The timing performance of the detector, associated to the intrinsic time resolution of the CMOS sensors.
- Study of hit grouping into event packets according to their bunch crossing (BXID) in order to reduce the data rate.
- Assessment of the detector modularity in order to allow an eventual replacement of the innermost modules beyond a given radiation dose.



### Reference and links:

[1] "Framework TDR for the LHCb Upgrade II Opportunities in flavour physics, and beyond, in the HL-LHC era", CERN, Geneva, LHCb Collaboration, CERN (Meyrin)

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