中国科学院高能物理研究所
Institute of High Energy Physics Chinese Academy of Sciences

The Upstream Tracker at LHCb

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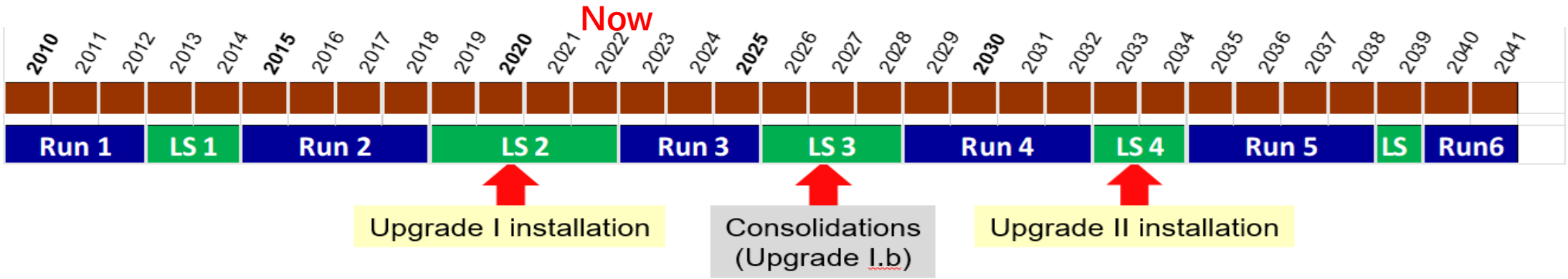
LHCb Upgrade

- LHCb is one of the four major experiments at the Large Hadron Collider (LHC)
- It is currently in Phase I upgrade :
  - Hardware trigger is removed; Front-end electronics will enable **40MHz** readout
  - Designed to cope with **a factor of five increase** in luminosity $L = 4 \times 10^{32} \rightarrow 2 \times 10^{33} cm^{-2} s^{-1}$
  - Most subdetectors are installed and being commissioned
  - Full installation expected by the end of the year

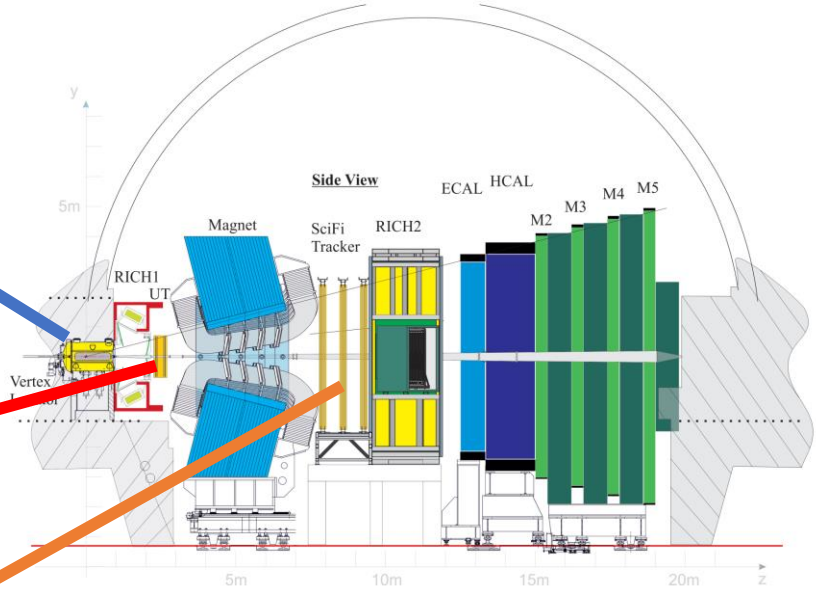


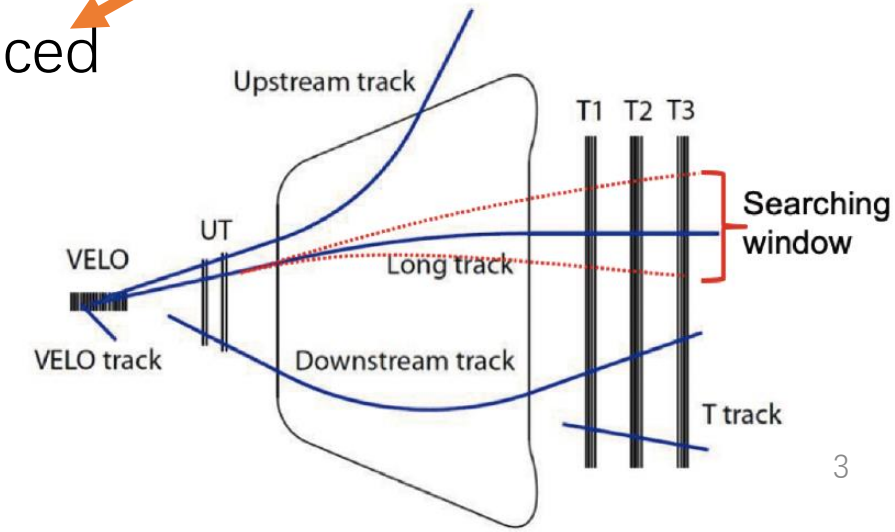
Quan Zou's Poster: More details of Upstream Tracker in Upgrade II

Xiaojie Jiang's poster: HVCMOS sensor option for Upgrade II

Tracking in LHCb Upgrade I

- The **Vertex Locator (VELO)** around the interaction region use a lightweight hybrid pixel detector.
- The tracking station in front of the LHCb dipole magnet will be replaced by new silicon strip detector, **Upstream Tracker (UT)**.
- The tracker stations behind the magnet is replaced by a **Scintillating Fiber Tracker (Sci-Fi).**





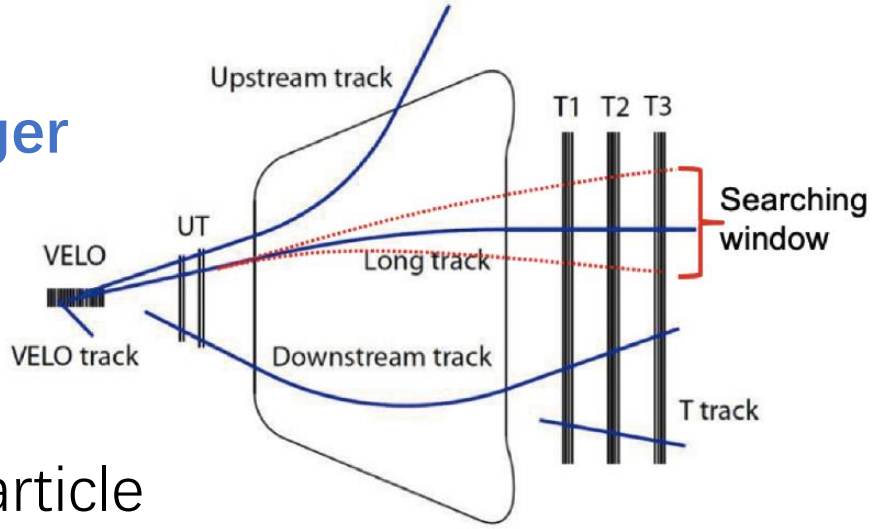
LHCb tracker upgrade TDR. CERN-LHCC-2014-001.
LHCb VELO upgrade TDR. CERN-LHCC-2013-021.

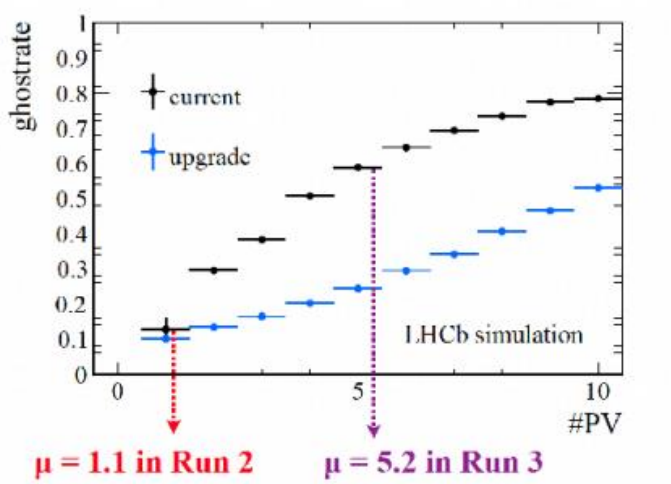
Chinese groups contributing to UT

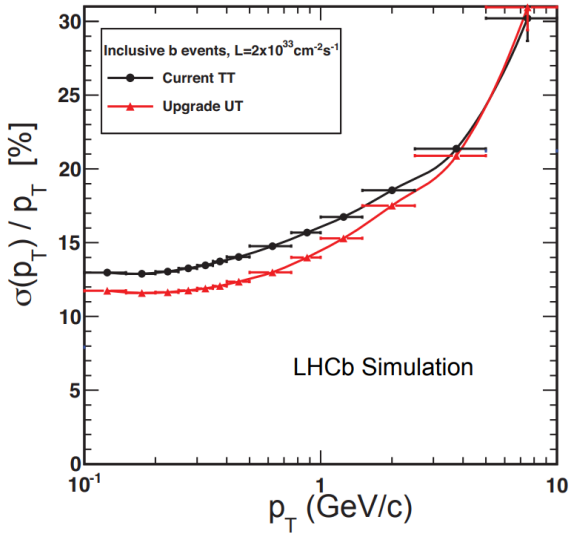
- 中国科学院高能物理研究所 (IHEP)
- 湖南大学 (HNU)
- 华中师范大学 (CCNU)
- 兰州大学 (LZU)
- 清华大学 (THU)
- 中国科学院大学 (UCAS)

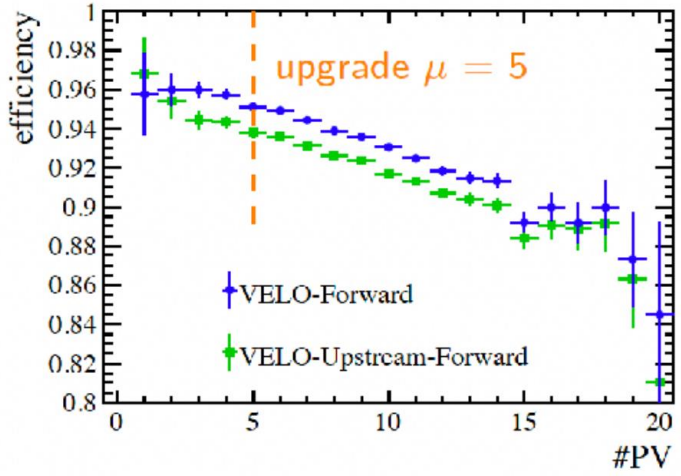
UT role in LHCb tracking

- Provide fast track reconstruction to **speed up trigger**
  - Tighten searching window in Sci-Fi
- Reduce **ghost rate** in long tracks
- Improve **momentum resolution**
- Increase **reconstruction efficiency** of long lived particle



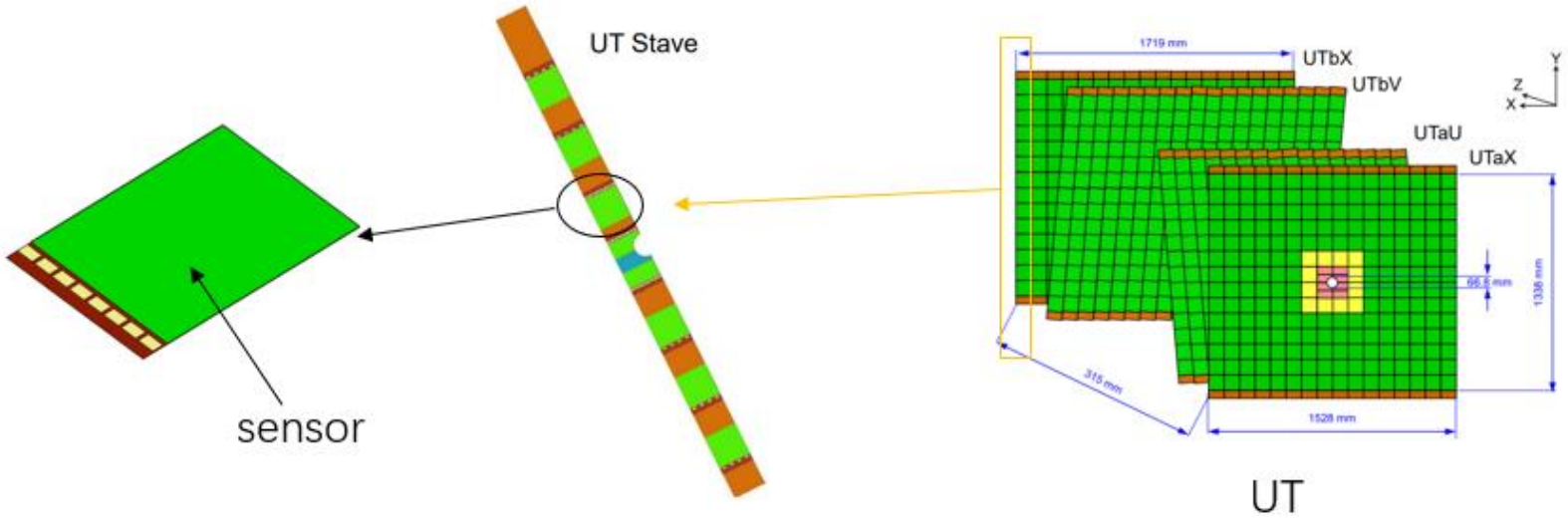






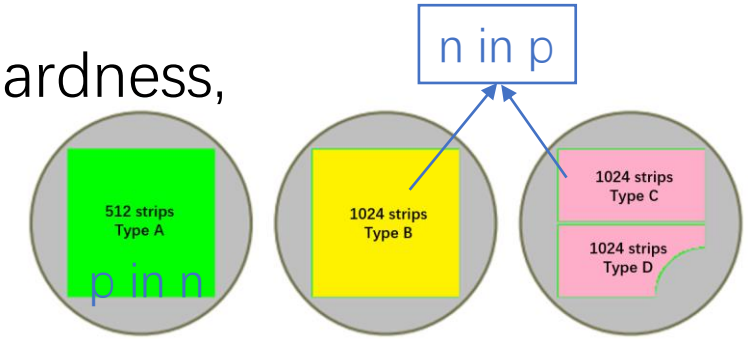
UT overview

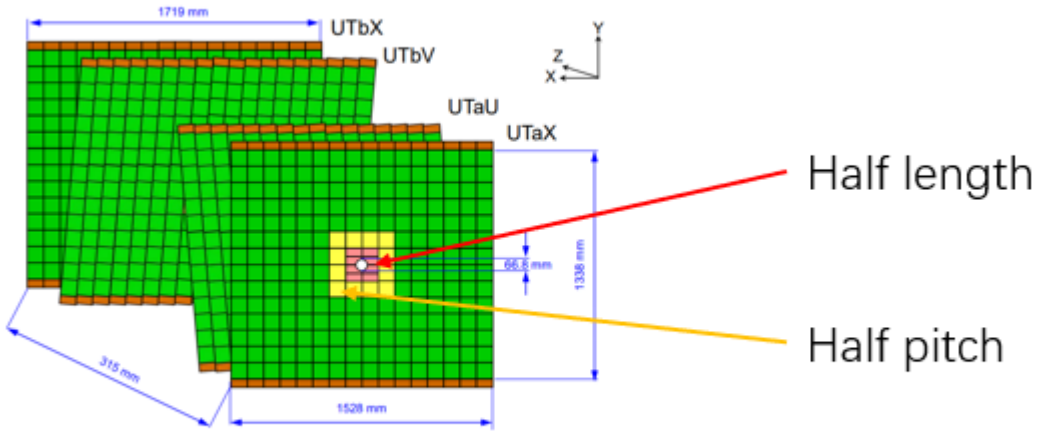
- Geometric configuration:
  - Four planes, each plane consists of 16/18 staves
  - Each stave bears 14/16 silicon strip sensors
- Improved coverage and segmentation
- Readout at 40MHz by SALT ASICs in the sensor proximity



UT sensor

- Outer region uses p-in-n sensors with strip $187.5\mu m \times 98mm$
- Inner region uses n-in-p sensors with better radiation hardness, reduced length or pitch.
- Φ_{max} ~5×10^{14} n_{eq}cm^{-2} for innermost region



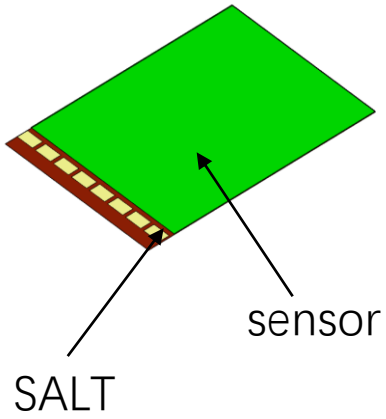


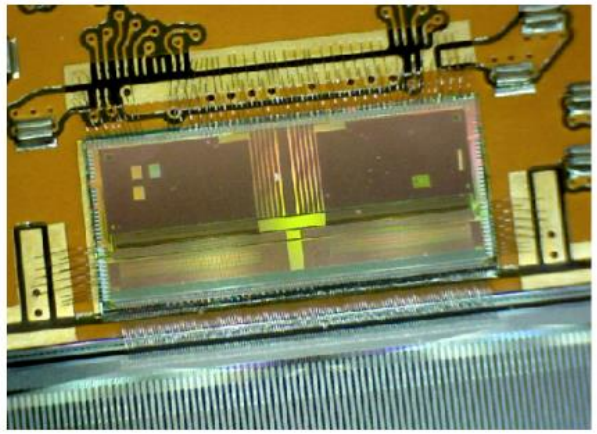
UT

Sensor	A	B	C	D
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16

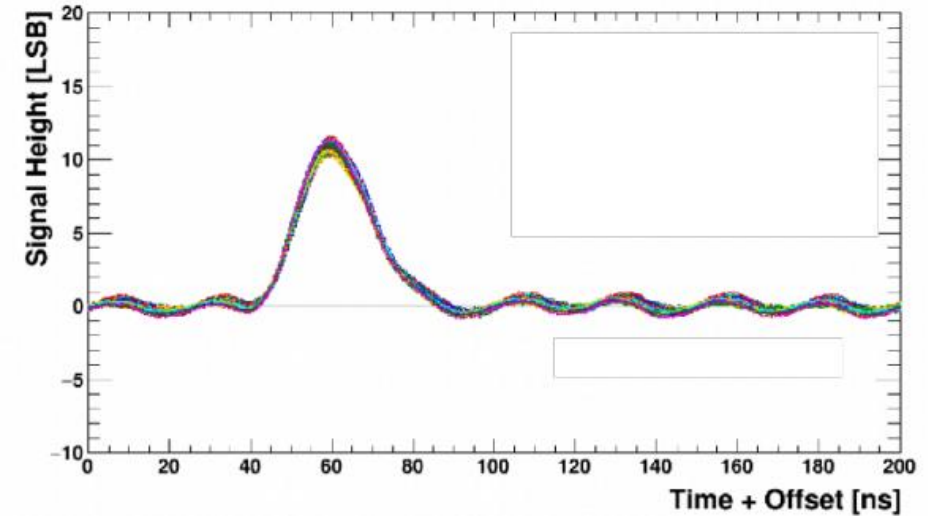
UT readout SALT (Silicon ASIC for LHCb Tracker)

- 128 Channels with 6-bit ADC, 40MHz readout, 4192 ASICs in total
  - A sensor is read out by 4/8 SALT chips
- CMOS 130nm technology (IBM, TSMC)
- Pulse shape: T_{peak} < 25ns (40MHz), short tail ~5% @ 25ns+T_{peak}.





SALT



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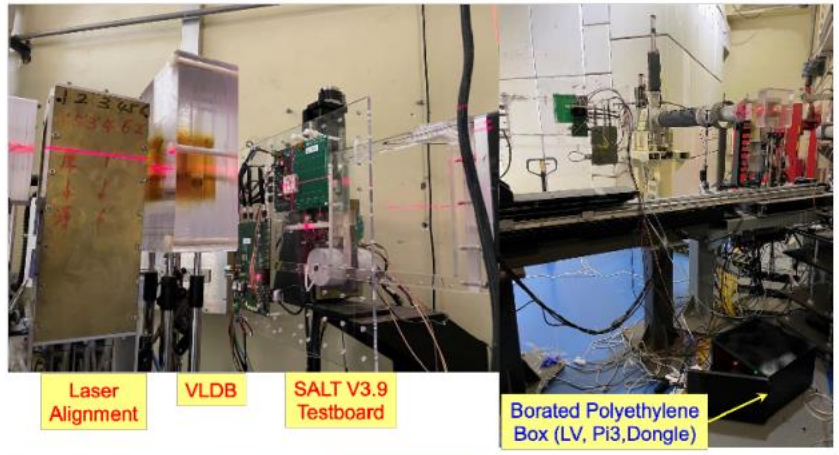
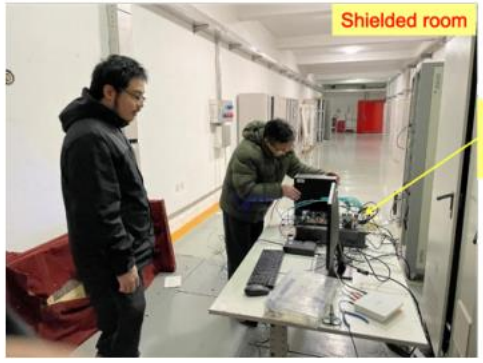
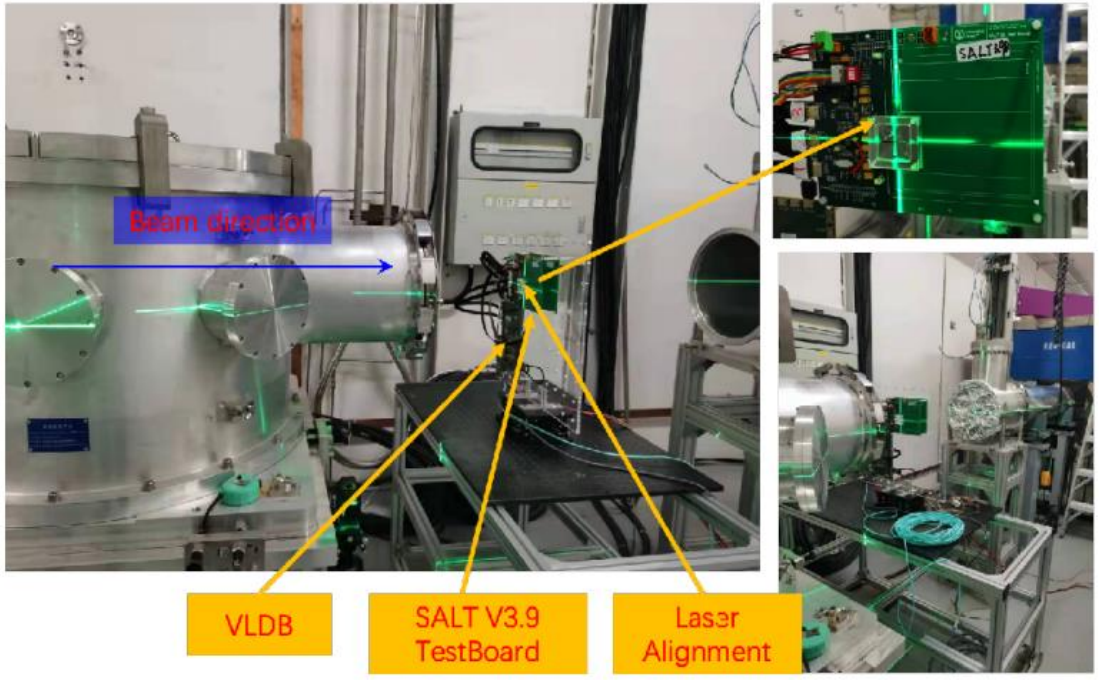
SALT radiation hardness against single-event effects

- Tested by IHEP team in Chinese facilities
  - China Institute of Atomic Energy (CIAE) Beijing, December 2020
  - China Spallation Neutron Source (CSNS) Dongguan, October 2021





At CIAE



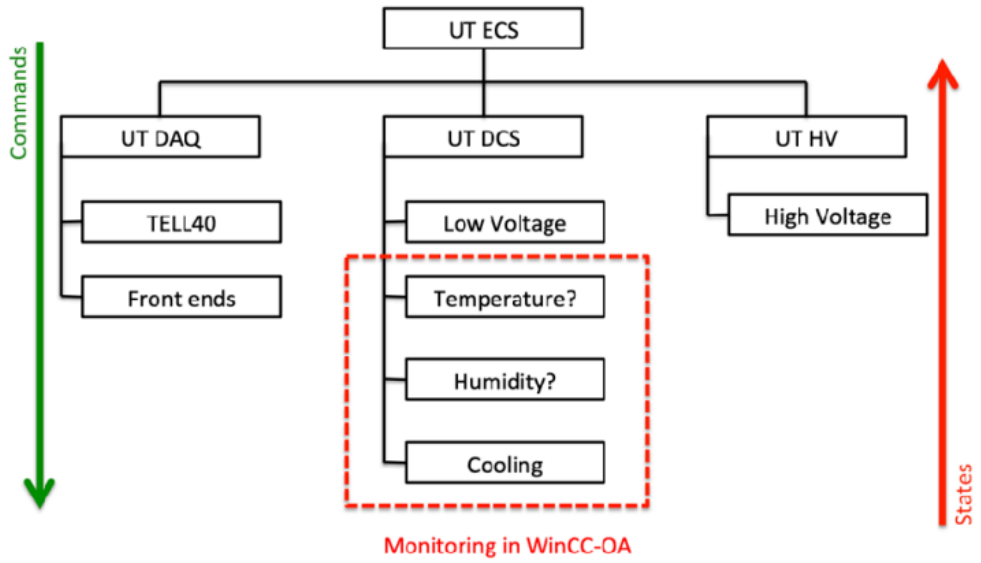
At CSNS

More details in Shuqi Sheng's poster.

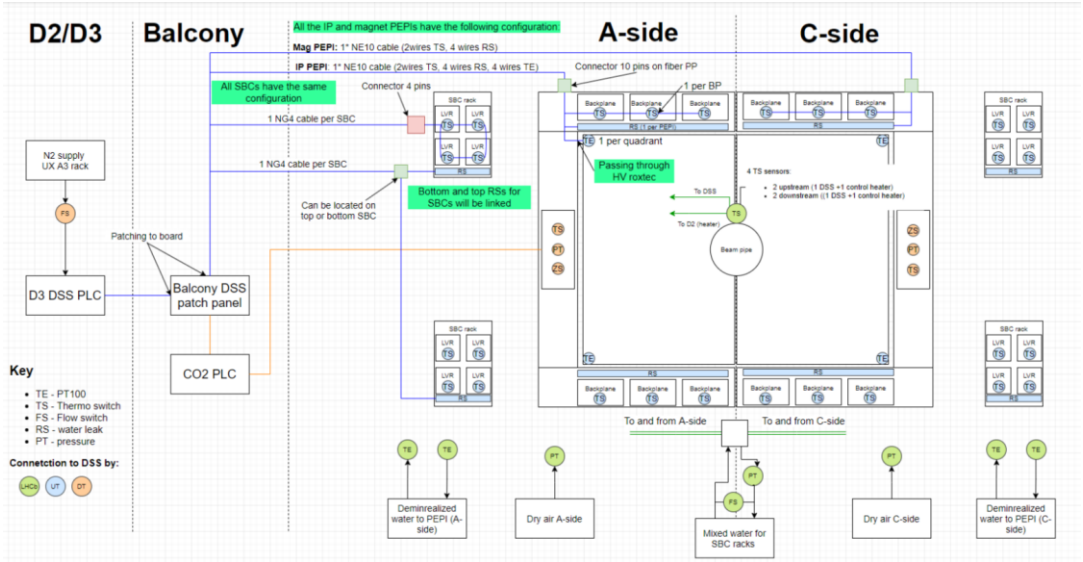
ECS and DSS systems

ECS, Experimental control system
DSS, Detector safety system

- IHEP members in charge of
  - Developing control system for UT stave test and final UT
  - Developing DSS system



ECS Overview

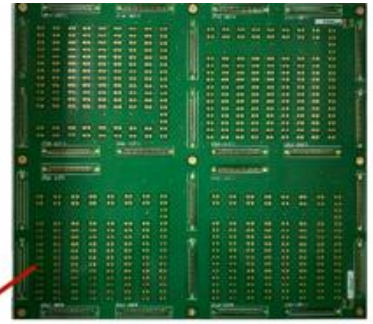


DSS Overview

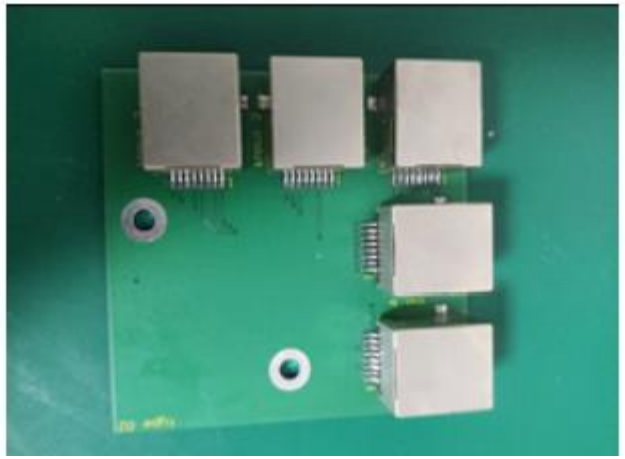
Supporting electronics conponents

Designed and produced by HNU & IHEP

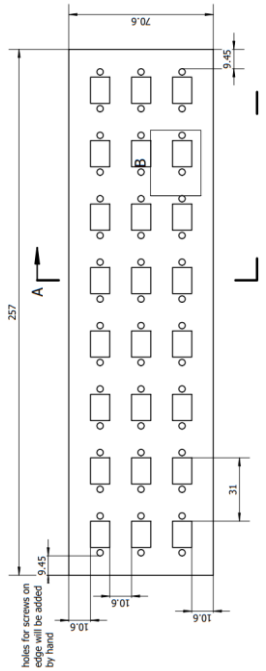
- HV patch panel, LV spilter, PEPI patch panel, HV cable



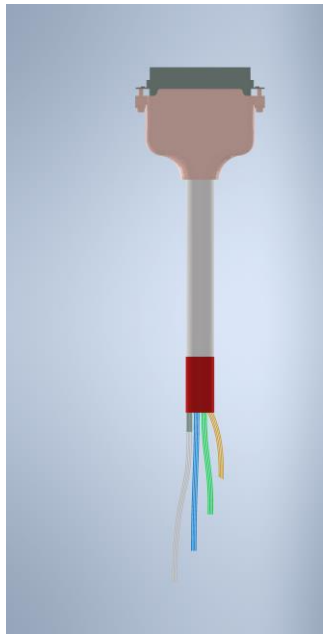
HV patch panel



LV spilter

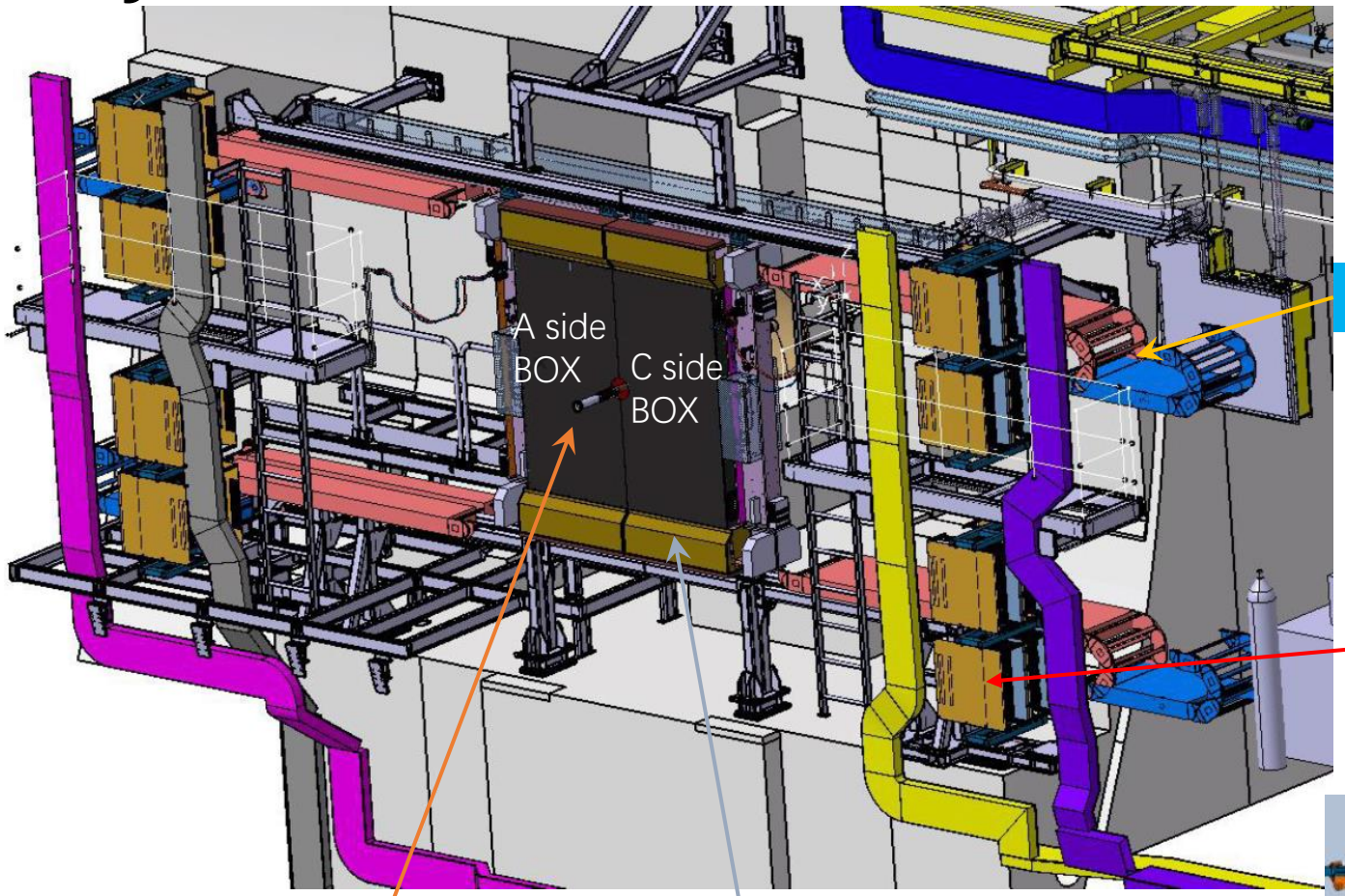


PEPI patch panel



HV cable

Layout of UT



Cable chain

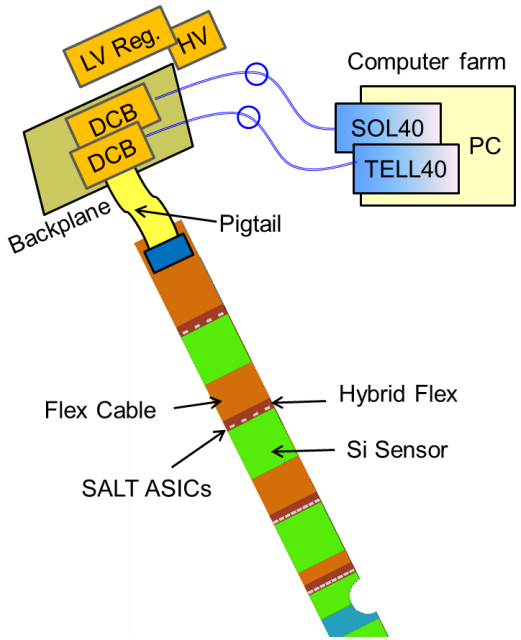
LV Regulator

UT Detector

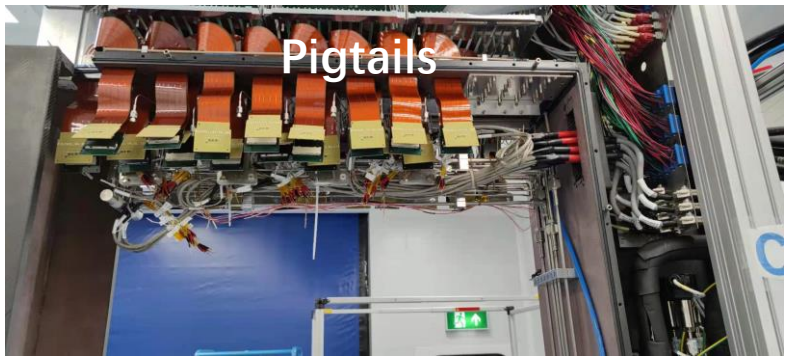
PEPI（Periphery Electronics）

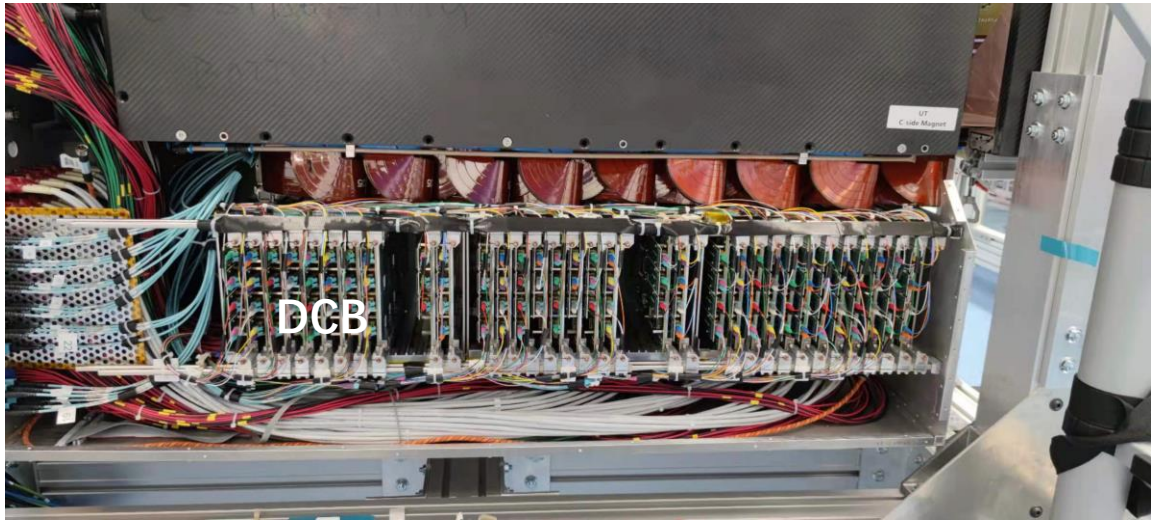
Installation Progress of UT

- PEPI (Periphery Electronics) installation:
  - Backplane
  - Pigtails
  - Data control board (DCB) and optical fibers
  - LV cables (for DCB, Front end ASICs) and sense cables (monitor the LV)
- HV cables
- Cooling system



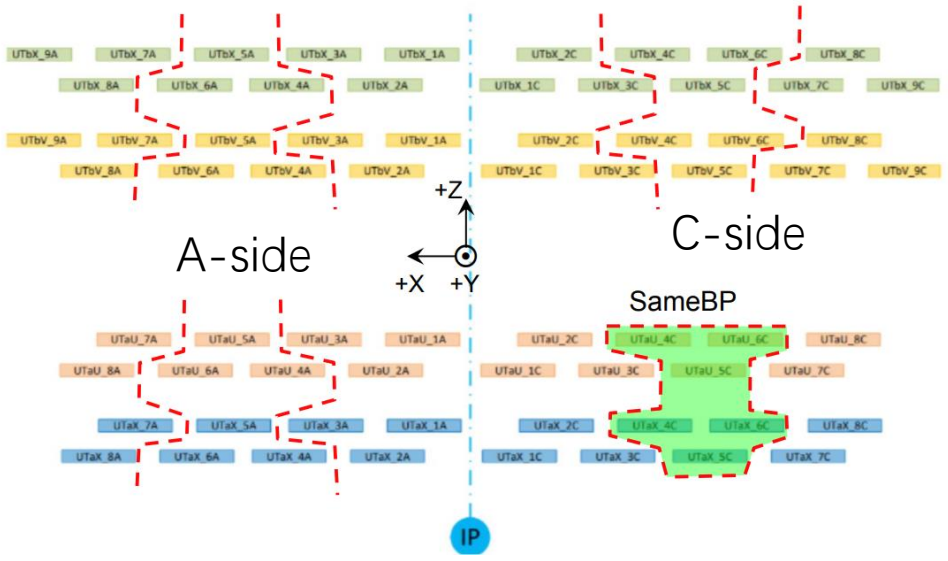
PEPI, HV, Cooling completed for C-side, partially done for A-side.

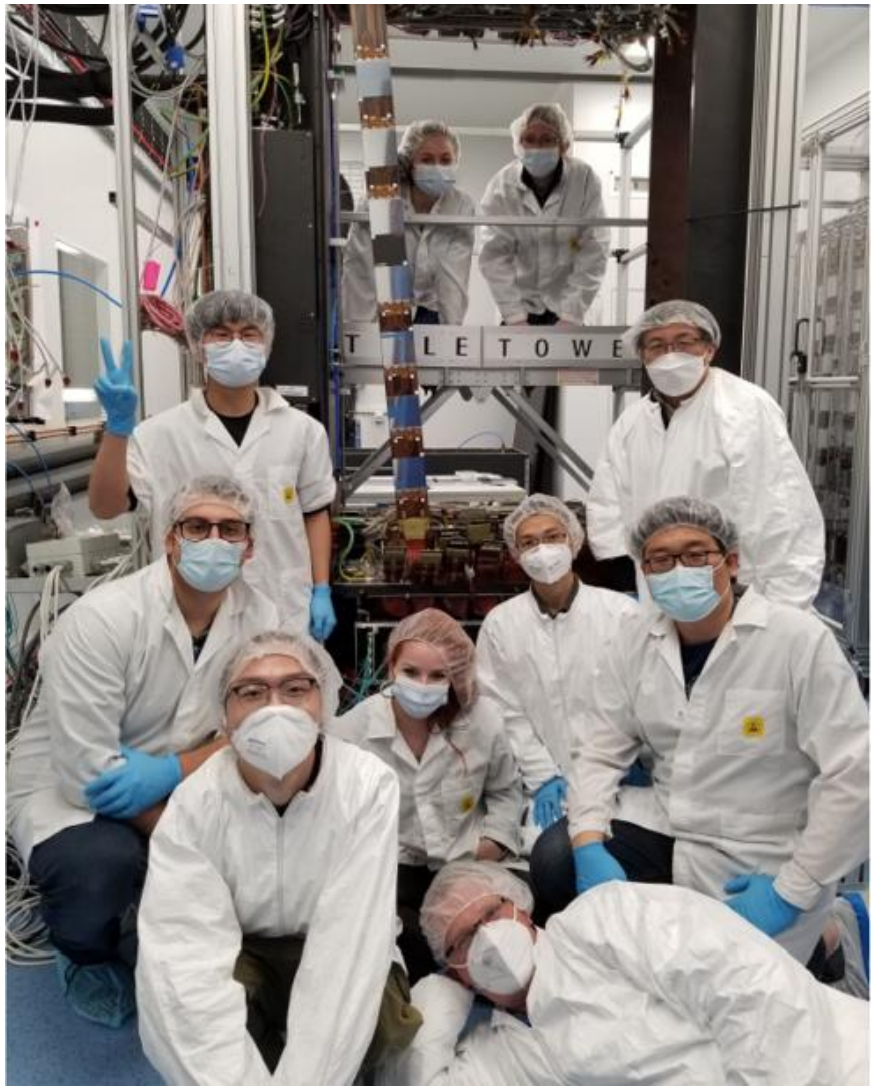




Stave installation

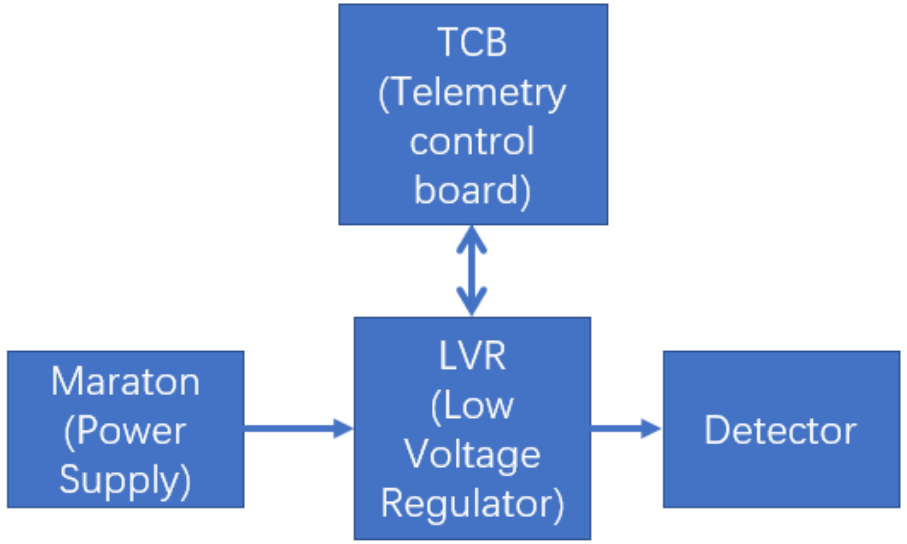
- Procedure: install the stave with the pigtails (flat cable) and support, cooling, HV
- A quarter staves for the C-side installed
  - Will be finished for C-side by Sep and A-side by Nov

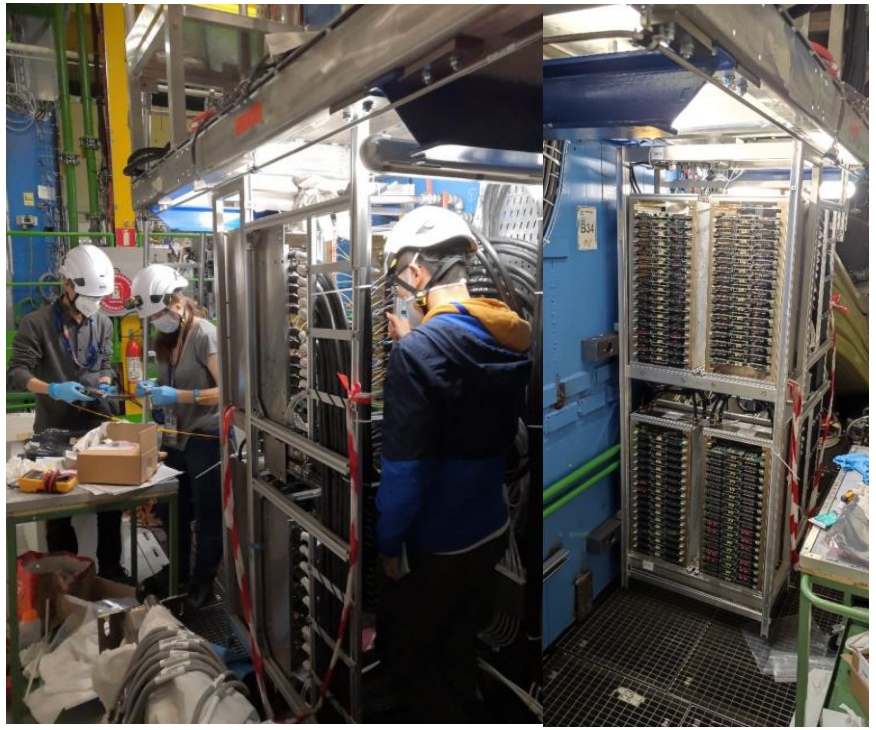




LV and cable installation

- 3/4 Low voltage system installed:





- Cable chain installation:
  - Cables mostly prepared: LV cables, HV cables, Sense cables, Fibers
  - Cable chain under preparation

Summary

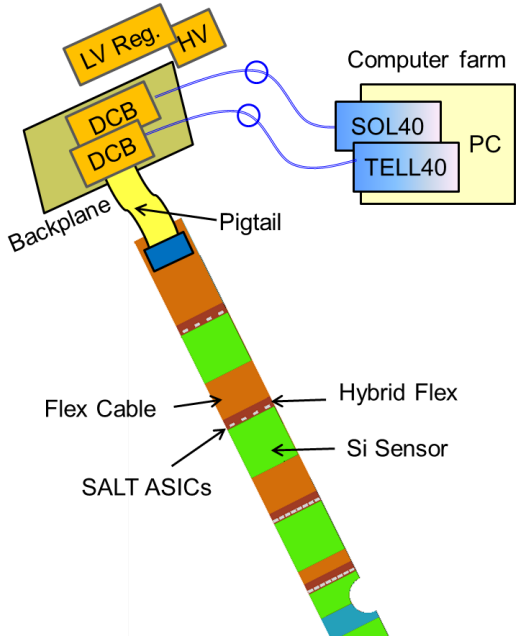
- LHCb Upgrade I is approaching completion:
  - A software-only trigger system implemented
  - 5-fold increase of luminosity
  - New silicon-strip based Upstream Tracker is a key subdetector
- **Chinese members have significant contributions**
- The installation status of UT at LHCb:
  - **C-side** detector is prepared except part of staves. It will be finished and installed in the experimental hall during a technical stop at **Sept. 2022**
  - **A-side** detector at the **year end technical stop**

Thanks!

BackUp

Installation Progress of UT

- PEPI (Periphery Electronics) installation:
  - Backplane (A central board of LV power, data board and connection to staves)
  - Pigtails (connect the stave and the electronics by connected to backplane)
  - DCB (data control board, transfer data from front to back by optical fibers) and optical fibers
  - LV cables (for DCB, Front end ASICs) and sense cables (monitor the LV)
- HV cables (power for sensors)
- Cooling system (CO_2 cooling)



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