High-precision Clock and Timing Distribution and Synchronization

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1. Introduction

In large-scale physics experiments or large accelerator systems, high-precision clock system is one of the indispensable and important components, which is the basis of precise time measurement. Meanwhile, a strict synchronization is necessary for multi-module cooperation, especially in accelerator systems.

The White Rabbit (WR) protocol is a well-known clock distribution technique and widely used in regular frequency clock distribution applications. However, because the standard WR network is based on the Ethernet structure with a reference clock of 62.5 MHz or 125 MHz, it cannot deal with the special working frequency. For example, in Shanghai high repetition rate X-ray Free Electron Lasers and Extreme light facility (SHINE), the exact frequency of reference clock fed into the clock distribution system is about 9.028 MHz, which is a 1.3 GHz accelerator RF clock divided by 144. A promising method is that extracting the frequency and phase messages of the input clock by the DDS circuit on the master node, broadcasting the characteristic messages to the slave nodes, and then recovering them on each slave node. While the working clocks of master and slave nodes are synchronized using standard WR network. Similarly, the timing signal could be also distributed as the same way. Measuring the time difference between the timing signal and the rising edge of working clock using high-precision FPGA TDC on master node, and then delivering the result to slave nodes to recover the timing signals. The structure of the clock and timing distribution system is shown in Fig.1.

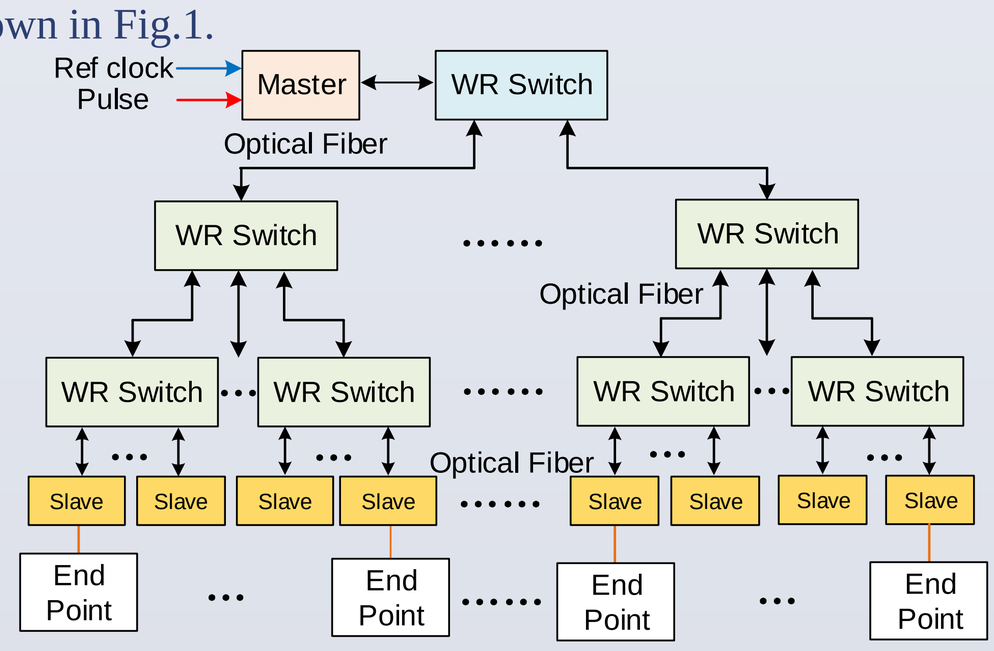

Fig. 1. Structure of the clock and timing distribution system.

2. Circuits Design

The architecture of the clock and timing distribution system is shown in Fig.2. The master node receives $clock_{ext}$ and keeps the output of local DDS locked to $clock_{ext}$ by automatic feedback adjustment. Consequently, the controlling values for DDS on the master node can fully characterize $clock_{ext}$. Then the controlling values are broadcasted to all slave nodes over the WR network and fed to the DDS circuits on slaves. Since the working clocks of master and slaves are synchronized using WR, the reproduced clocks on slave nodes are identical with the master. Furthermore, fine phase adjustment and frequency tuning for the machine clocks are performed according to the requirements of devices. Timing distribution

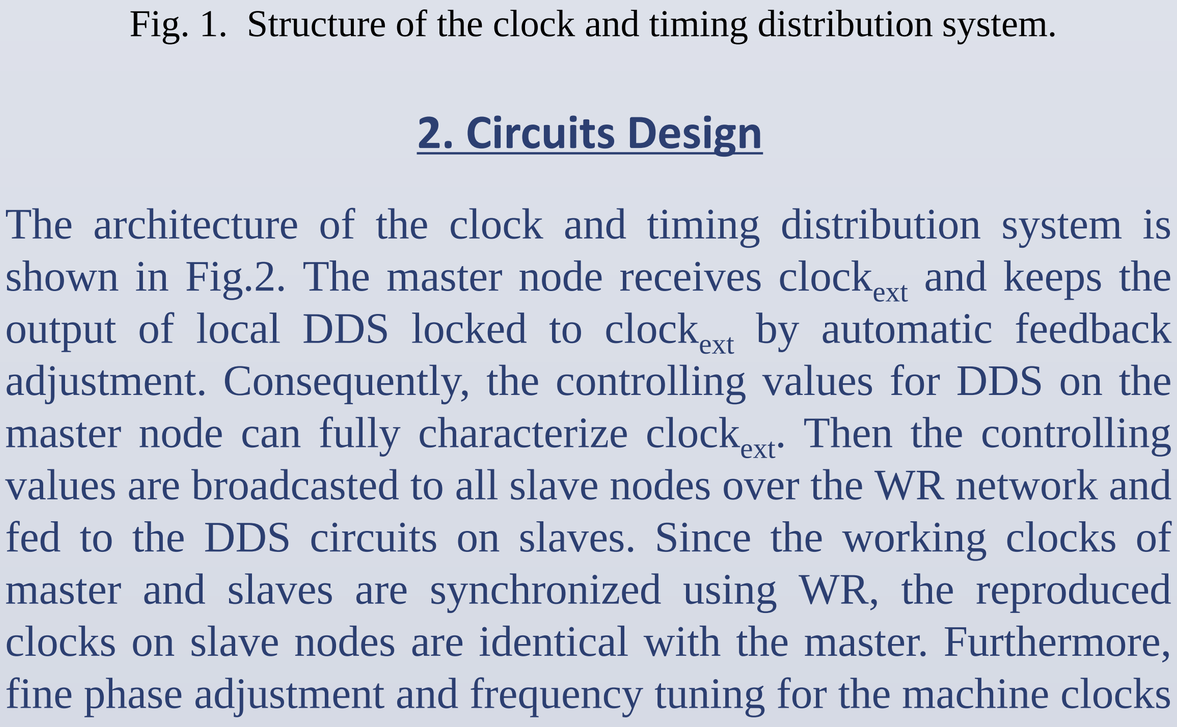

Fig. 2. Architecture of the distribution system

The block diagrams of the DDS circuits on master and slave nodes are depicted in Fig.3.

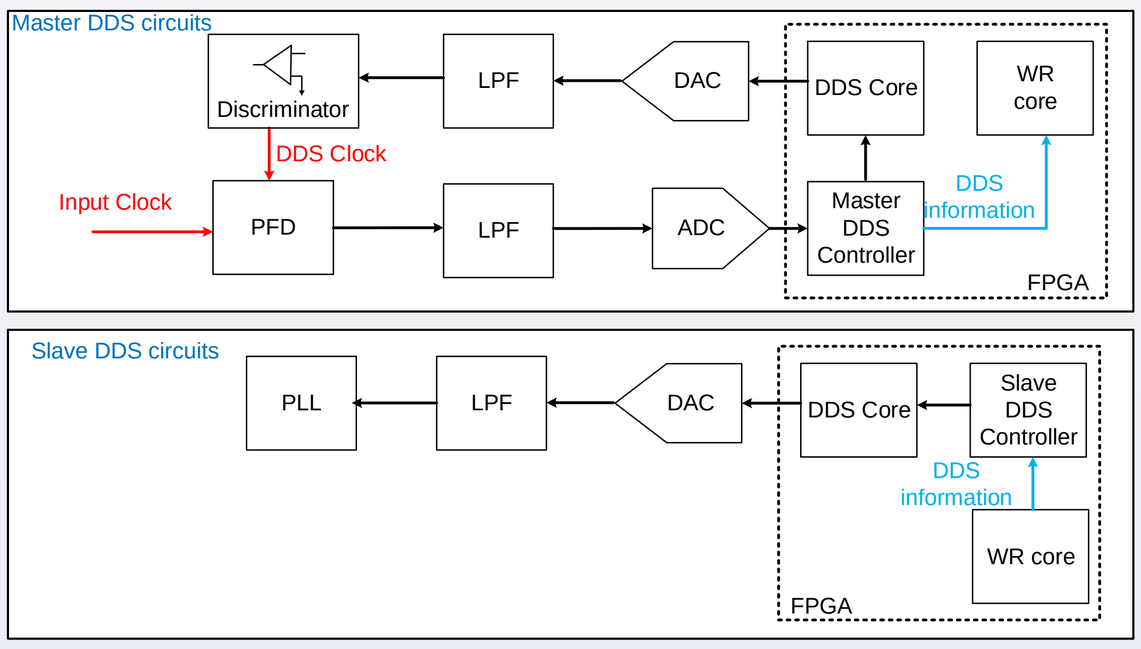

Fig. 3. The block diagram of DDS circuits on master and slave.

3. Test Results

As shown in Fig.4, the clock synchronization accuracy between the master node and slave node is better than 0.7 ns and the variation of the skew is less than 120 ps when powering on and off several times. The skew jitter of clocks between the master and different slave channels are all better than 18 ps RMS.

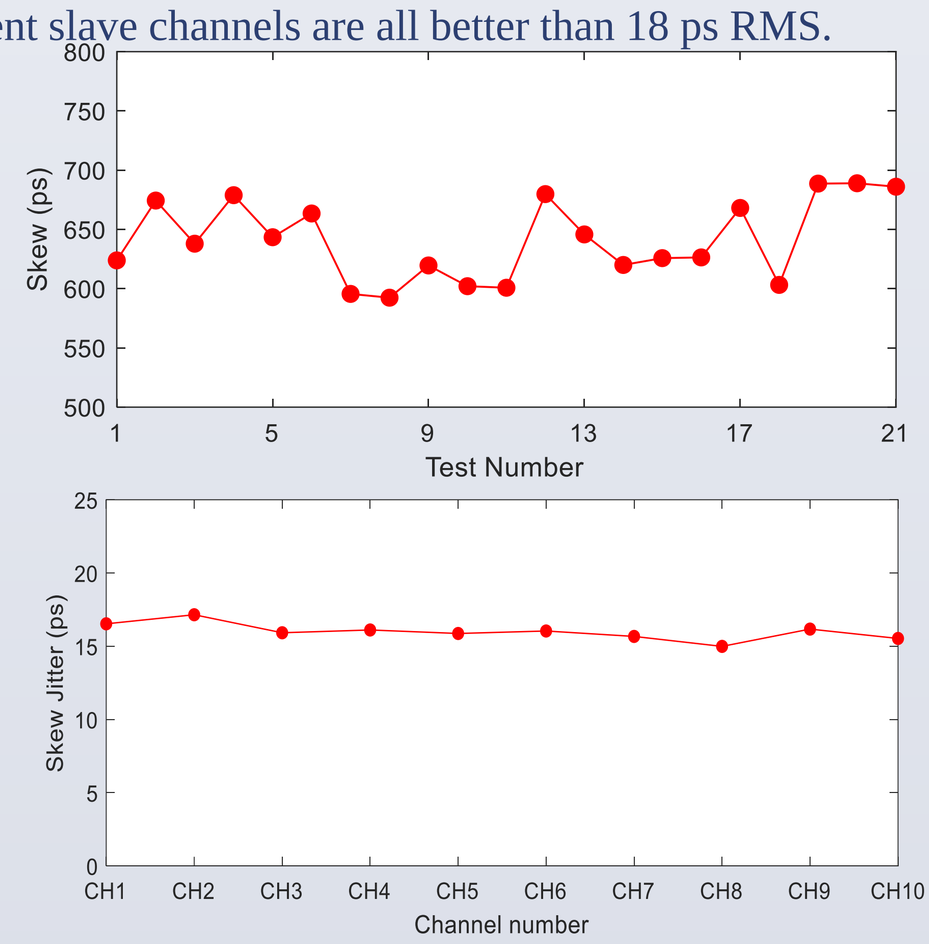

Fig. 4. Measurement results. (UP) Clock skew between master node and one slave node after powering up and down multiple times; (DOWN) The skew jitter between the master and different slave channels.

The skew jitter of the timing pulses between slave nodes is less than 30 ps, as shown in Fig.5.

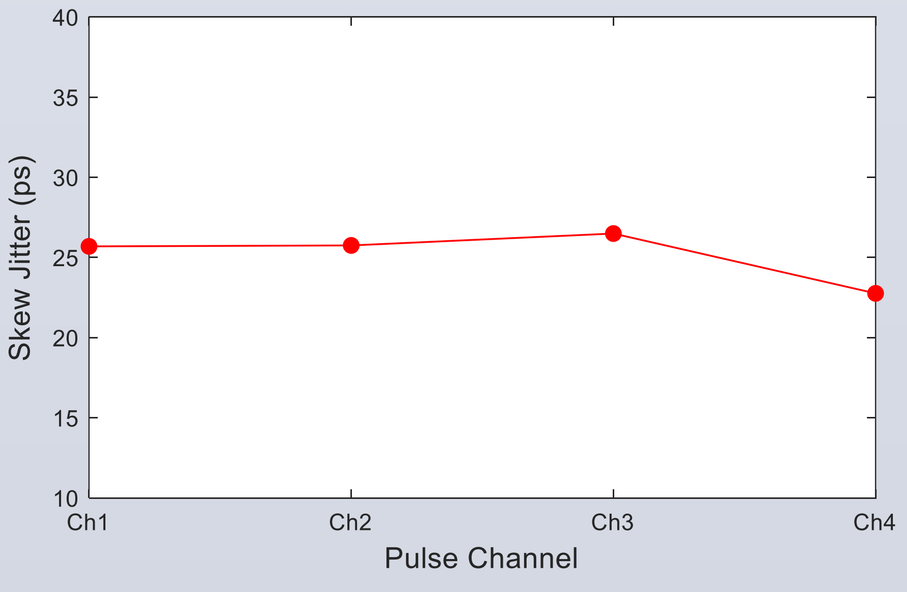

Fig. 5. Skew jitter of the timing pulses between the slave nodes.

Reference

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