中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

中国物理学会高能物理分会第十一届全国会员代表大会暨学术年会

Development of SOI pixel sensor for the CEPC vertex detector

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Hongyu Zhang, Jing Dong, Mingyi Dong,
Qun Ouyang

2022.8.9

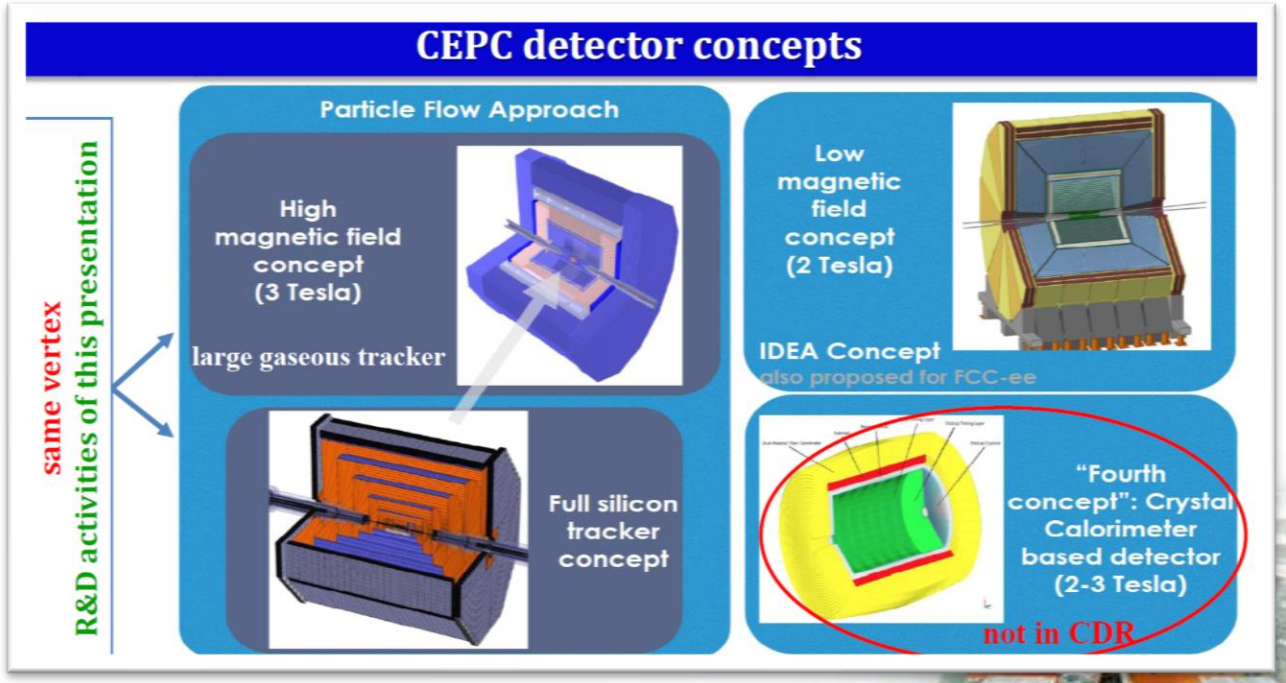
报告内容

- CEPC Vertex探测器的概念设计
  - 最内层silicon pixel sensor的指标要求
- SOI pixel sensor介绍
  - 需解决的关键问题
  - 工艺发展的三个阶段
- CPV系列芯片的研发
  - 高空间分辨率的深入研究（CPV-2）
  - 3D垂直集成技术的引入（CPV-4）
- 总结与展望

CEPC的物理目标

- Circular Electron-Positron Collider (90, 160, 250 GeV)
  - Higgs factory (10^6 Higgs)
    - Precision study of Higgs (m_H, J^{PC}, couplings), Similar & complementary to ILC
    - Looking for hints of new physics
  - Z & W factory (10^{10} Z^0)
    - Precision test of SM
    - Rare decays
  - Flavor factory: b, c, t and QCD studies

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV}) \sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV}) \times \sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

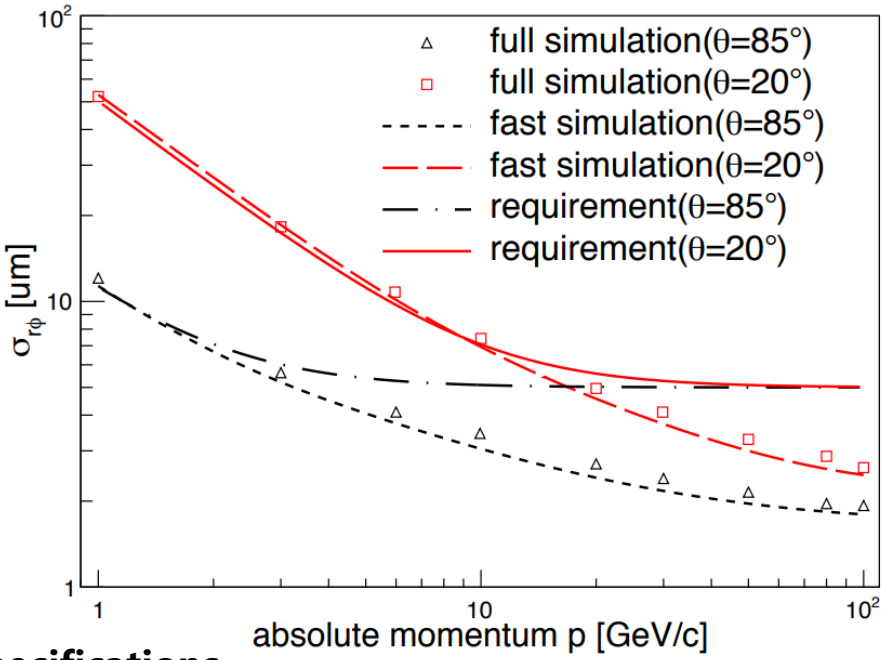


Silicon Pixel Sensor的指标要求

- Efficient tagging of heavy quarks (b/c) and τ leptons

→ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\ (\mu m)$$



Physics driven requirements | **Running constraints** | **Sensor specifications**

$\sigma_{s.p.}$ 2.8 μm → Small pixel 16 μm

Material budget 0.15% X_0 / layer → Thinning 50 μm

→ Air cooling → Low power 50 mW / cm^2

r of Inner most layer 16 mm → beam-related background → Fast readout 1 ~ 100 μs

→ radiation damage → Radiation tolerance

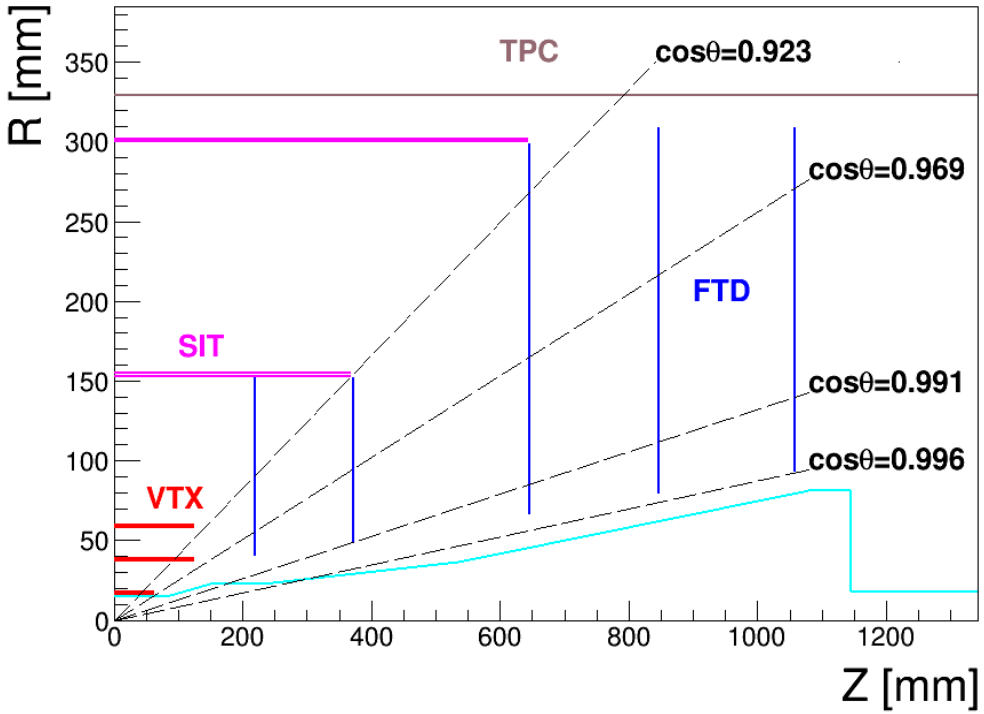
3.4 Mrad / year

$6.2\times10^{12} n_{eq}$ / (cm^2 year)

如何实现?

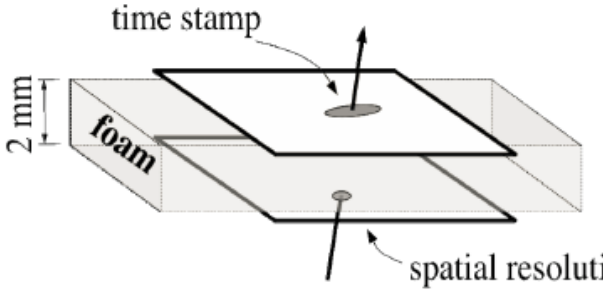
CEPC Vertex探测器概念设计

Silicon tracking system



- SIT： Silicon Internal Tracker
- FTD： Forward Tracking Detector
- SET： Silicon External Tracker
- ETD： End-cap Tracking Detector

- VTX:
  - 3 layers of **double-sided** structure
  - σ_{SP} = 2.8 μm in L1
  - Total number of pixels: 690M



Outer side像素芯片

Inner side像素芯片

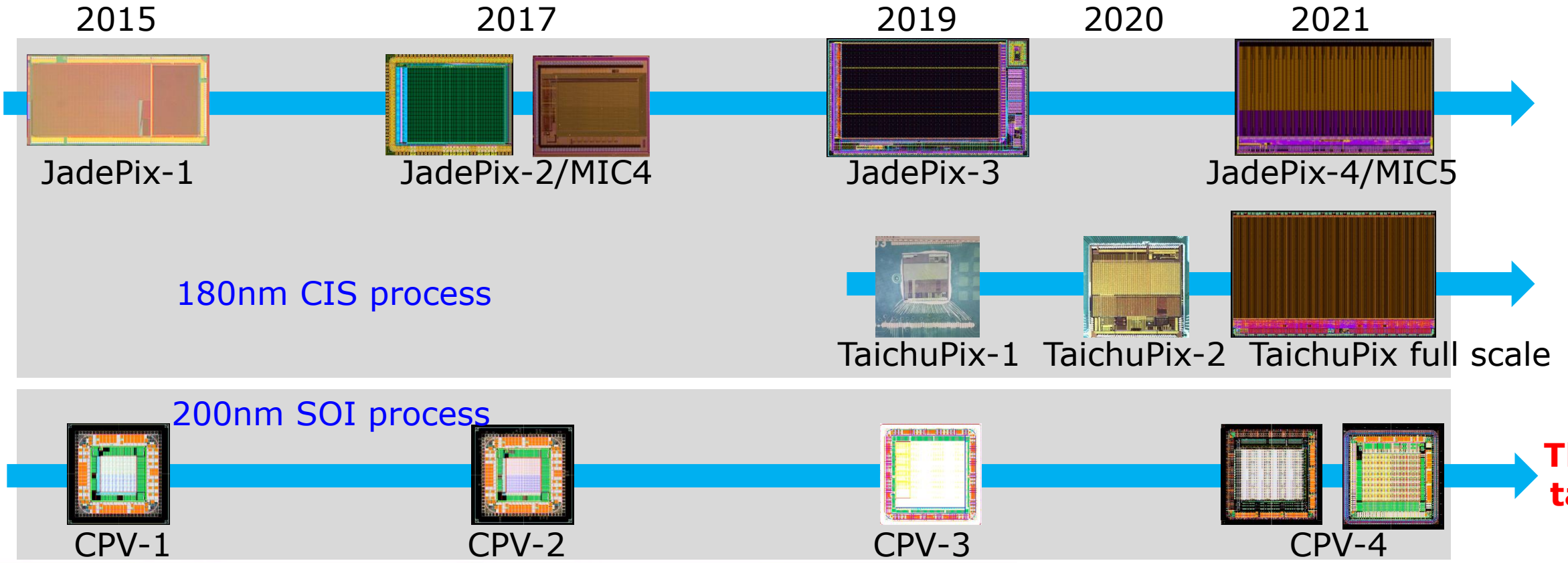
Concept of double-sided structure

Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	0.15%/X_0
	18	62.5	6	0.15%/X_0
Layer 2	37	125.0	4	0.15%/X_0
	39	125.0	4	0.15%/X_0
Layer 3	58	125.0	4	0.15%/X_0
	60	125.0	4	0.15%/X_0

Silicon Pixel Sensor预研工作（国内）

- Development of pixel sensor for CEPC are supported by
  - Ministry of Science and Technology (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation



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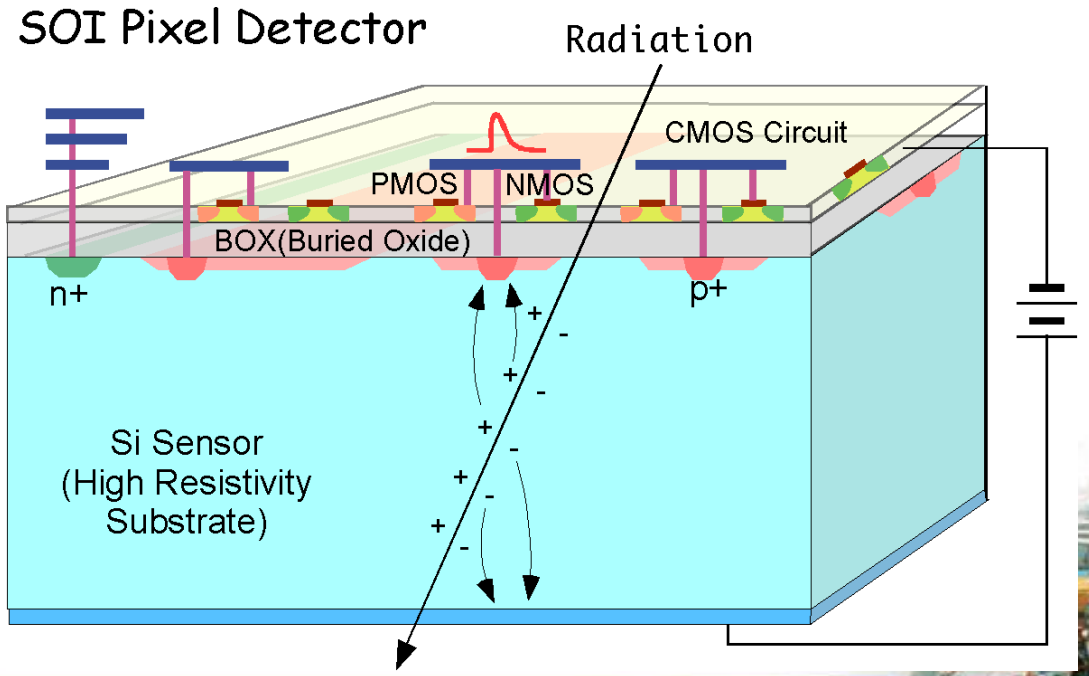
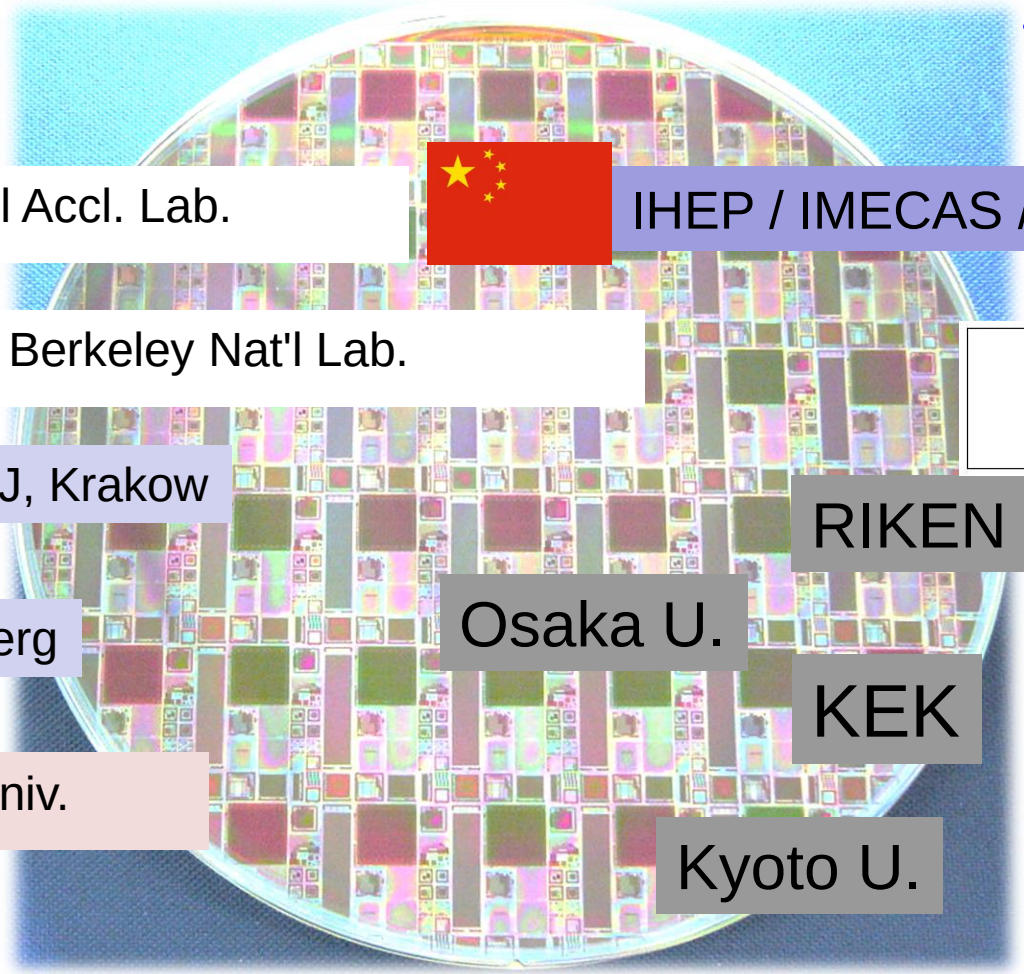
SOI像素探测器工艺

- 三明治结构
  - 上：以像素为单元的独立信号处理电路（ Device Layer），继承了SOI集成电路的优点
  - 中：SiO_2绝缘层（金属通孔阵列实现一对一电连接）
  - 下：以像素为单元的sensor diode阵列
- 挑战性：
  - 像素电路与sensor diode之间的**电场耦合**（背栅效应和电荷注入效应）
  - BOX层的TID效应



200nm FD-SOI@KEK

- SOIPIX合作组的MPW流片班车，自2005年起，1~2次/年
  - 广泛的用户群体，持续的工艺改进



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KEK

Louvain Univ.

Kyoto U.

Tsukuba U.

Buried P-Well (BPW)

- 《Development of SOI pixel process technology》
  - Y. Arai, etc., NIMA, Vol. 636, S31-S36, Apr. 2011
  - Sensor偏压不会显著影响MOS管阈值，**解决了背栅效应问题**
- 《Test of a fine pitch SOI pixel detector with laser beam》
  - Yi Liu, Yunpeng Lu, Xudong Ju, Qun Ouyang, Chinese Physics C, Vol. 40, No. 1 (2016) 016202
  - 芯片设计与测试验证（ INTPIX2P5 ）

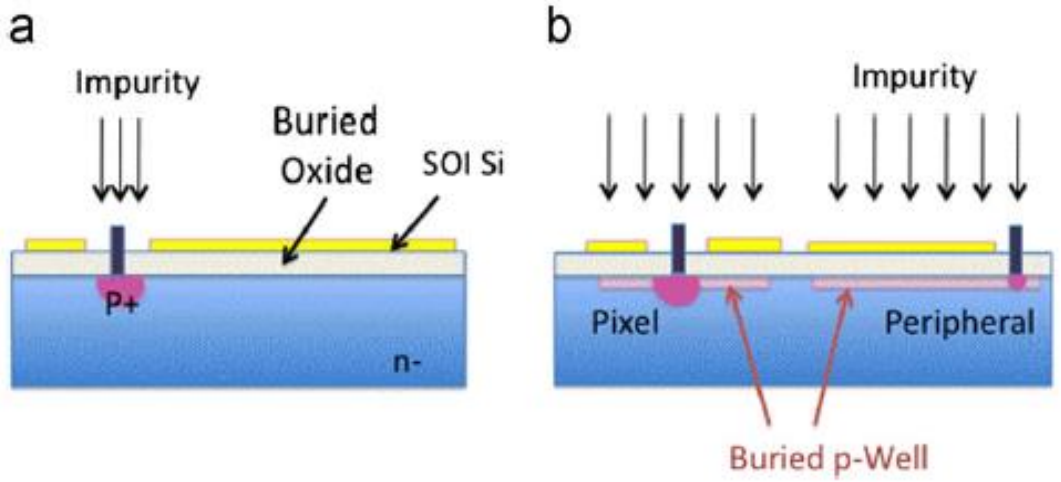


Fig. 5. (a) Normal implantation method to create p–n junction in the substrate and (b) buried p-well implantation method. By fixing the BPW potential under peripheral circuit, the back gate effect is completely suppressed. In the pixel area, BPW may be used to extend sensor area.

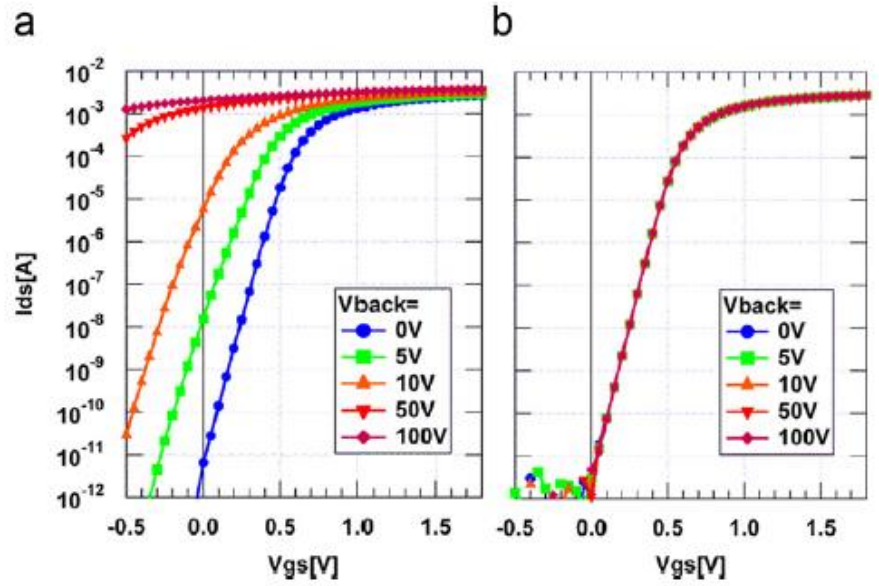
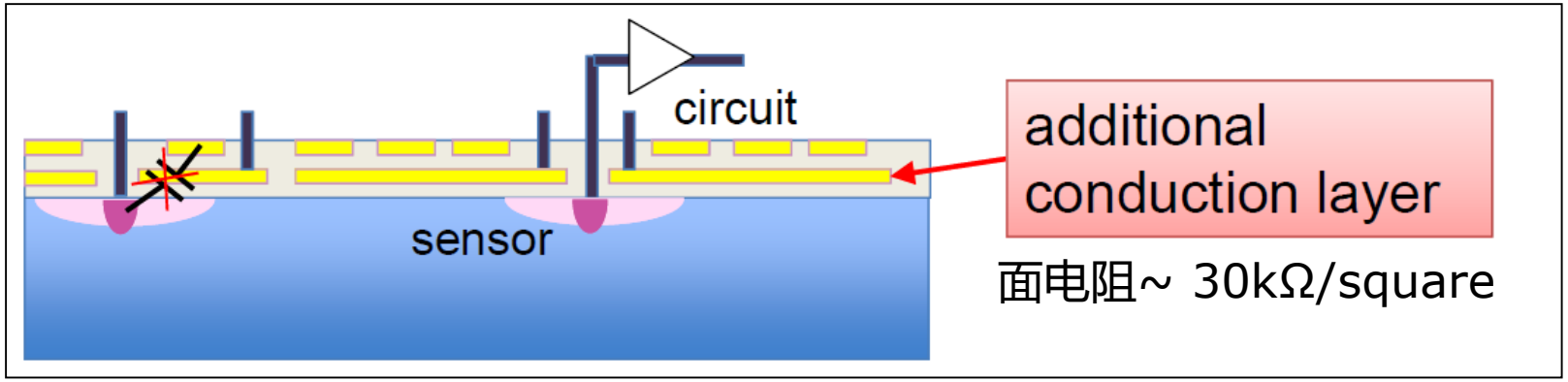


Fig. 6. Backside voltage dependence of an NMOS Id–Vgs curve (a) without BPW and (b) with BPW connected to 0 V.

Double-SOI (DSOI)

- SOI2层作为MOS管的背栅：
  - 可施加独立电压，用于TID电荷补偿
  - 切断MOS管和电荷收集极之间的电容耦合通道 ⟹ **高能所团队在实验验证方面做出了突出贡献！**
- 定制DSOI晶圆
  - Validation and verification

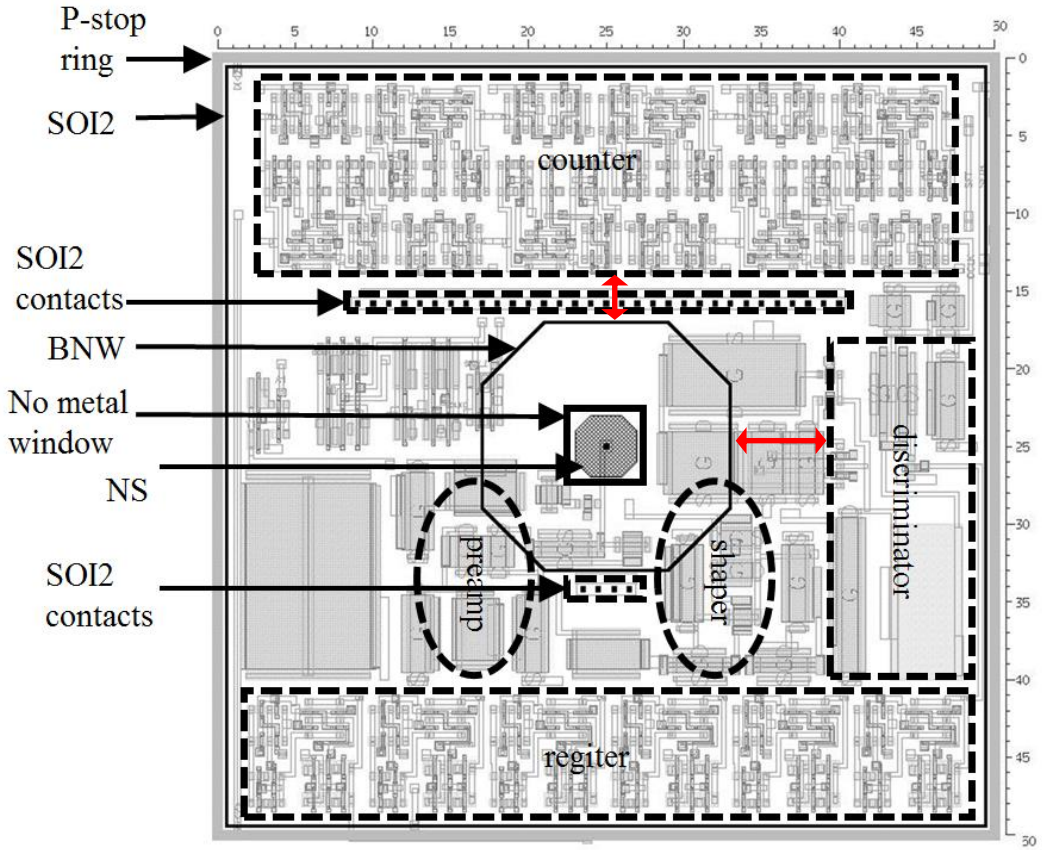


《A study on the shielding mechanisms of SOI pixel detector》, Yunpeng Lu, Yi Liu, Zhigang Wu, Qun Ouyang, Yasuo Arai, ECONF, 2016

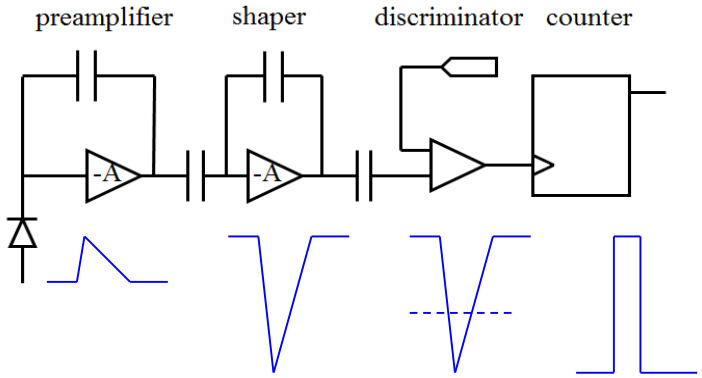
《 First results of a Double-SOI pixel chip for X-ray imaging 》, Yunpeng Lu, Qun Ouyang, Yasuo Arai, Yi Liu, Zhigang Wu, Yang Zhou, NIMA 831 (2016) 44-48

计数型SOI像素芯片的研究

- CPIXTEG3b芯片 (DSOI工艺)
  - 像素电路结构：Amplifier-Shaper-Discriminator-Counter
  - 该结构对电荷注入效应敏感，是理想的“试金石”



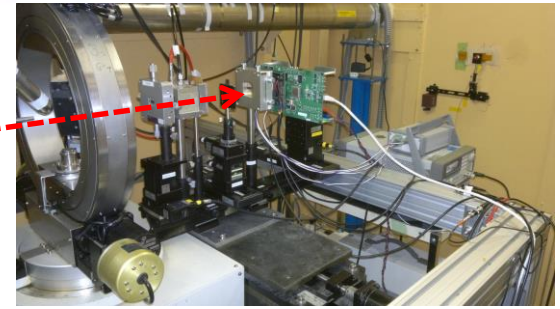
Pixel layout



Signal processing chain in-pixel

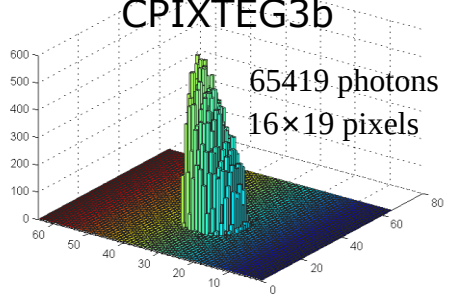
X-ray束流测试结果

- DSOI工艺的探测性能得到了充分验证，**解决了电荷注入效应问题**
  - 最低阈值~3keV
  - 零噪声计数



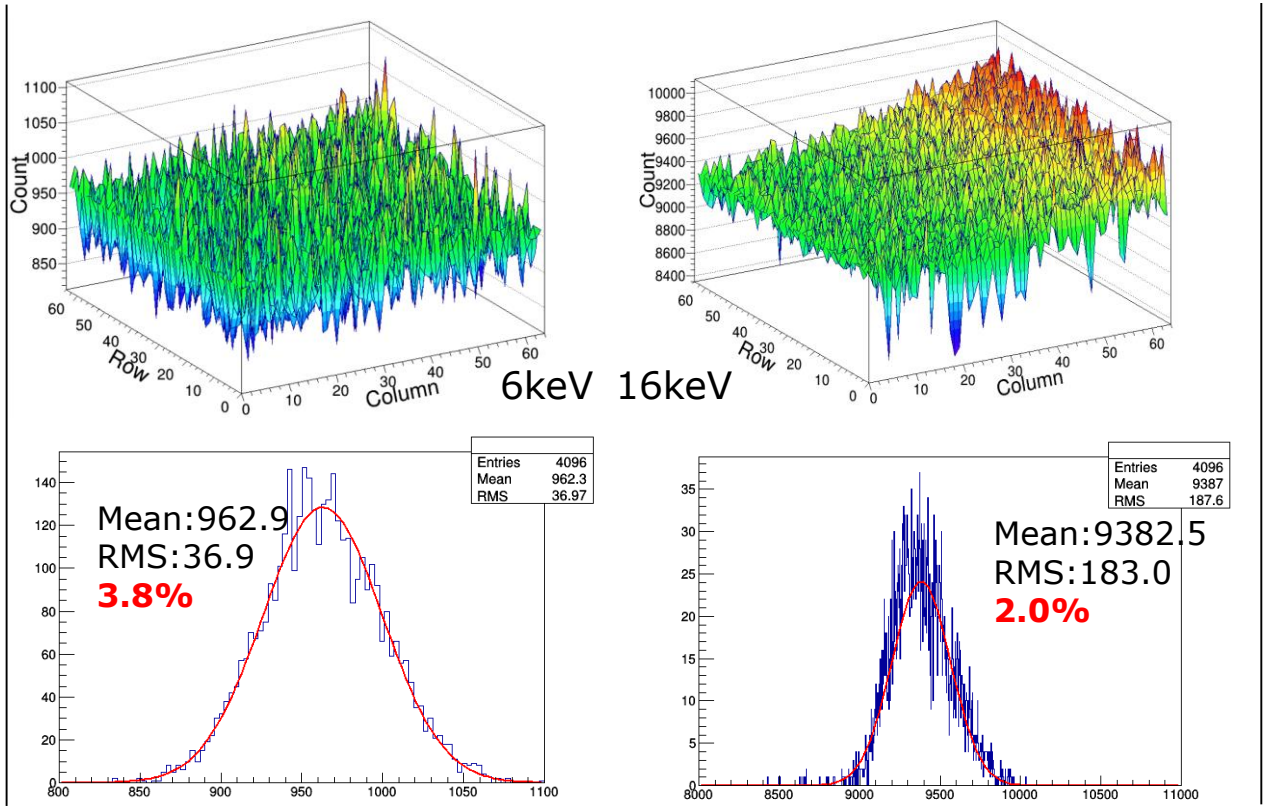
16 keV X-ray signal(shaper)

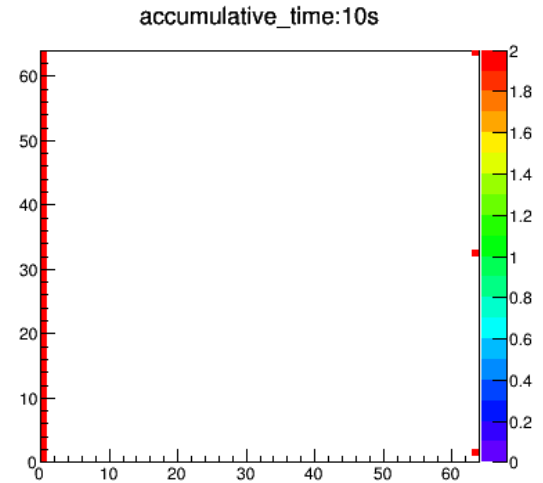
Beam profile measured by CPIXTEG3b



(16keV, threshold~1600e⁻)

Count distribution under flat field





1小时本底事例回放
(PPT版本可播放)

Pinned-Depleted-Diode（PDD）

- 《A Low-Noise X-ray Astronomical Silicon-On-Insulator Pixel Detector Using a Pinned Depleted Diode Structure》
  - Hiroki Kamehama, etc., Sensors 2018, 18,27;
  - 基于**嵌套注入阱**的Diode解决方案，替代DSOI定制晶圆
- 《Characterization of AC coupled SOI pixel sensor with pinned depleted diode structure》,
  - Jing Dong, Yunpeng Lu, Zhigang Wu, Yang Zhou, Qun Ouyang, NIMA 1040 (2022) 167204

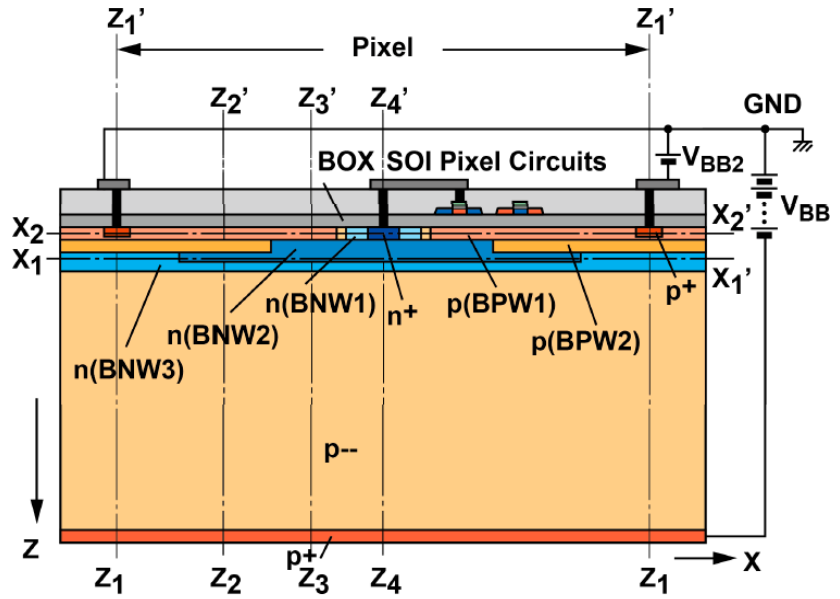


Figure 3. Cross-sectional view of the SOIPIX-PDD with multiple buried wells.

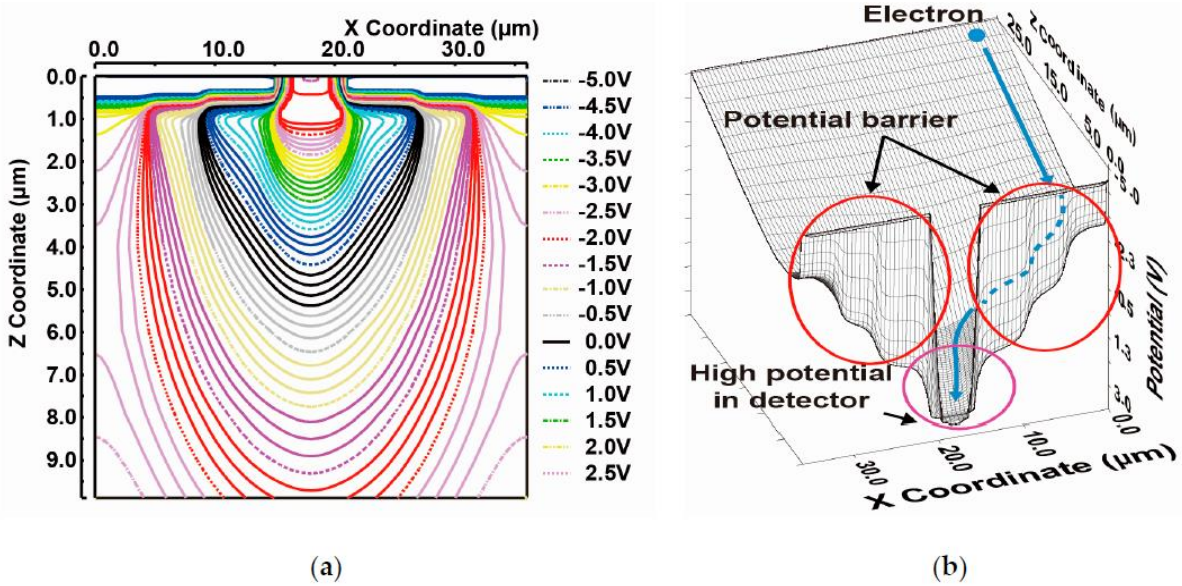


Figure 7. 2-D (X-Z) Equipotential plot (a) and Bird's Eye View of the 2-D (X-Z) Potential (b).

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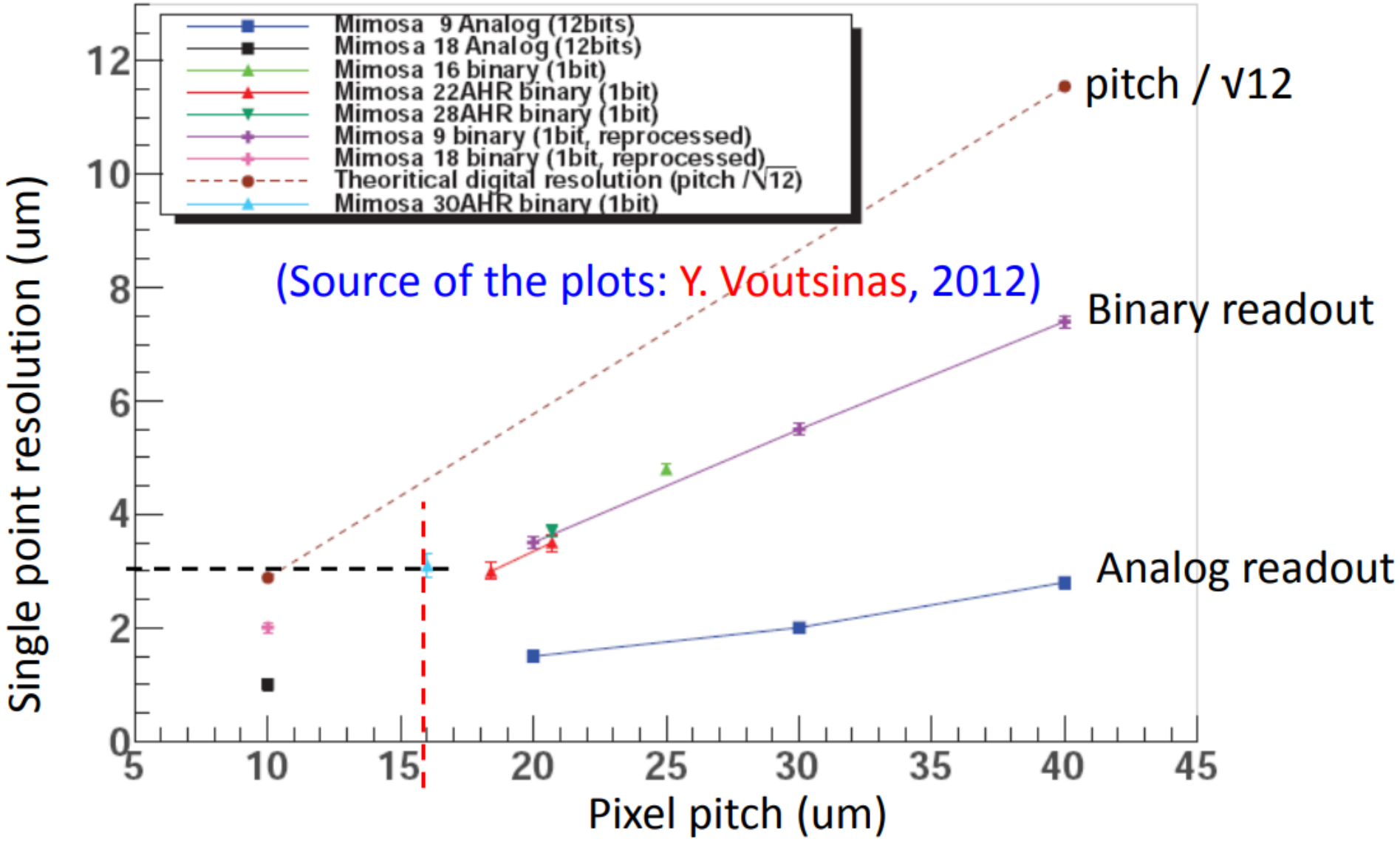
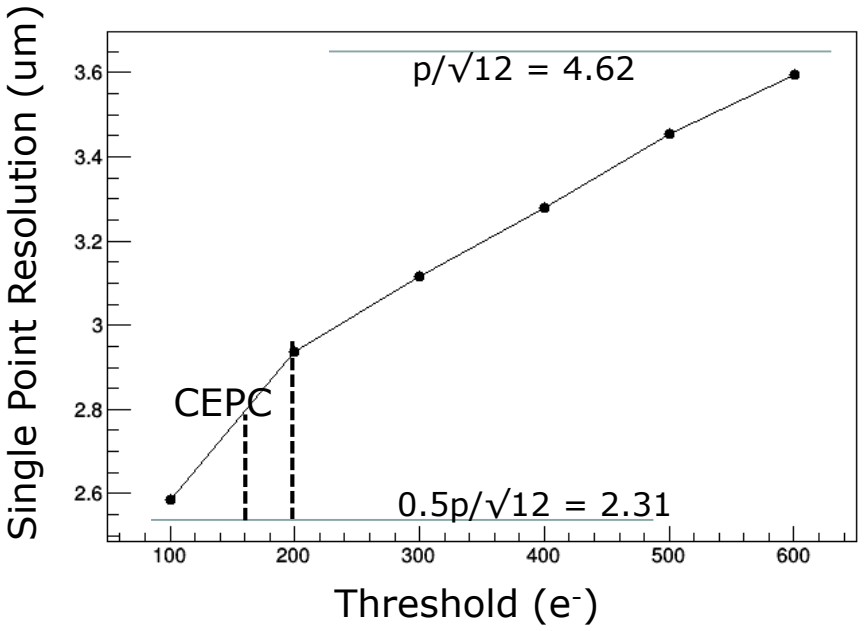
空间分辨率与像素Pitch的关系

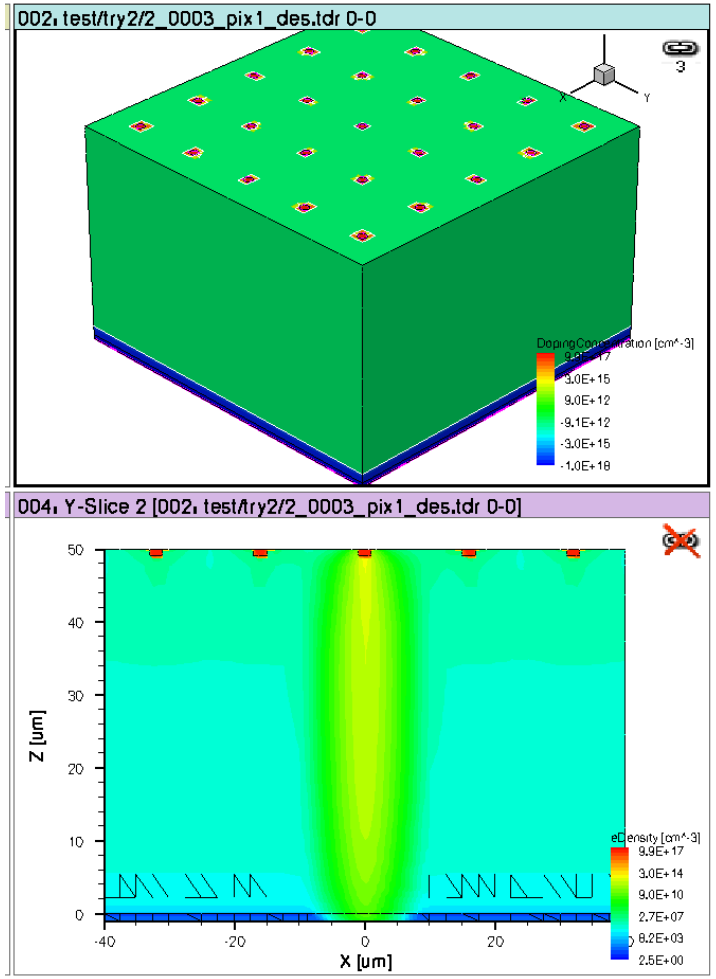


器件仿真（TCAD）

- Pixel pitch = 16 um & Sensor thickness = 50 um
- **低噪声前放**是实现高空间分辨率的必要条件
  - ENC ~ 20e⁻
  - Threshold < 200e⁻

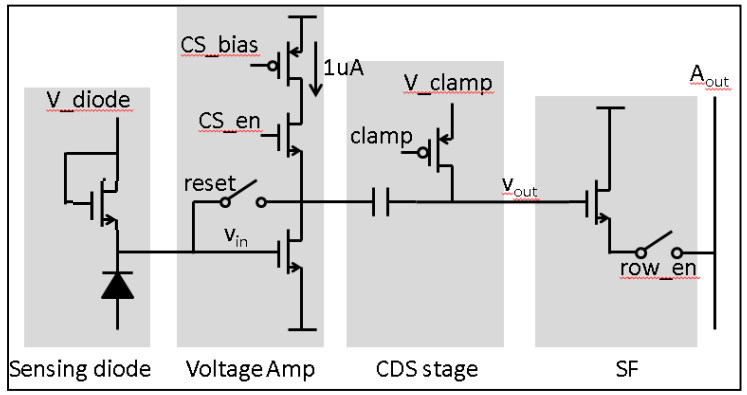


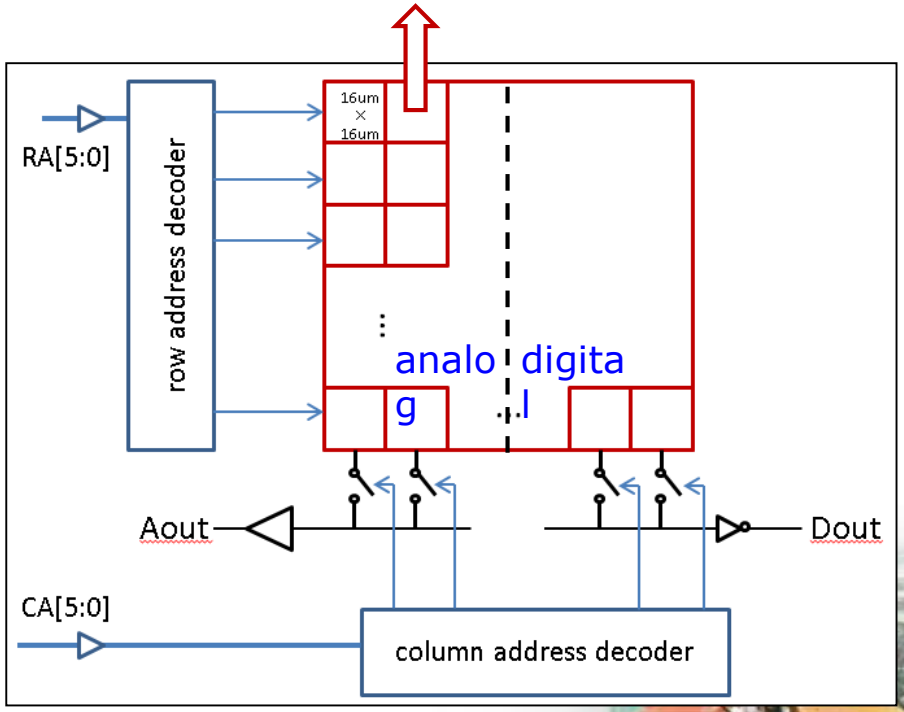
TCAD仿真载流子输运过程



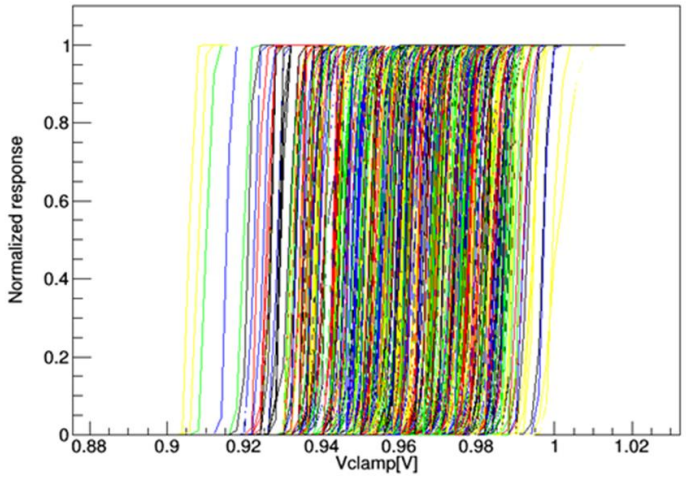
CPV-2芯片架构

- 像素尺寸预设为16 um * 16 um
  - 验证器件仿真的结果
- 有限的像素版图面积约束下
  - 最简化的前端电路设计→非连续工作模式
  - 像素阵列共用读出端口→读出速度慢
- DSOI工艺流片并测试
  - ENC = 6 e-

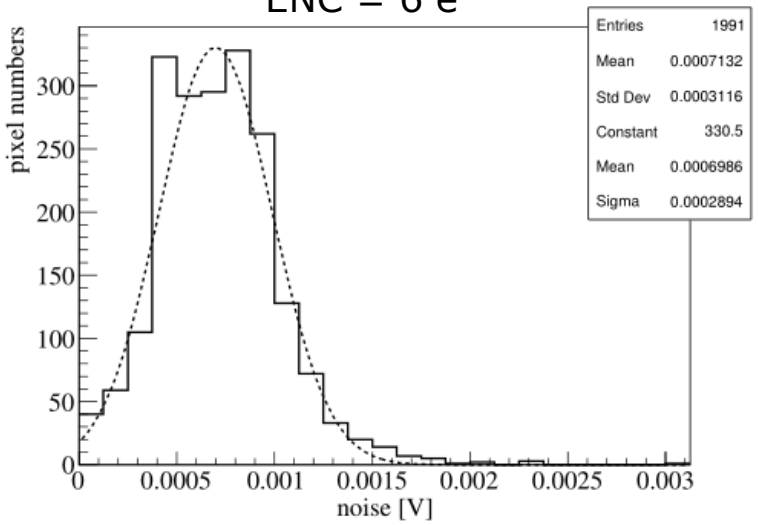




Digital array S-Curve

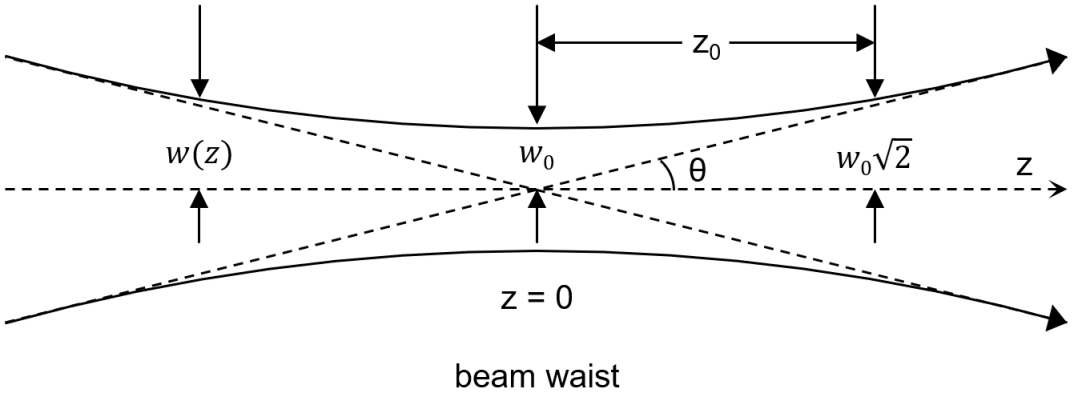


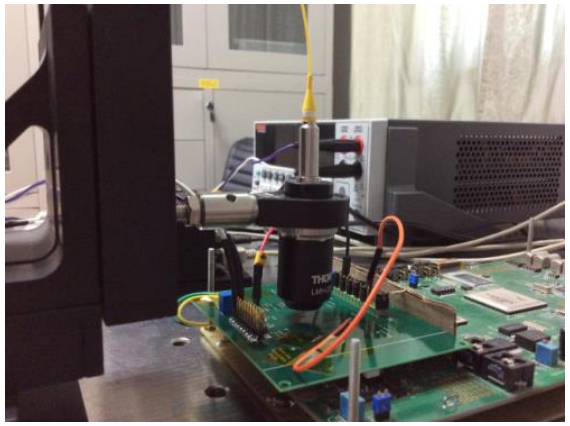
ENC = 6 e-

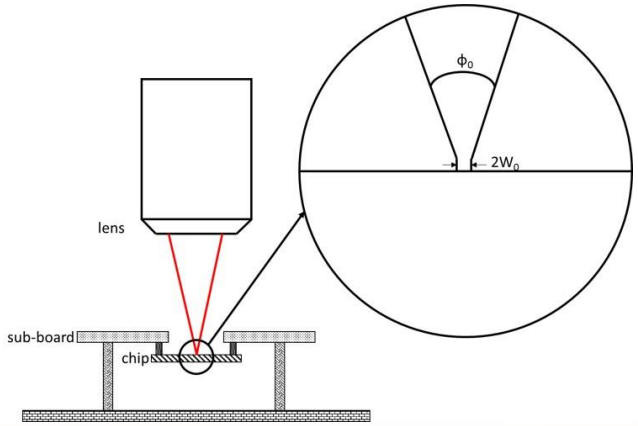


CPV-2空间分辨率的性能研究

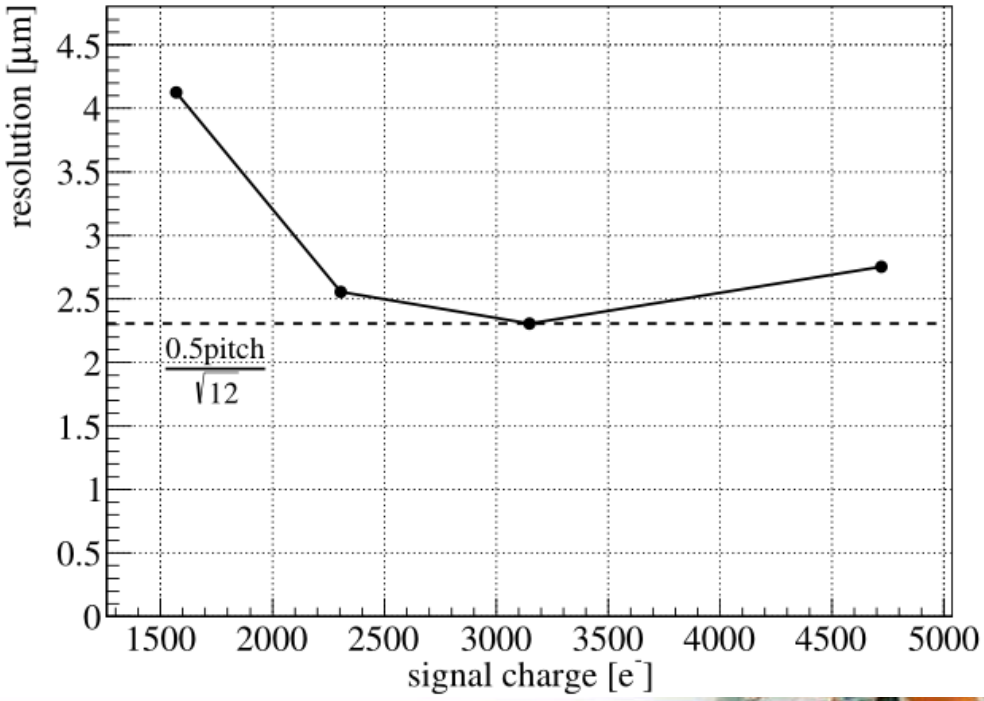
- 红外激光测试平台
  - 1064nm波长，光强可调
  - 光学透镜聚焦，束腰半径ω_0=1.7 um
  - 三维步进电机控制位置，重复精度1μm





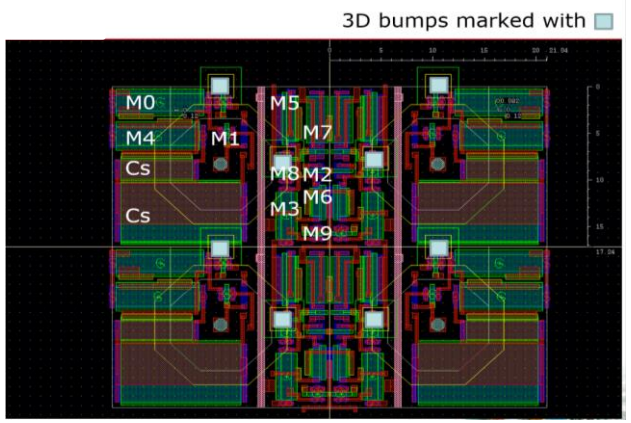


- 深入理解了空间分辨率与Cluster size的关系
  - Pixel pitch、耗尽区厚度、电场分布
  - 优化“信号/阈值”比值，可获得最佳空间分辨率
- 结论：**Pitch ~ 16 um, Threshold < 200 e-**



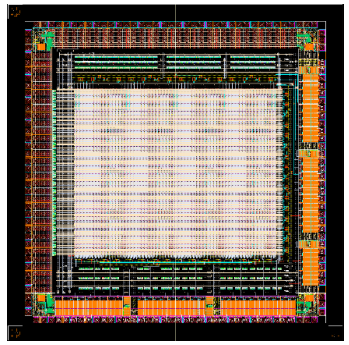
引入3D垂直集成的CPV-4芯片

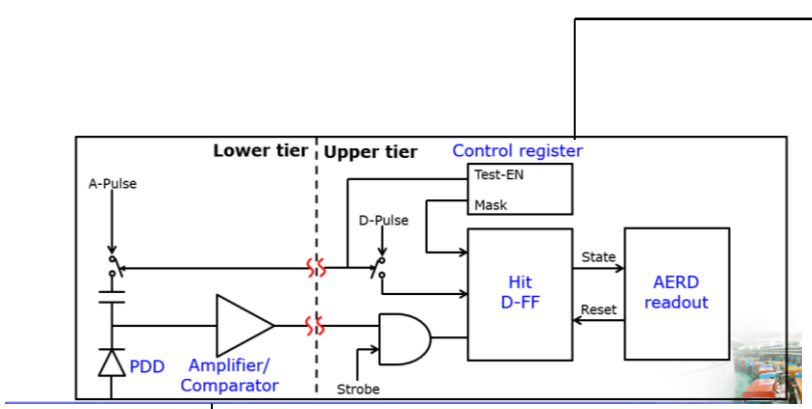
- Sensor+Analog+digital垂直堆叠
  - **2倍的**版图面积和金属布线资源
  - 比常规SOI像素芯片仅增厚10 um
  - 像素尺寸17um * 21um

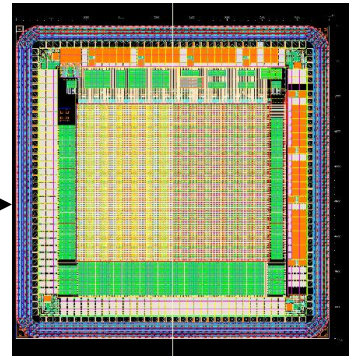


4 pixels arranged in 2 columns

CPV4_Upper

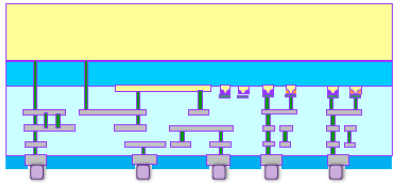


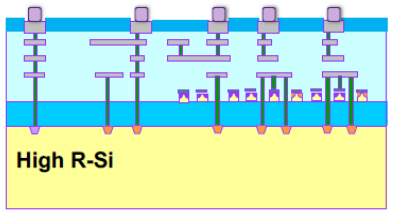




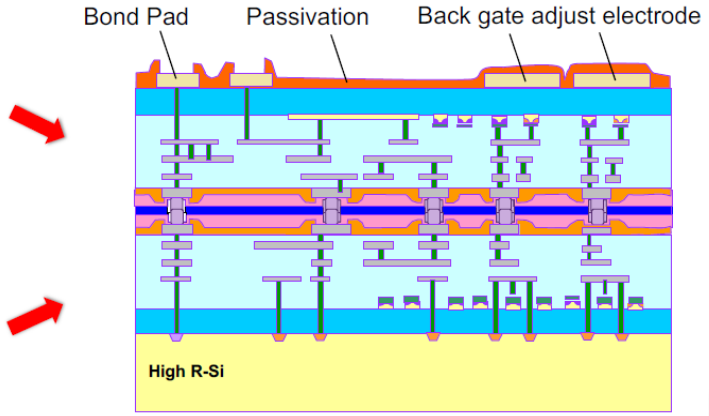
CPV4_Lower

Upper Chip





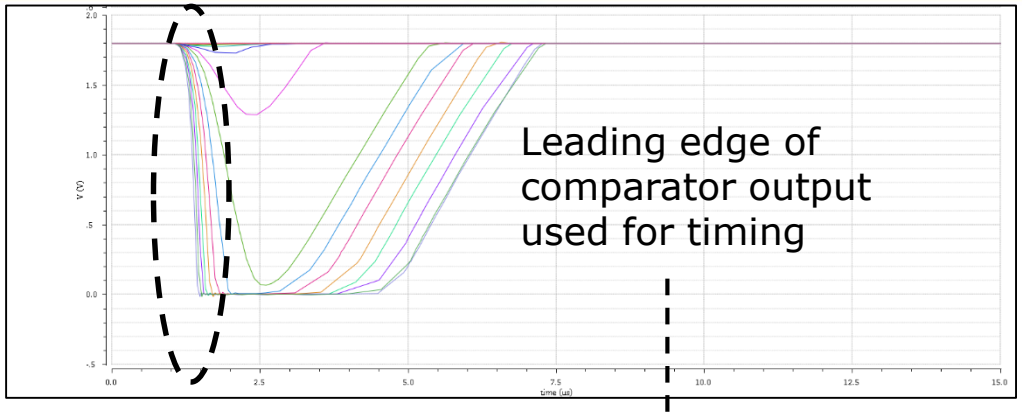
Lower Chip

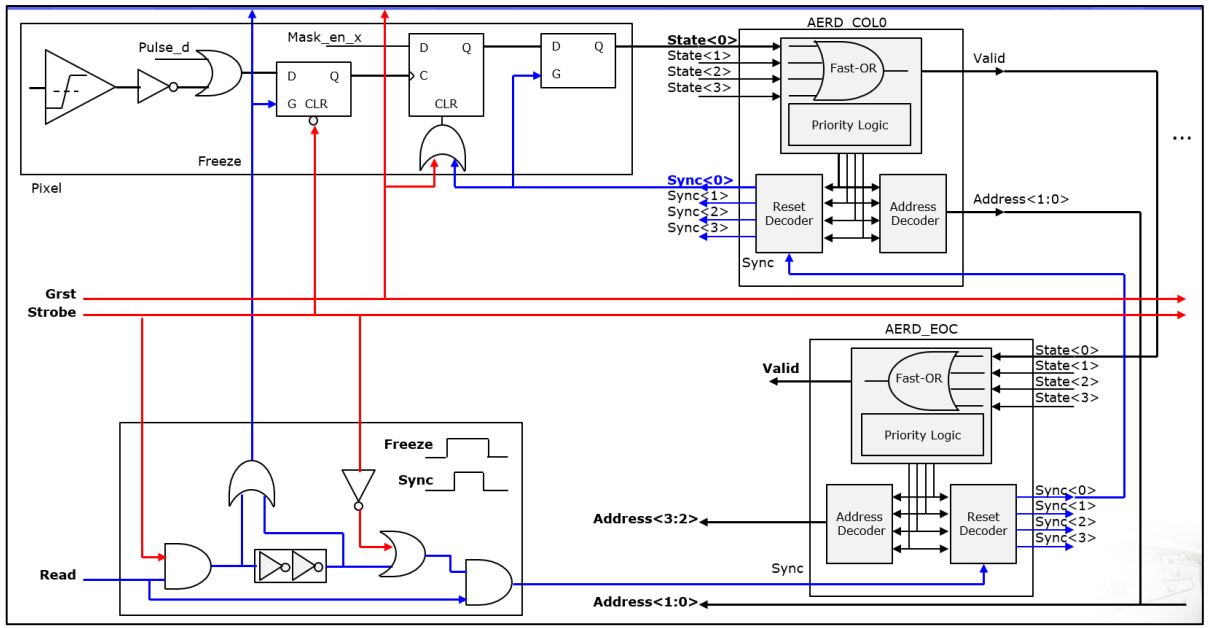


CPV-4设计方案

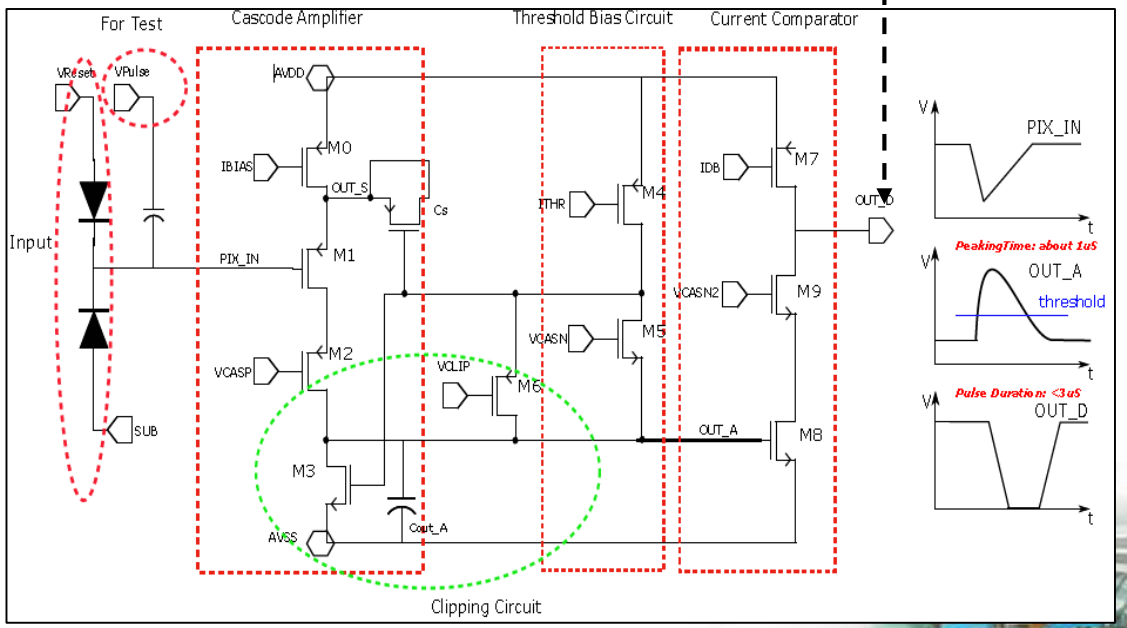
- Low power front-end: 连续工作模式
  - 在PDD工艺上的首次尝试（有技术风险）
- Data-driven readout (Asynchronous Encode Reset Decode*)
  - Using its leading edge for timing < 1us
- Power consumption ~ 50mW/cm^2

*Ping Yang, NIMA 785 (2015) 61-69





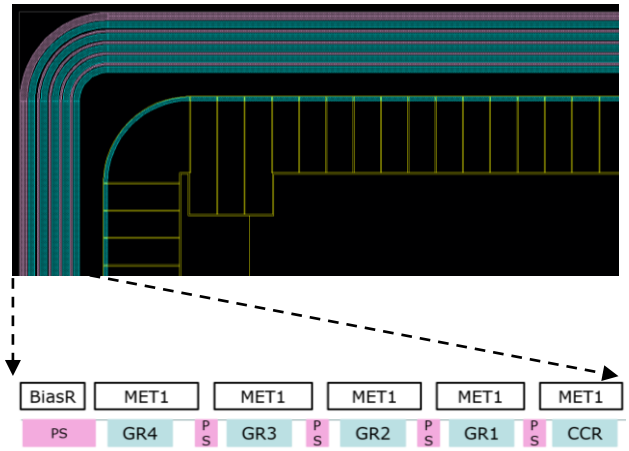
Explanatory diagram of CPV4 design scheme

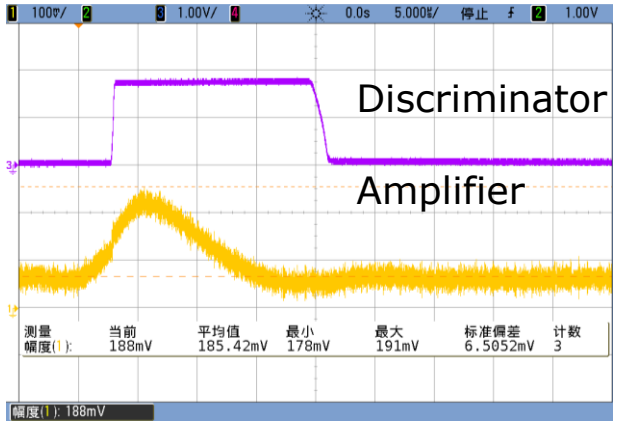


amplifier and comparator

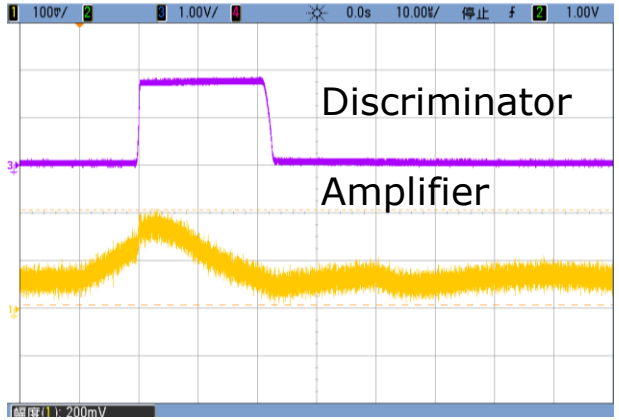
CPV-4初步测试结果

- 3D集成之前对CPV4_Lower和Upper独立测试
  - ✓ 漏电流相比CPV-3显著降低（PDD优化+Guard Ring）
  - ✓ PDD+模拟前端正常输出波形
  - ✓ 数字逻辑功能正常响应
- 首批3D集成芯片已完成
  - 已运抵高能所
  - 本月开始测试

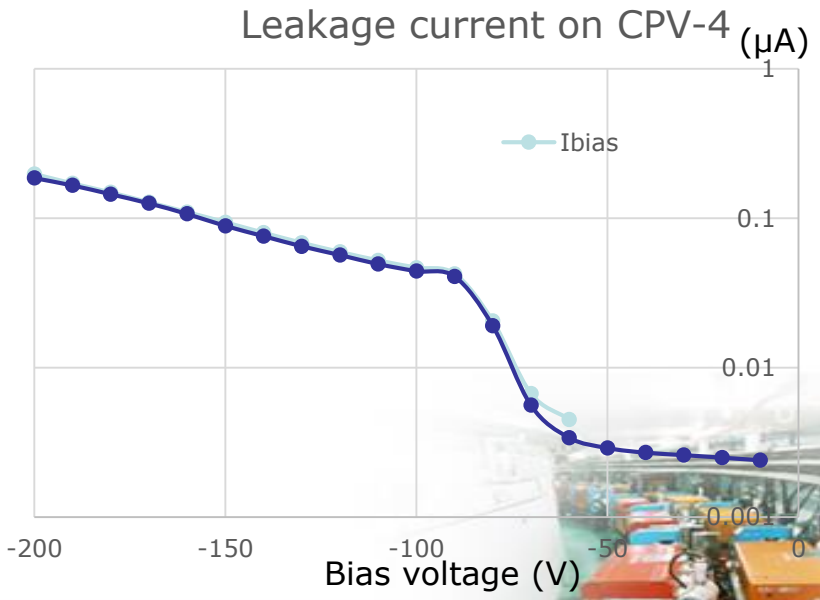




Analog frontend w/o PDD
Test charge injected ~ 100 e-



Analog frontend with PDD
Test charge injected ~ 750 e-



总结与展望

- 针对CEPC Vertex探测器对Silicon Pixel Sensor的要求开展了预研工作
  - 高分辨、低功耗、快读出
- 通过CPV-2的研究确定了影响空间分辨的关键参数
  - Pixel pitch ~ 16 um, Threshold < 200 e^-
- 在CPV-4的设计中引入3D垂直集成技术，提升了设计指标
  - Pixel pitch： 17um * 21 um
  - Time stamp： ~1us
  - Average Power: 50 mW/cm^2
- A telescope for particle beam test in preparation
  - 可用于CPV系列芯片的束流测试
  - 见董胜报告

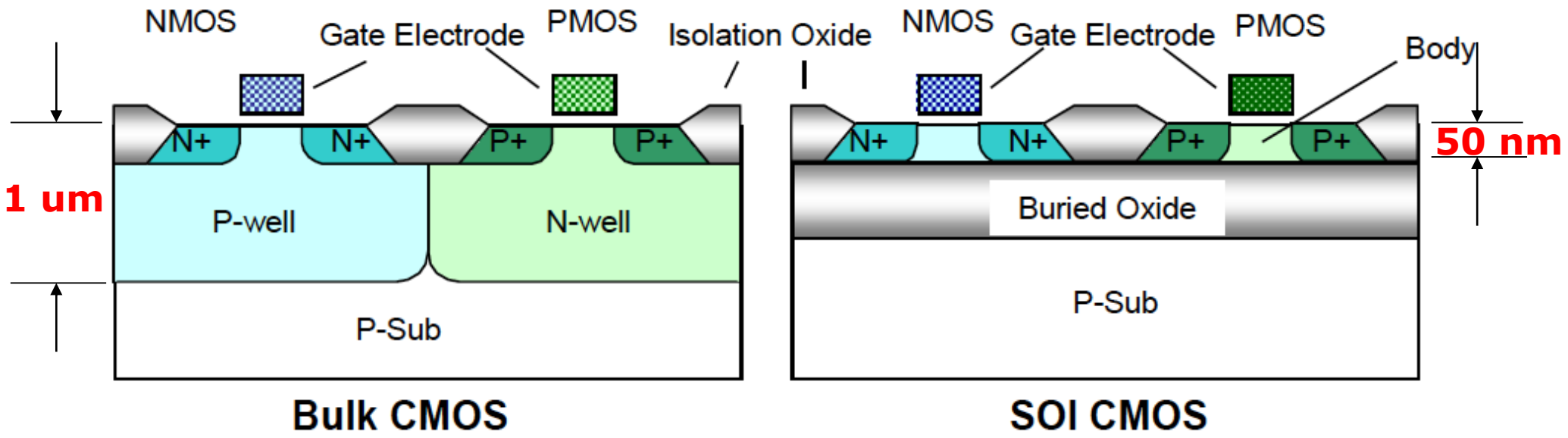
致谢

- 本工作得到国家自然科学基金（11935019，11575220，11375226）的资助
- 同时得到“核探测与核电子学国家重点实验室”的资助
- 以及“粒子物理前沿卓越创新中心”的资助

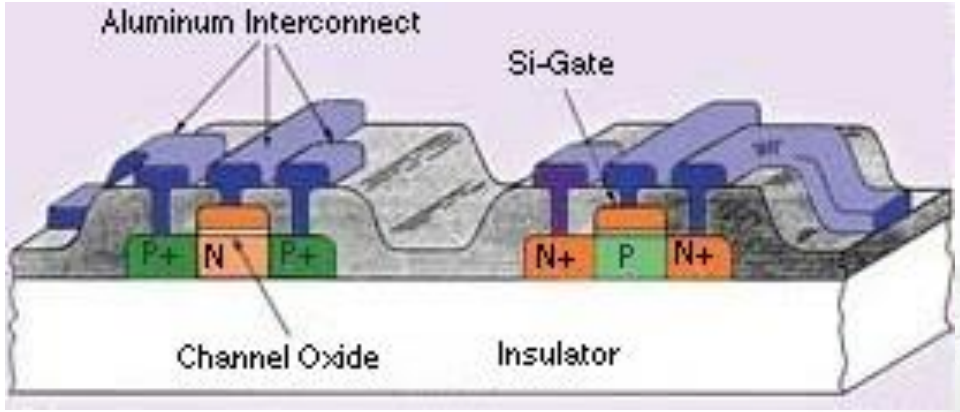
Thank you for your time!

- Backup Slides

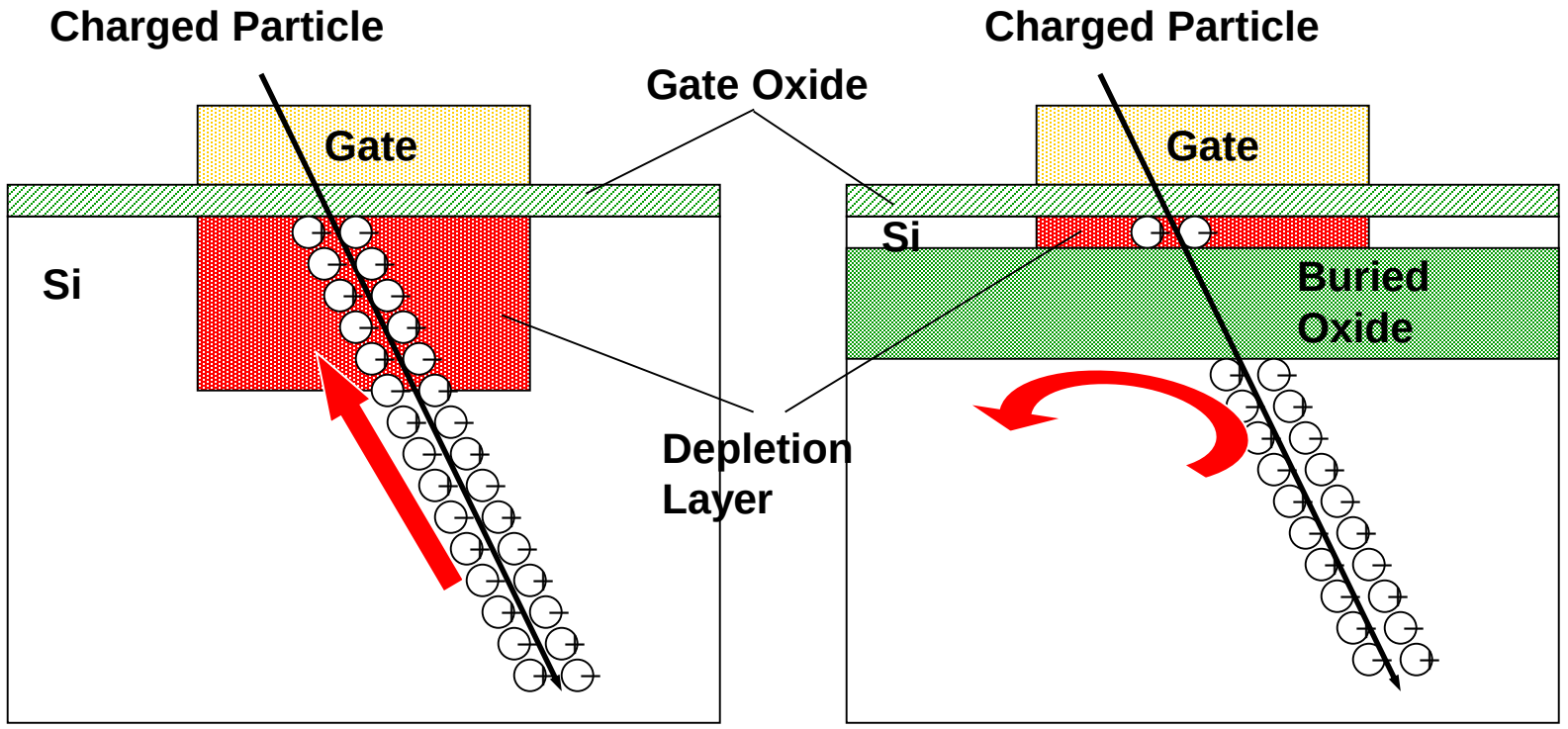
SOI集成电路工艺



SOI Transistors are completely isolated and has lower capacitance. So it is Low Power & High Speed.



Single Event Upset



Bulk Device

SOI Device

SOI has higher immunity to SEU due to its ultra thin body Silicon.