中国科学院高能物理研究所
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Exploration of new technologies for silicon vertex detector

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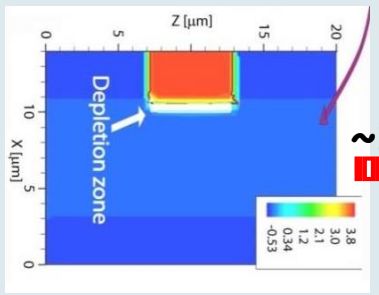
On behalf of the pixel detector study group

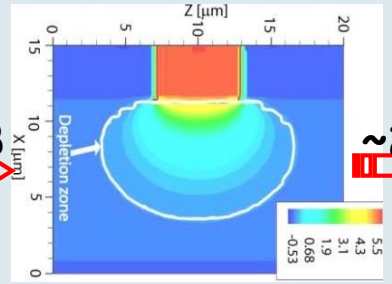
2022.2.23

A brief sketch of technology moving used by CMOS pixel sensors developed for vertex detector

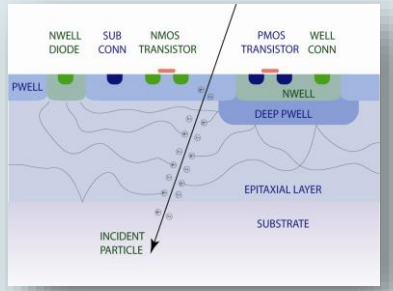
Technology node used was shrinking with industry progress. Brings benefits like: more functions integrated, faster charge collection, lower power per function.



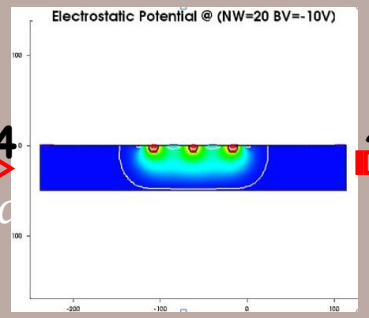
~2008



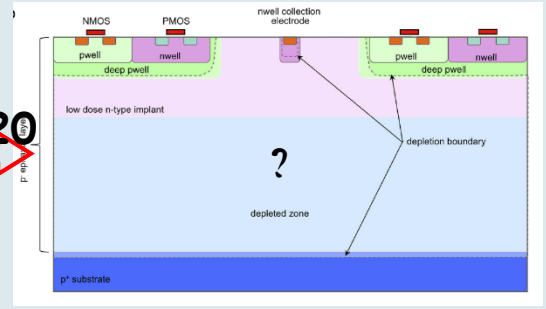
~2010



~2014



~2020



Charge collection: mainly on diffusion
Epi-thickness: 14-20 µm

~~diffusion~~ drift
Epi:~20 µm

drift,
Epi: ~10cm ?

Non-depleted, thick epi substrate:
several Ω·cm
• AMS 0.6 µm

Semi-depleted, HR epi substrate
500 – 2k Ω·cm
•AMS 0.35 µm

Quadruple-well CMOS:
both type of transistors admitted in the pixel array
> 1k Ω·cm
• TOWER 0.18µm

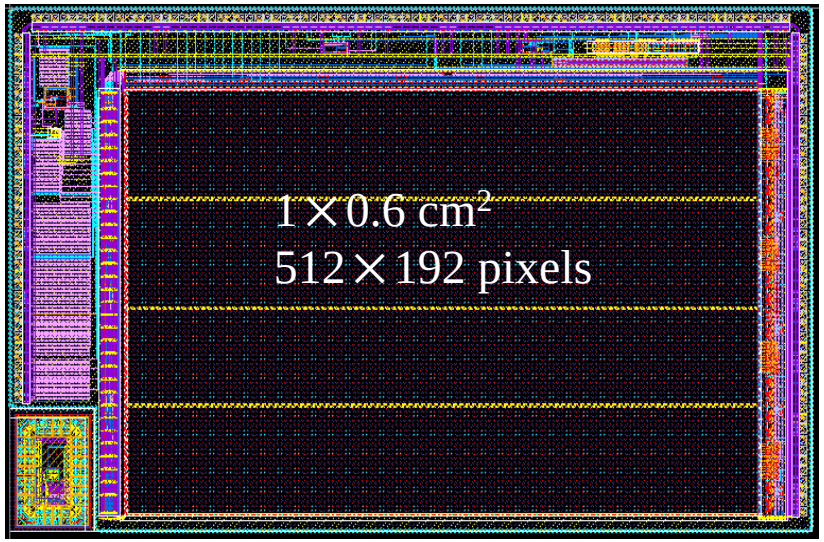
Fully depleted
> 1k Ω·cm
•ESPROS 0.15 µm
• TOWER 0.18 µm modified

Leading-edge technology node
•TOWER 65 nm
•HLMC 55 nm

> 10 years of development, the main technology for ALICE-ITK2, CBM-MVD and CEPC vertex detector R&D

Sensor performances achieved in Jadepix series：

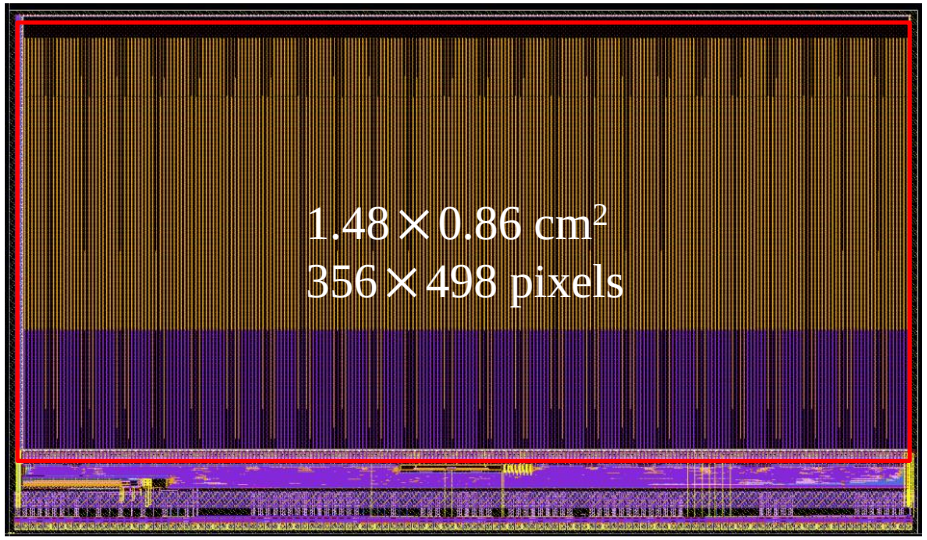
@developed by MOST1 Vertex detector study group



Layout of Jadepix3

Test performances:

- Noise： ~15e-
- Readout speed： 98.3μs/frame；
- Average power dissipation： ~52.8mW/cm²;
- Spatial resolution： σ_x ~2.7-4.4 μm, σ_y ~3.4-5 μm



Layout of Jadepix4，submitted： 2021.11.5

While the pixel analogue FE and periphery circuits keep similar with JadePix3： changed the pixel readout structure.

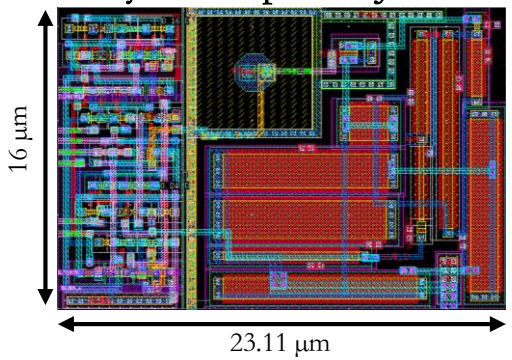
time resolution improved： ~100 μs -> ~1 μs;

paid by pixel size increased： 16μm×23μm -> 20μm×29μm

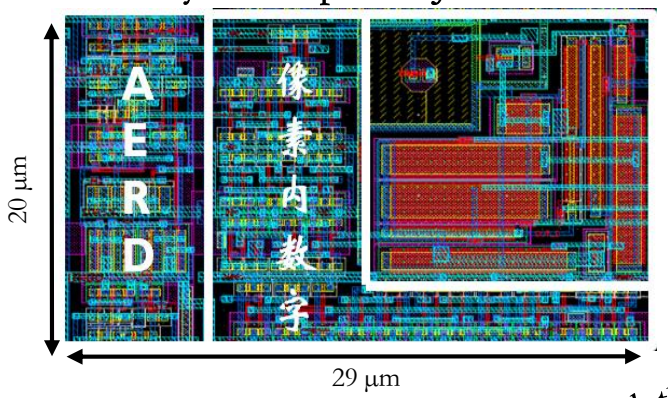
*Design details have been reported by Yunpeng on 2021/10/27

Interested performances may directly affected by new technologies

Layout of a pixel in JadePix3



Layout of a pixel in JadePix4



bring opportunities to shrink the pixel size of current design:

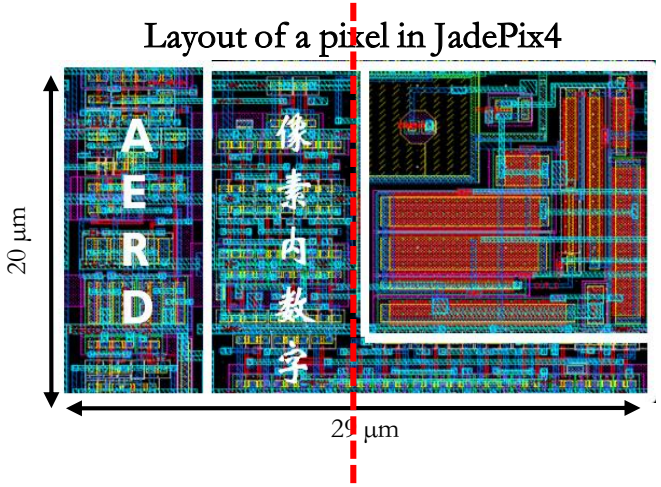
Specifications required by CEPC vertex sensor (from CDR)	
Spatial resolution≤ 3μm	**Required a pixel size ≤16 ×16 μm²**
Material budget ≤ 0.15%X_0 /layer	**Sensor back thinned down to ~50μm**
Average power dissipation	**<50 mW/cm²**
Time resolution	**~1μs**
Radiation tolerance	**< 3.4 Mrad / year , <6.2 × 10^{12} n_{eq}/ (cm^2 year)**

New technologies exploration introduced in this talk:

1. 3D technology;
2. Smaller technology node;
3. Stitching technique

may reduce the material budget to 1/3 of the requirement by removing the supporting structures.

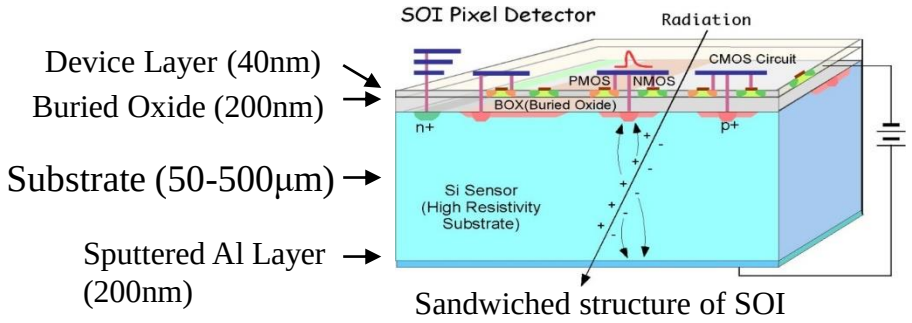
1. 3D technology： SOI-3D

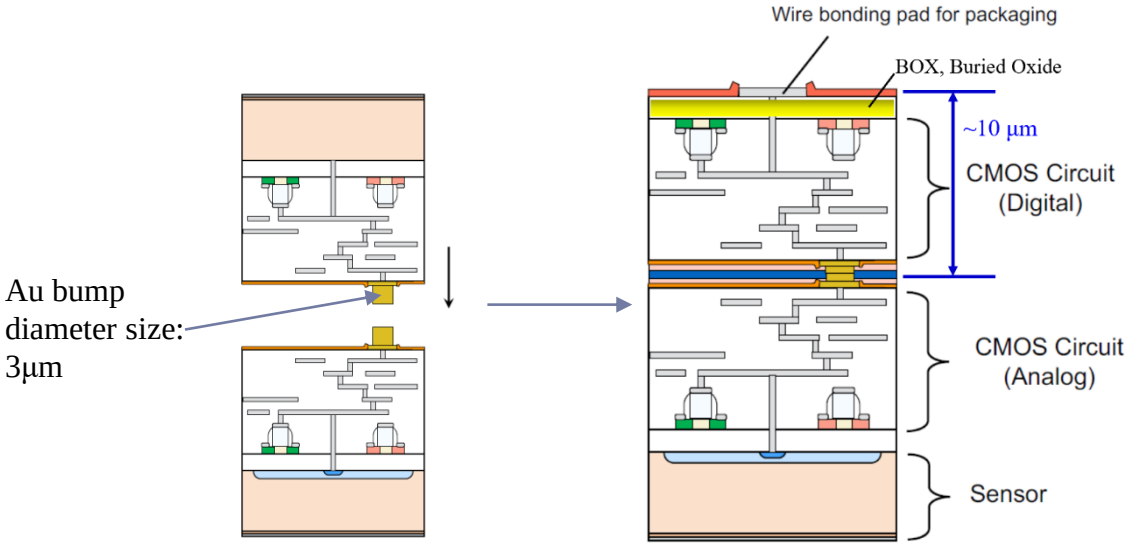


The idea is: split the pixel into two parts, then connected them vertically, so the pixel layout size could shrink to half.

Extra requirements for the 3D technology:

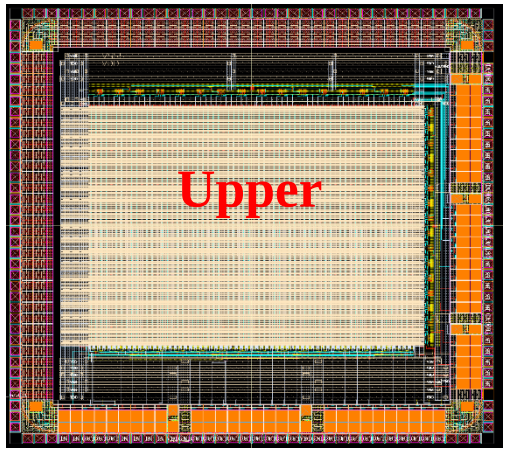
1. The bump size should be small enough to integrated at least two in the small pixel area;
2. The final thickness should meet the low material budget requirement.

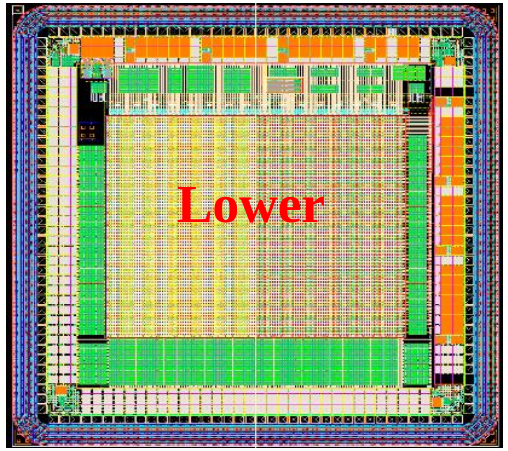




First try was on the SOI 0.2μm 3D technology,
Supported buy :“高精度SOI像素顶点探测器研究”, NSFC key program, 2020-2024

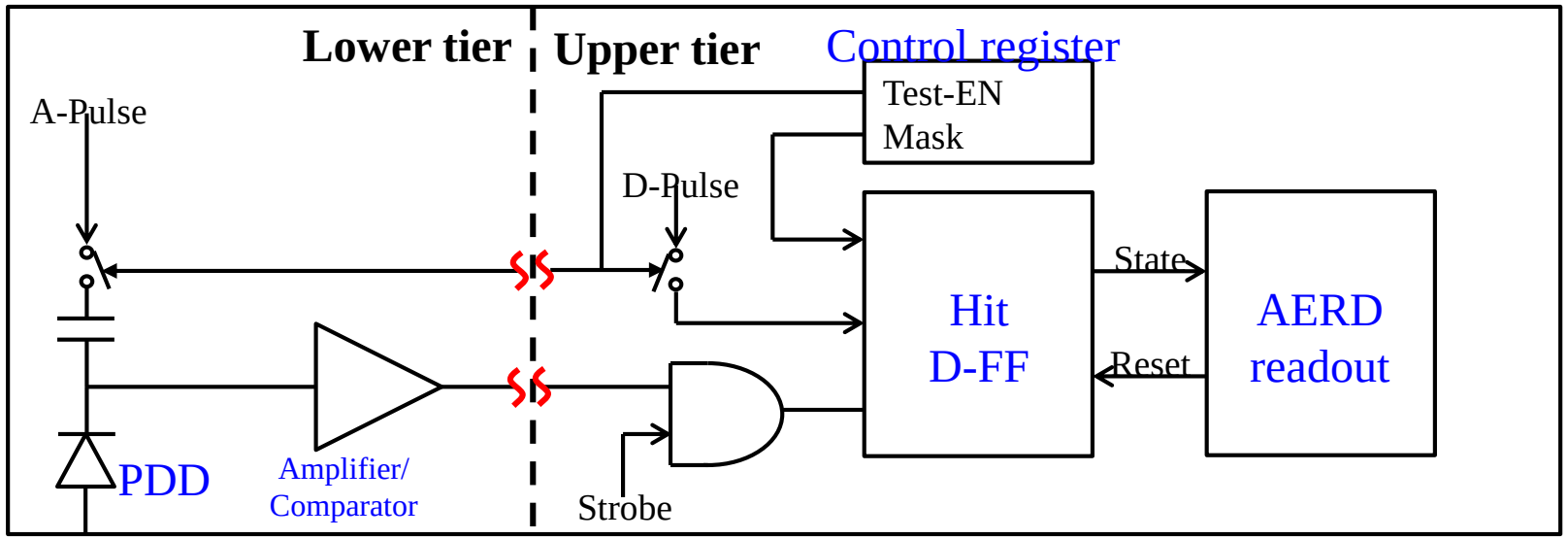
1. 3D technology： CPV4-3D design overview





Layout of CPV4-3D

Division of upper and lower functionalities

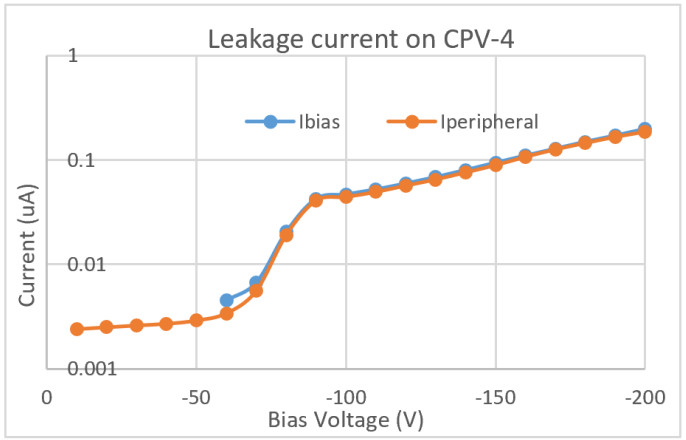


Pixel size	17.24×21.04 μm^2
Time resolution	~1 μs or ~3 μs in different operation mode
Pixel array	128×128
Chip size	4.5mm×4.5mm
Delivered	Nov. 2020

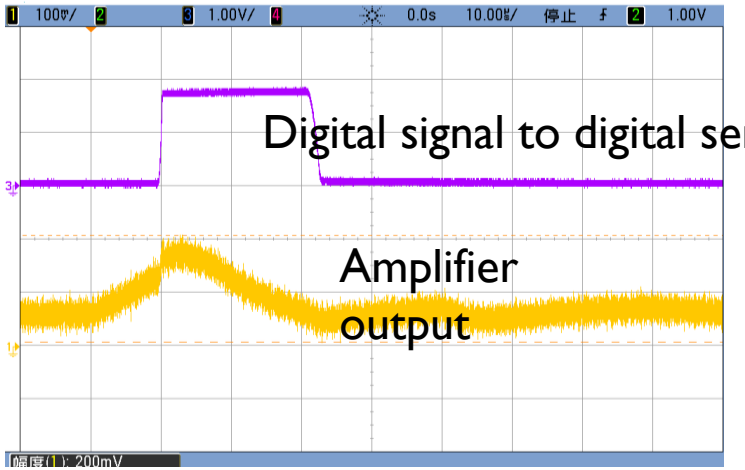
- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit D-Flipflop + Control register + AERD readout
- **2 vertical connections** in each pixel: comparator output and test switch;
- Analog and Digital power/ground are also separated

@ design details was introduced by Yunpeng on 2020/12/28

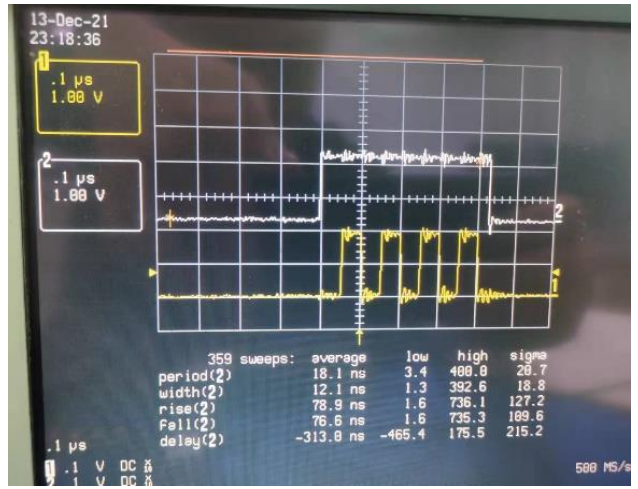
1. 3D technology : basic functions of the two sensors have been validated



1. Leakage current on CPV4, the analogue sensor can be biased at -200V.

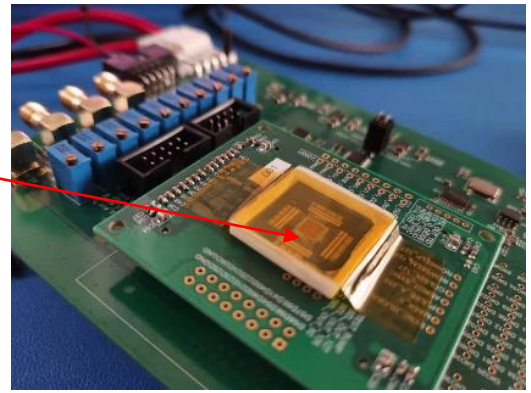


2. Pulse inject test of analogue sensor.

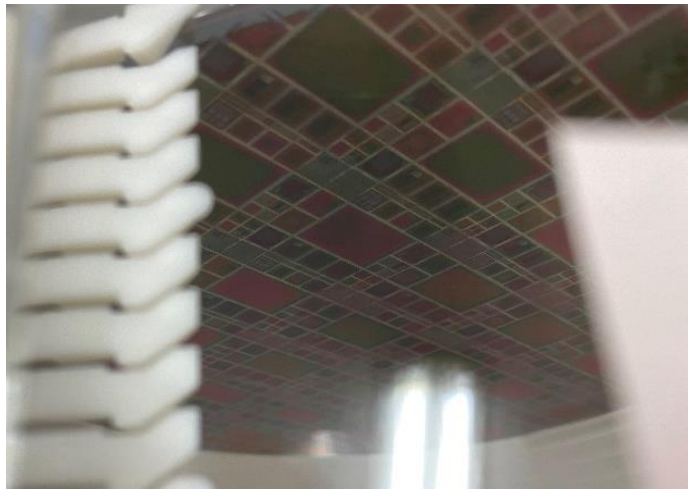


3. Pulse inject test of digital sensor.
-Valid signal from sensor (white line)
-Reset signal after read the pixel addresses. (yellow line, 4 pixels was fired)

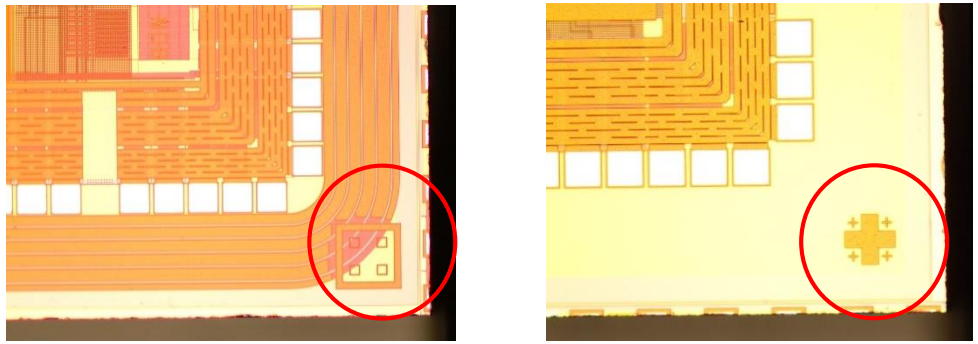
CPV4 digital sensor bonding on test system



1. 3D technology: ongoing work



Ordered an extra wafer for 3D integration



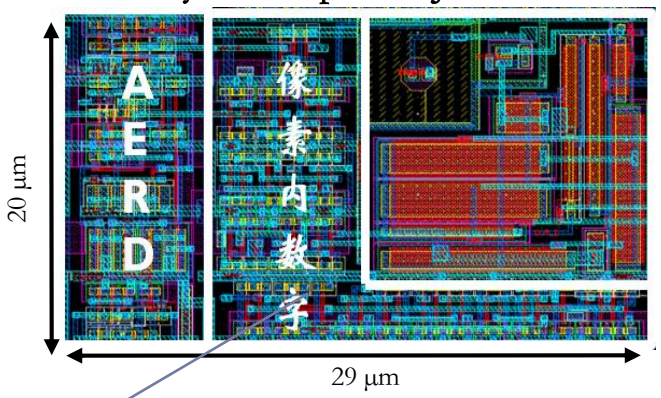
Alignment mark on the two sensors

- 3D integration (by foundry in Japan) order is still in-progress;
- A DAQ and test control system is in developing;

2. Smaller technology node： more possibilities

Per digital function: smaller layout size; lower dynamic power consumption (directly proportion to core VDD^2)

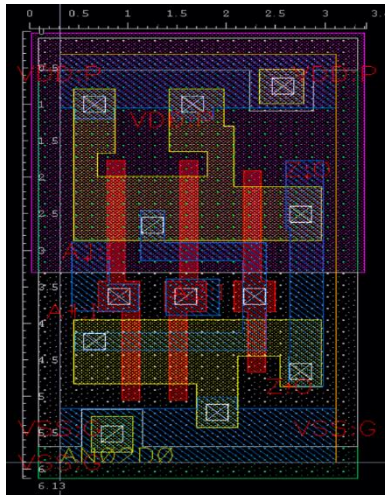
Layout of a pixel in JadePix4



Digital part: 133 transistors, ~324 μm²

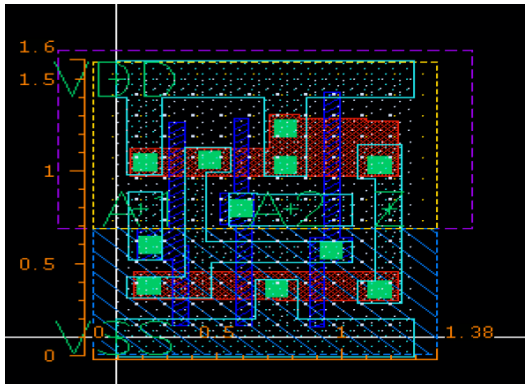
~1/8

Digital part may be reduced to: ~16*2.5 μm²



6*3 μm²

~1/8



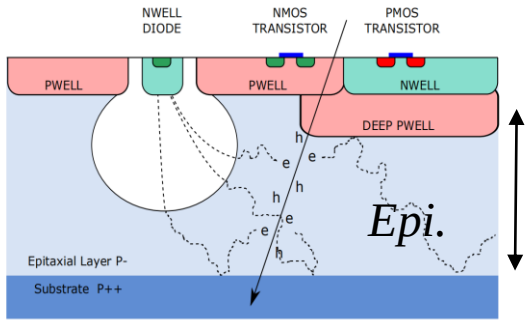
1.6*1.4 μm²

Layout of a standard digital cell “and” in Tower 0.18μm (left) and HLMC 55nm process (right).

It seems possible to realize current pixel design in 16*16 μm², using a smaller technology node around 65/55nm.

2. Smaller technology node： HLMC 55nm

- Supported by：中俄“重离子超导同步加速器”国际合作研究项目，National key research and development program, 2020-2025
- Design team from: IHEP, CCNU, IMP



Some studies have been started in HLMC 55nm process:

1. Process modification;

2. Diode, and charge collection study;

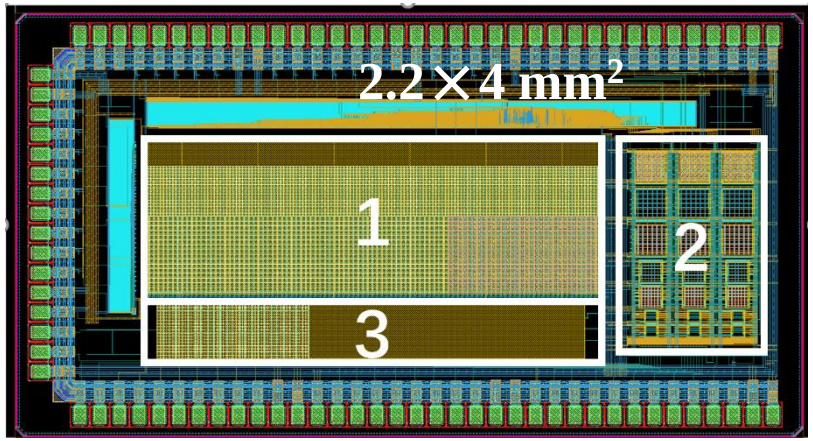
3. Necessary electronic function blocks design: DAC , buffer, PLL and so on.

Basic information:

- 55nm CIS process;
- Voltage for core transistor 1.2V， for IO transistor: 3.3V;
- Epi. thinness: 5.4 μm
- Resistance: 10 Ω·cm
- Quadruple-well process:
  - Deep P-well and deep N-well injection parameters were customer designed。(by TCAD simulation)

2. Smaller technology node： 1st prototype overview

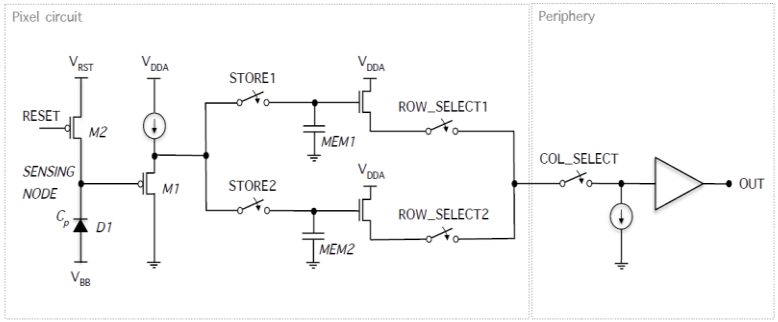
Diode and charge collection study:



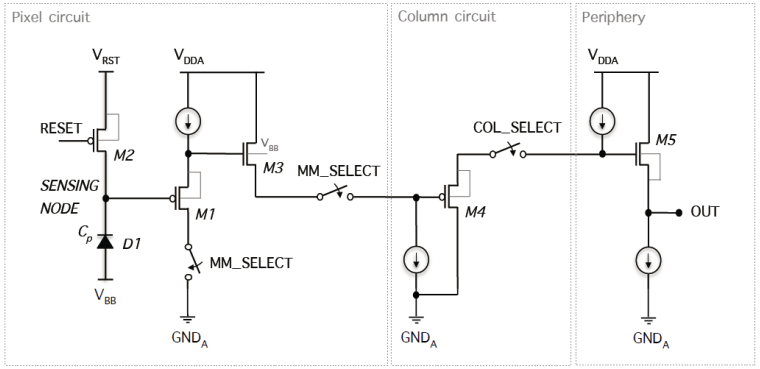
Layout of the first prototype on HL55nm process to study diode and charge collection， submitted: 2021.6

Including 42 sub pixel arrays：

- 3 type of pixel pitch size: 8 / 16 / 24 μm;
- 6 type diode structures: different surface and footprint size;
- 3 type of in-pixel circuits:
- One pure diode matrix for leakage current/equivalent capacitances test

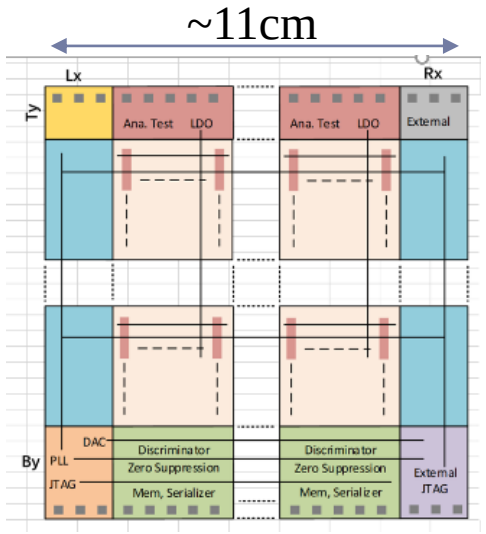


In-pixel circuits in block1: for charge collection amount study;



In-pixel circuits in block2: for charge collection time study;

3. Stitching technique: wafer-scale sensor



Floor plan of our first chip design with large scale.

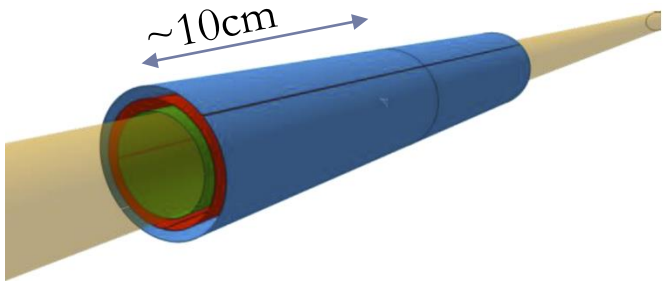
- Chip size 11cm *11cm,
- XFAB 0.35μm process;
- Rowling-shutter readout mode;
- Plan to submitted in Apr.

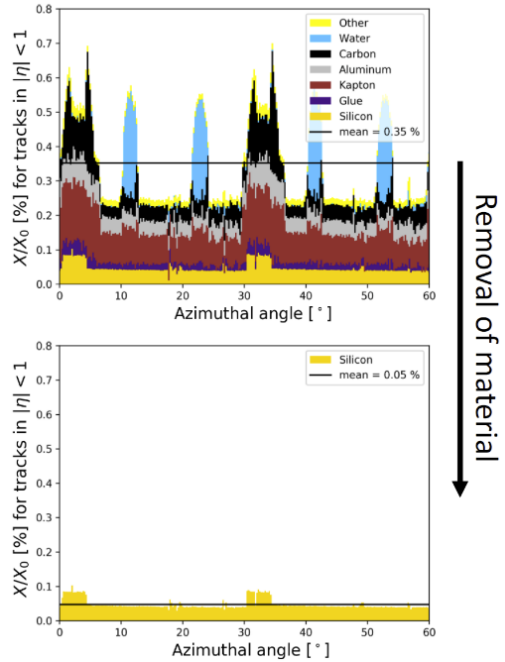
- Normally a chip size is limited by the mask size: < ~2cm × 2cm;
- Stitching-technique could extend the chip size ~100 times larger: < ~30cm × 30cm;

- Supported by "基于大面积超薄CMOS像素传感器BESIII内径迹室关键技术研究" NSFC KEY Program, 2021 - 2024
- Aiming for the application of BESIII inner tracking system;
- Deign team from: IHEP, Shandong University, Harbin Institute of Technology , Dalian Minzu University

Beyond CEPC expect:

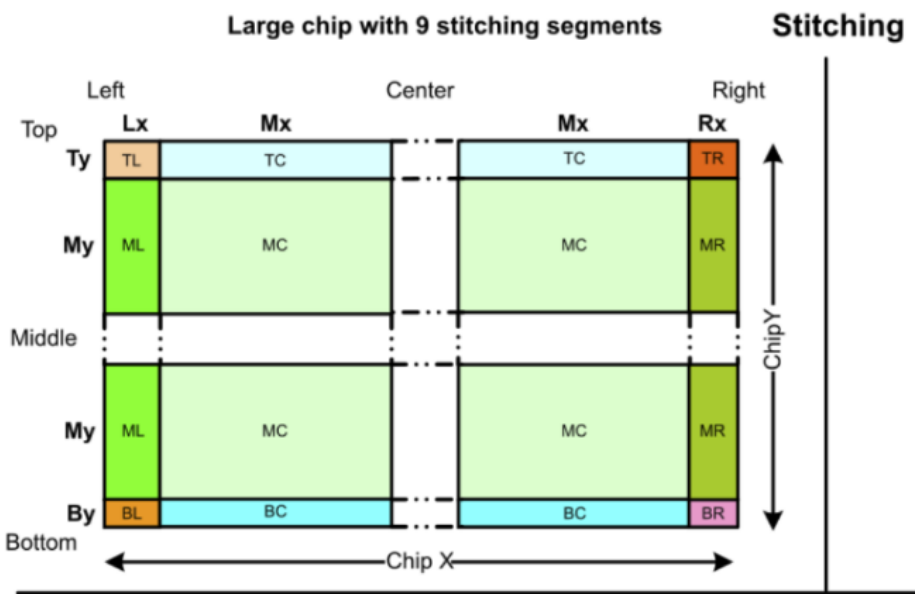
- Wafer-scale sensor, after thinned down to 50μm, can be bend like a A4 paper, so the so-called "self-support" structure would be possible;
- Material budget of the tracking detector system could be significantly reduced, less affect to particle multiple scattering。





Material budget of one layer is possible down to ~0.05% X_0 (1/3 of CEPC expectation in CDR)

3. Stitching technique: general experiences



Sketch map of how masks organized for a wafer-scale large sensor

1. A wafer-scale sensor may include: ~100 MC, ~10 ML/MR/TC/BC, and 1 TL/TR/BR/BL;
2. The block layout with a same name have to be exactly the same. Need special consideration for the periphery/pixel circuits design, not only the function but also how to realize physically;
3. Parasitic Capacitances on long signal/biasing lines may increase ~10-100 times. Has to do something to reduce this influence to the power and speed.
4. Power-ring, IR drop should be taking care;

Summary and Outlooks

Beside Towerjazz 0.18μm CIS process, 3 new technologies/techniques exploration is ongoing, which may bring more possibilities for CEPC vertex detector R&D: eg. Higher spatial resolution, lower power dissipation/per function, less material budget…….

An ideal technology may have features like:

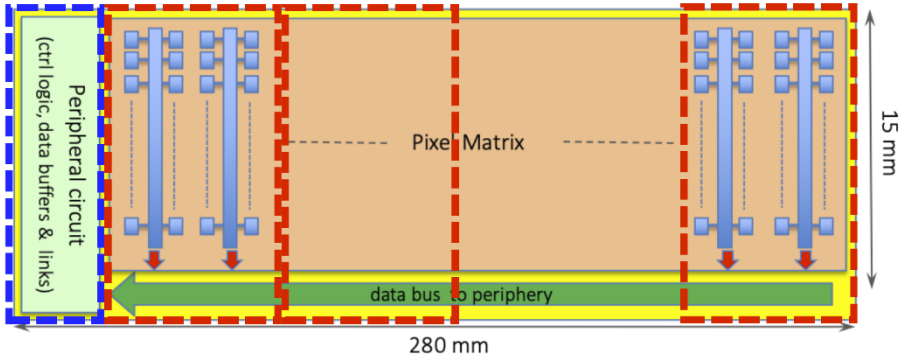
- 65/55nm CIS;
- ~10μm thick, high resistance epi.
- Quadruple-well process;
- Custom process modification possible;
- Stitching technique support;

Outlooks:

- Looking for an accessible foundry provide the technology has close features we expect;
- Gain more design experiences in smaller technique node: eg. leakage current, lower voltage margin for transistors…….
- Gain more design experiences and ideas for a wafer-scale chip;
- Exploring new ideas for the affect of "time resolution", " power dissipation" , "radiation tolerance" of new technologies;
- Further test of the CPV4-3D : eg. "yield"

Thank you for your attention!

Wafer-scale chip – architecture



- Uses ALPIDE as a baseline architecture, double column priority encoders
- One thing to take into account is that stitching requires a regular, periodic structure
- Chip is split into 2 sections:
  - Periphery – housing data, logic and electrical interfaces
  - Pixel matrix – housing pixels and data bus to the periphery and repeated N times