Requirements on the process for the next generation CMOS pixel sensor

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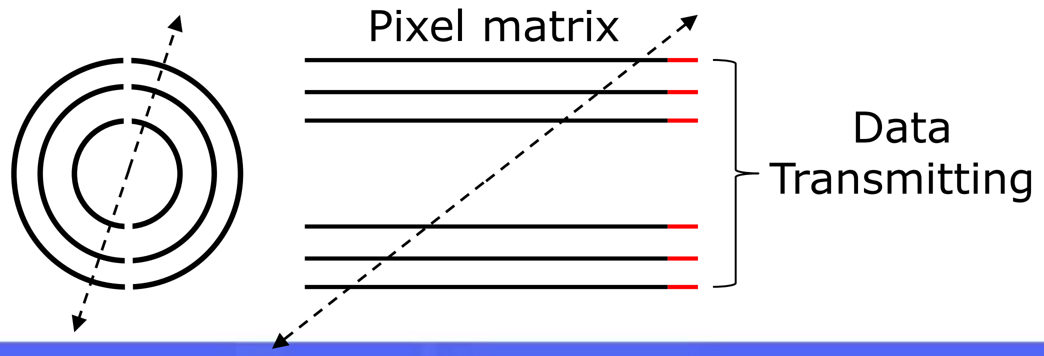
Outline

- Motivation
- Strategic approach
- What we want
- What we may expect as the first step
- Summary

Disclaimers:
- This talk is **NOT** results of direct discussion with any capable foundry.
- The contents in this talk are more of personal view shared for internal discussion.
- The requirements listed here are subject to change when it is necessary.

Motivation

- Wafer-scale single sensor for one **half cylinder**
  - 12-inch wafer can accommodate 15cm * 25cm large sensor
  - Bendable when thinned down to < 50 um
- Extremely **low material budget**
  - Only silicon sensor in the acceptance region, gentle air cooling
  - Data transmitting as concentrated heat source outside the acceptance region
  - All power and signal lines integrated into the **stitched** sensor
- Improved position resolution
  - To shrink the pixel pitch with smaller feature size of MOS transistors

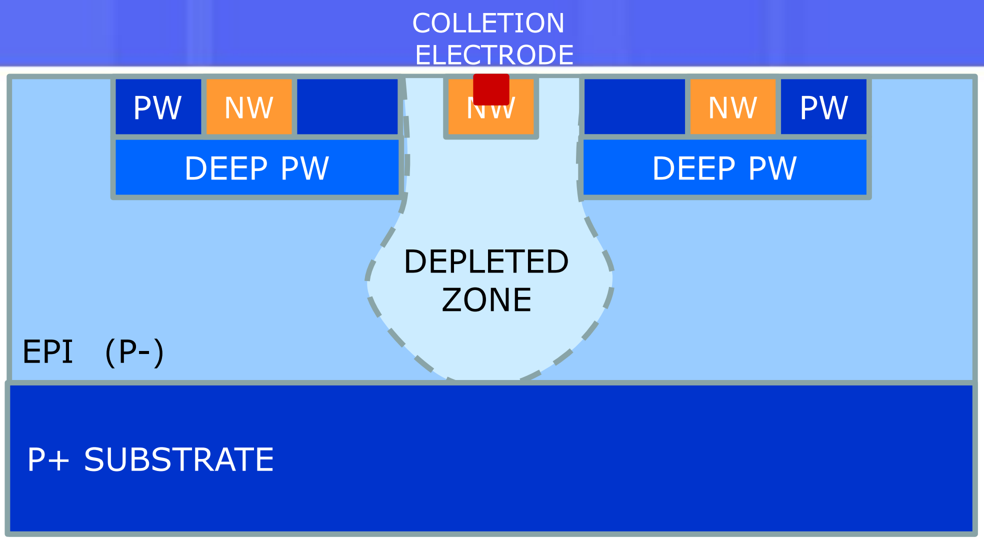


ECFA detector R&D roadmap

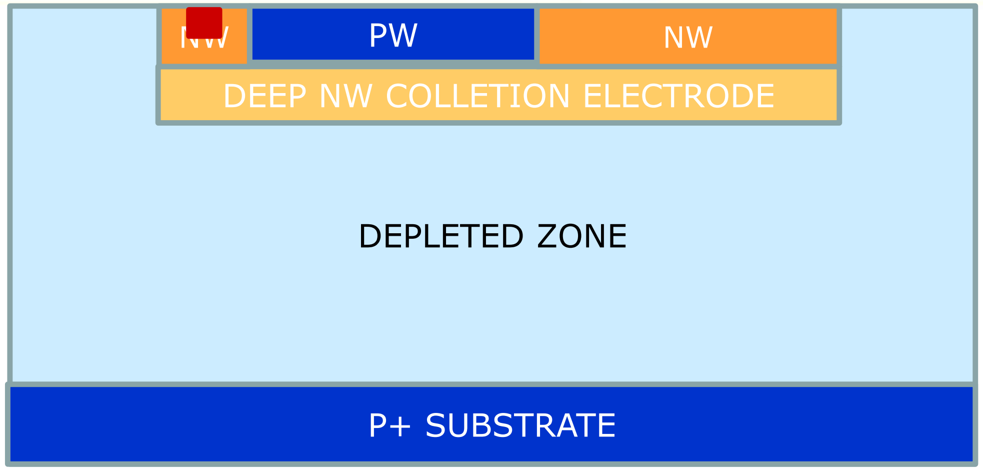
- 65 nm stitching process for the next generation CMOS pixel sensor
  - To cover the developments and experiments in 2020-2030
  - Specs to converge with hybrid in the long run

"Technical" Start Date		< 2030			2030 -2035		2035 -2040	2040 - 2045		> 2045	
		ALICE LS3	Belle II CBM	NA62	LHCb, ATLAS, CMS ($\gtrsim$ LS4)[7]	ALICE 3 - EIC	ILC	FCC-ee	CLIC	FCC-hh	Muon Collider
MAPS	technology node[1]	65 nm - stitching	65 nm - stitching			28 nm		$\lesssim$ 28 nm		$\simeq$ 10 nm	$\lesssim$ 28 nm
	pitch	10 - 20 μm	10 - 20 μm			pitch $\lesssim$ 10 μm for $\sigma_{hit} \lesssim$ 3 μm in VD					
					Reduce z-granularity in TK - pad granularity in analog Cal.						
	wafer size[2]	12"	12"			12"					
	rate[3]		O(100) MHz/cm^2						5 GHz/cm^2	30 GHz/cm^2	
	ultrafast timing[4]				$\sigma_t \lesssim$ 100 ps					$\sigma_t \lesssim$ 20 ps	
	radiation tolerance				3 x 10^{15} neq/cm^2					10$^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	
Planar/3D/Passive CMOS	technology node[1]				ASIC 28 nm	ASIC 28 nm		ASIC $\lesssim$ 28 nm		ASIC $\simeq$ 10 nm	ASIC $\lesssim$ 28 nm
	pitch				$\lesssim$ 25 μm in VD	$\lesssim$ 10 μm for $\sigma_{hit} \lesssim$ 3 μm in VD					
					$\lesssim$ 50 μm for $\sigma_{hit} \lesssim$ 10 μm in Trk						
	wafer size[2]					12"					
	rate[3]				6 GHz /cm^2					30 GHz/cm^2	
	ultrafast timing[4]			$\sigma_t \simeq$ 50 - 100 ps		$\sigma_t \lesssim$ 100 ps				$\sigma_t \lesssim$ 20 ps	
	radiation tolerance				6 x 10^{16} neq/cm^2					10$^{18(16)}$ neq/cm^2 VD/Cal.(Trk)	

CIS or HV-CMOS



CIS



HV-CMOS

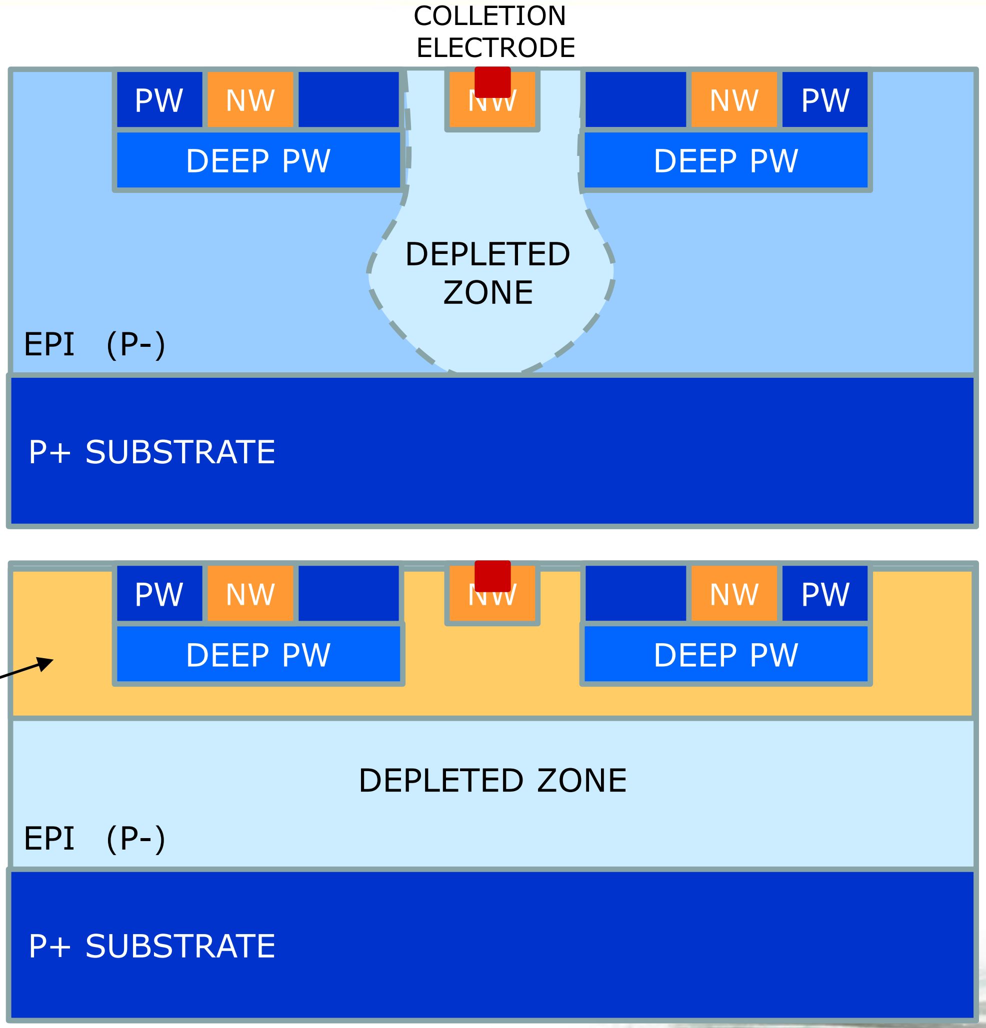
- Choice seems obvious: CIS for vertex, HV-CMOS for tracker
- Be reminded that the choice depends on
  - How much depletion achieved
  - Availability and cost
  - Stitching option
  - **Low power and radiation hardness**
- Other possible technologies, such as placing the junction on the backside of wafer

Maximum or minimum requirements

- Maximum requirements can stretch our capability to the utmost potential
  - 65/55 nm CIS process with stitching option
  - Limited to a few major foundries in the mainland of China
  - Difficult but should try firstly
- Minimum requirements allows more flexibility and accessibility
  - 180 nm or smaller process line
  - 8-inch wafer without stitching
  - Open to possibly more foundries and process lines accessible
  - A survey may be made depending on situations.

What we want

- CIS process
  - 12-inch wafer, **stitching**
  - 65nm / 55nm feature size
  - N-Well / P-Well / Deep-N-Well / **Deep-P-Well**
  - 5~6 metal layers
- Starting material (to be validated and verified by the foundry)
  - Thickness of epitaxial layer **~10 um**
  - Resistivity **~kΩ·cm**
- Possible adding-on implantation
  - **Low dose N-TYPE IMPLANT**
  - To improve the NIEL and/or CCE



CIS

What we may expect as first step

- Manufacturing process
  - 12-inch wafer, **stitching**
  - 65nm / 55nm feature size
  - N-Well / P-Well / Deep-N-Well / **Deep-P-Well (**User obliged to define and verify it**)**
  - ~~5~6~~ **4** metal layers
- Starting material (standard wafer)
  - Thickness of epitaxial layer **~~~10~~ 5 um**
  - Resistivity **~~~kΩ·cm~~ 10 Ω·cm**
- ~~Possible adding-on implantation~~
  - **Low dose N-TYPE IMPLANT**
  - To improve the NIEL and/or CCE
- **Long turnaround time** due to the chip shortage in IC industry

Process Simulation

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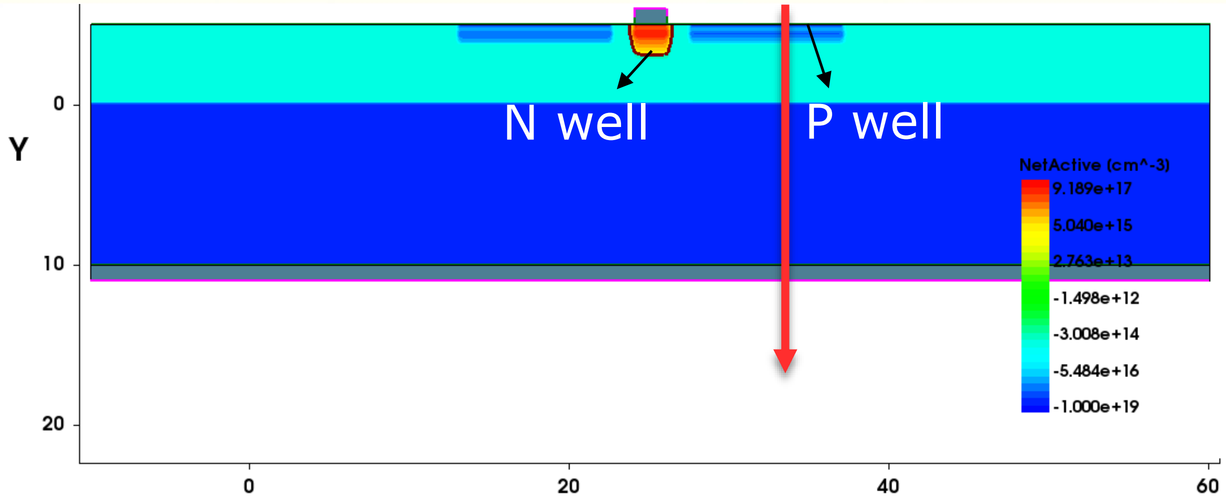
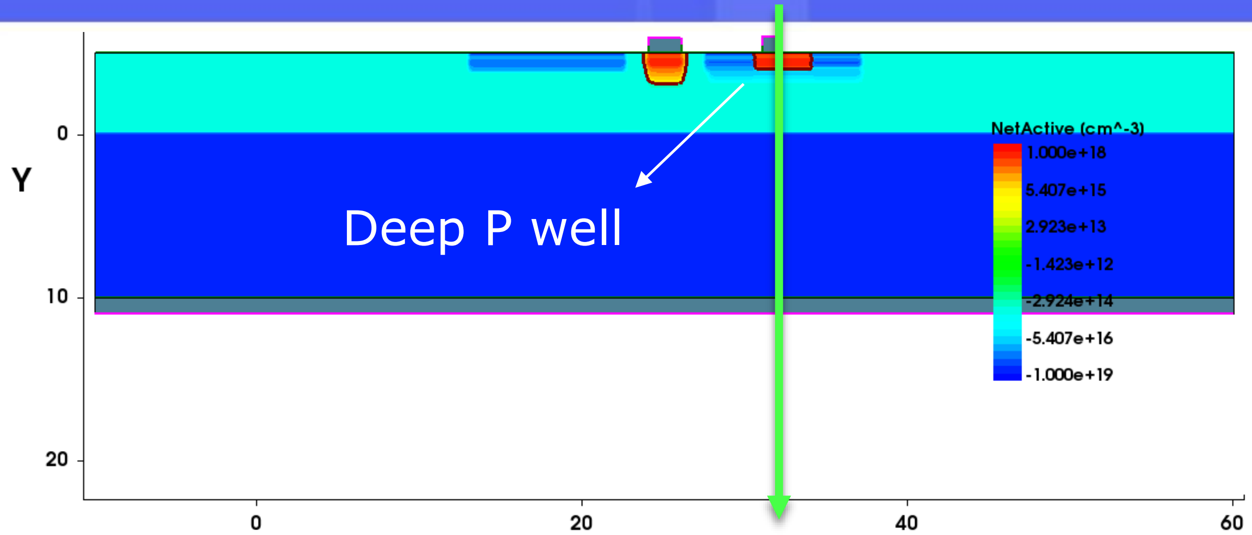
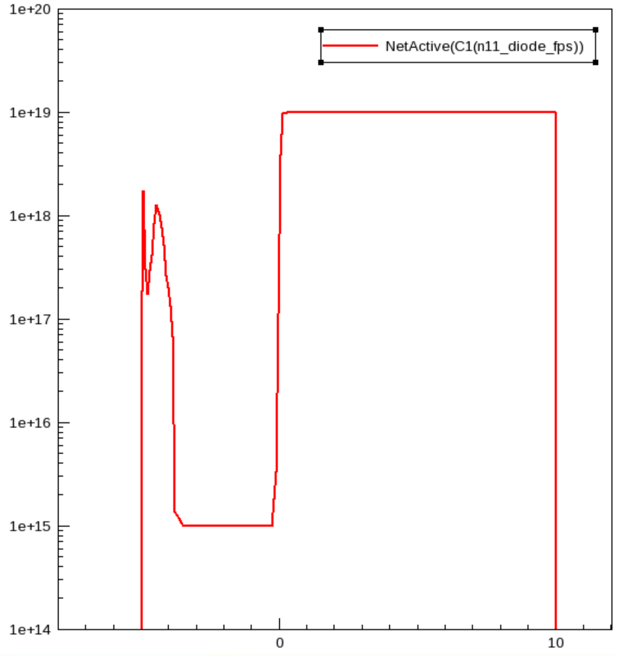
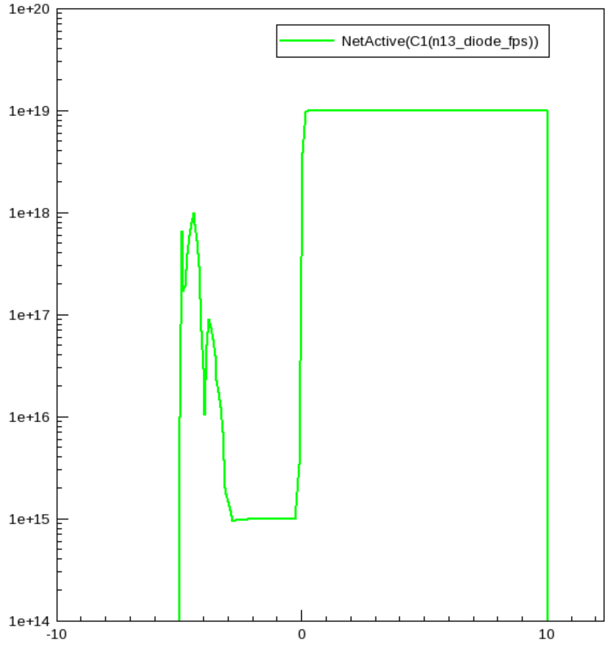




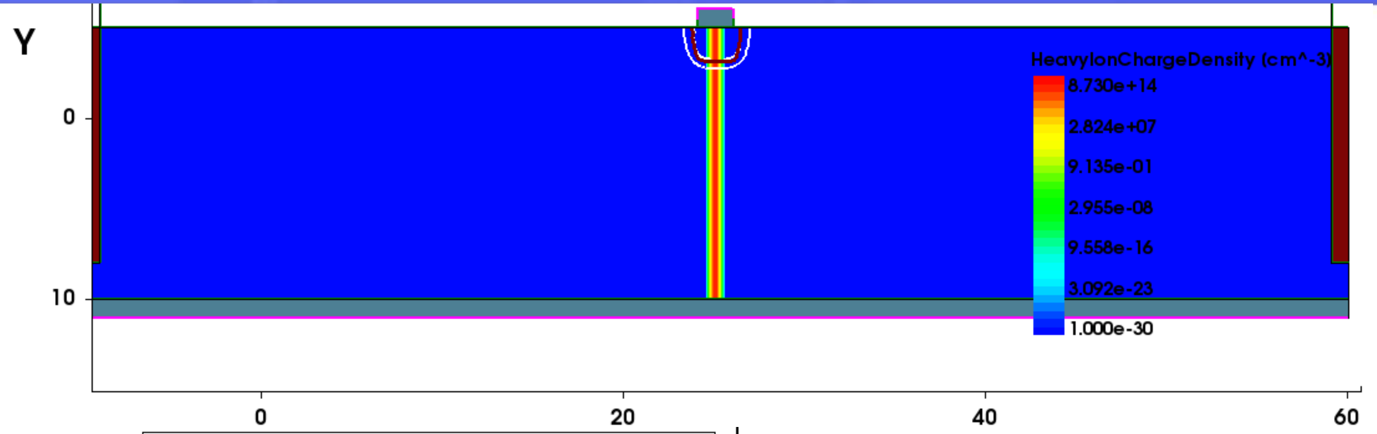
- Epi. thickness: **~ 5** um
- Epi. resistivity: **~ 10** Ω · cm
- DPW implant: **defined by user**
- Width of pixel: 24 um
- Diode width: 2 um
- Spacing: 0.5 um

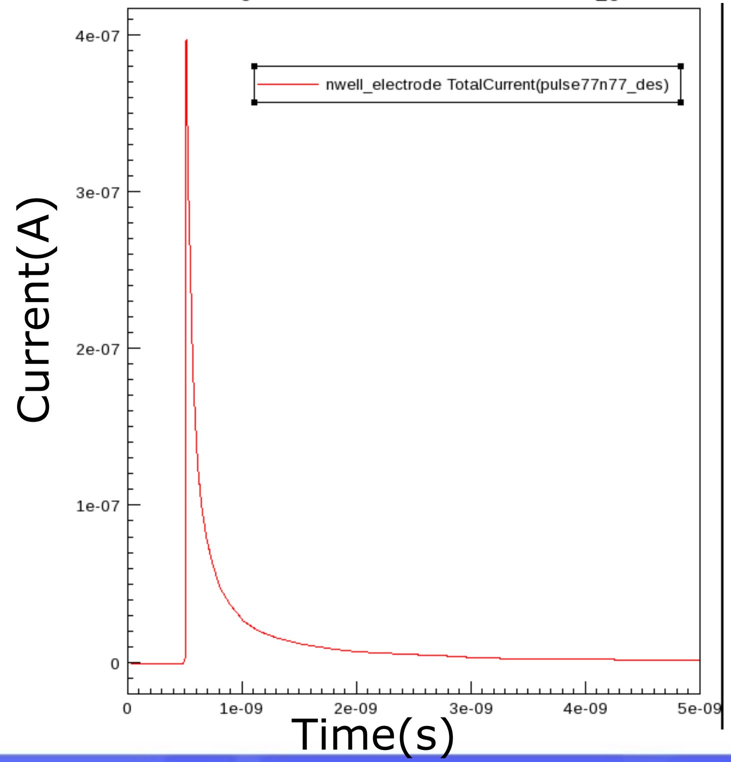


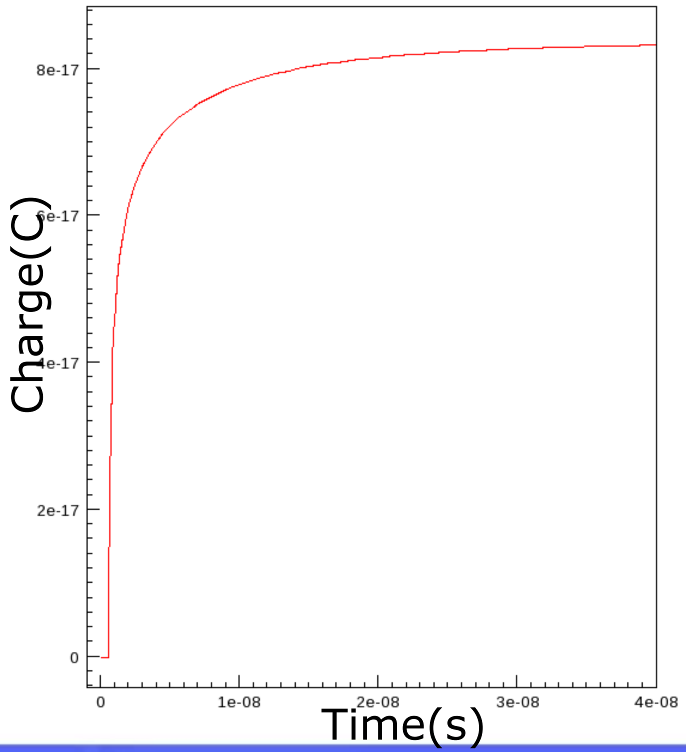


Simulation of Charge Collection

Chunhao Tian / USTC







- MIP: 80 pairs / um
- Charge deposited: 400e (epitaxial layer)
- Charge collected: **526e**
  - Substrate contributing 20% of charge
- Charge collection time: **5ns** (90%)
  - Hit on the center of N-Well

Summary

- Next generation CMOS pixel sensor based on 12-inch wafer and stitching
  - Extremely low material budget
  - Improved position resolution
- Maximum and minimum requirements are listed for discussion
  - **65/55 nm CIS process** with **stitching** option on **12-inch** wafer
  - **90 nm or even larger** process line on **8-inch wafer w/o stitching**
- Modification of process can rely on users, while customized wafers have to be accepted and validated by foundry.

Thanks for your time!