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# Status of CEPC MOST2 vertex detector prototype

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On behalf of the CEPC MOST2 Vertex detector study group
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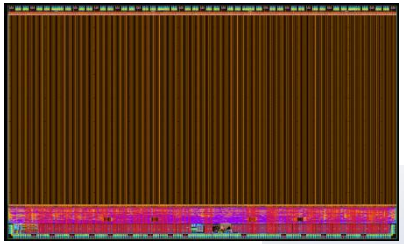
# Outline

- Overview of MOST2 vertex detector R&D
- Recent test results of TaichuPix2 chip
- Updates on mechanics
- Summary

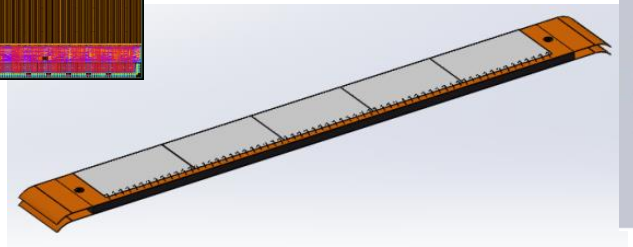
# Overview of MOST2 vertex detector R&D

- **Can break down into sub-tasks**
  - CMOS Pixel Sensor chip R&D
  - Detector layout optimization, ladder and vertex detector support structure R&D
  - Detector assembly
  - Data acquisition system R&D

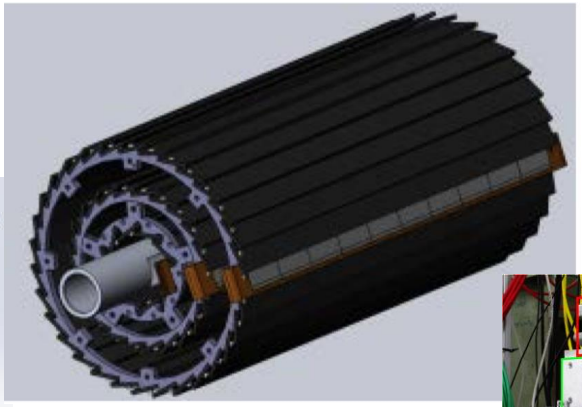
CMOS pixel sensor prototyping



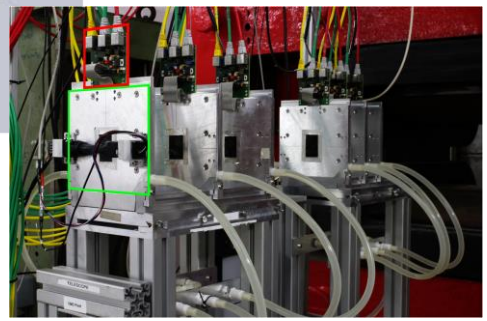
Detector module (ladder) prototyping

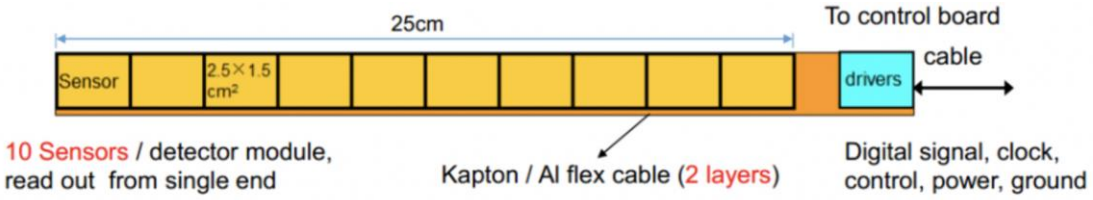


Full size vertex detector Prototype



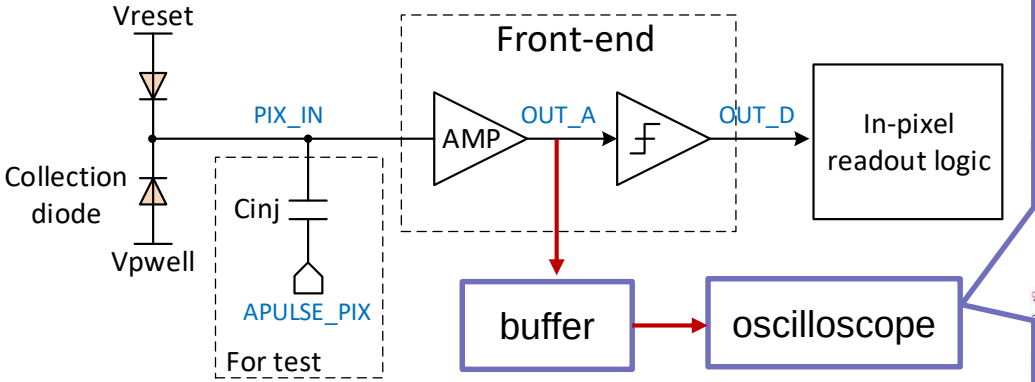
Beam test to verify its spatial resolution

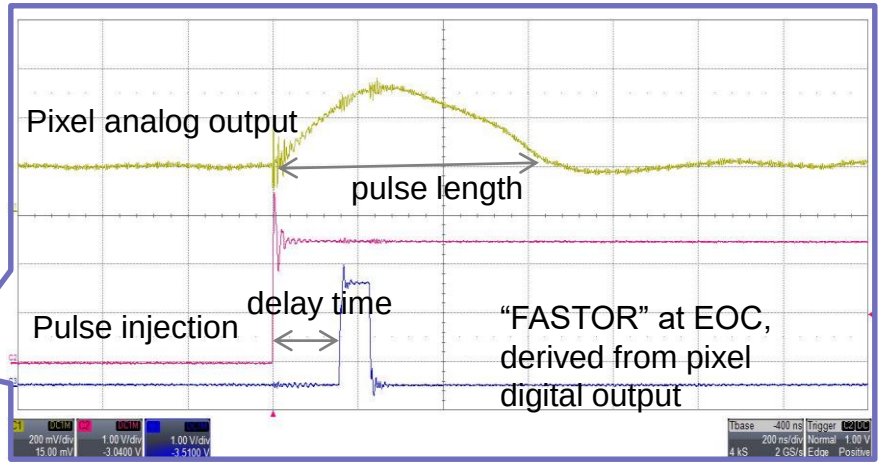




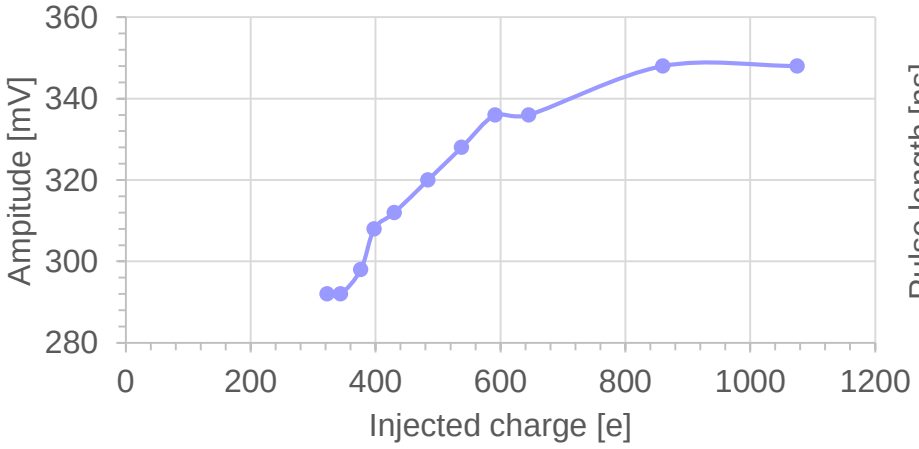
# Properties of the TaichuPix2 pixels

- **Some pixels were integrated with analog buffer for probing the analog output directly**

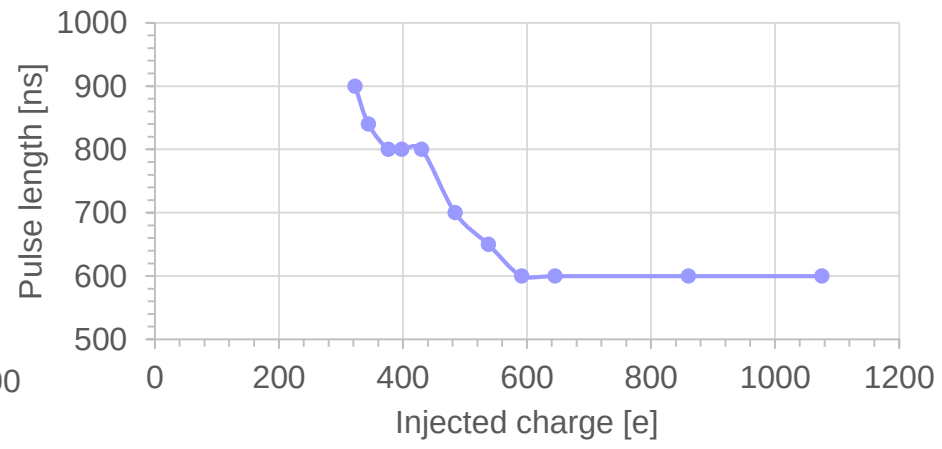



Amplitude vs. Injected charge




Pulse length vs. Injected charge

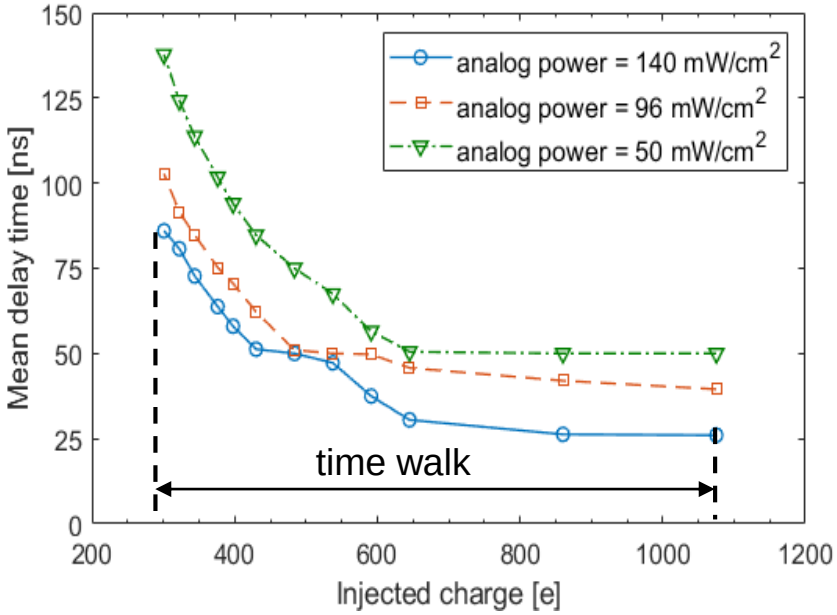



**Demonstrates the nonlinear response of Front-end**

**Pulse length less than 1 μs (~6 μs in ALPIDE )**

# Properties of the TaichuPix2 pixels

- **TaichuPix prototypes record the timestamp of hit at the End of Column (EOC)**
  - The delay of the FASTOR was measured with respect to the moment of the pulse injection via the timestamp with a step of 25 ns



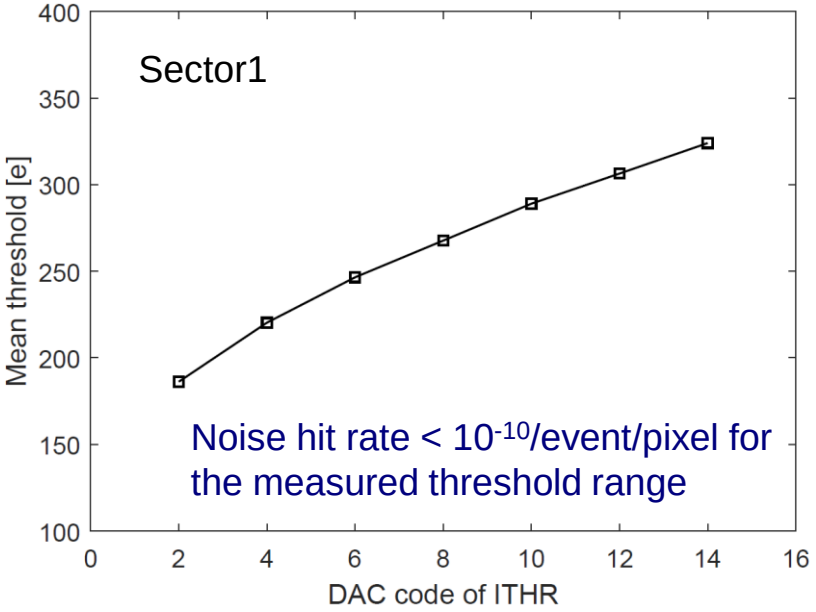

Delay time of FASTOR with respect to the pulse injection measured by the time stamp for different power

- Larger analog power cons. leads to faster response
- For the nominal power cons., time walk ~60 ns larger than simulation (~33 ns) due to the parasitic C
  - Measured value includes delay of logic and transmission
- **Compromise made between fast timing and low power**
  - **The case of 140/96 mW/cm$^2$ could fit the default trigger window of ±75 ns (± 3LSB)**

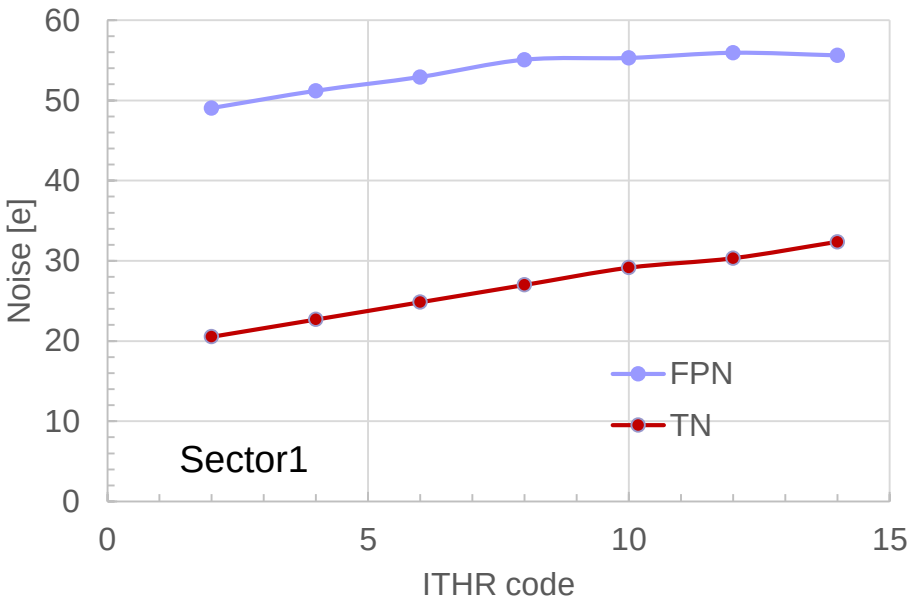
# Threshold tuning

- **Threshold of pixels setting by a common current bias ITHR**

Mean threshold of Sector1 vs. ITHR setting




Noise vs. ITHR



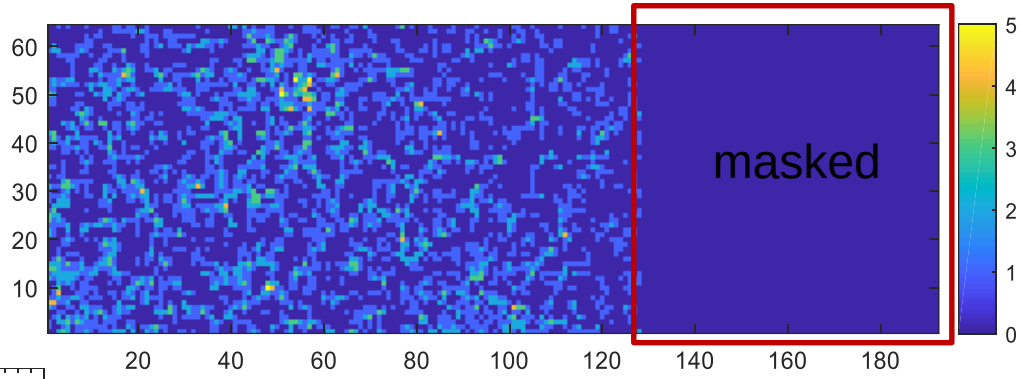

- **Mean threshold increases with ITHR as expected**
- ITHR provided by a 8-bit DAC in the chip periphery, but the min. value much larger than the design, resulting in the desired threshold setting being unachievable. The DAC has been modified in TC3.

- **Threshold dispersion (i.e. FPN, Fix Pattern Noise) dominates the total noise**
- TN (Temporal noise) increases with threshold, due to the nonlinear gain feature of Front-end

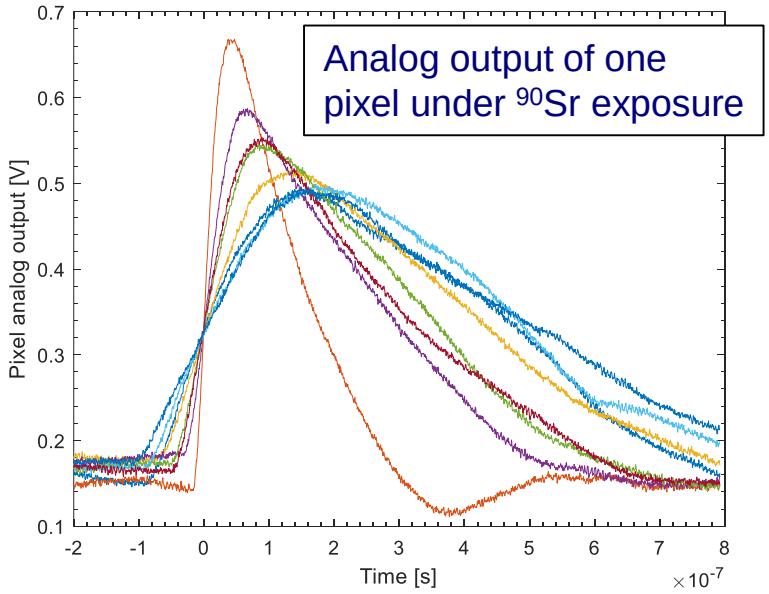
# TaichuPix2 test with $^{90}$Sr

- **TC2 exposure to $^{90}$Sr source at different threshold setting (ITHR)**
  - S1-S4 function normally, while S5-S6 were masked. Because S5-S6 were found to be problematic in the in-pixel digital part in electrical tests.

- S1-S4 have different analog front-end & same digital readout (FE-I3-like)
- S4-S5 using the other digital scheme (ALPIDE-like)



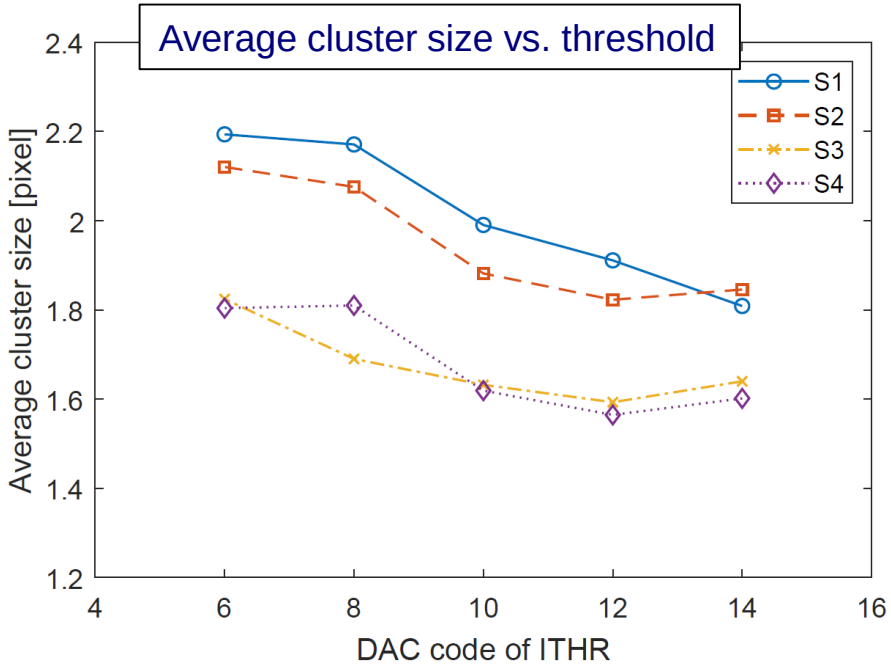

Hit map of TC2 exposure to $^{90}$Sr for 400 s




- Shape and amplitude of analog signal as expected
- **But peaking time and pulse length larger than simulation. One of the reasons is the relatively large charge collection time of sensor in the standard process (~ 150 ns) .**
- **The modified process expected to lead to full depletion of sensors, thus then a faster charge coll.**

# TaichuPix2 test with $^{90}$Sr

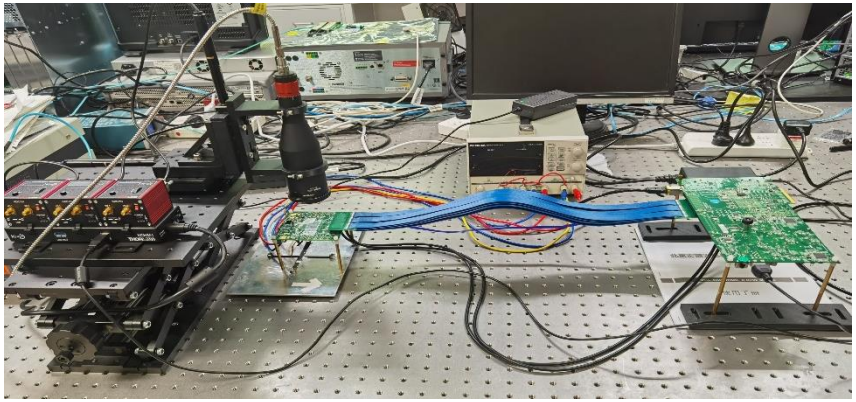
- **TC2 exposure to $^{90}$Sr source at different threshold setting (ITHR)**
  - Finding a cluster for adjacent pixels with a timestamp window of 150 ns



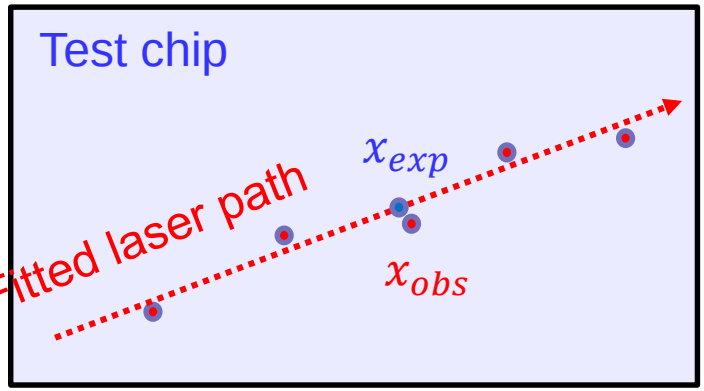

- Average cluster size decreases with threshold as expected
- **Average cluster size less than 3 as expected**
  - **Indicates the estimated maximum hit rate (36 MHz/cm$^2$) reasonable**
  - **Cluster size >1, benefits the spatial resolution (better than $pitch/\sqrt{12}$ = 7.2 μm)**

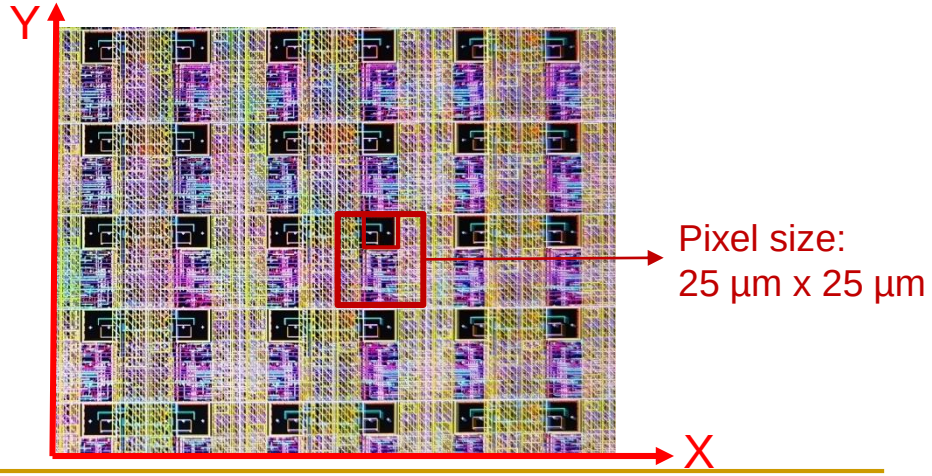
# Laser test on TaichuPix2

- **Test setup**
  - 3-D linear translation stage
    - XY-plane for testing, Z-axis for focusing
    - Min repeatable step 0.2 μm
  - Optical system
    - Laser diode with 658nm wavelength
    - Expected min spot size ~1.13 μm



- **Test method**
  - One dimension laser scan on the test chip with fixed step of 1 μm
  - Take the linear fit of the observed X,Y position as the expected laser position

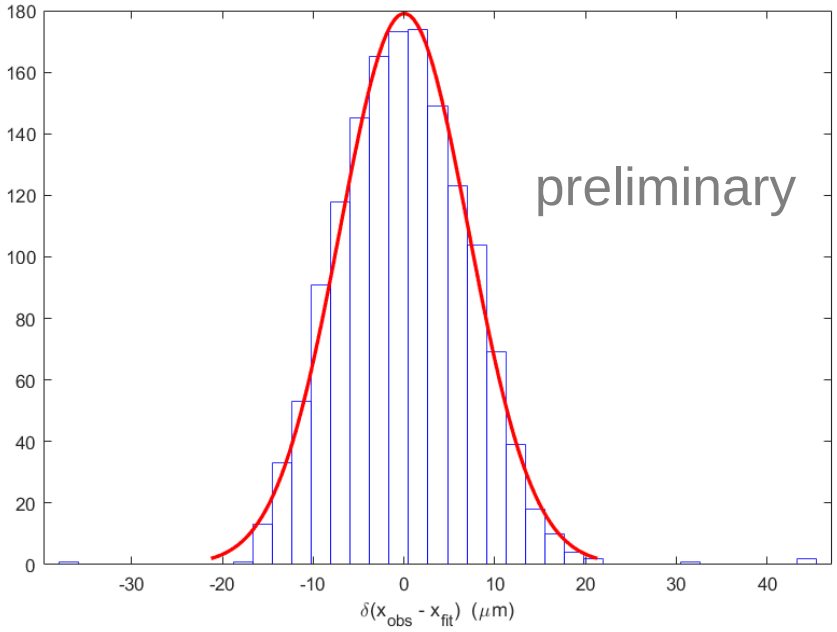


# Laser test on TaichuPix2

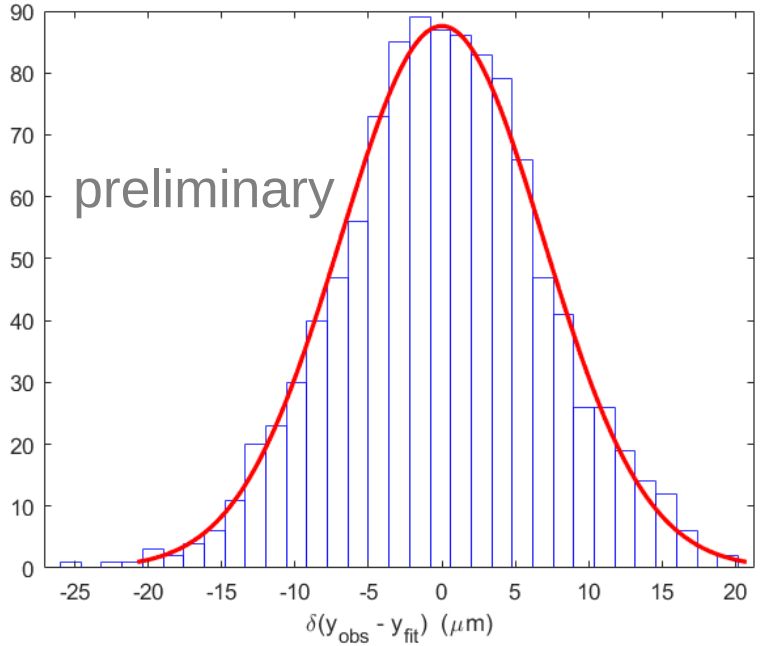
- **Test with different laser intensities result in diff. cluster size**
  - Cluster size ≤ 2

Residual x




```
mu = 0.0358385   [-0.324855, 0.396532]
sigma = 7.09312  [6.84713, 7.35759]
```

Residual y

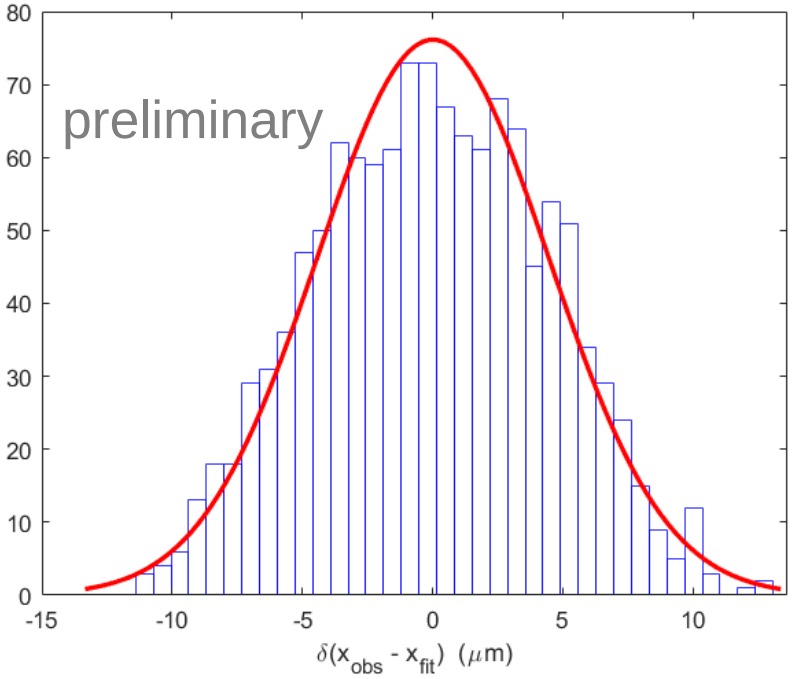



```
mu = 0.00247667   [-0.409703, 0.414656]
sigma = 6.92258   [6.6432, 7.22668]
```

# Laser test on TaichuPix2

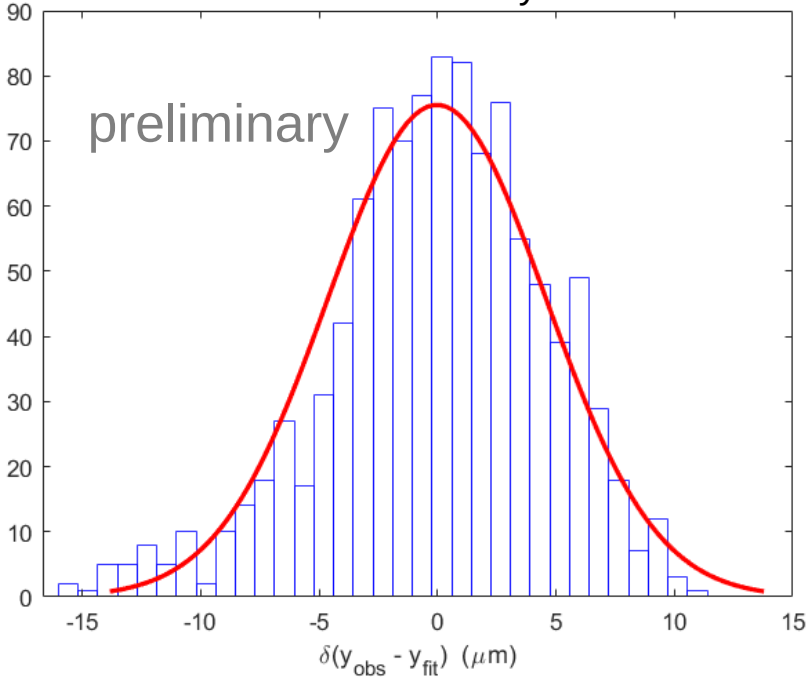
- **Test with different laser intensities result in diff. cluster size**
  - Cluster size ≤ 9 (cluster analysis needs further verification)

Residual x




mu = 0.0157959 [-0.231266, 0.262858]
sigma = 4.45238 [4.28443, 4.63413]

Residual y



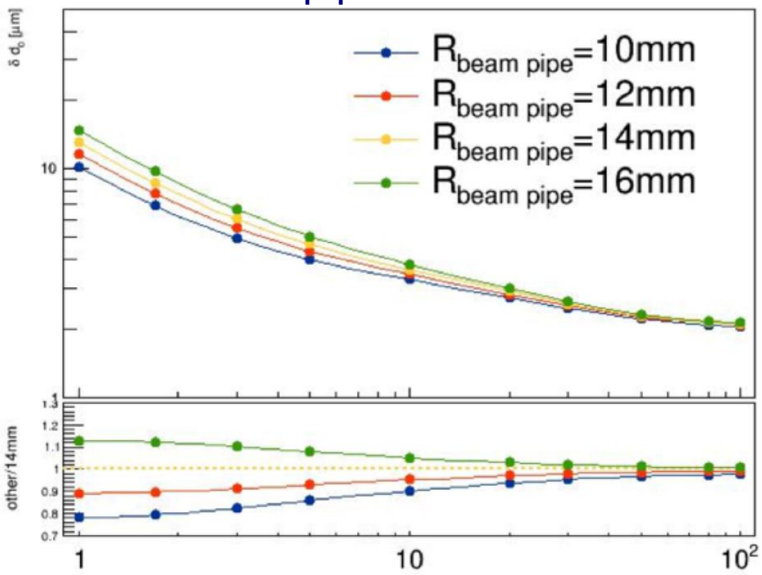

mu = -0.0225294 [-0.301203, 0.256144]
sigma = 4.60194 [4.41318, 4.80769]

**Test with various laser intensities/pixel threshold ongoing**

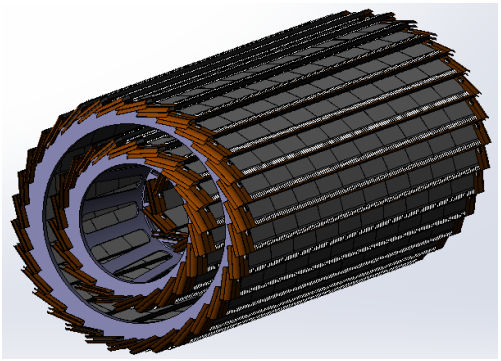
# Vertex detector prototype R&D

- **Completed preliminary version of detector engineering design**
  - 3 double layer barrel design
  - 7 modules in inner layer, 22 modules in 2nd layer, 32 modules in outer layer
- **Physics simulation to optimize vertex detector layout design**
  - The length of inner layer pixel should be the same as other two layers
  - Inner pixel radium should be as close to beam pipe as possible

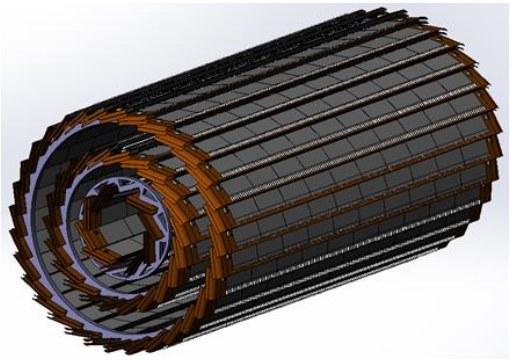
Impact parameter resolution
vs. beam pipe radius




Old design



After optimization

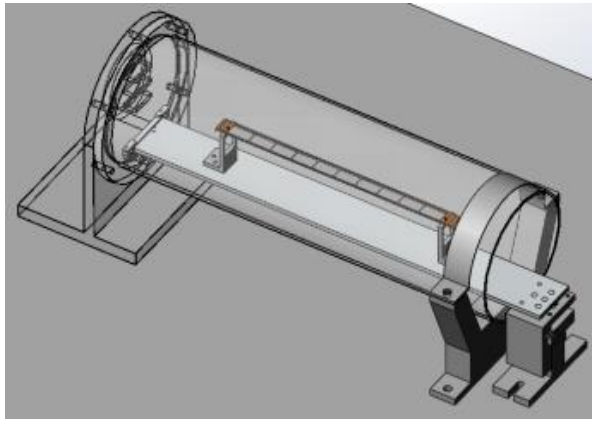


# Cooling design

- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix : ~100 mW/cm$^2$. (trigger mode) ; CEPC final goal : ≤ 50 mW/cm$^2$
- **Cooling simulations of a single complete ladder**
  - Test bench setup has been designed and built for air cooling , vibration tests
  - Need 2 m/s air flow to cool down the ladder to 30 ℃

| Max temperature of ladder (℃) (air temperature 5 ℃) | | | | | |
|---|---|---|---|---|---|
| Power Dissipation (mW/cm2) \ Air speed (m/s) | 5 | 4 | 3 | 2 | 1 |
| 100 | 19.6 | 21.8 | 25.0 | *30.6* | *43.4* |
| 150 | 26.9 | 30.1 | 35 | *43.4* | *62.6* |
| 200 | 34.2 | 38.6 | 45.1 | *56.2* | *81.8* |

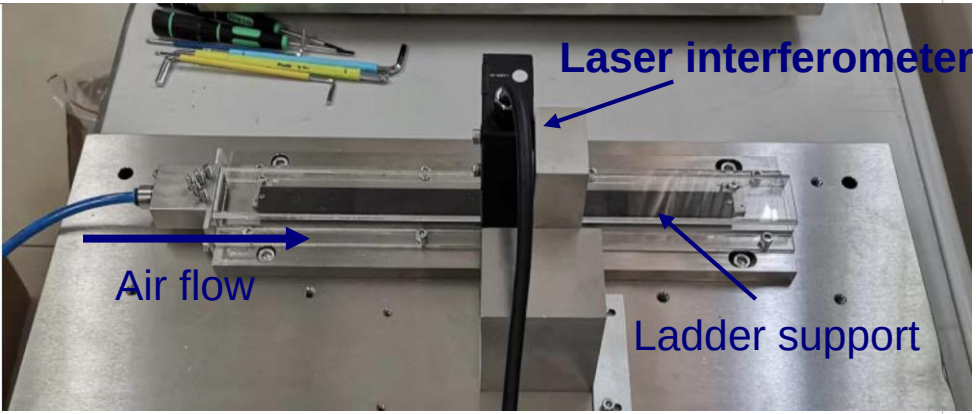
Test setup for ladder cooling
Use compressed air for cooling

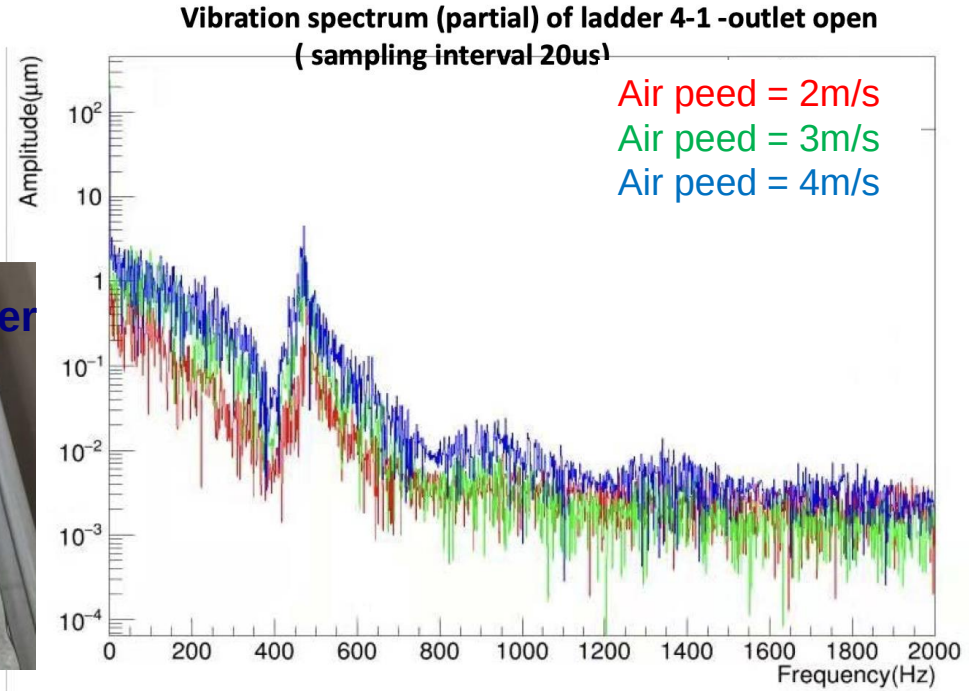


# Air Cooling test

- **Test bench setup for air-cooling**
- **Vibration follows Gaussian distribution**
  - Maximum displacement can below 1 μm for air speed = 2 m/s
  - Expect to cool it down to 30 ℃

Test setup prototype for ladder cooling
Use compressed air for cooling



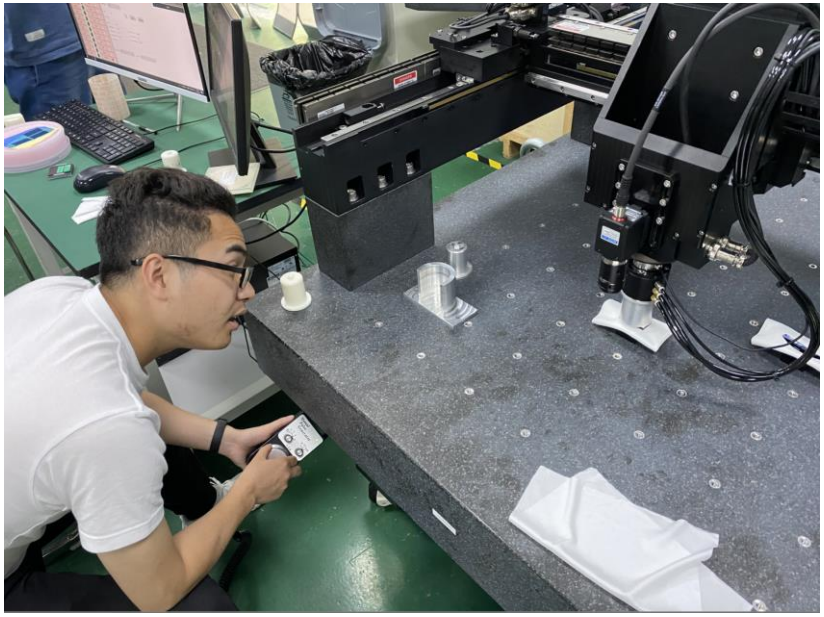




A few resonant peaks were confirmed at frequencies below 2000 Hz.

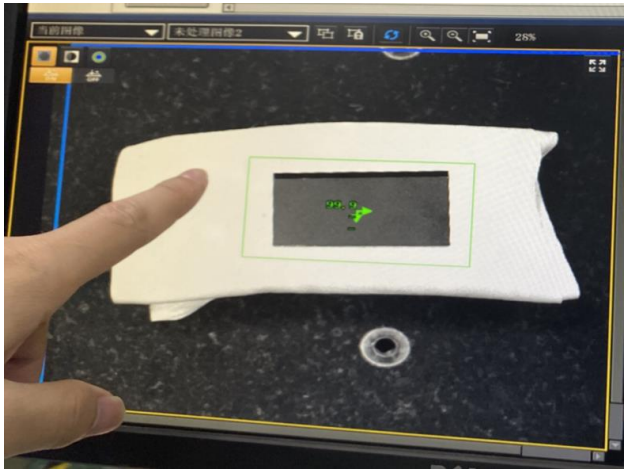
# Gantry for vertex detector prototype assembly

- **3~5 μm good position resolution require high assembly precision**
- **Cooperate with domestic company on R & D Gantry automatic module assembly**
  - Pattern recognition with high resolution camera
  - Automatic chip pick-up and positioning
  - Automatic Glue dispending

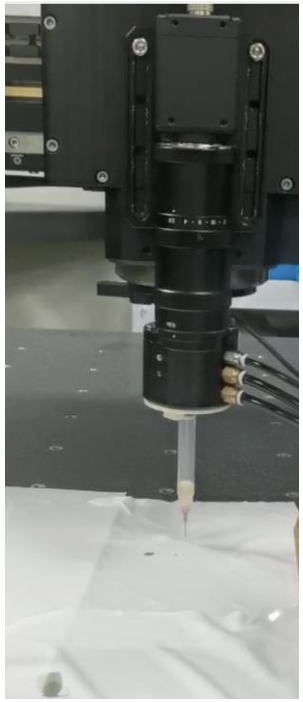
Gantry system



Pattern recognition



Automatic glue dispending

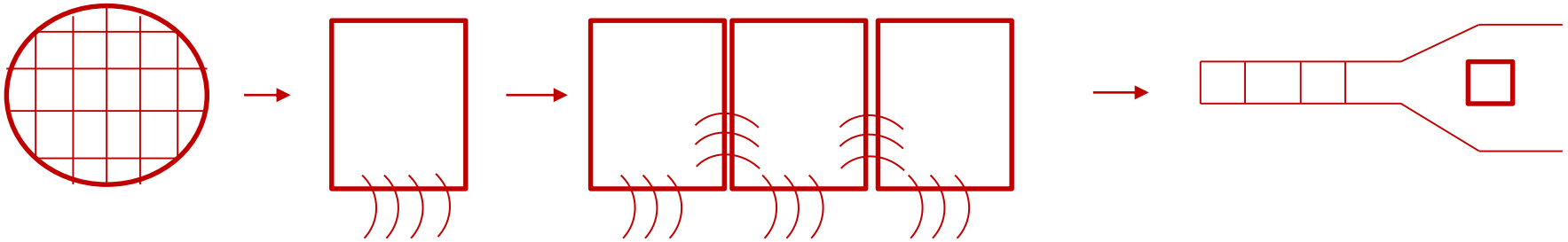


# Test plan for the TaichuPix-3

- **The first full-scale prototype, TaichuPix-3, was submitted**
- **Tests proposed to be done with 4 steps**

1. **Probe Card design for the wafer test**
   - **Prepared detailed test plan document and contacted with test company (W. Wei)**

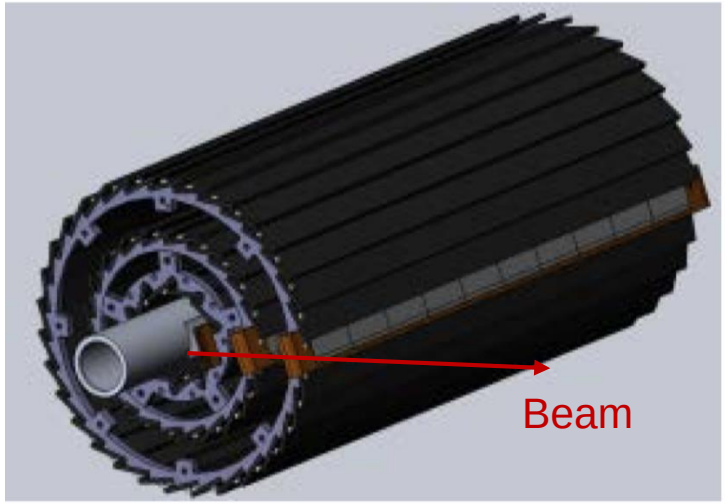
2. **Single chip test board design**
   - Designed with all the test features for the chip functional study
3. **Multiple chip test board for the ladder debugging**
   - Designed following the same manner as the ladder but on PCB
   - Signals and power supplies will be limited just with the ladder's dimension
   - Extra test signals can be connected to the extended area, to help debugging
4. **The real flex cable design for the ladder**
   - Core design and lessons will be exported from 3

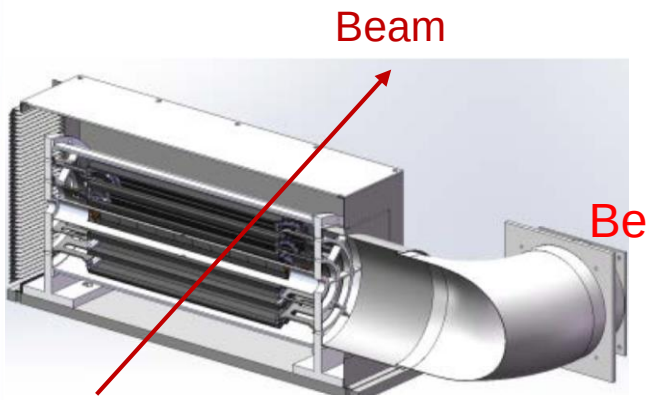


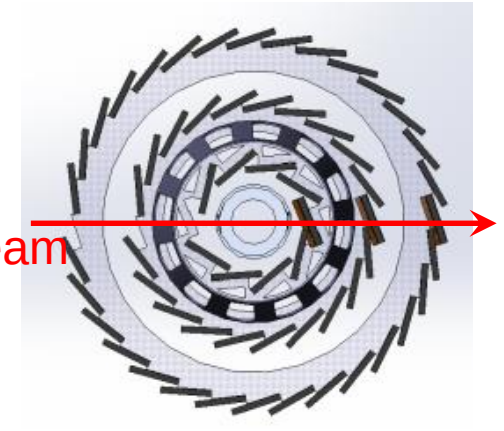
# Plan for test beam

- **Expect to perform beam test in DESY (3 - 7GeV electron beams)**
  - IHEP test beam facility as backup plan (a few hundreds MeV - 2.5 GeV electrons )
- **Enclosure for detector with air cooling is developed for beam test**
  - Beam is shooting at one sectors of vertex detectors

Install one sector of ladder in vertex detector



# Summary

- **Promising test results obtained with small-scale sensor chip**
  - Main functional blocks work normally, design bugs found & fix in next version
- **The first full-scale prototype (TaichuPix3) in fabrication**
  - Chip size 25.7 mm × 15.9 mm.
  - 12 wafers ordered, expected to be assembled on the ladder prototype
- **Finalize the design for full vertex detector**
- **Air cooling test verified the max. displacement can below 1μm**
- **Recent plan for sensor prototype**
  - TID tests with X-ray machine, comparing with the previous result at BSRF beamline
  - Preparation for the full-scale chip test (probe card, test PCB, flex cable …)

**Thank you very much for your attention!**