Status of the CEPC SDHCAL

Weihao Wu (SJTU)

On behalf of the CEPC Calorimeter Group

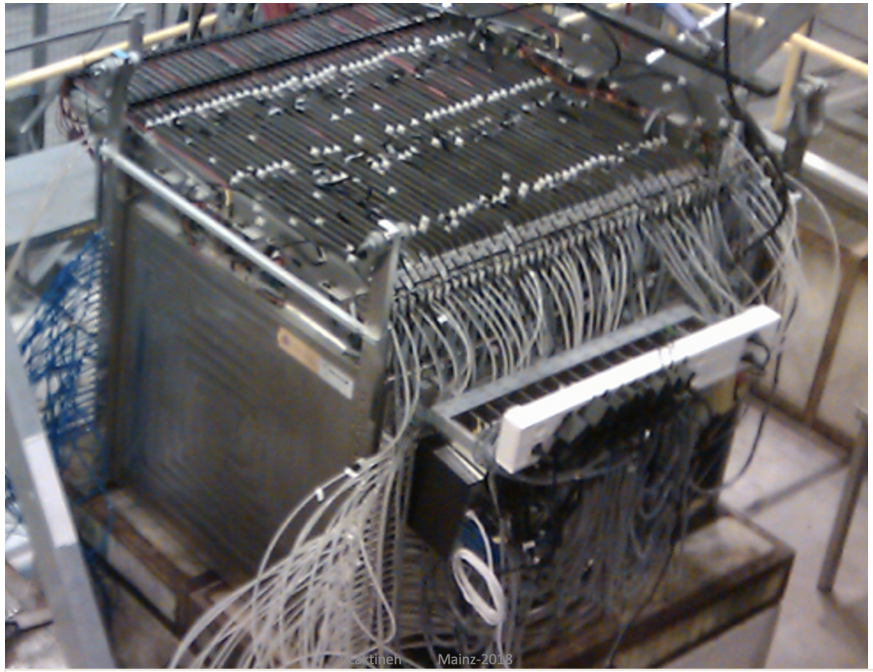
3/25/2022

Outline

- Background introduction
- SDHCAL prototype testbeam data analysis
- GRPC built and performance study
- Timing electronics development
- RPWELL prototype and testbeam results
- Summary

SDHCAL Prototype

- **Semi-Digital Hadronic CALorimeter** (SDHCAL) is one of the PFA calorimeter solutions for CEPC.
- High granularity calorimeter based on Glass RPC (cell size 1cm × 1cm)
- **Hits associated to three thresholds**:
  - 1^{st} threshold = 110fC
  - 2^{nd} threshold = 5pC
  - 3^{rd} threshold = 15pC
- 48 layers with GRPC as sensitive medium
  → Dimensions: 1m × 1m × 1.3m
- 6 Interaction length ($6\lambda_I$)
  → Semi-digital readout



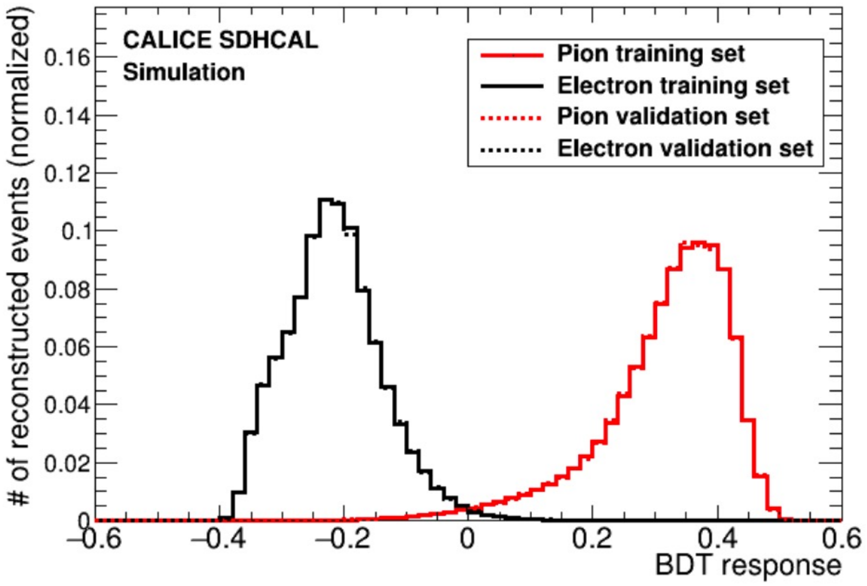
SDHCAL prototype at testbeam in 2015

Particle Identification using BDT

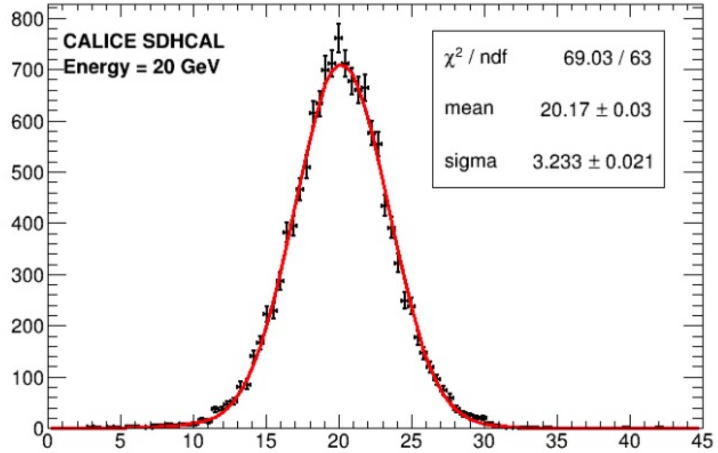
- PS and SPS testbeam at CERN in 2015
  - PS beamline: 3, 4, 5, 6, 7, 8, 9, 10, 11 GeV
  - SPS beamline: 10, 20, 30, 40, 50, 60, 70, 80 GeV
  - Contamination particles: eletrons and muons

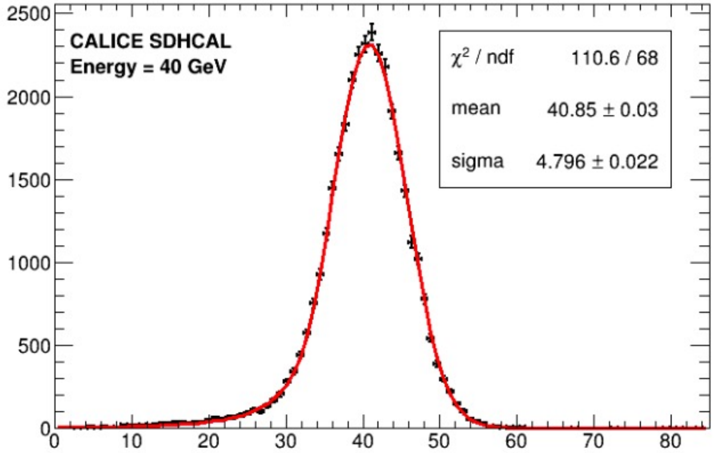
https://arxiv.org/pdf/2202.09684.pdf

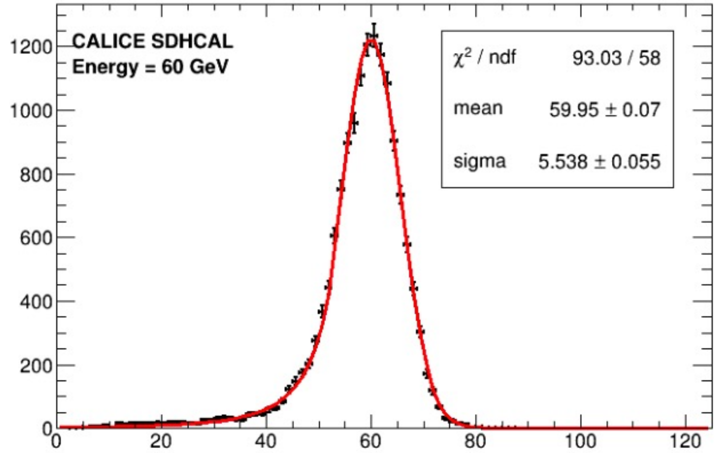
- A testbeam data analysis draft recently has been submitted to Jinst.
  - Use BDT to reject electron background from pion samples in the energy range of 10 to 80 GeV

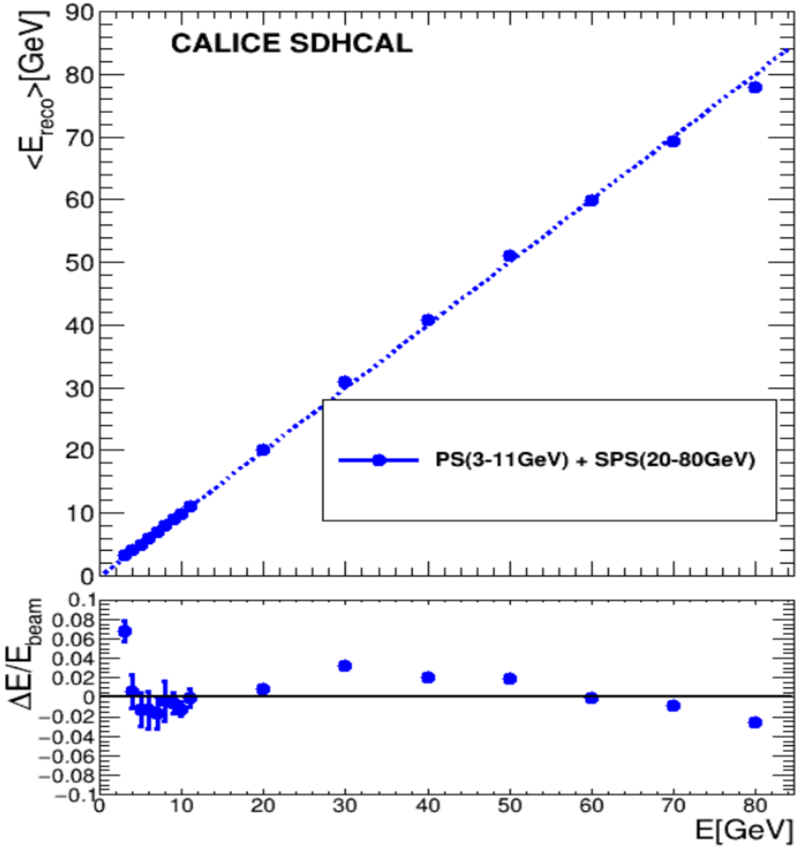


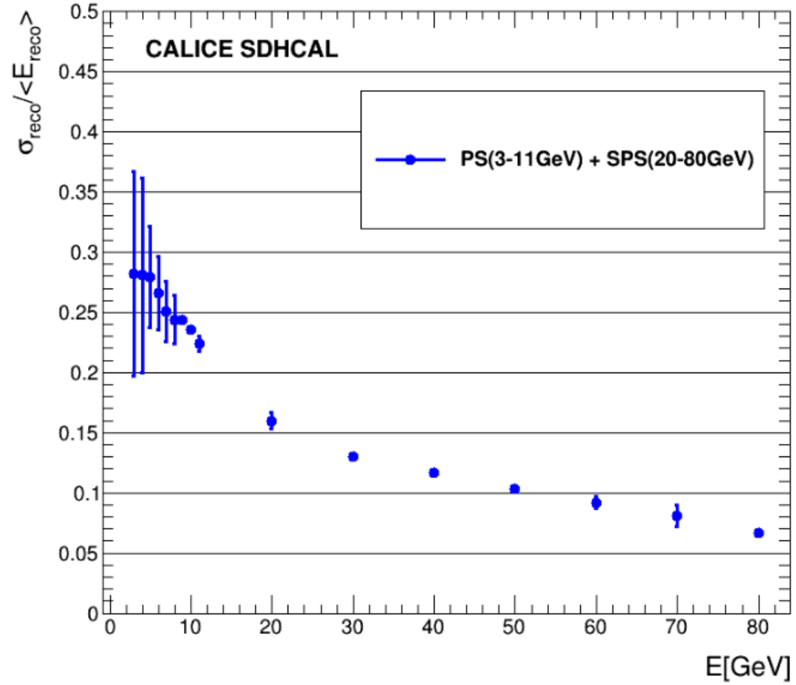
Distribution of the BDT output of training and validation set using the simulated electron (black) and pion (red) events from 1 GeV to 80 GeV.







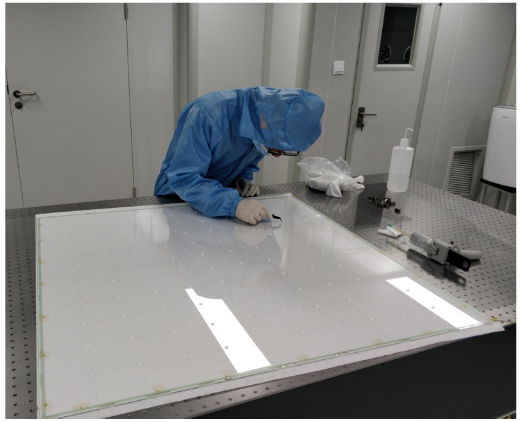


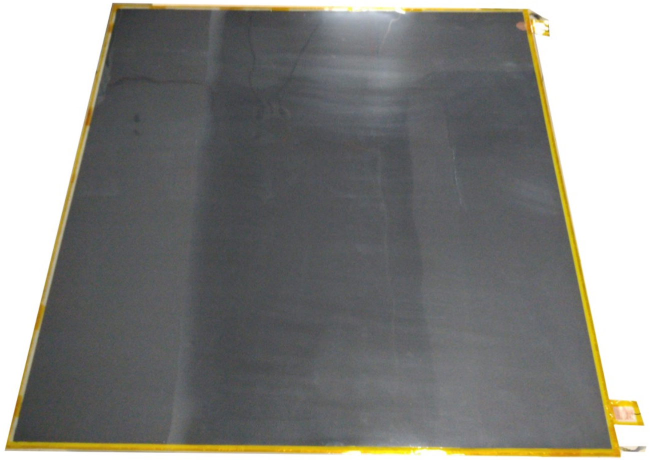


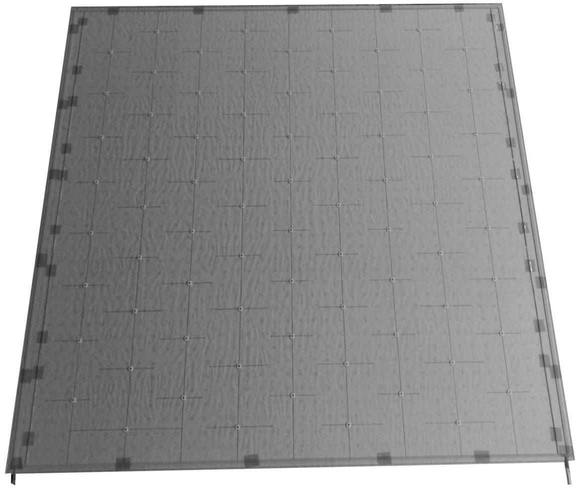
excellent linearity and energy resolution from 3 to 80 GeV

Glass RPC Build and Test

1m × 1m RPC chambers has been built and tested at SJTU



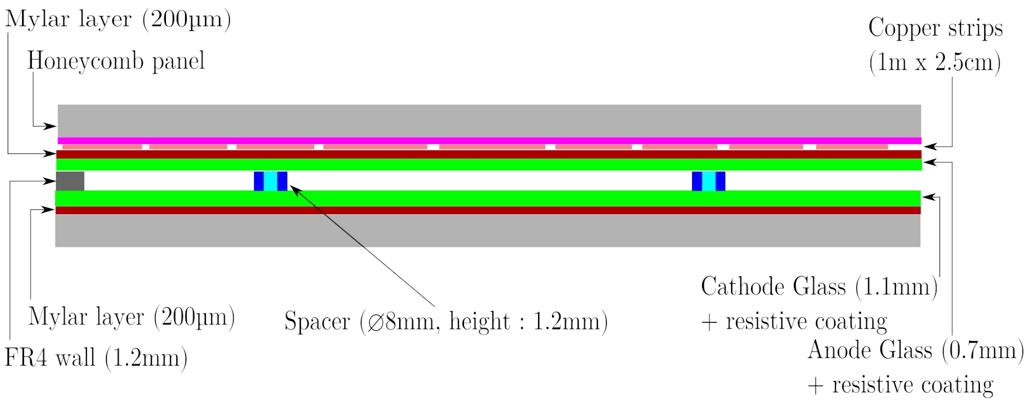




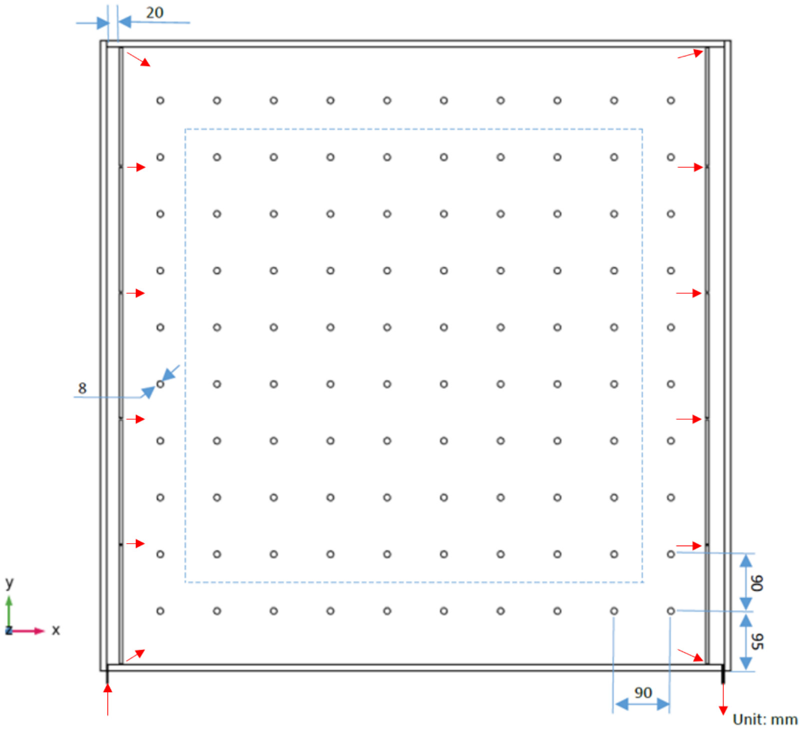
Cosmic muons test setup

Glass RPC Build and Test

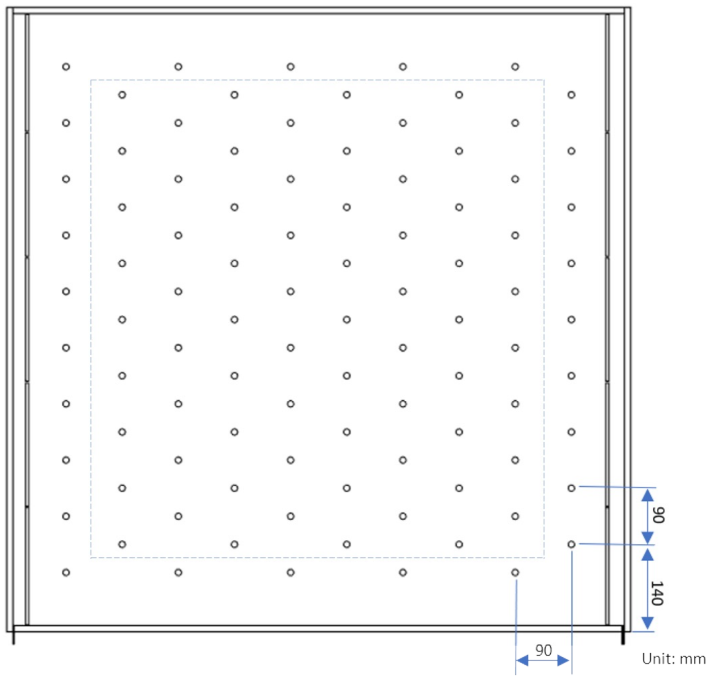
- The uniformity of the gas flow in the chamber and the deformation of the electrode plates are critical to the performance and/or aging of RPC.
- During the course of making a RPC, we need spacers to keep the thickness of gas gap uniform. Also, the spacers will affect the gas flow.
- Here a software named COMSOL Multiphysics® is used to simulate the gas flow and deformation of the electrodes for RPCs with different spacer configuration by finite element method.



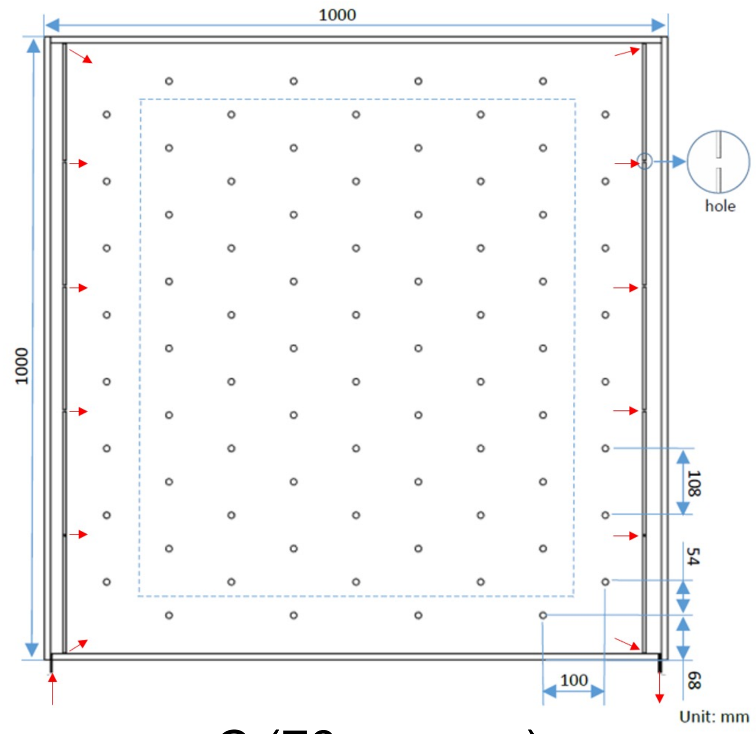
Different Spacer Configurations in RPC



A (10×10 spacers)



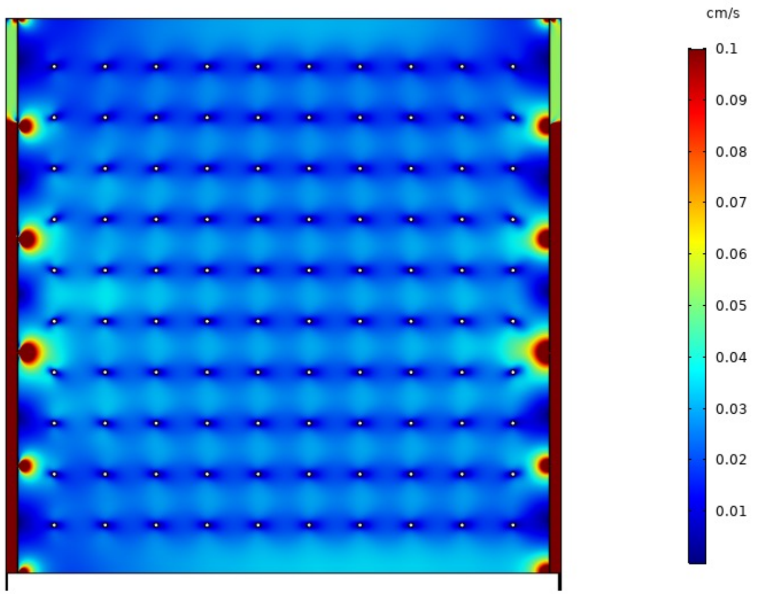
B (95 spacers)



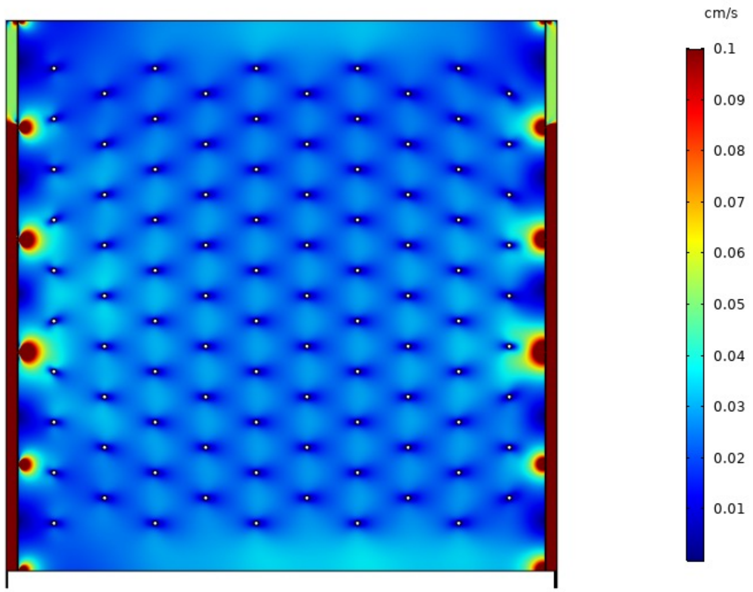
C (76 spacers)

- Red arrows show the routine of the gas flow
- The center part of the chamber marked by the dashed lines is used for result comparison

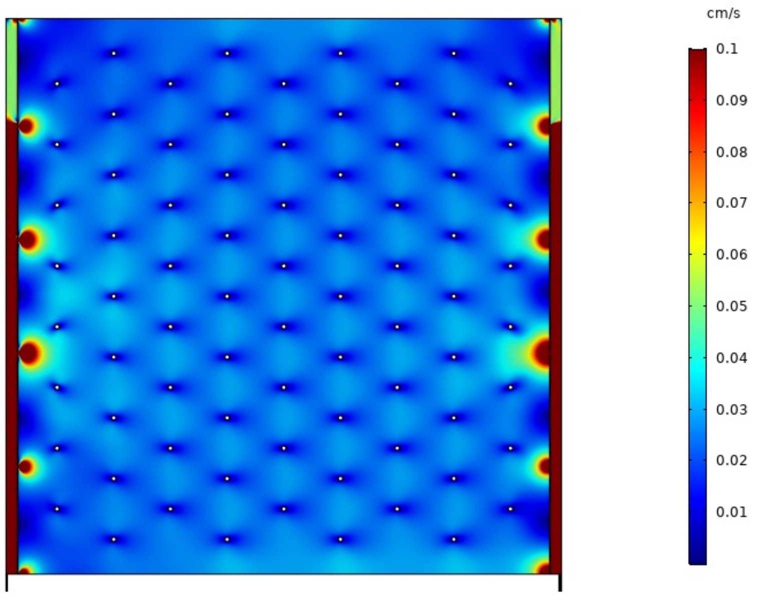
Velocity inside the RPC Chamber(Input: 1L/h)



A



B



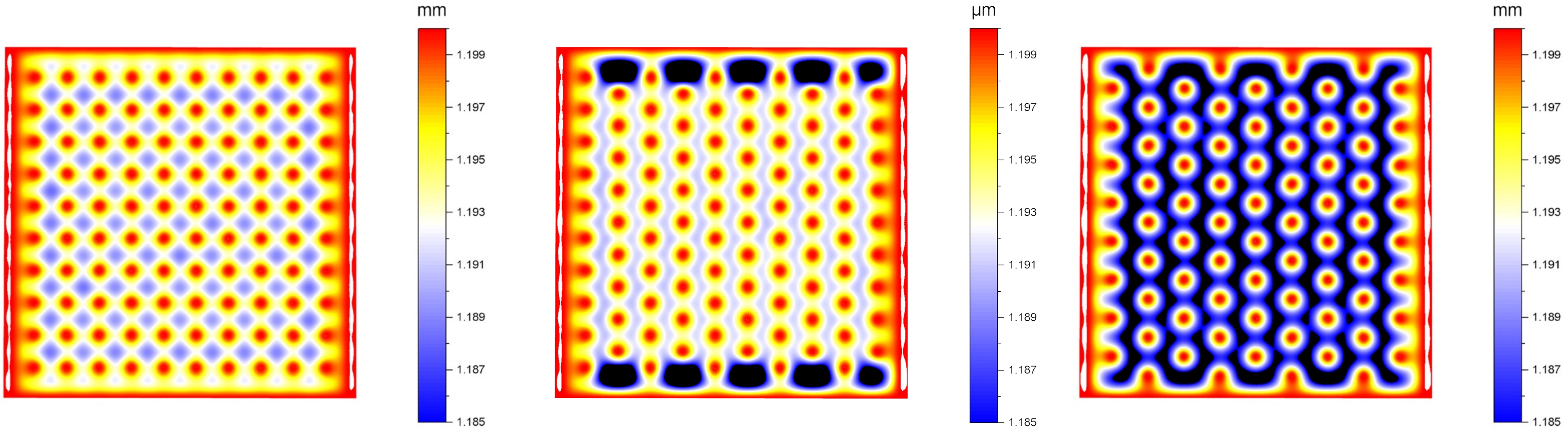
C

Model	A	B	C
Mean velocity(mm/s)	0.238	0.234	0.241
RMS of velocity(cm/s)	0.049	0.045	0.042
RMS/mean	20.3%	19.3%	17.5%

- Shifting the spacers helps to make the distribution of velocity more uniform
- The distribution of velocity gets more uniform after reducing the number of the spacers

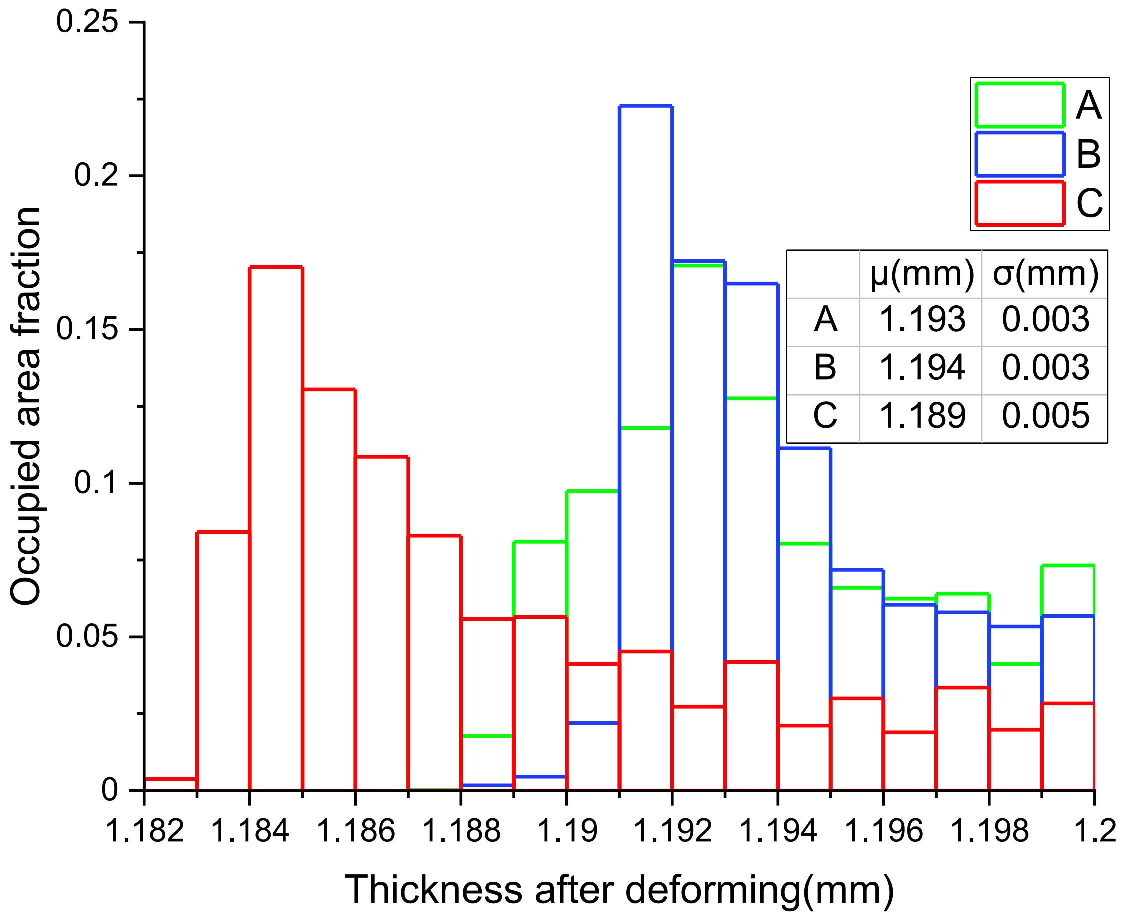
Deformation of the Glass Electrodes

- The simulation of chamber deformation on the electrodes is carried out by using pressure of gas flow and an electric field between two electrodes which is applied at 6.6 kV (working voltage of our RPC).



Distribution of the thickness of the gas gap after deformation(1.2mm before)

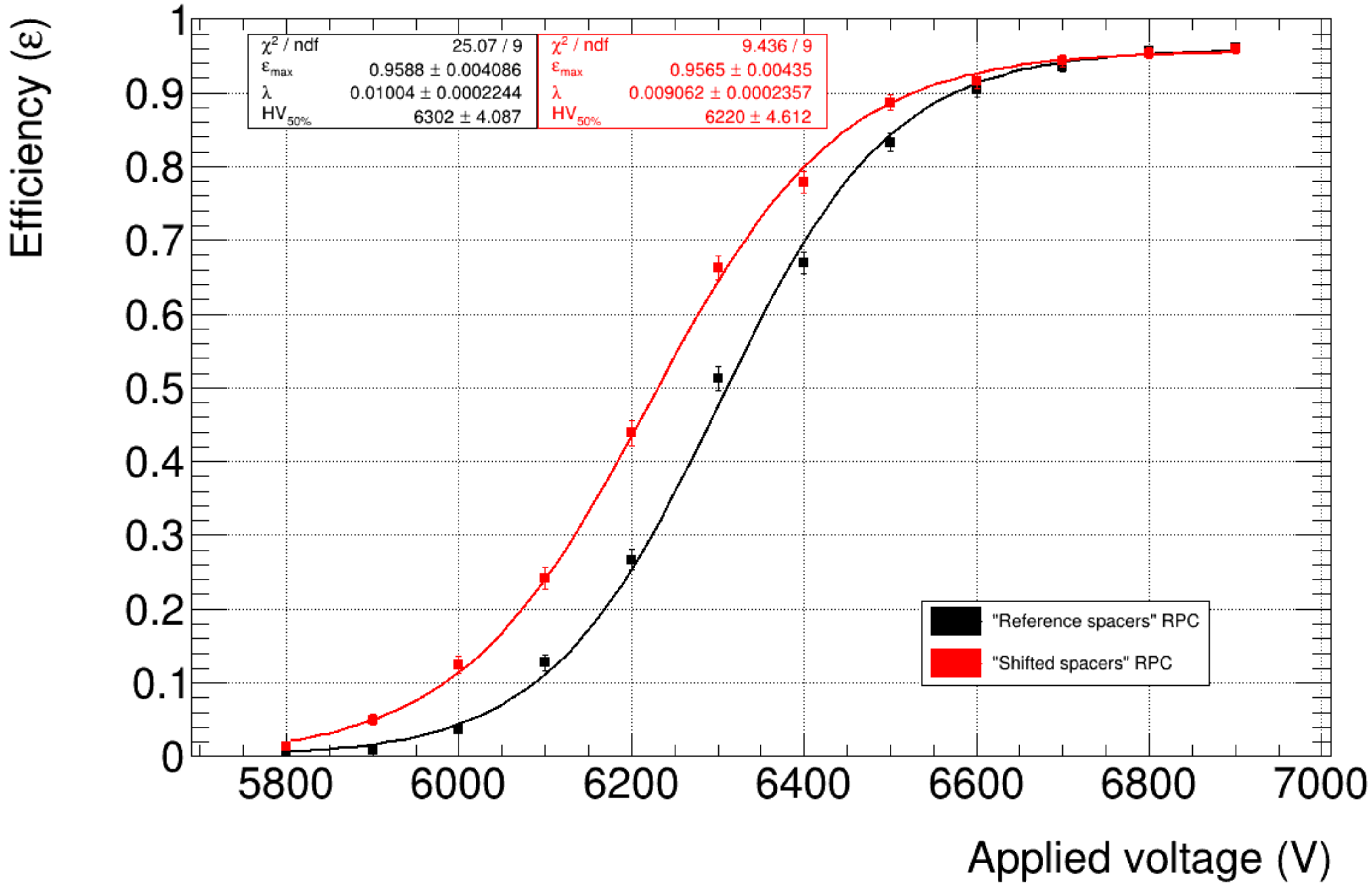
Thickness Distribution of the Gas Gap

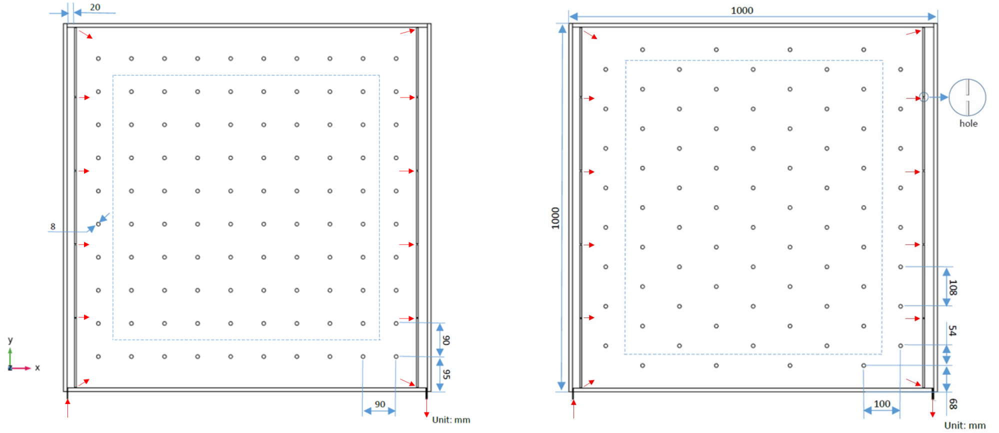


Model	A	B	C
RMS/mean	0.25%	0.25%	0.34%

- The increase of the distance between spacers would cause more deformation on both electrodes, but still within 1%

Performance Comparision

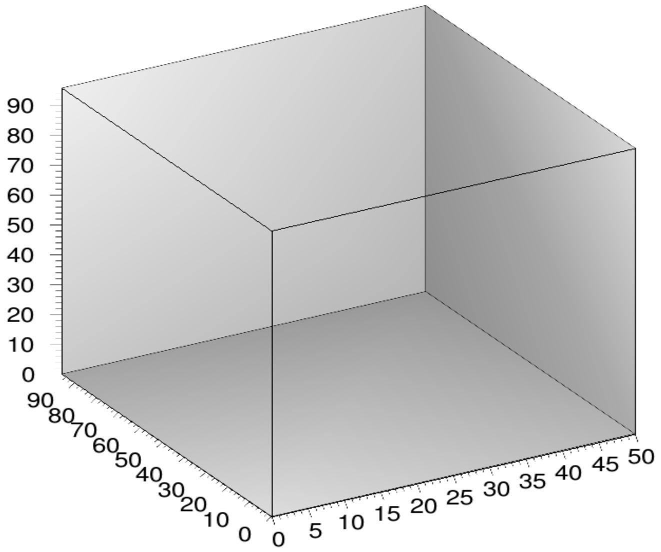


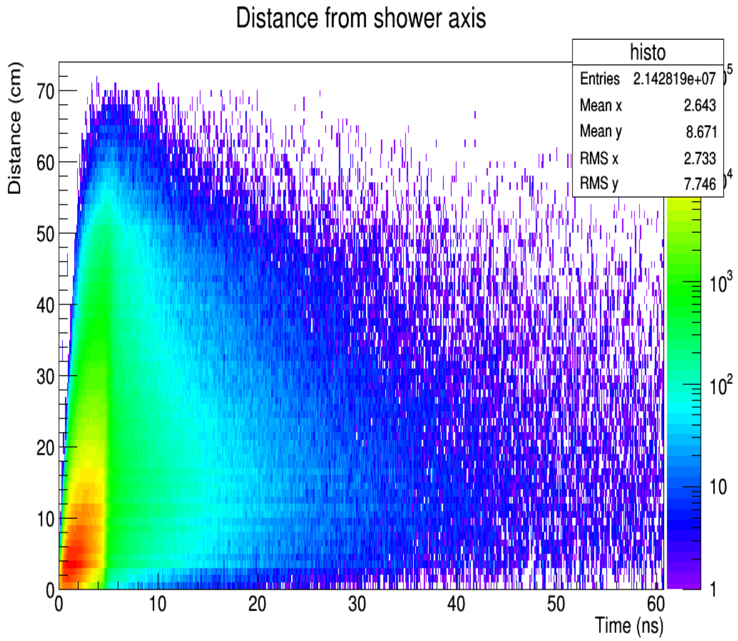


- The efficiency plateaus are comparable for the two chambers are both greater than 95%
- 2021 JINST 16 P12022

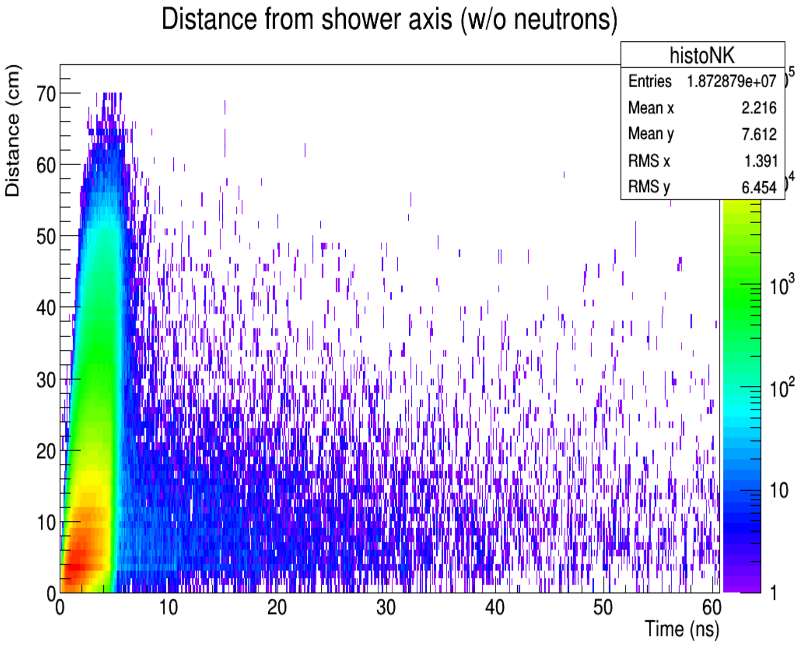
Motivation using Timing Information

- Timing could be an important factor to identify delayed neutrons.





With Neutrons

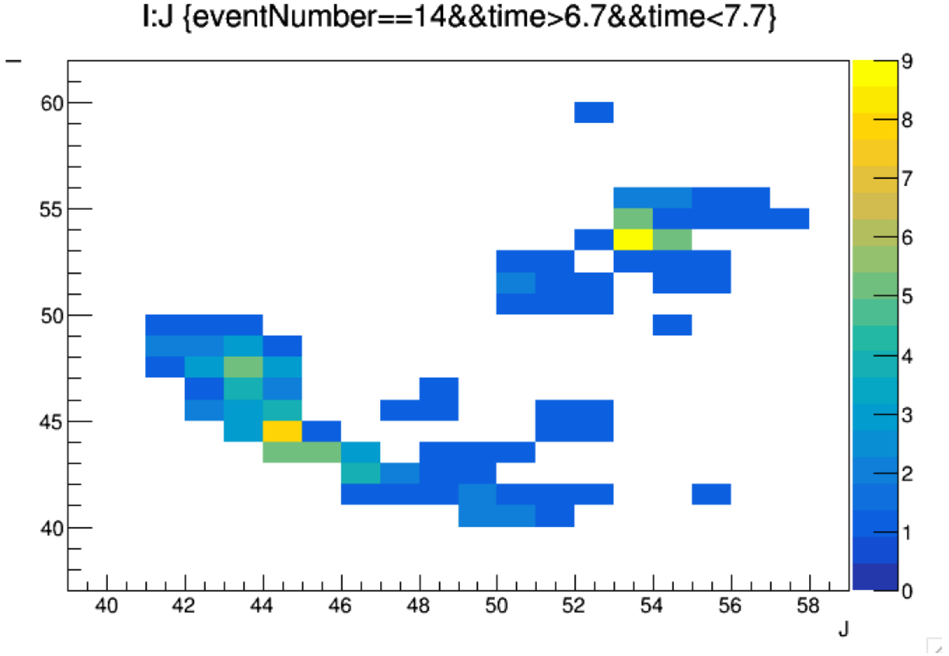


Without Neutrons

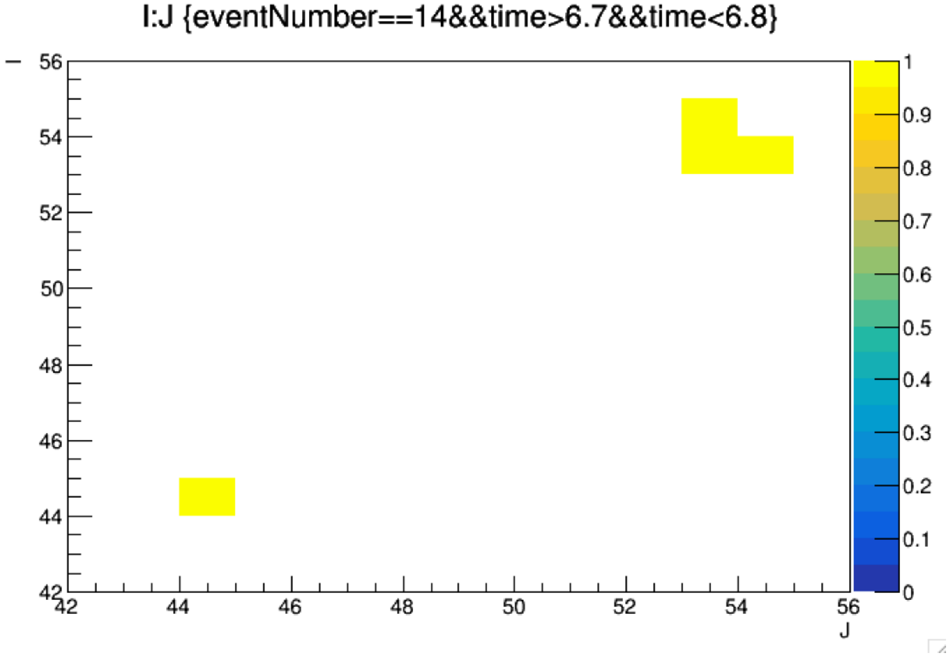
Motivation using Timing Information

- Time information can be very helpful to **separate close-by showers** and **reduce the confusion** for a better PFA application.

1 ns resolution



100ps resolution

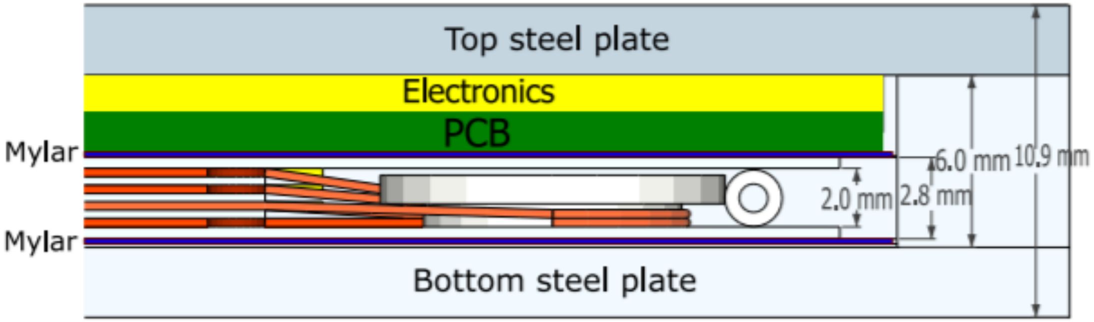


Fast Timing Measurement

- Purpose: => Identify neutral and charged hadrons
- Position, Energy and Timing => 5D HCAL

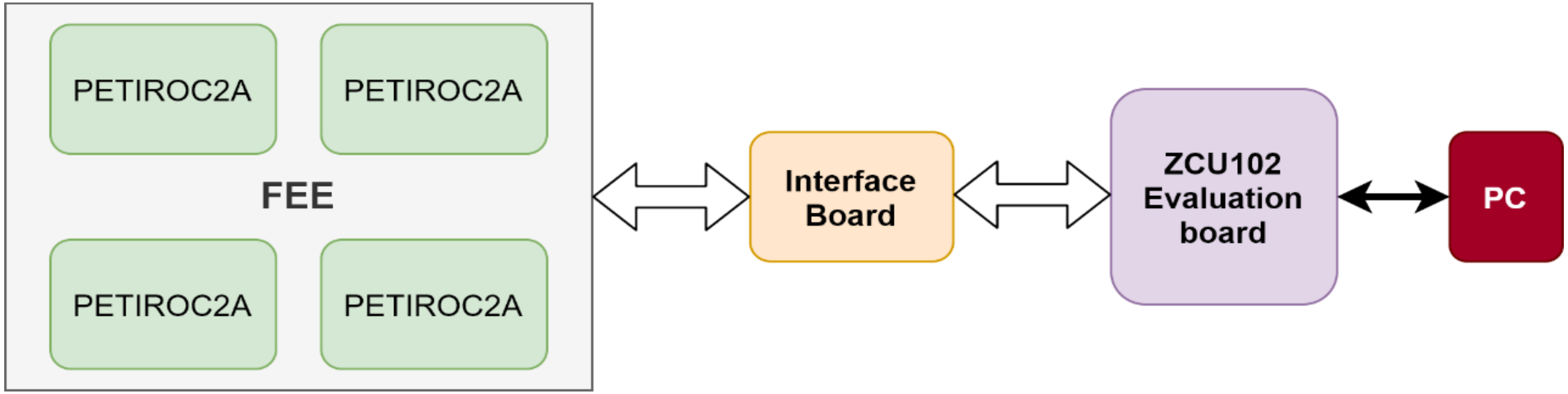
- Adding MRPC layers in the SDHCAL
- Fast timing readout electronics for MRPC readout
  - PETIROC from Omega group (resolution: ~40 ps)

- First step：
  - Design a FE prototype with four PETIROC2B chips



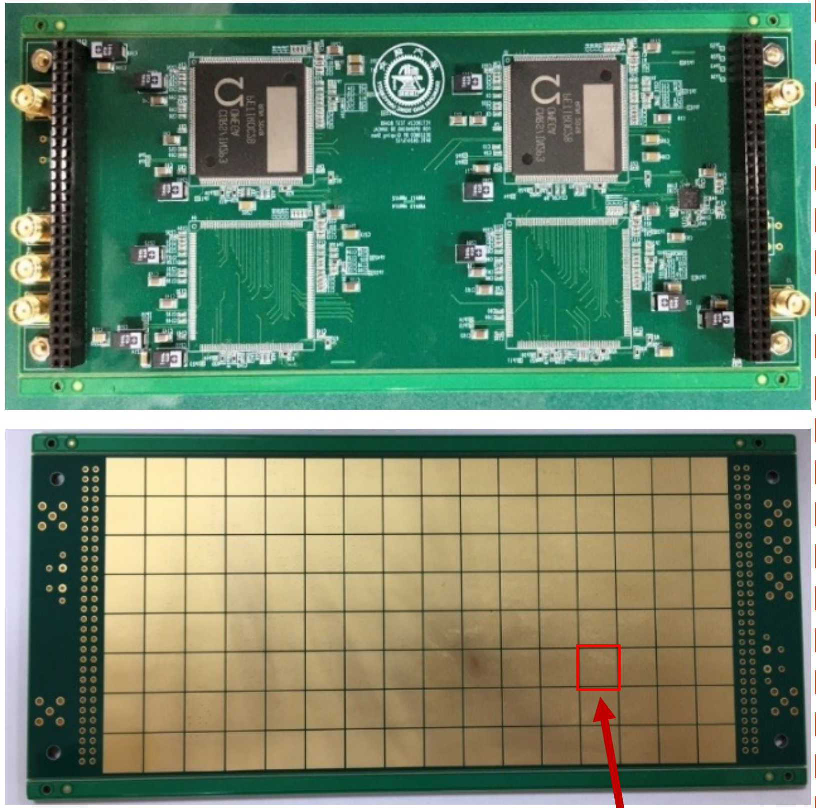
Prototype of Timing Electronics

- The FEE prototype includes four PETIROC chips, 128 readout pads on the PCB bottom side for MRPC induction signals.
- Detector Interface(DIF) card was designed to connect FEE and FPGA board
  - Data transmission, power rail and clock source.
- The DAQ system should be developed to transfer data between FEE and PC.



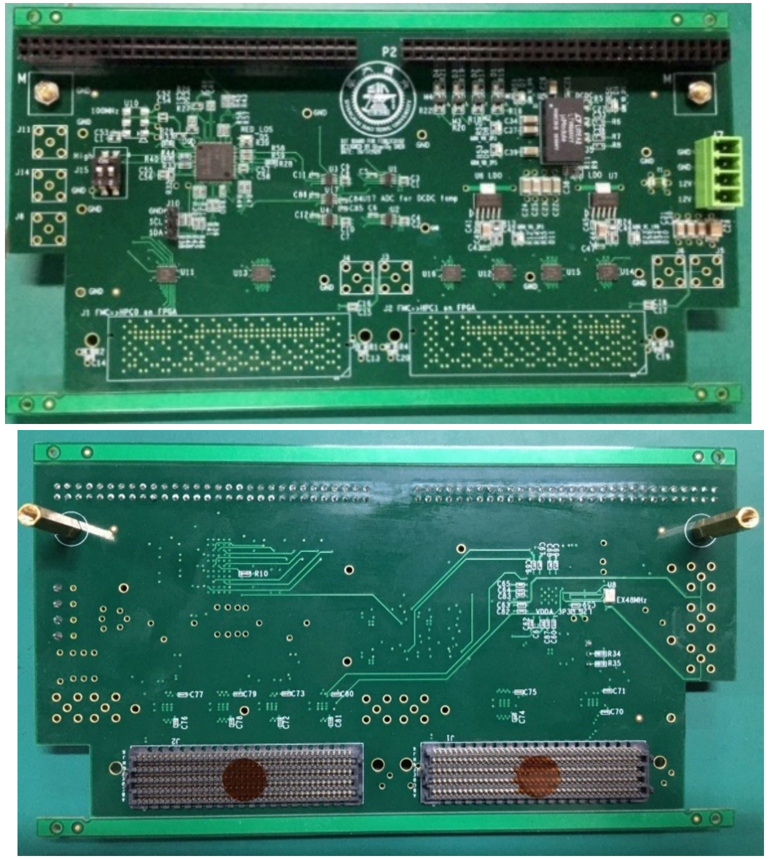
Block diagram of timing electronics prototype

Hardware of Timing Electronics Prototype

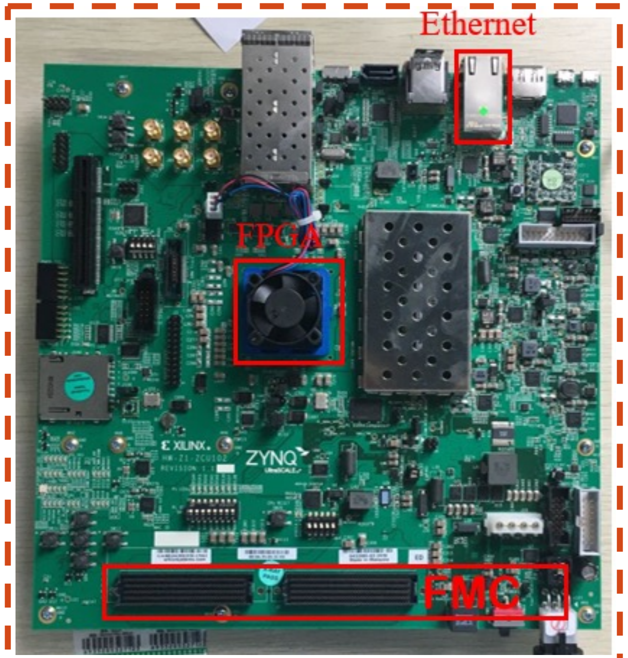


FE Board

128 pads with the cell size 1cm × 1cm



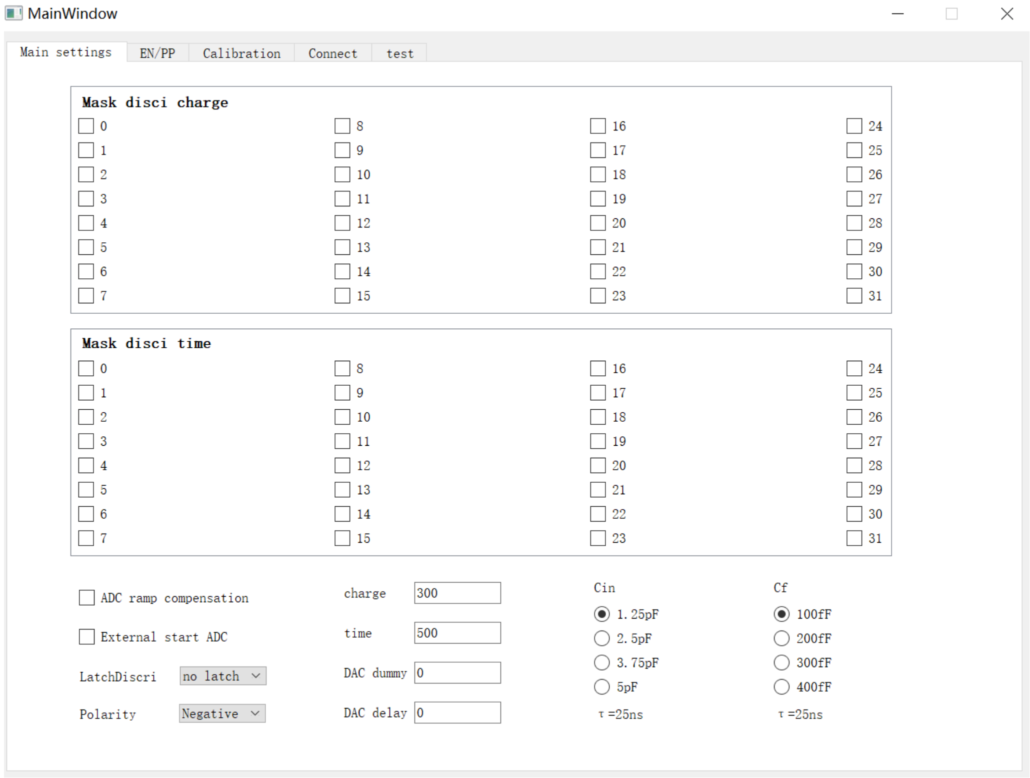
DIF Card

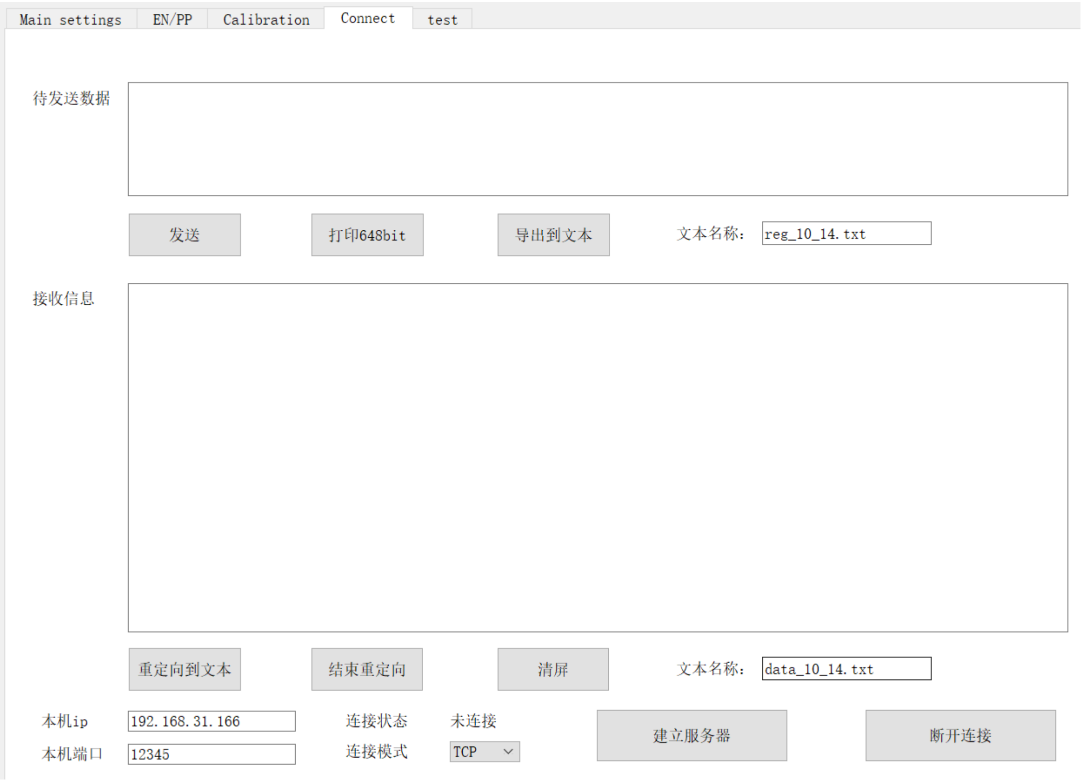


ZCU102

DAQ Software

- Software developed with python language by QtCreator
- The configuration set in the software and sent to the FPGA over ethernet with TCP
- Data received from FEB, saved to the PC side.

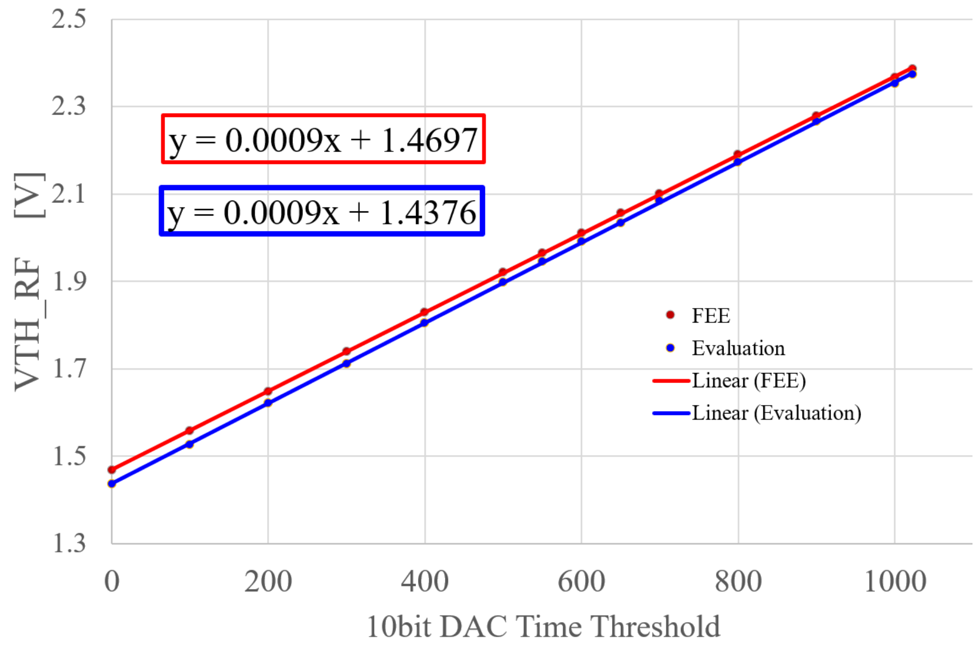


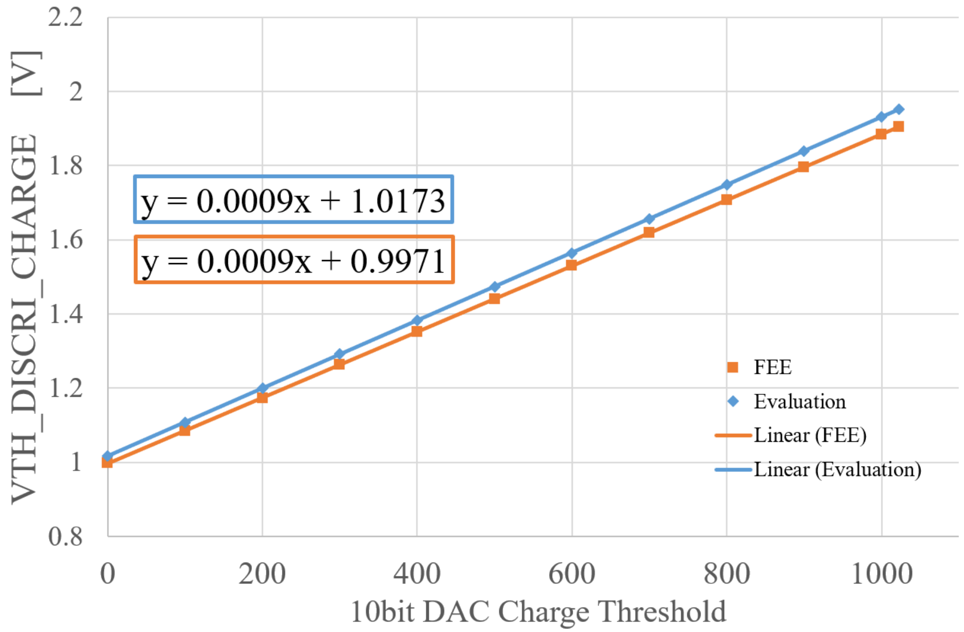


Time and Charge Threshold Voltage Test

Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658

- All of bias voltage values are correct.
- Output data has been checked, after sending trigger signals.
- Time threshold is correct according to the voltage value with 10bit DAC.
- Time and Charge threshold can be well controlled.

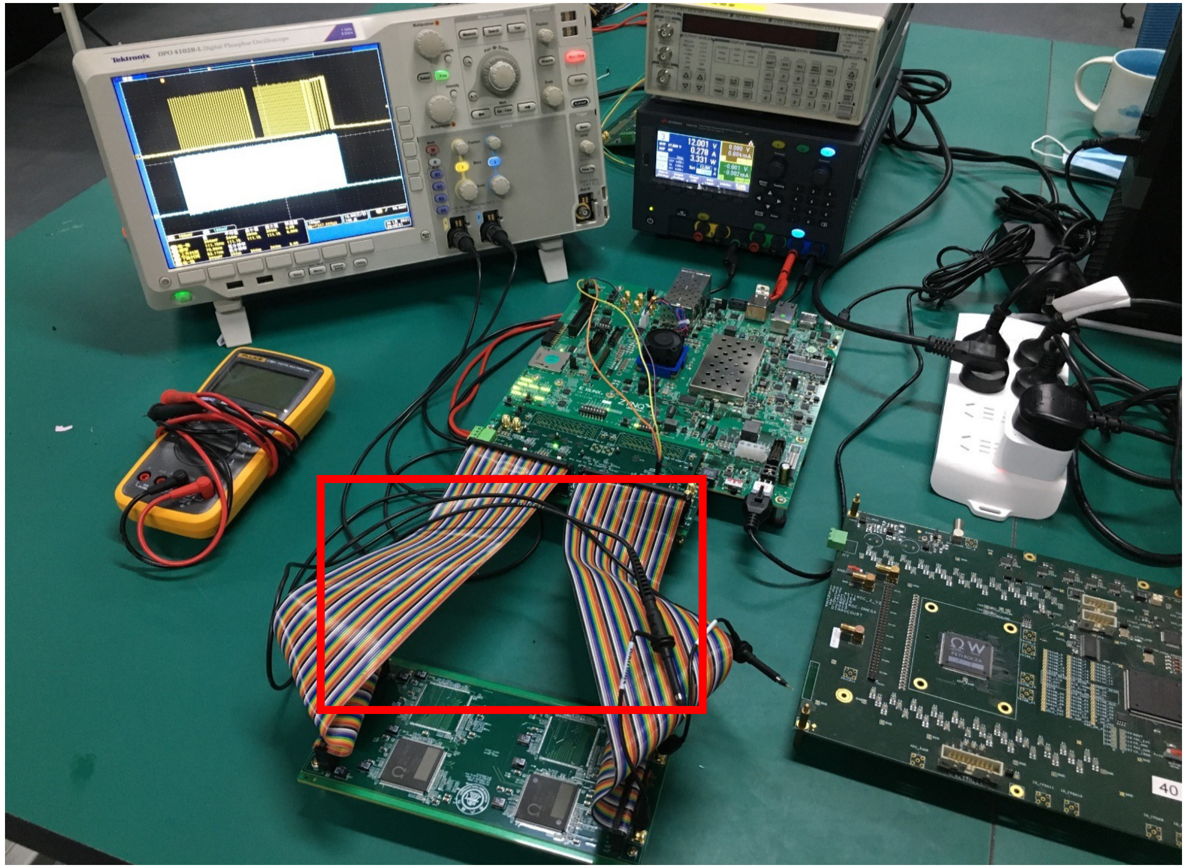




Status of System Test

- Crossstalk exists in the injection test!

```
==========================10 bit step============================
Ch0 : 64 Coarsetime: 1100011101, Decode: 100001011 ==> Counter: 267, Hit: 1
Ch1 : 65 Coarsetime: 1000010110, Decode: 111110010 ==> Counter: 498, Hit: 0
Ch2 : 66 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch3 : 67 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch4 : 68 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch5 : 69 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch6 : 70 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch7 : 71 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch8 : 72 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch9 : 73 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch10: 74 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch11: 75 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch12: 76 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch13: 77 Coarsetime: 1001011110, Decode: 111001010 ==> Counter: 458, Hit: 0
Ch14: 78 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch15: 79 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch16: 80 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch17: 81 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch18: 82 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch19: 83 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch20: 84 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch21: 85 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch22: 86 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch23: 87 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch24: 88 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch25: 89 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch26: 90 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch27: 91 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch28: 92 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch29: 93 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch30: 94 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch31: 95 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
```

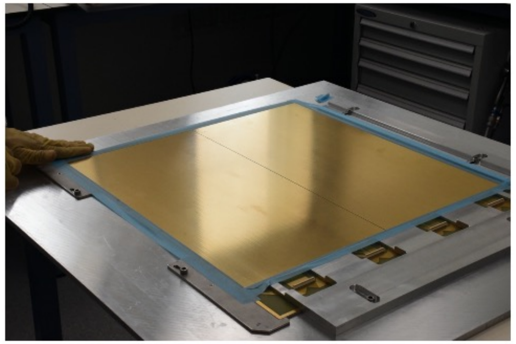


A new version of hardware is under development!

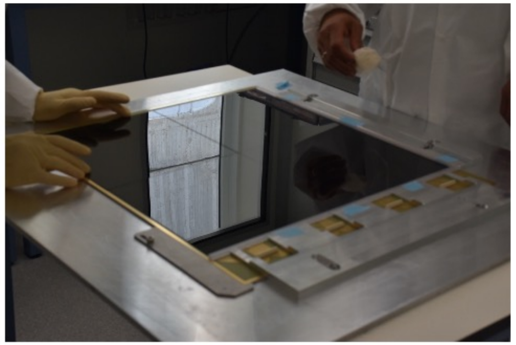
RPWELL Detector Prototype

(from Weizmann)

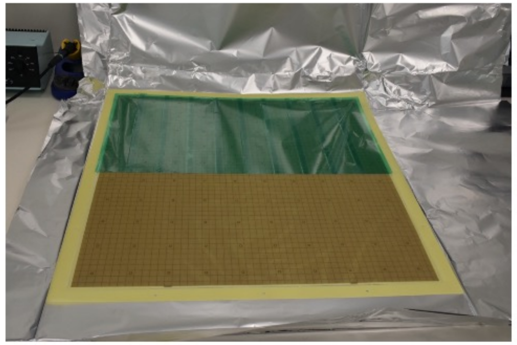
- Resistive Plate WELL is considered to be used as a sampling element in SDHCAL.
- 50×50cm^2 RPWELL prototype has been built.



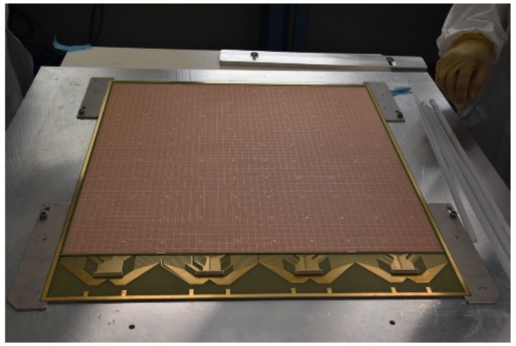
Strips readout (1mm pitch)



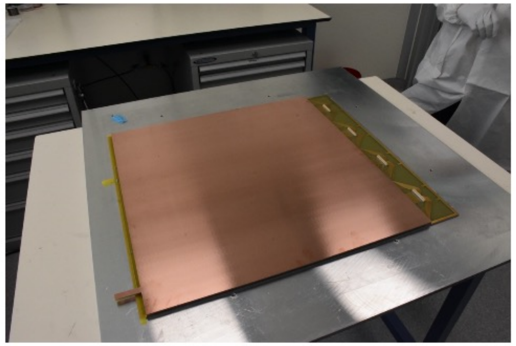
Resistive glass



Masking bottom of the THGEM



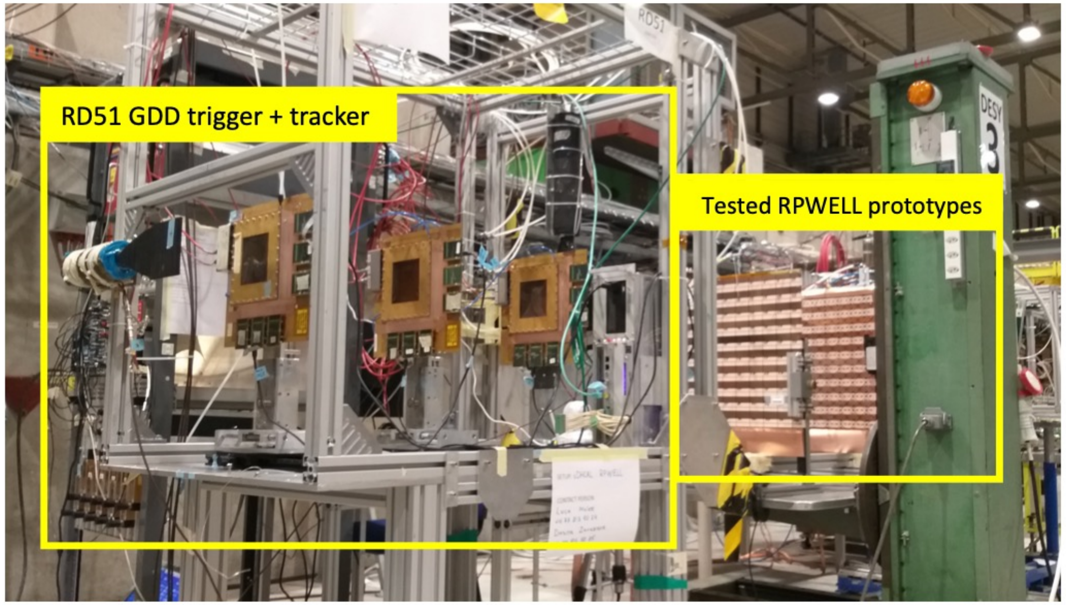
THGEM glued on the glass

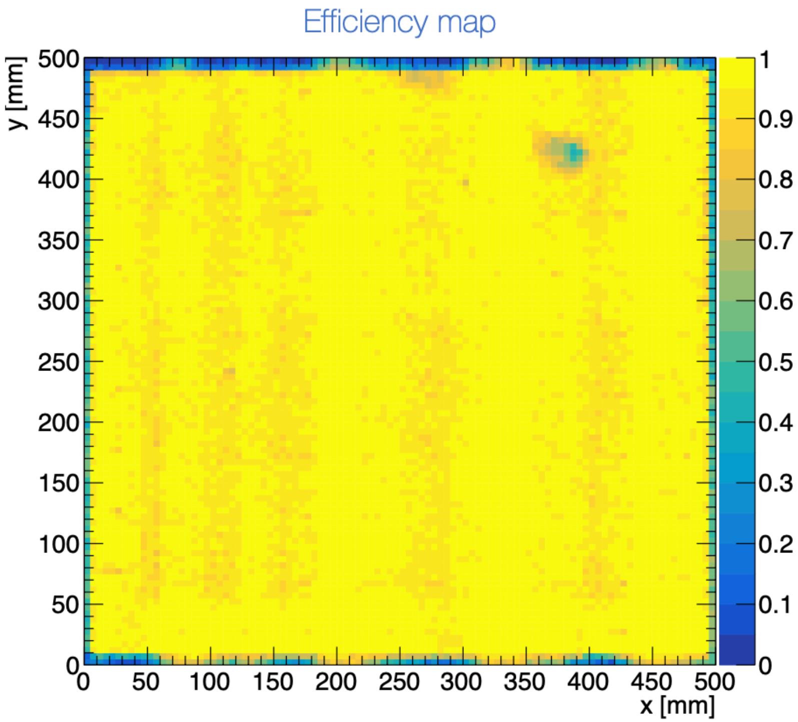


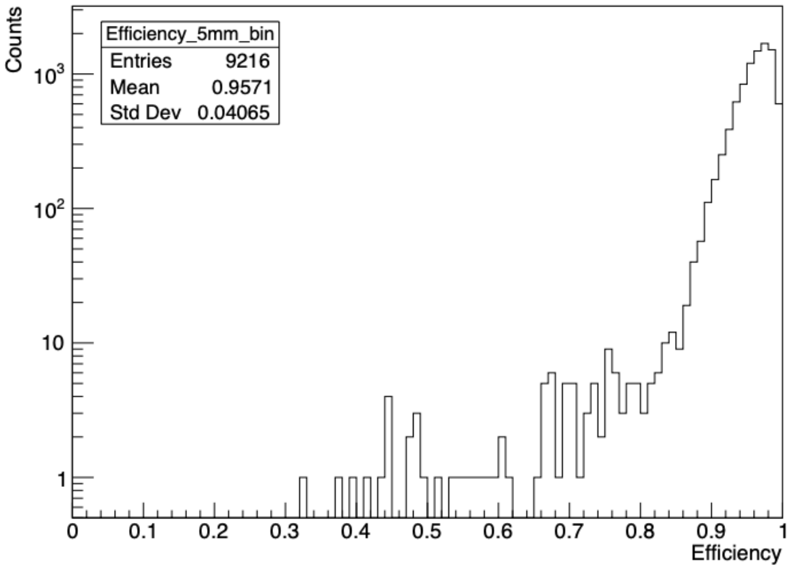
Closing chamber

80-GeV Muon Testbeam

- Muon beam, E = 80GeV
- RD51 GDD 6cm2 trigger + tracker: 3 SCs, 3 Micromegas
- DAQ: APV25 SRS







- Average efficiency ≈ 96%, std (spread) = 4%
- Low efficiency values (40 – 85%) are measured at the edges and at the low efficiency ”blub” probably related to gluing point

Summary

- A testbeam data analysis draft has been submitted to Jinst recently.
- 1x1 m^2 Glass RPC has been built and tested at SJTU.
  - A RPC performance study paper has been accepted by Jinst.
- The timing electronics prototype have been designed and tested.
  - A new version of hardware is under development.
- 50x50cm^2 RPWELL detector prototype has been build by Weizmann, and its performance was tested in a 80-GeV muon beam.

- An international effort towards building MRPC + readout electronics based on Petiroc2B.
  - University of Lyon (France), Shanghai Jiao Tong University (China), CIEMAT (Spain), Gangneung-Wonju National University (Korean), etc.

Thanks for your attention!

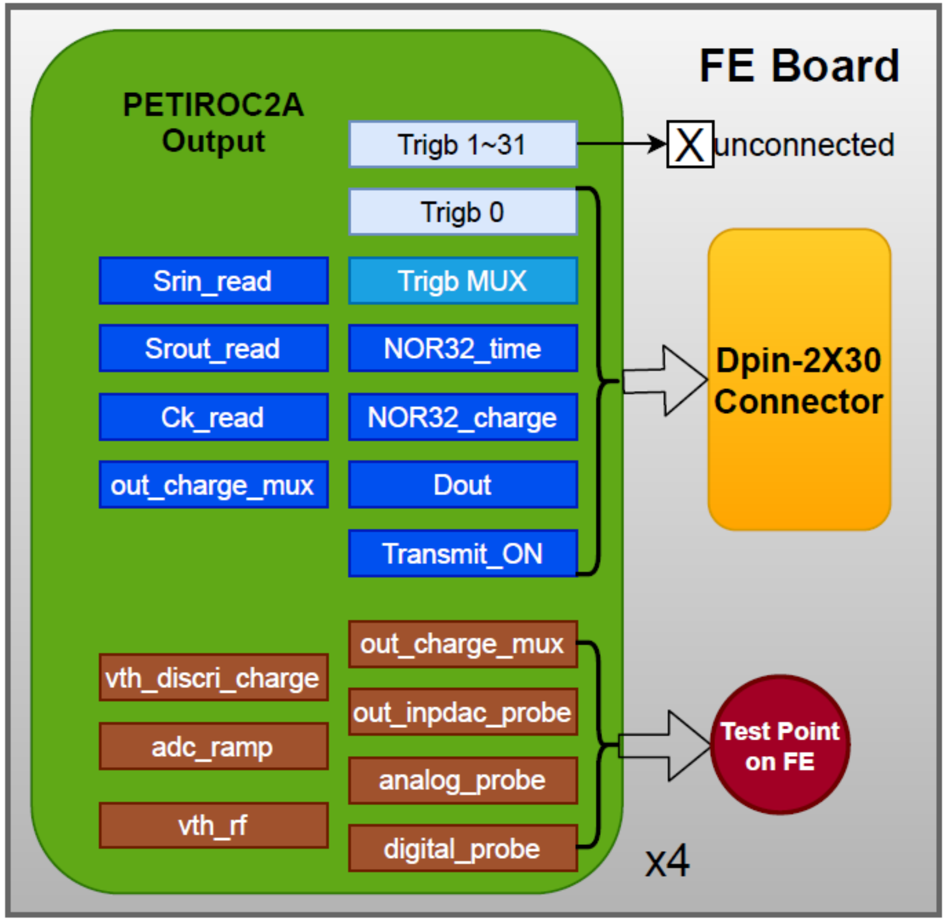
Backup Slides

Introduction of PETIROC chip

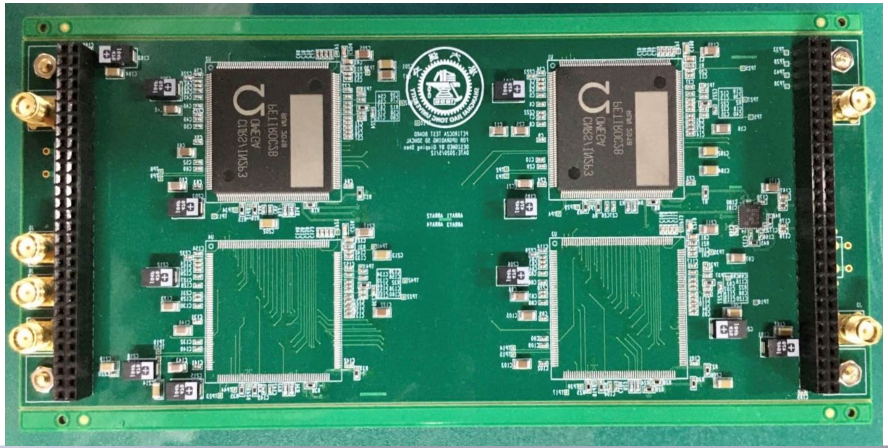
- Time measurement with 10bits TDC interpolating 40MHz coarse time
- Charge measurement (Q>50fC) with 10bits DAC
- Voltage input amplifier, 200Ohm matching
- High bandwidth preamp (GBWP> 1.2 GHz)
- PETIROC parameters:
  - One chip with 32-channels and mixed analog/digital
  - The 32chs input connected with PAD (detector unit)
  - One channel split into two parts, respectively for charge and time measurement
  - Internal DAC for each channel to adjust the amplitude of the input signal
  - Lower power consumption (~6mW/channel)
  - Jitter ~18 ps RMS on trigger output (4 photoelectrons injected)

Sub-component Design and Testing

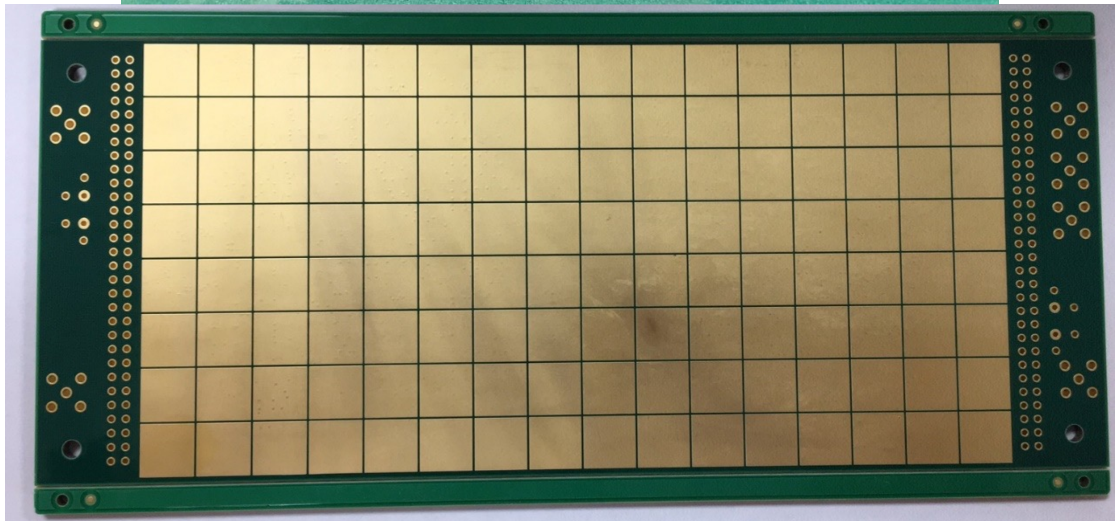
- Front-End readout Board Design with pads and four petiroc2b



Block diagram of front-end electronics



Front



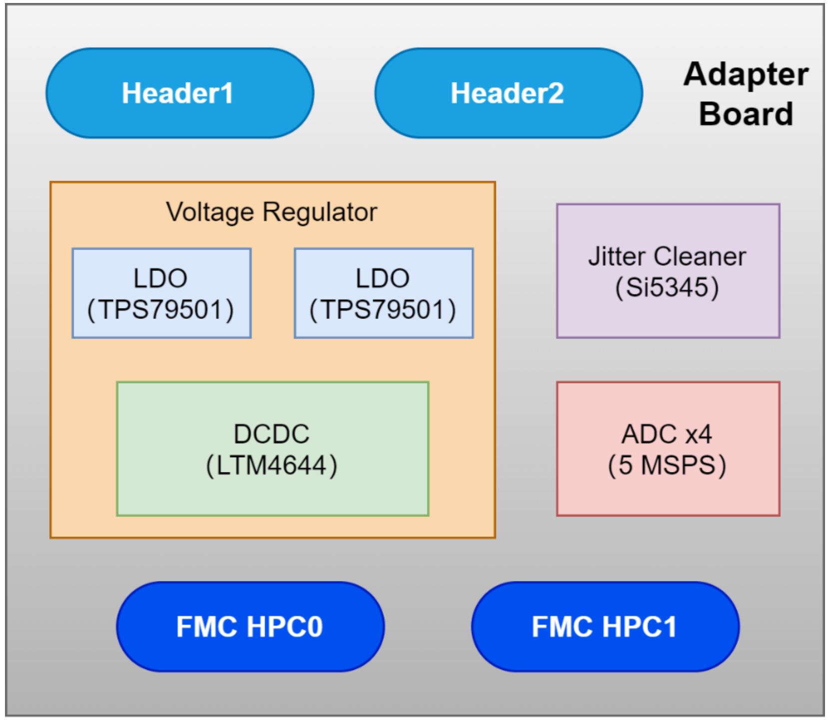
Back

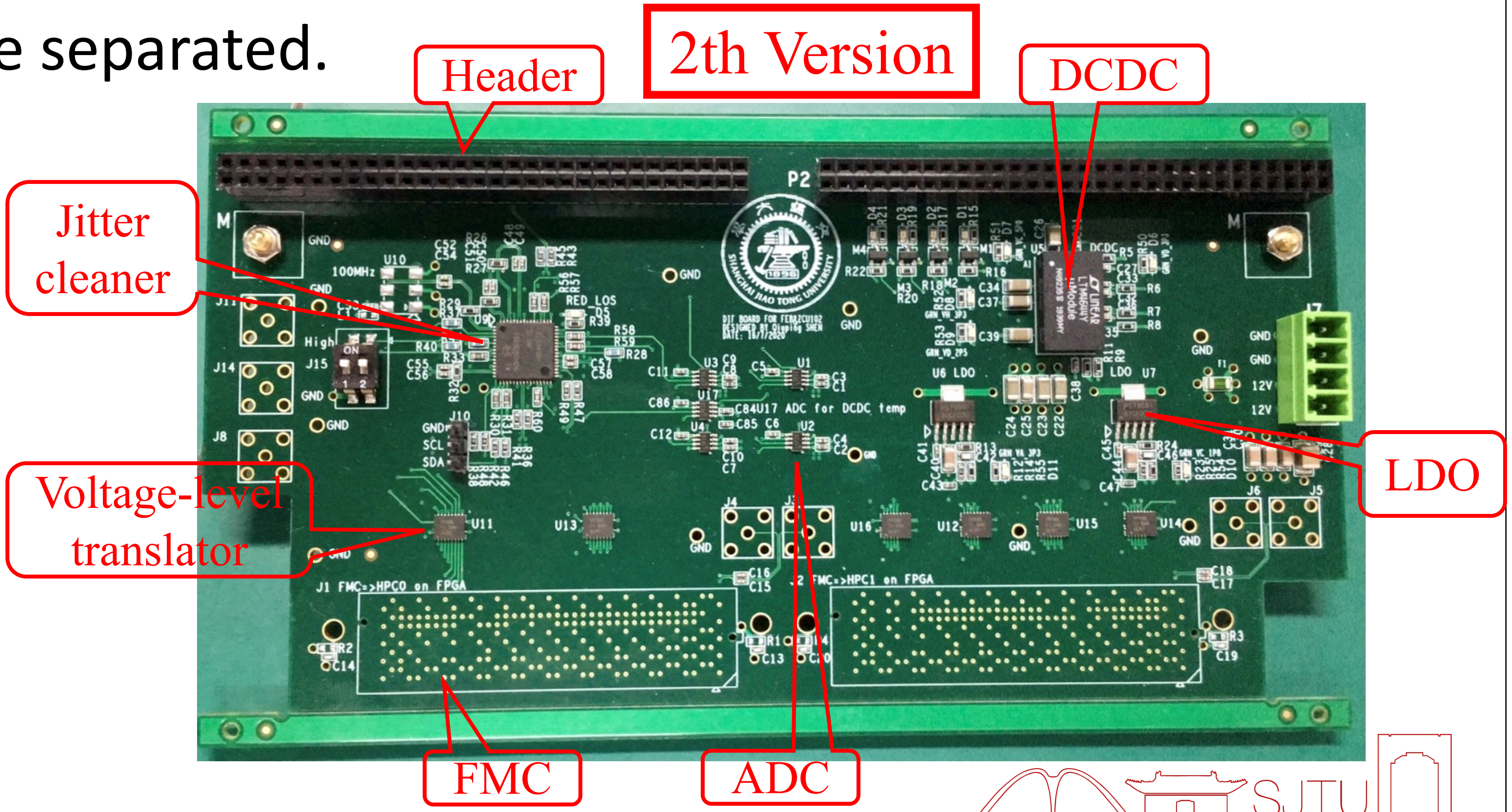
Sub-component Design and Testing

- Detector Interface Card Design: mainly jitter cleaner and power system
- DIF card will be in charge of the communication and data transfer with the FE electronics(two headers) and ZCU102(two FMCs).

More Details

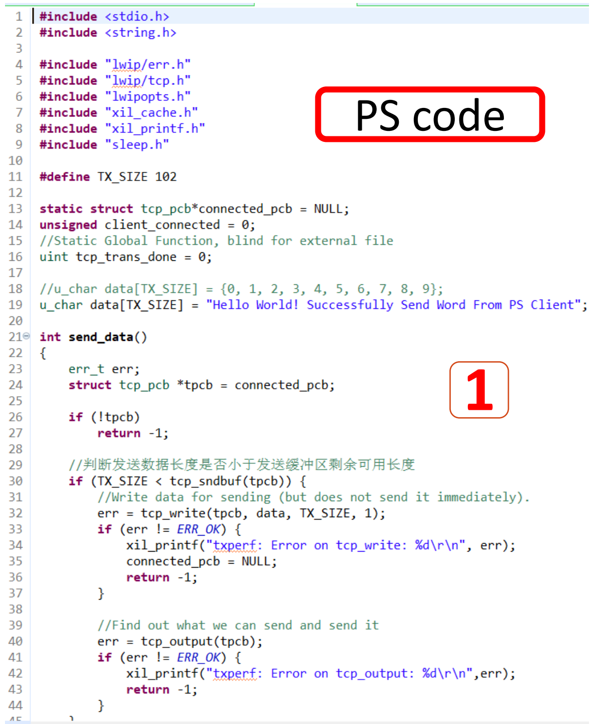
- Analog and digital power are separated.

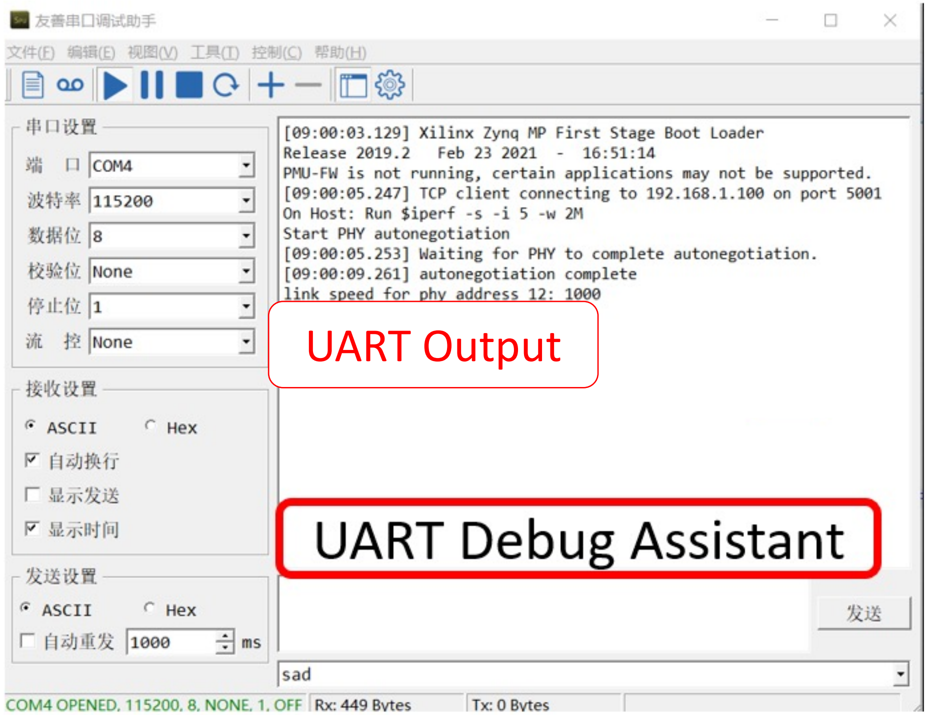




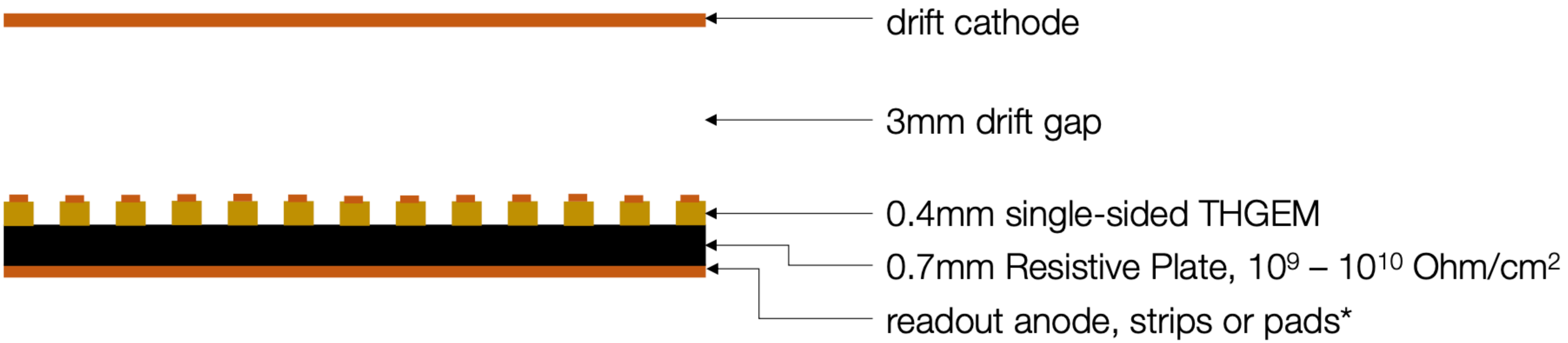
Embedded design based on FPGA -- UART

- The embedded design in ZCU102(PS side) mainly contains serial port communication(UART), ethernet communication(TCP/IP) and PETIROC configuration(Slow Control).
- UART test in PS side:
  - Hardware only needs Processing System part on ZCU102.
  - Write the C/C++ code and run on the hardware platform.
  - Information is printed on the tool window through UART port.





UART communication test


drift cathode
3mm drift gap
0.4mm single-sided THGEM
0.7mm Resistive Plate, $10^9 – 10^{10}$ Ohm/cm^2
readout anode, strips or pads*