Ladder design discussion

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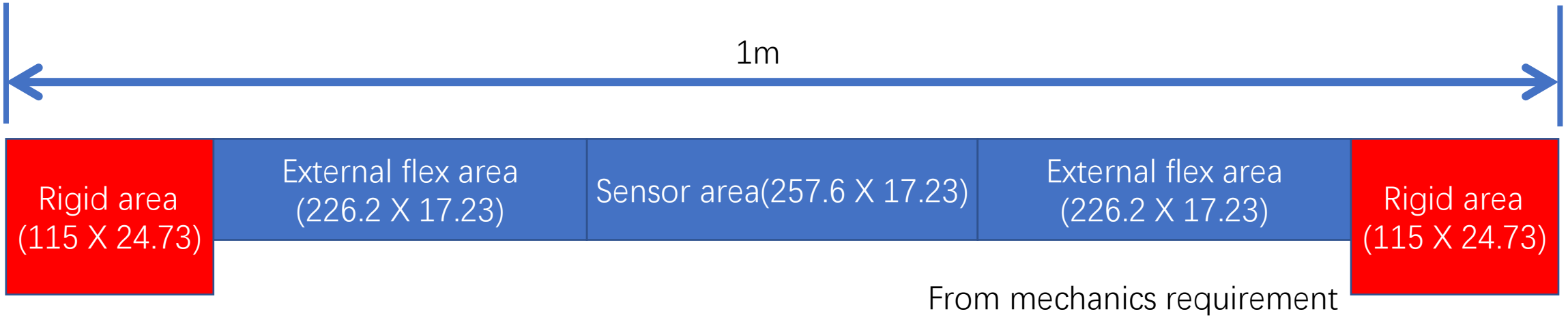
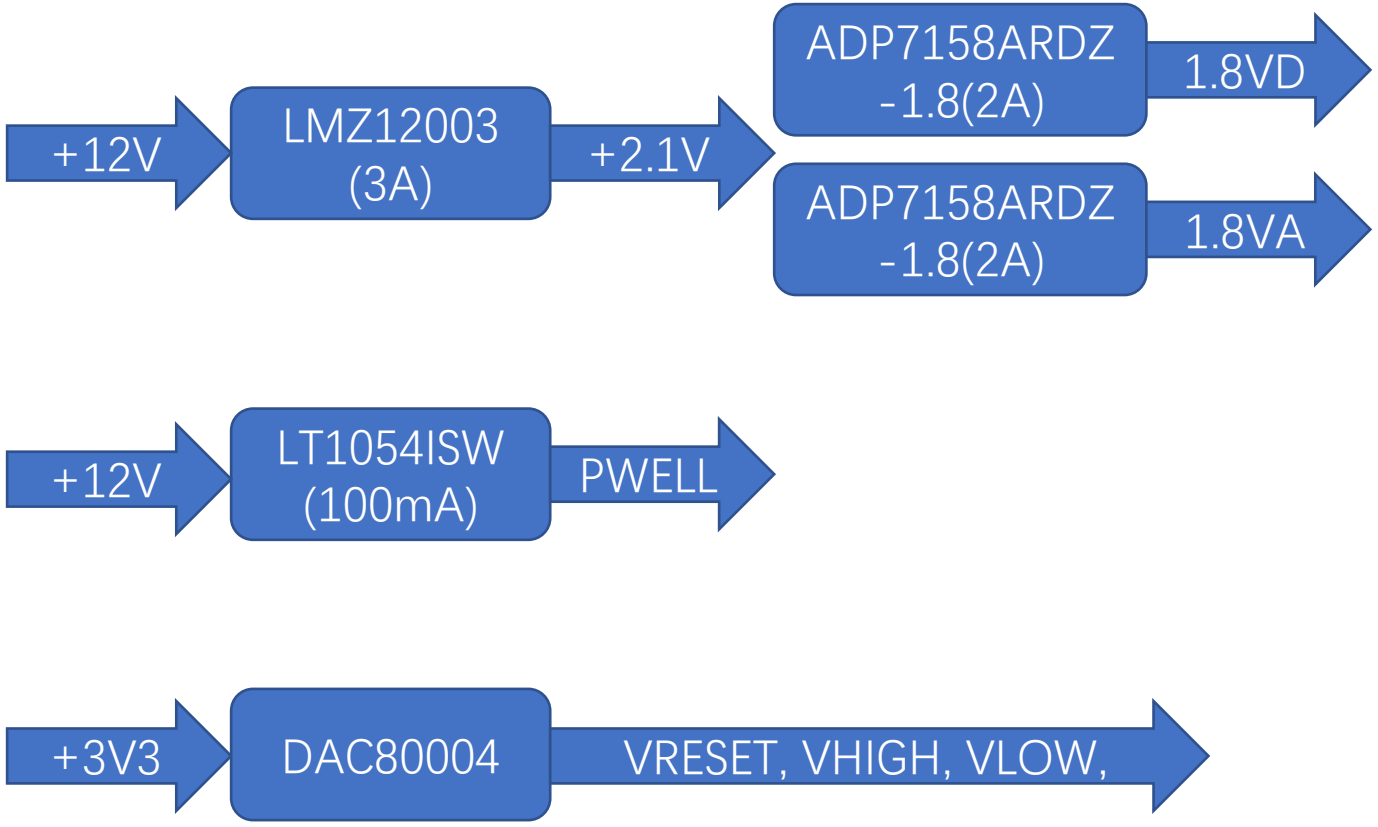
Outline



- Dual sides readout, 5 chips per side
- Socket, power supply and filter are placed on rigid area
- 1 meter is the limitation of manufactory

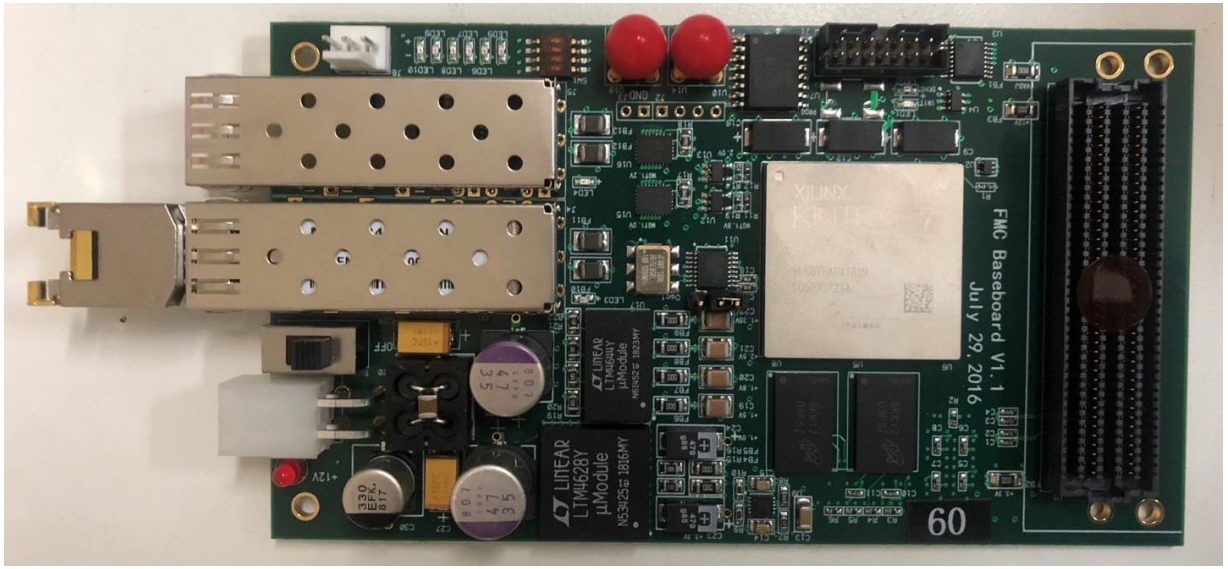
Power supply

- Requirement:
  - 1.8VDDA < 8.3mA
  - 1.8VDDD ≈ 0.21A
  - PWELL (-6V – 0)
  - VRESET, VHIGH, VLOW from DAC



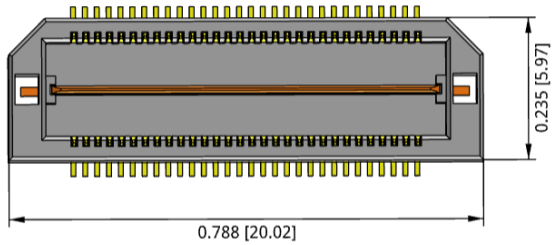
Socket

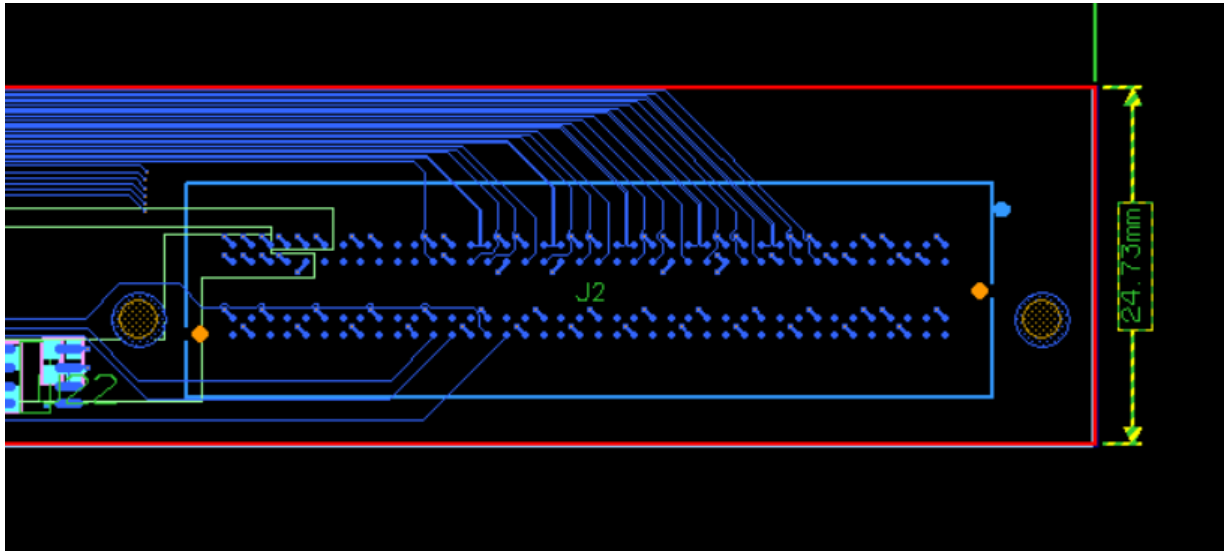
- FMC standard
  - ASP-134606-01: 8.5mm height



FPGA board

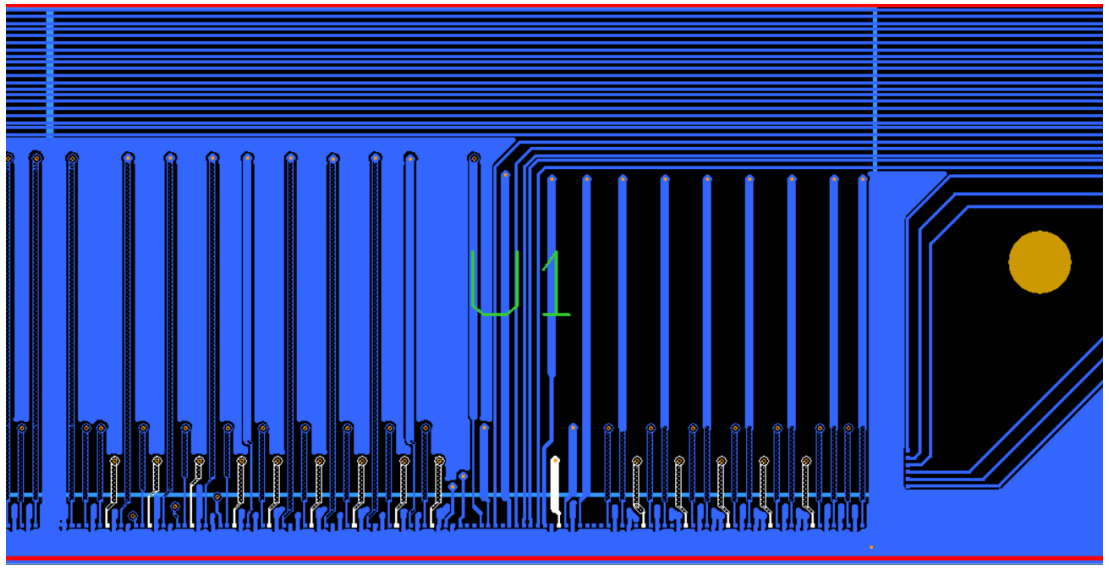
- Backup
  - Qth-030-01-F-D(0.5 mm pitch)



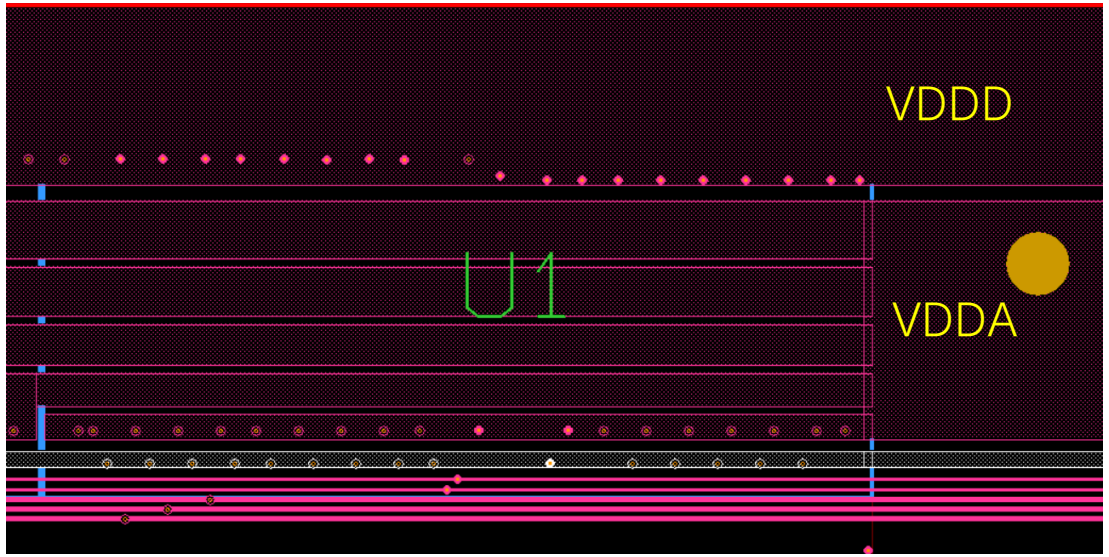


Layout topological

- Independent signals:
  - CLK40M, SPI_CSB, DOUT_P, DOUT_N, SER_VALID
- Shared signals:
  - APULSE, TRIGGER, VRESET, VHIGH, VLOW
- SPI signal
  - Inter-conn / shared
- Power supply
  - VDDD, VDDA, PWELL, GND



Bonding side

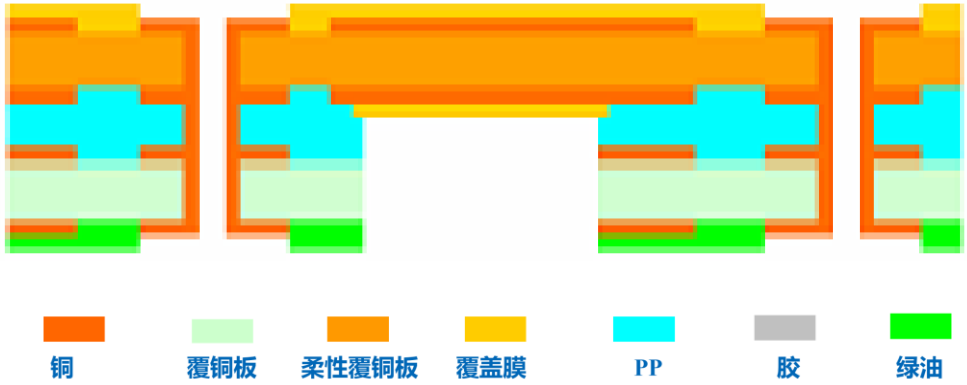


Plane side

- Vdrop: 0.03Ω = (1mmX25.6mmX0.5oz)
  - VDDD 6mm width, 0.21A * 0.03 / 6 *12.5 = 13mV
  - VDDA 4mm width, 0.0083A * 0.03 / 4 * 12.5 = 1mV
  - GND 2mm width, 0.22A * 0.03 / 2 *12.5 = 39mV

- Attenuation: 0.1db = 1 inch @ 1GHz
  - 50cm : -2db

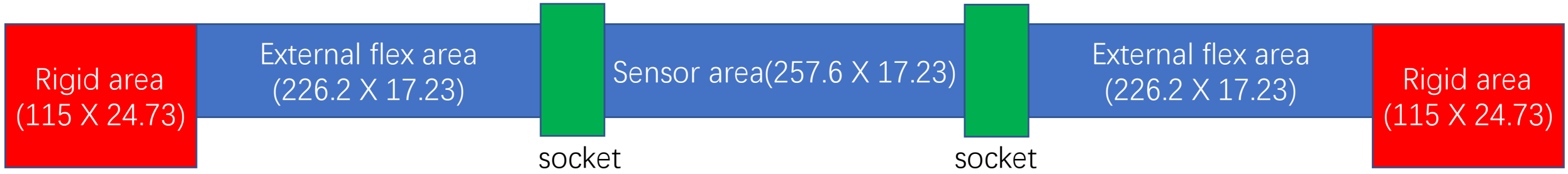
2 options



- Option1
  - 2 layers flex + 4 layers rigid
  - Inter-conn signal used
  - worse signal integrity
    - Noise
    - Ground bounce

- Option2
  - 4 layers flex + stiffener
  - Shared spi signal used
  - better signal integrity
    - complete ground plane

discussion


Rigid area
(115 X 24.73)
External flex area
(226.2 X 17.23)
socket
Sensor area(257.6 X 17.23)
socket
External flex area
(226.2 X 17.23)
Rigid area
(115 X 24.73)

Plan

- After discussion，1 week for design and 2~3 weeks for production.