SDHCAL R&D Activities

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On behalf of SDHCAL Group

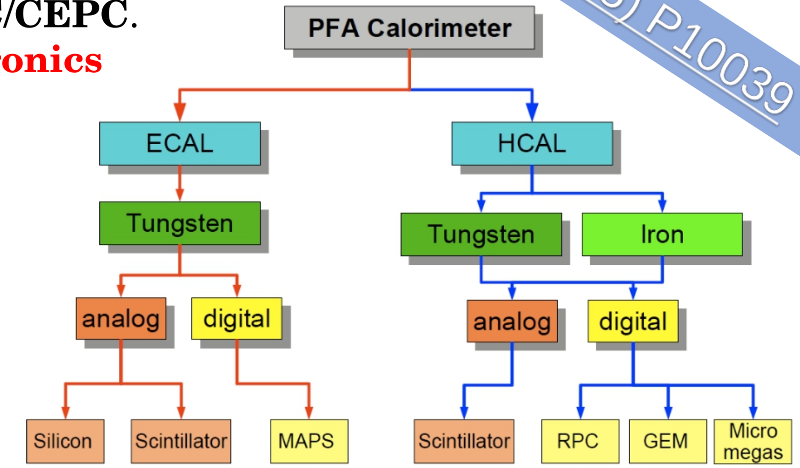
Outline

- Introduction
- New SDHCAL prototype
- Timing developments
- RPC and MRPC developments
- Woven strips
- Summary

JINST 10 (2015) P10039

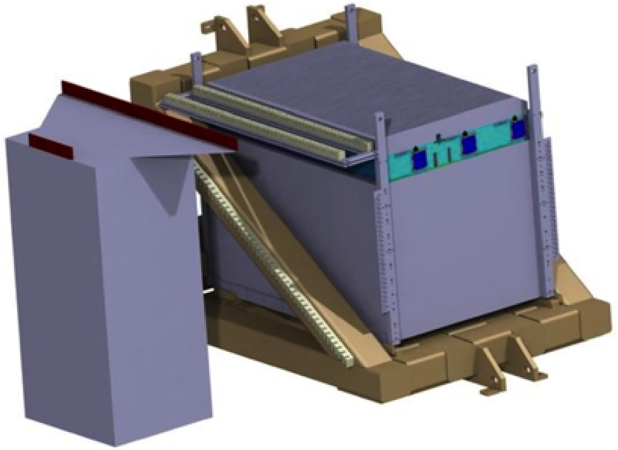
Semi-Digital Hadronic CALorimeter

The SDHCAL-GRPC is one of the two HCAL options based on PFA and proposed for **ILD of ILC/CEPC**. Modules are made of **48/40 RPC chambers** equipped with **semi-digital, power-pulsed electronics** readout and placed in **self-supporting mechanical** structure to serve as absorber as well.



The structure of SDHCAL :

- Very compact with negligible dead zones
- Eliminates projective cracks
- Minimizes barrel / endcap separation (services leaving from the outer radius)

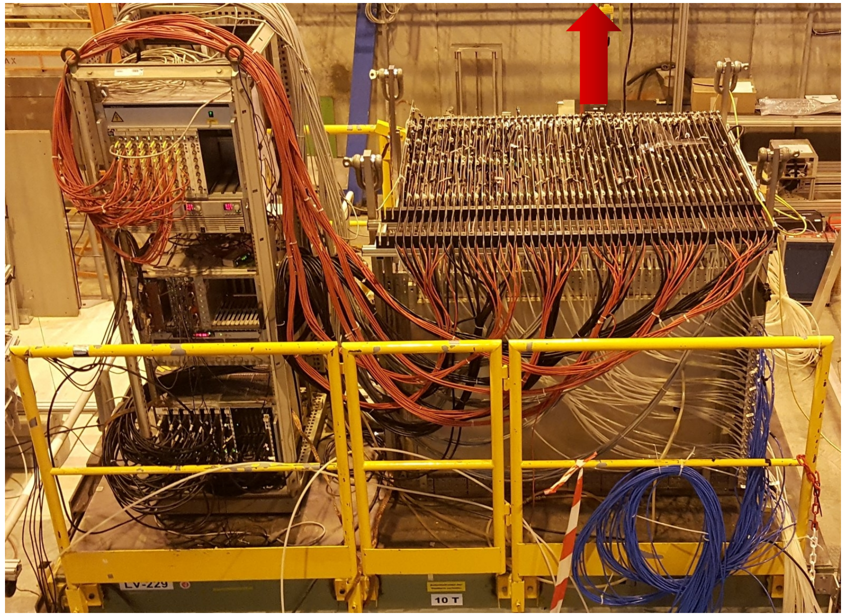


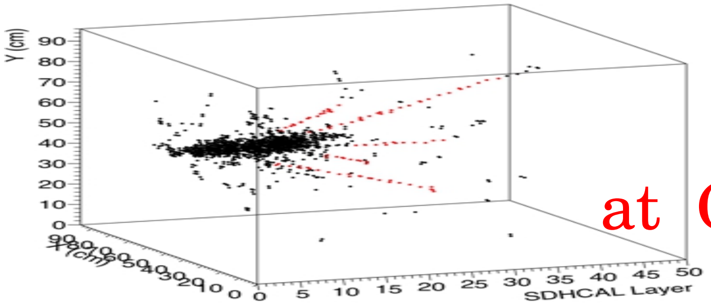
Challenges :

- Homogeneity for large surfaces
- Thickness of only few mms
- Lateral segmentation of 1 cm X 1 cm
- Services from one side
- Embedded power-cycled electronics
- Self-supporting mechanical structure

Hits associated to 3 different thresholds :
- 1st threshold = 110fC
- 2nd threshold = 5pC
- 3rd threshold = 15pC

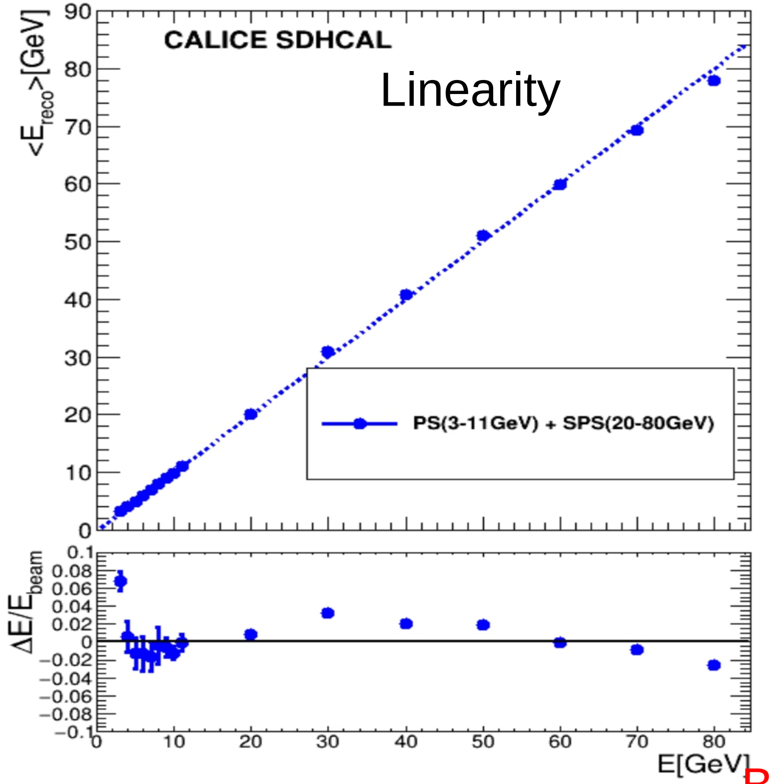
Active medium : 48 GRPC layers (~$6\lambda_I$)
Dimensions : 1m×1m×1.3m
Granularity : 1cmx1cm (~500 000ch)
Power-pulsed electronics
Self-supported mechanical structure

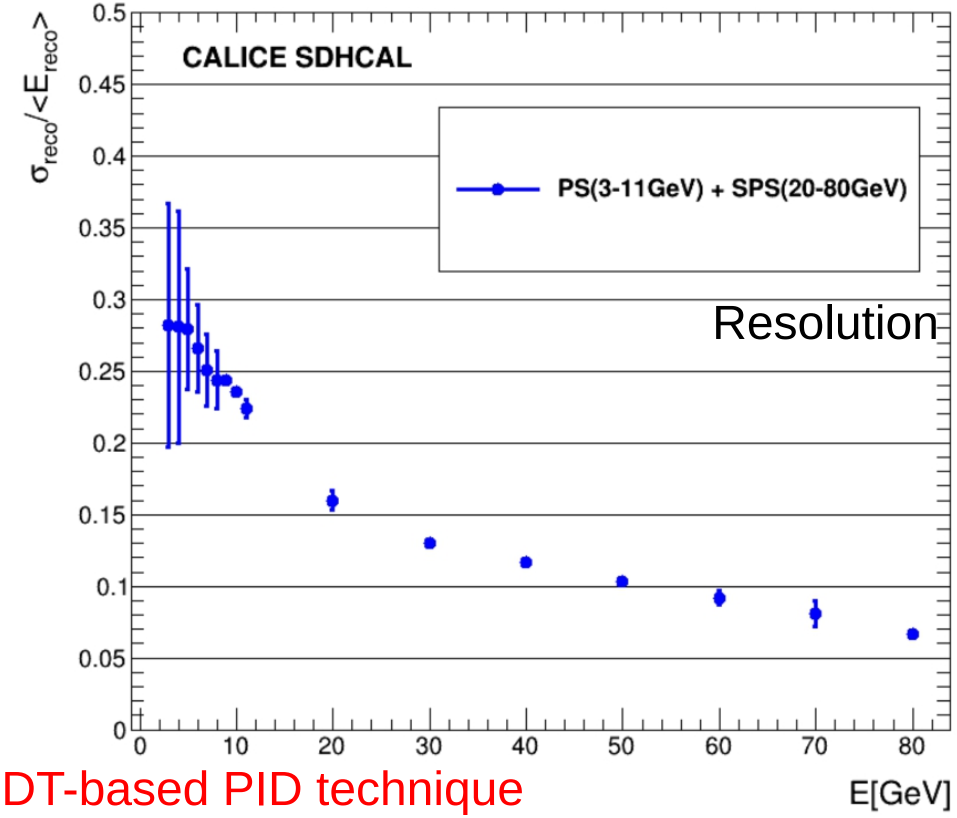




Energy reconstruction

SDHCAL was exposed to beam particles
at CERN PS, SPS in 2012, 2015, 2017 and 2018





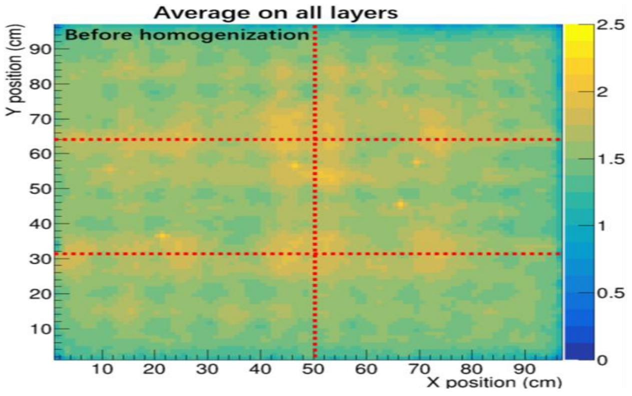
BDT-based PID technique

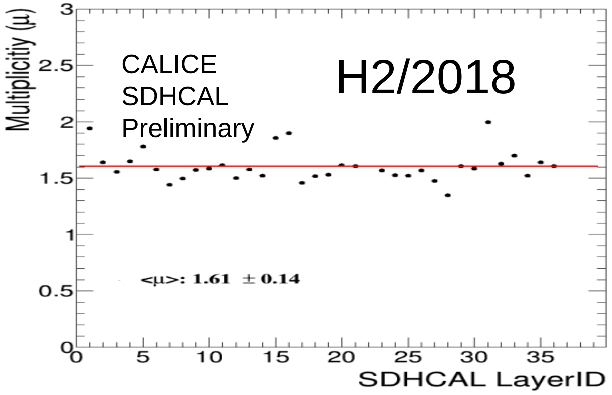
Papers :

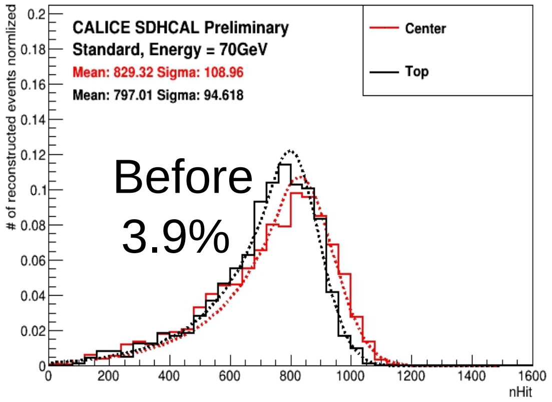
CALICE note CAN054
JINST 11 (2016) P04001
JINST 12 (2017) P05009
JINST 15 (2020) P10009
arXiv:2202.09684

Futher improvements on the energy reconstruction

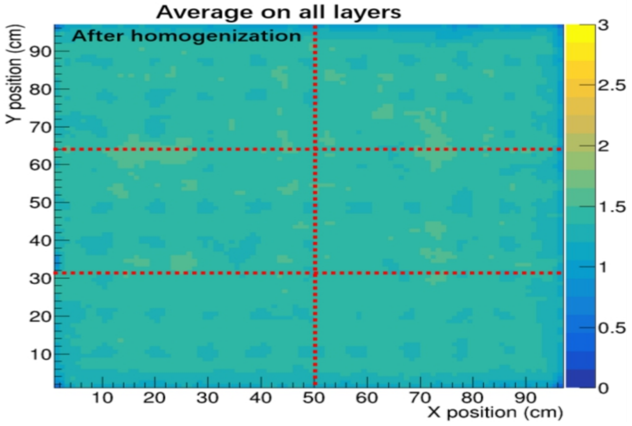
The homogeneity of the detector response is important to achieve better energy reconstruction

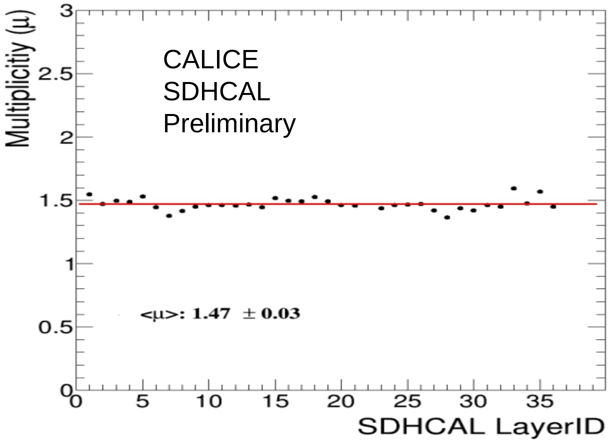


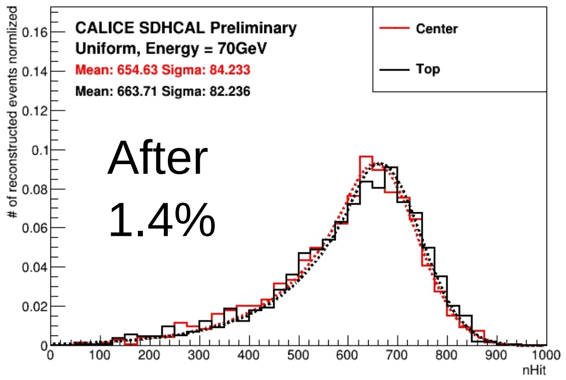




Multiplicity







A new calibration method based on varying the thresholds rather than the electronic gain was found to be powerful. Muon runs with different thresholds Thr1: 0.1-0.42 pC, Thr2: 0.4-5, Thr3:4.7-24) and efficiency and multiplicity were measured for each value. The values of the three thresholds of each ASIC were fixed to obtain same multiplicity (first threshold) and the same efficiency for thr2 and thr3.

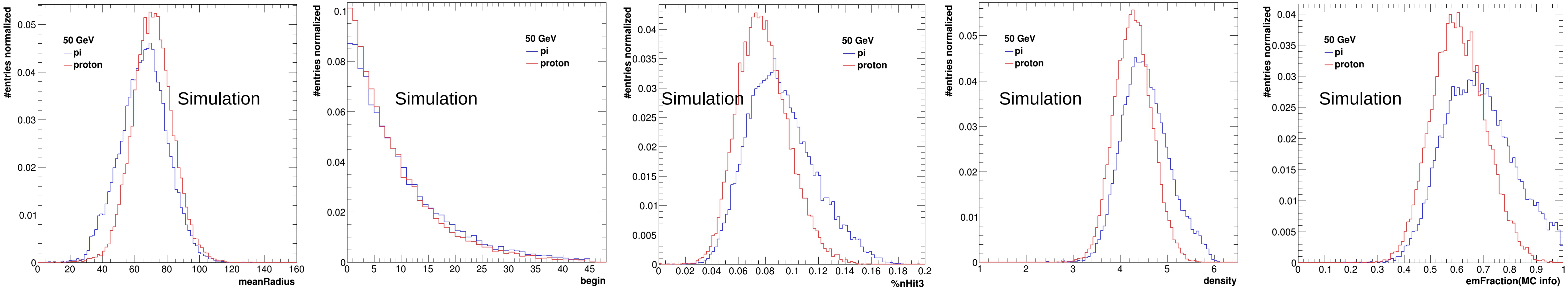
SDHCAL

- ✓ Excellent not only to apply PFA by separating nearby showers but also to measure their energy.
- ✓ Excellent linearity and very good resolution.
- ✓ Hadronic shower is an excellent asset to identify particles and then better measure their energy.

Next step : Hadron identification

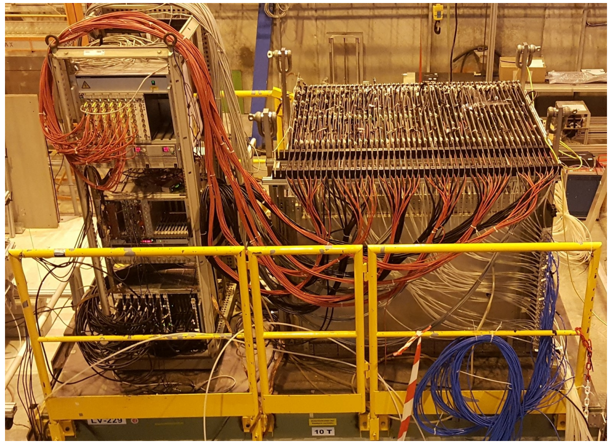
Identify the nature of the hadrons. → Better reconstruction

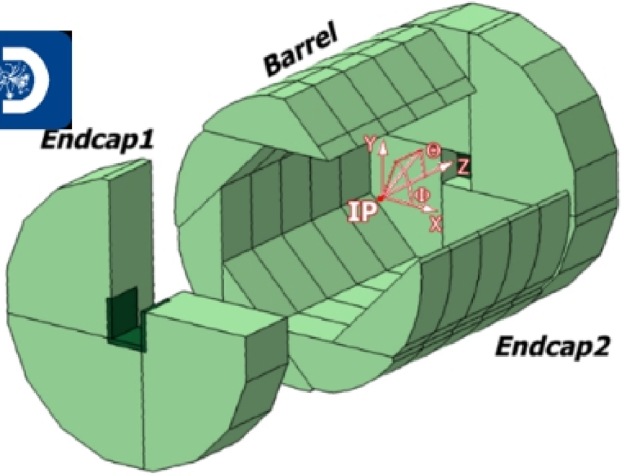
No distinction was made between pions and protons or others. Hadronic showers of pions and protons are not identical

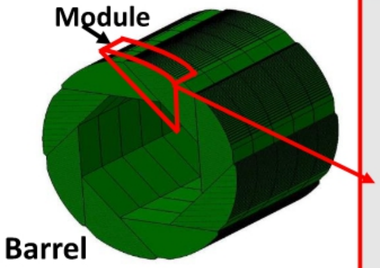


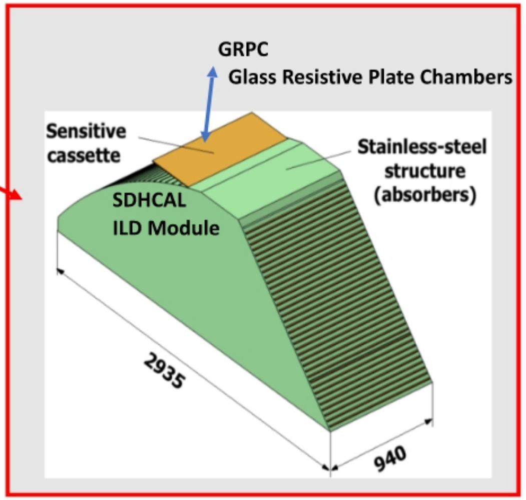
2022 beam test : study pion vs proton and kaon showers using Cerenkov detectors.
Use BDT technique to develop hadron PID and then energy construction algorithm with different parameters could be used.

New SDHCAL prototype









Move from 1m*1m to ~3m*1m (real design)

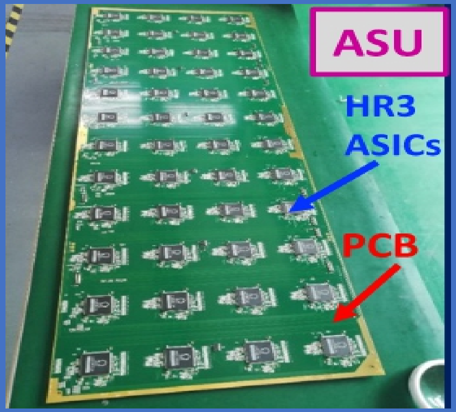
.implies new challenges for the detector, embedded electronics and mechanics.

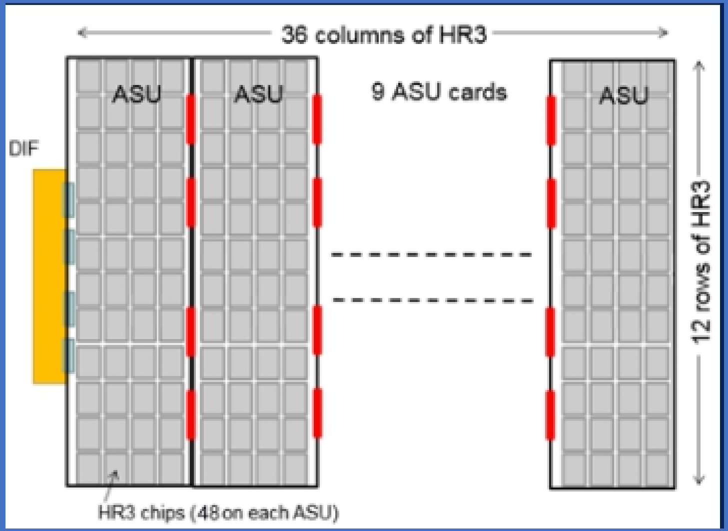
New prototype with a mechanical structure of 4 plates of ~1x3m^2
(assembled with similar procedures to the final one) with large RPCs equipped with a new improved electronics.

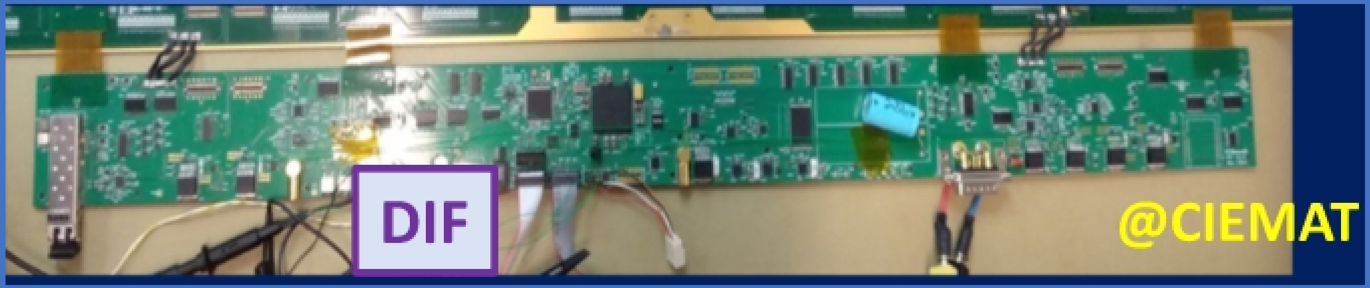
Status of the new prototype

Electronics

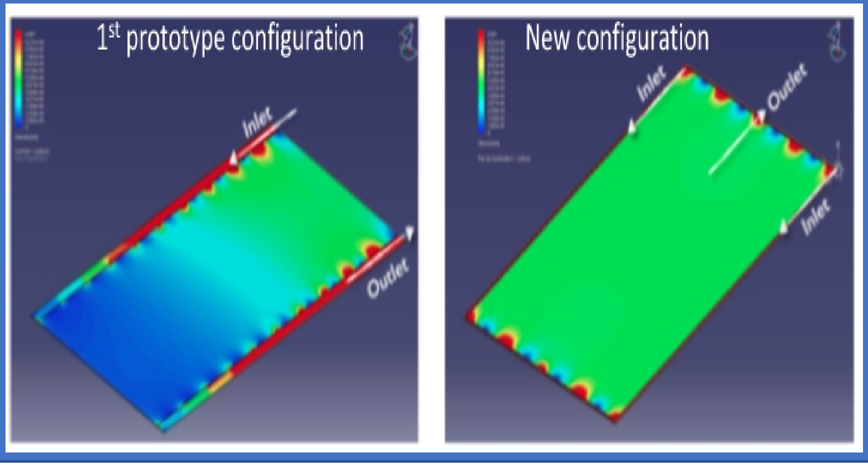
- New ASIC : HARDROC3
- ASU: 1x0.33 m^2 with 13 layers
- 1 DIF / chamber (up to 1x3 cm^2)
- 432 chips ~38k ch



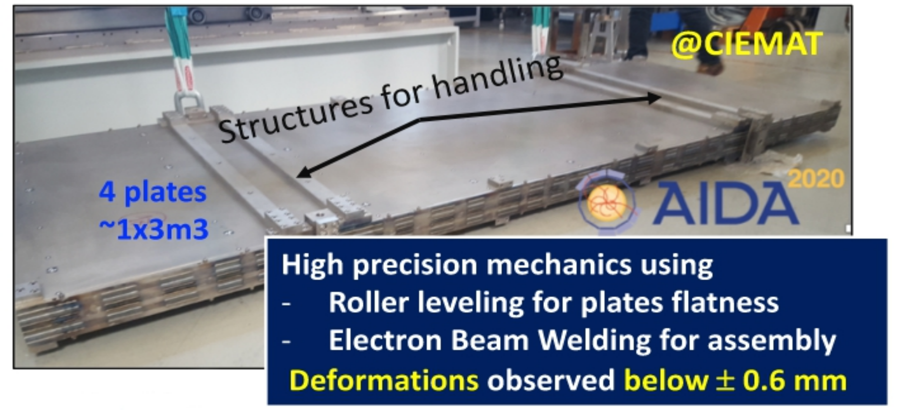




Chambers



Mechanical structure

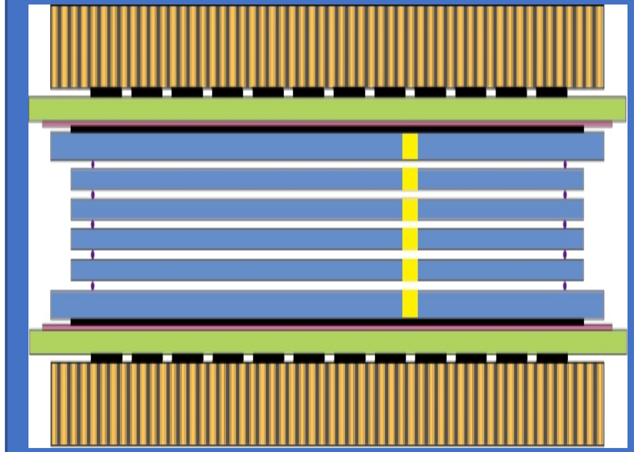


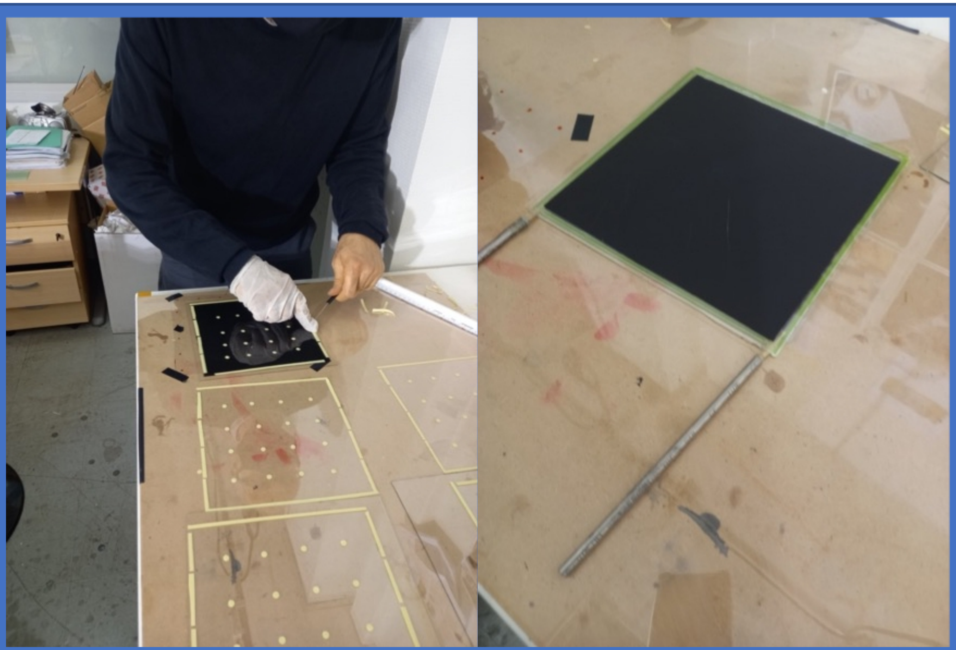
Timing developments

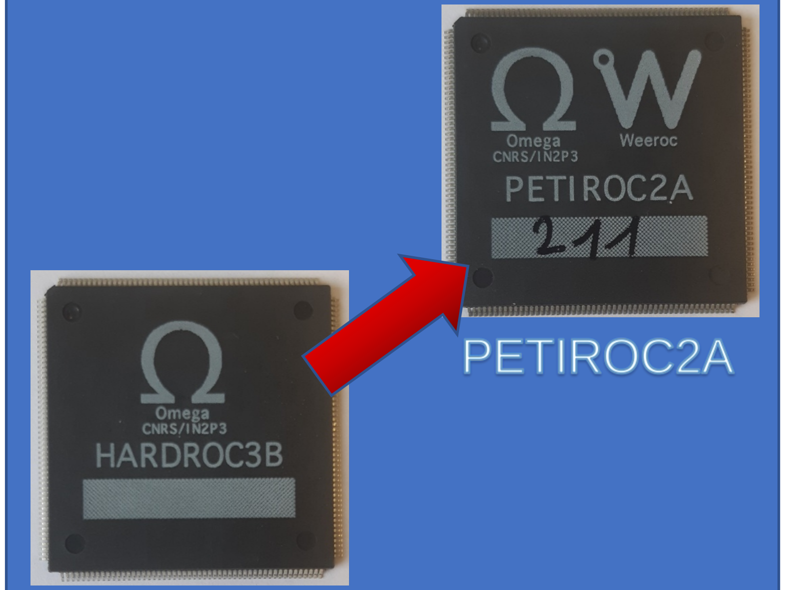
Goal : Extend the SDHCAL to include timing information (**100-200ps resolution**) for a **5D-calorimeter (x,y,z,E,t).**

Need to move to Multi-gap RPC (~1ns to ~20-100ps).
Need to change the electronics : from HARDROC2B to PETIROC2A (200ns to <40 ps)

MRPC





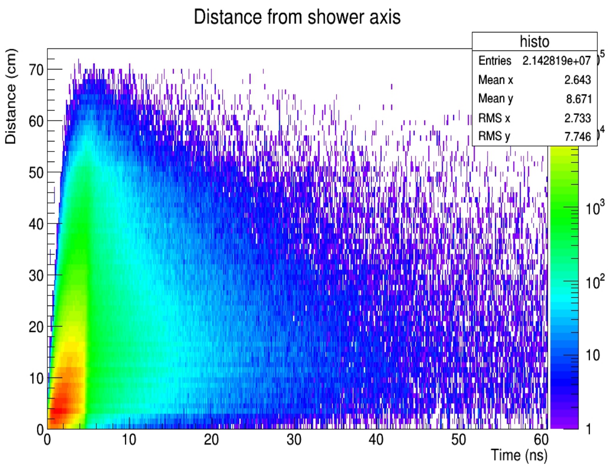


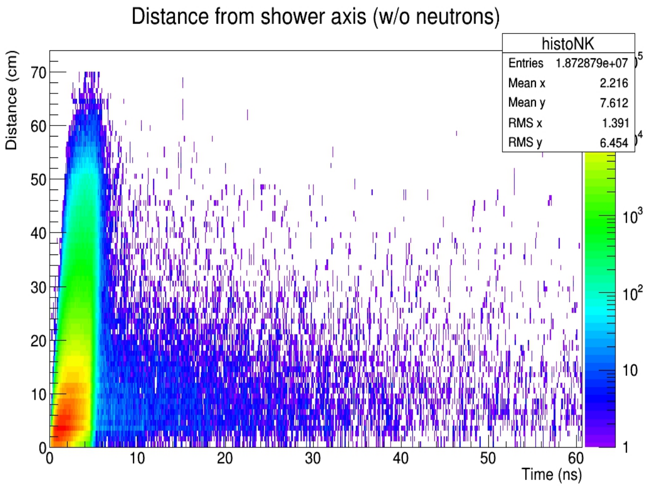
PETIROC2A

HARDROC3B

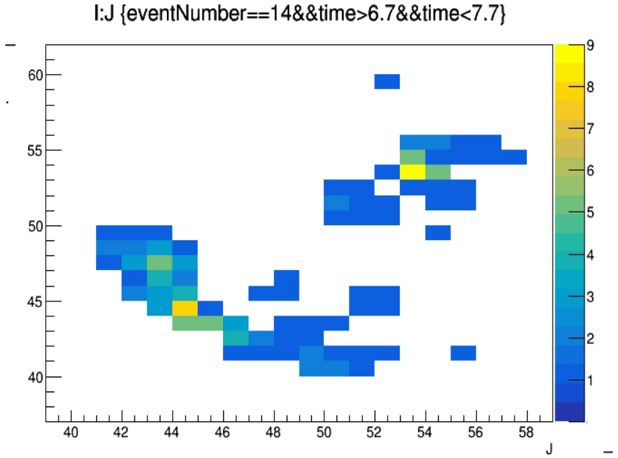
Timing information

- Timing could be an important factor to identify delayed neutrons.

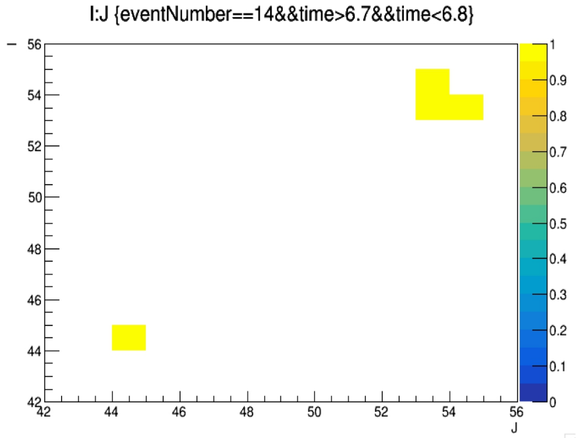




- Separate close-by showers and reduce the confusion. Improve PFA.



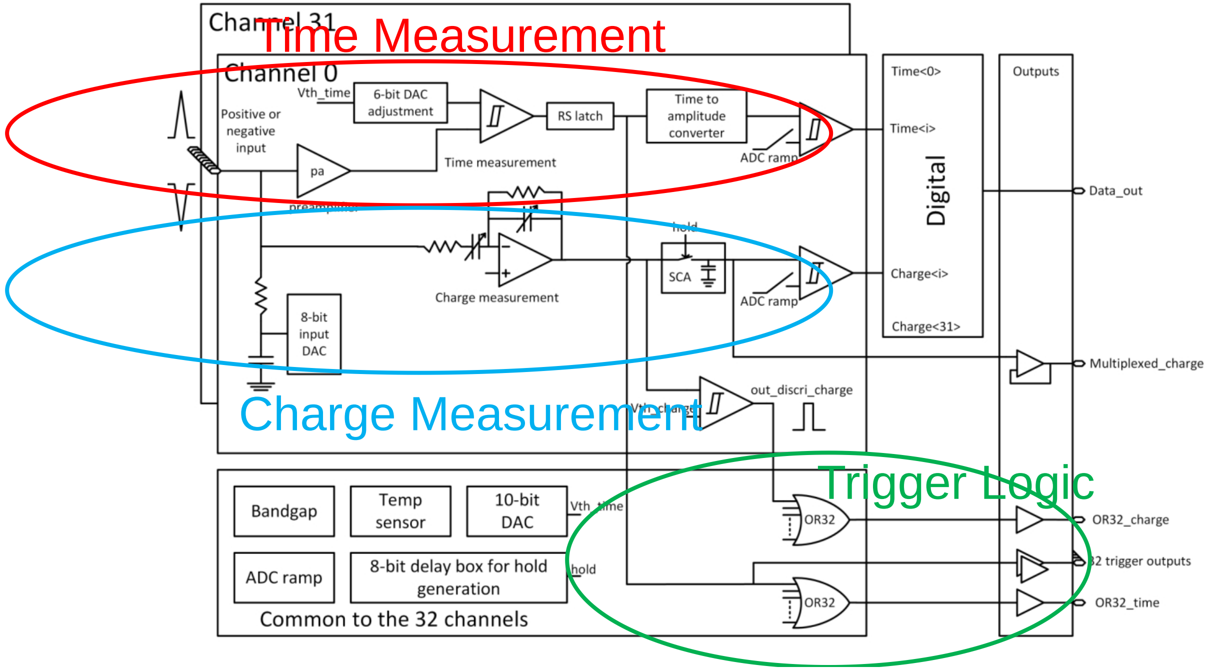
1 ns resolution

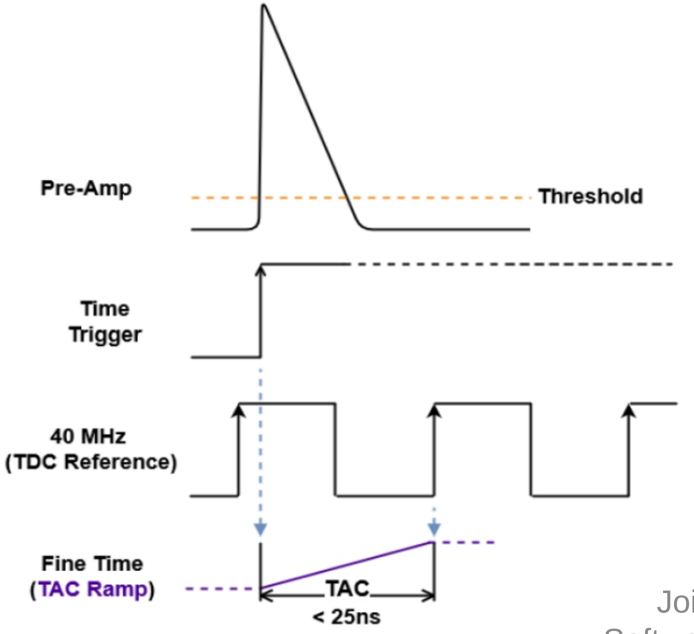


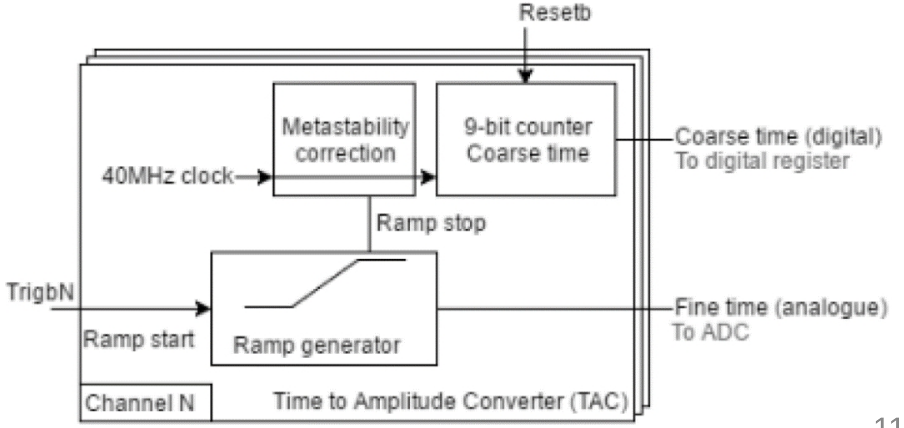
100ps resolution

PETIROC 2A

- Time measurement with 10 bits TDC interpolating 40MHz clock
- Timing resolution below 40 ps
- 32 input channels
- charge and time measurement
- Power consumption: ~6mW/channel

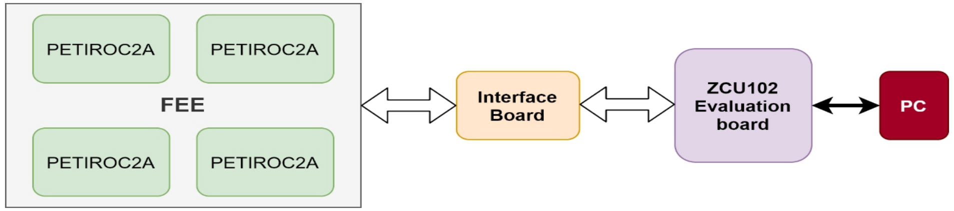




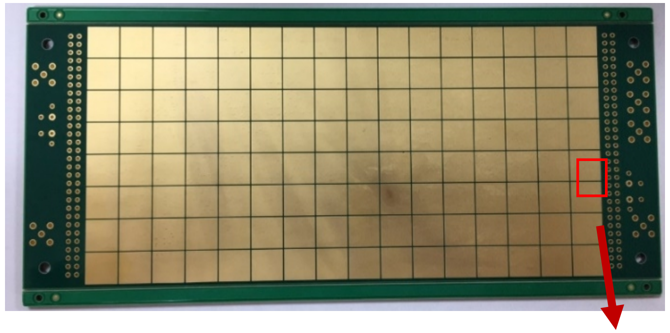


FEE Prototype

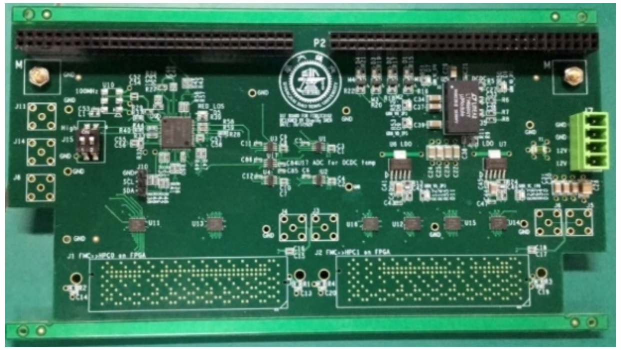
- The FEE : 4 PETIROC, 128 pads.
- Detector Interface (DIF) : connect FEE and FPGA board, data transmission
- power rail, clock source.



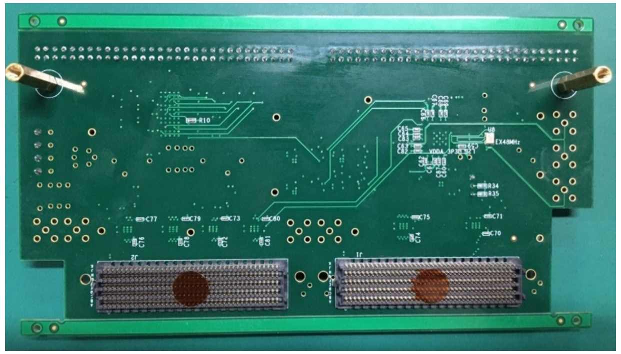
FE Board

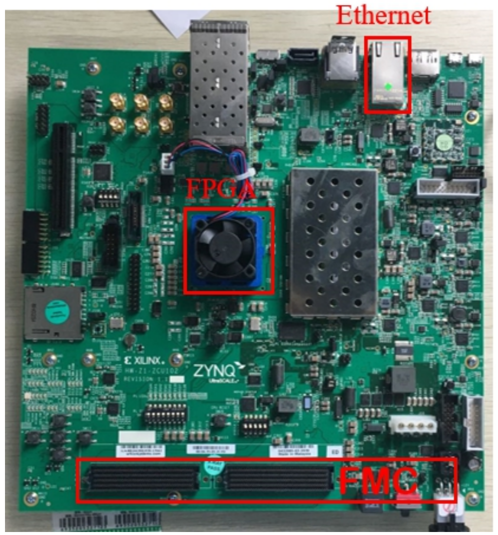


128 pads with the cell size 1cm × 1cm



DIF Card



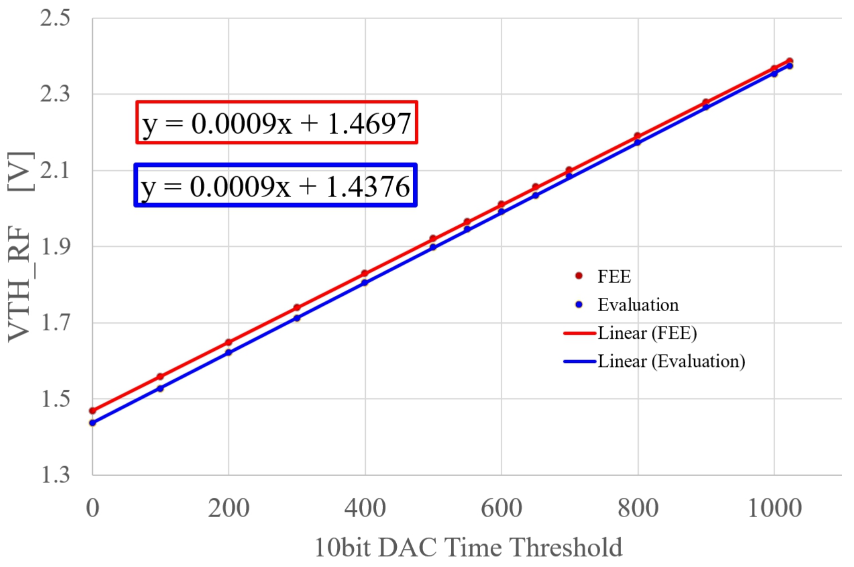


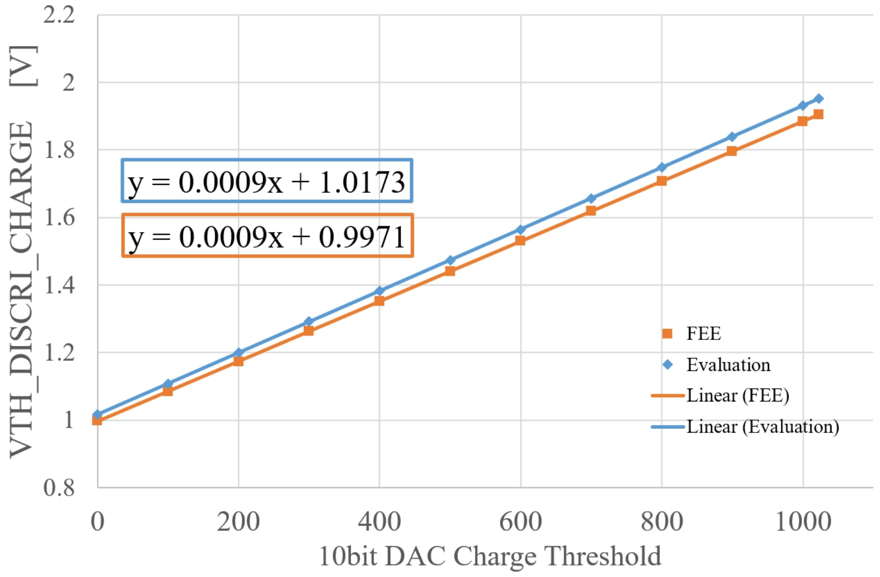
ZCU102

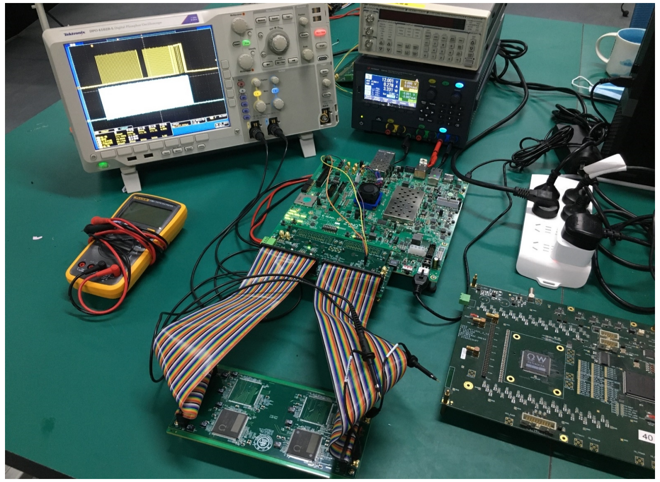
Time and Charge Threshold Voltage Test

- All of bias voltage values are correct.
- Output data has been checked, after sending trigger signals.
- Time threshold is correct according to the voltage value with 10bit DAC.
- Time and Charge threshold can be well controlled.

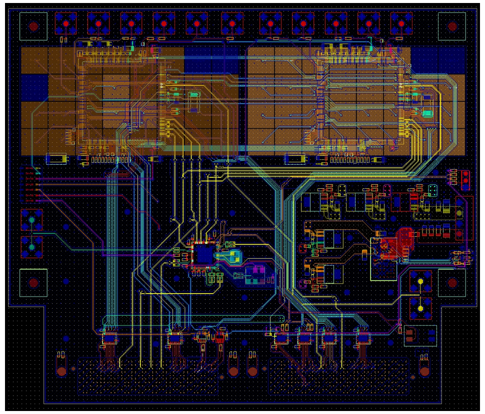
Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658







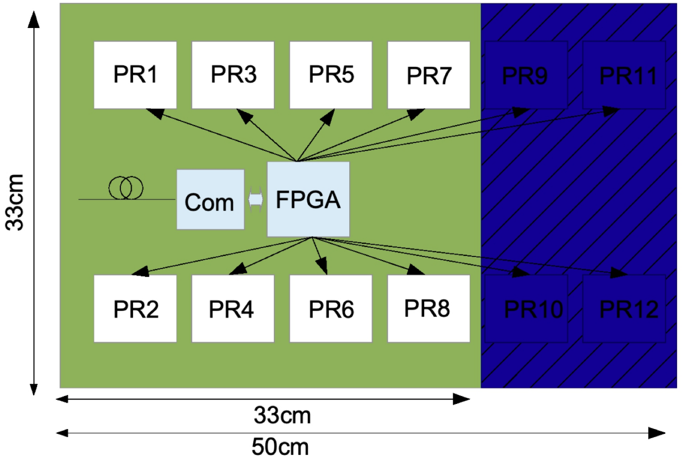
Crosstalk exists in the injection test : New version of FE Hardware



New version of FE Hardware

- Purpose : test Petiroc timing measurement performance
- Remove jump cables to reduce noise and crosstalk.
- Schematic and layout design has been finished, fabrication is starting soon.

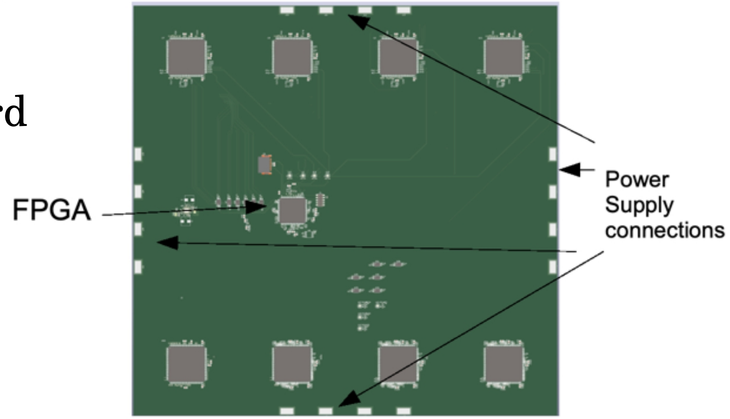
Toward Larger prototypes



Board with 8 (could be extended to 12) Petircoc2B ASICs

Pads 2cm x 2cm, 256 channels

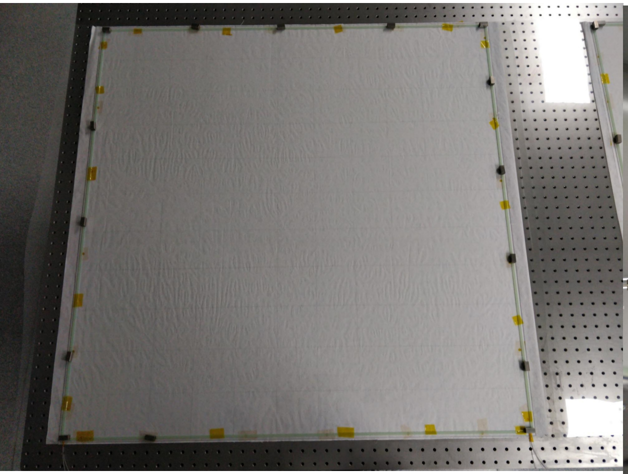
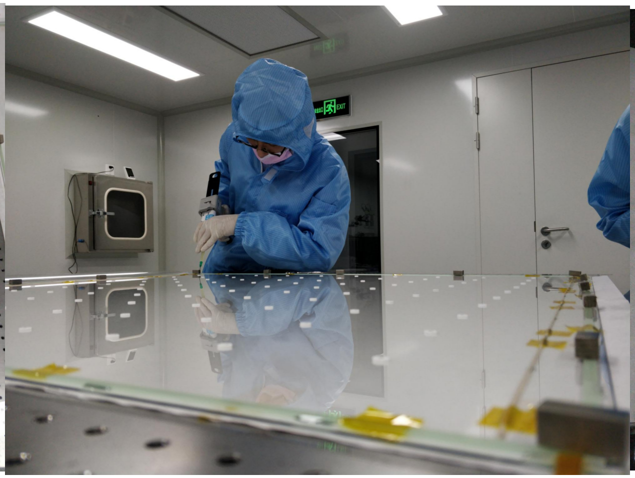
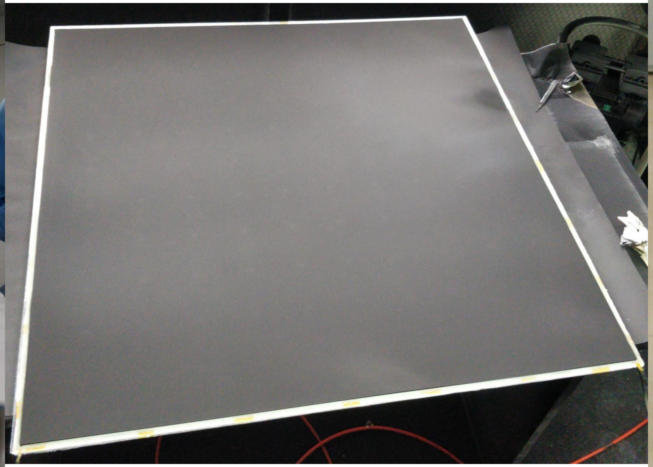
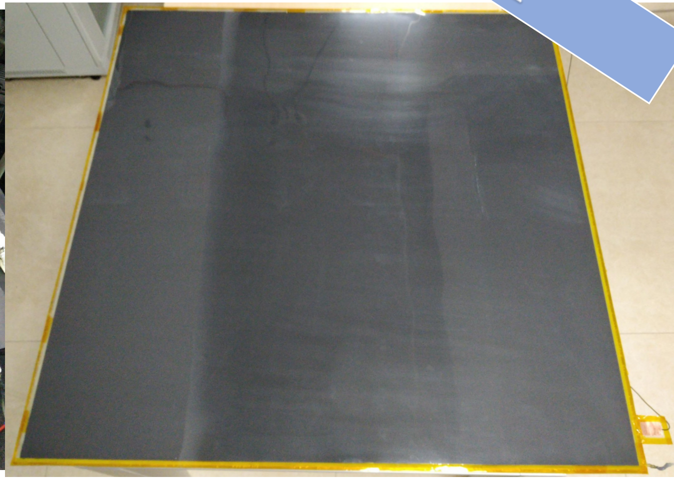
Local FPGA (Xilinx Spartan-6 TQFP) embedded on board

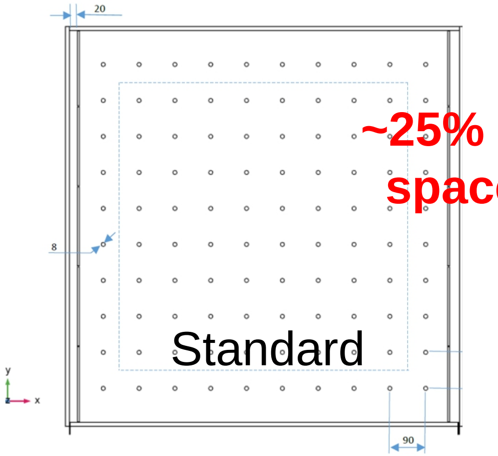


RPC and MRPC developments

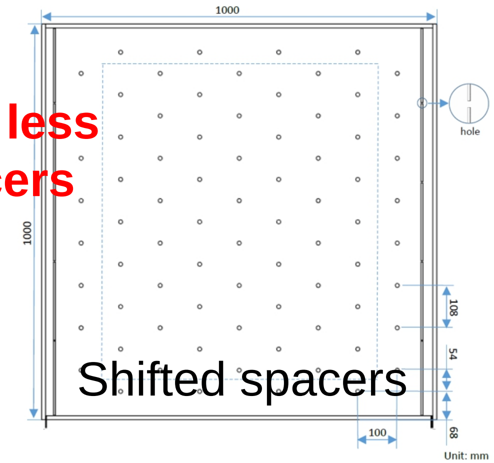
JINST 2108.12843

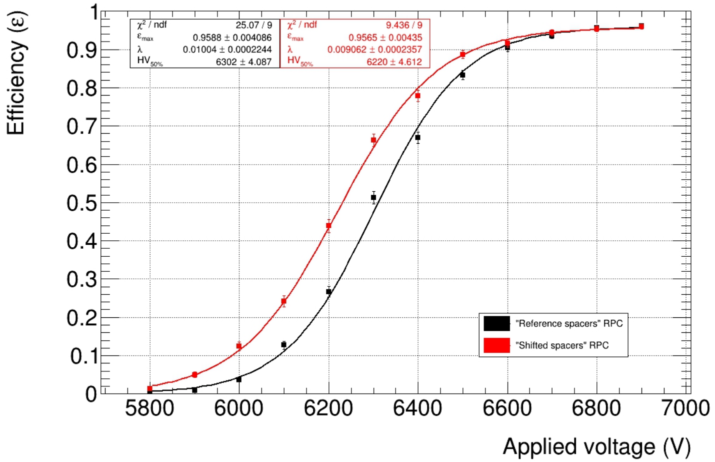
1m² RPC chamber has been built @ SJTU and a new spacer configuration has been studied



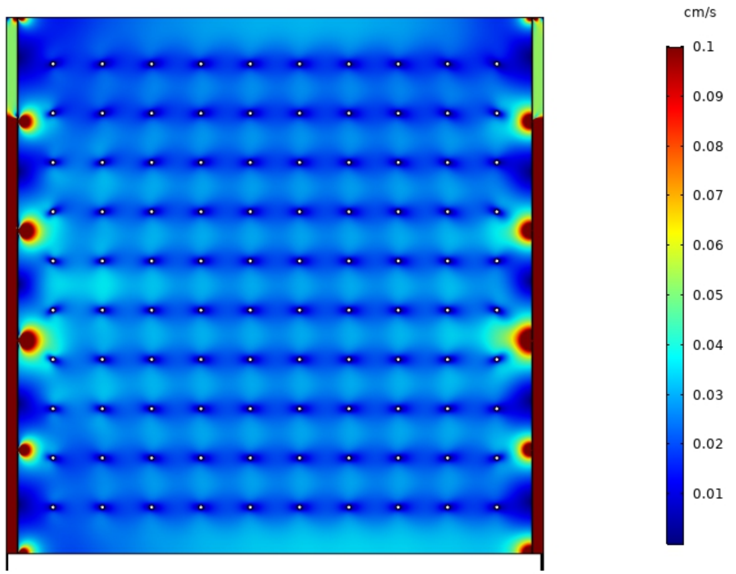
~25% less spacers

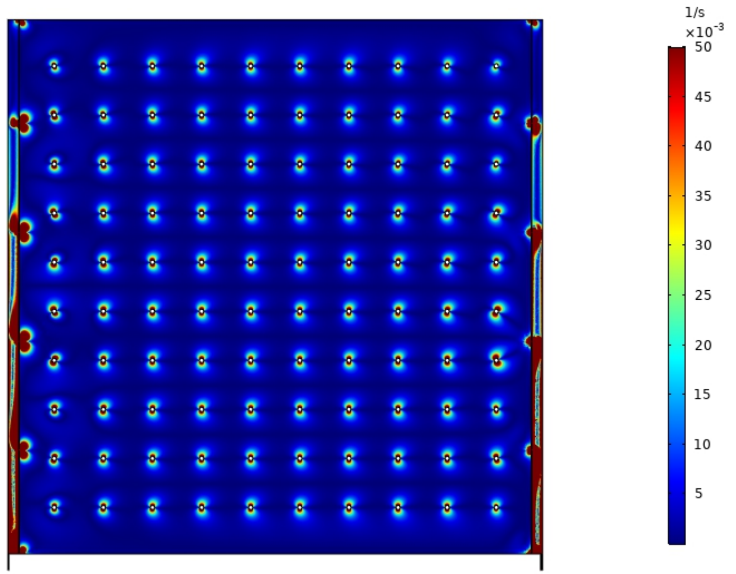


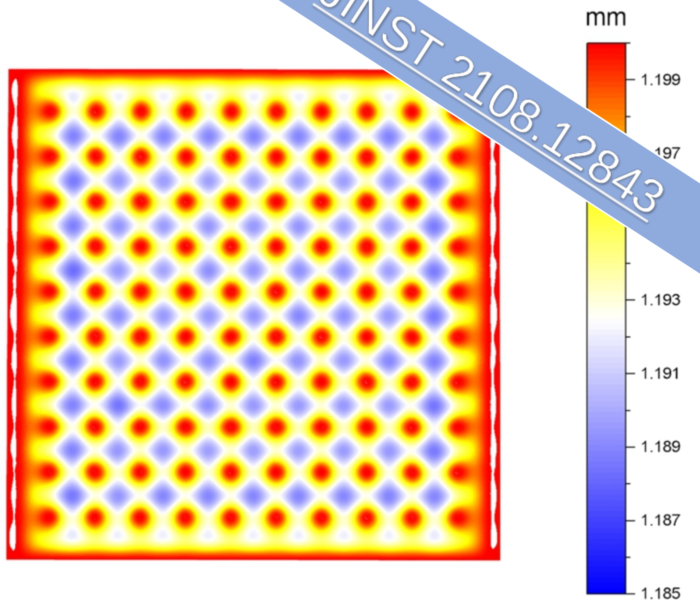


Comparable efficicency at the plateau

JINST 2108.12843



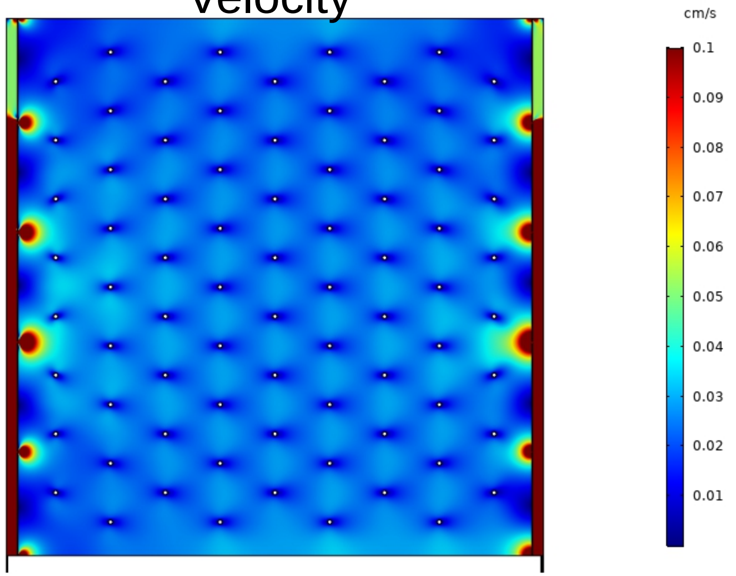


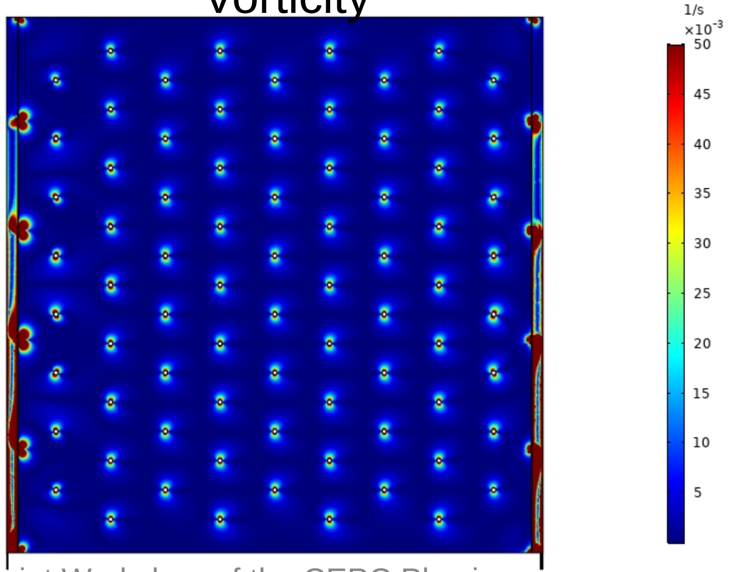


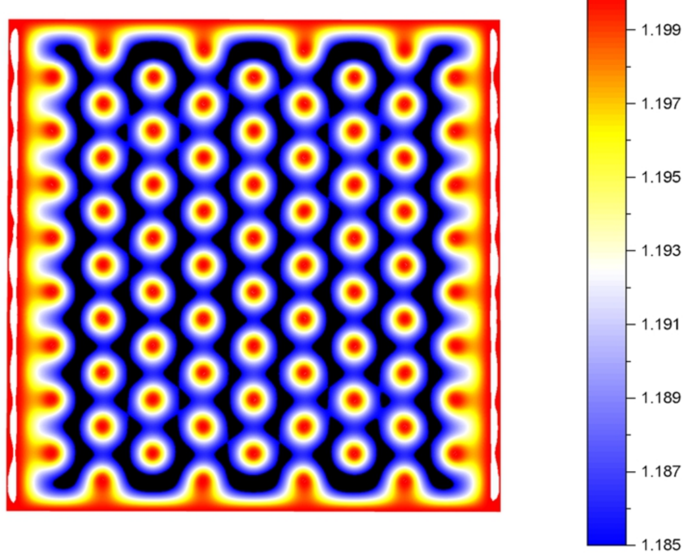
Velocity

Vorticity

Deformation







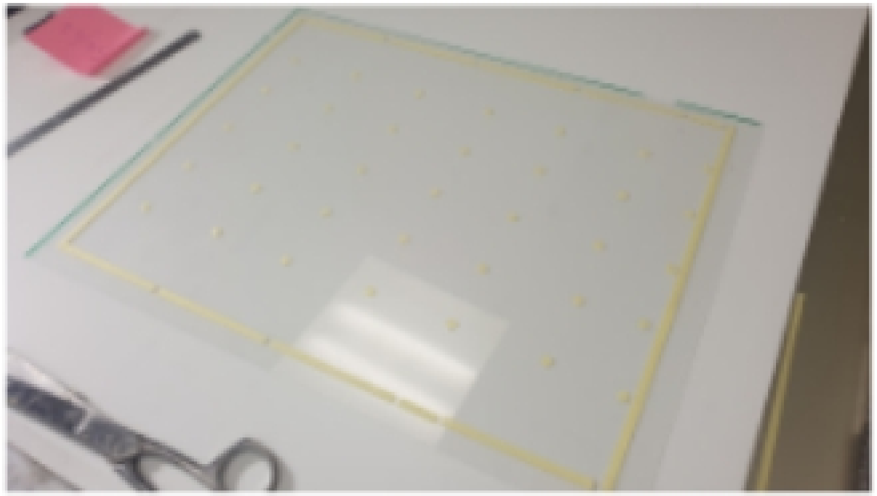
JINST 2108.12843

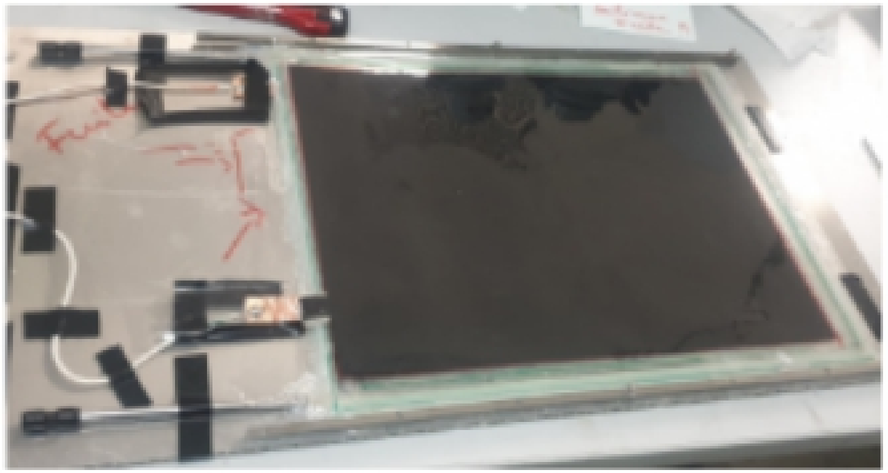
Model	"Reference spacers" RPC	"Shifted spacers" RPC
Mean velocity $\bar{v}$	0.238 ($\mathrm{mm\,s^{-1}}$)	0.241 ($\mathrm{mm\,s^{-1}}$)
RMS of velocity σ_v	0.049 ($\mathrm{mm\,s^{-1}}$)	0.042 ($\mathrm{mm\,s^{-1}}$)
$\sigma_v/\bar{v}$	20.3 (%)	17.5 (%)
Mean vorticity near spacers region	0.0199 ($\mathrm{s^{-1}}$)	0.0196 ($\mathrm{s^{-1}}$)
RMS of vorticity near spacers region	0.0129 ($\mathrm{s^{-1}}$)	0.0127 ($\mathrm{s^{-1}}$)
Mean vorticity excluding the vicinity of spacers	0.0022 ($\mathrm{s^{-1}}$)	0.0018 ($\mathrm{s^{-1}}$)
RMS of vorticity excluding the vicinity of spacers	0.0028 ($\mathrm{s^{-1}}$)	0.0026 ($\mathrm{s^{-1}}$)
Mean thickness between gas gap $\bar{d}$	1.193 (mm)	1.189 (mm)
RMS of deformation σ_d	0.003 (mm)	0.005 (mm)
$\sigma_d/\bar{d}$	0.25 (%)	0.42 (%)

Next step : Build MRPCs with Shifted spacer configuration

MRPC construction

- MRPCs are planed to be built @ SJTU, small size started @ Lyon
- Use spacer, study the new spacer configuration on MRPC



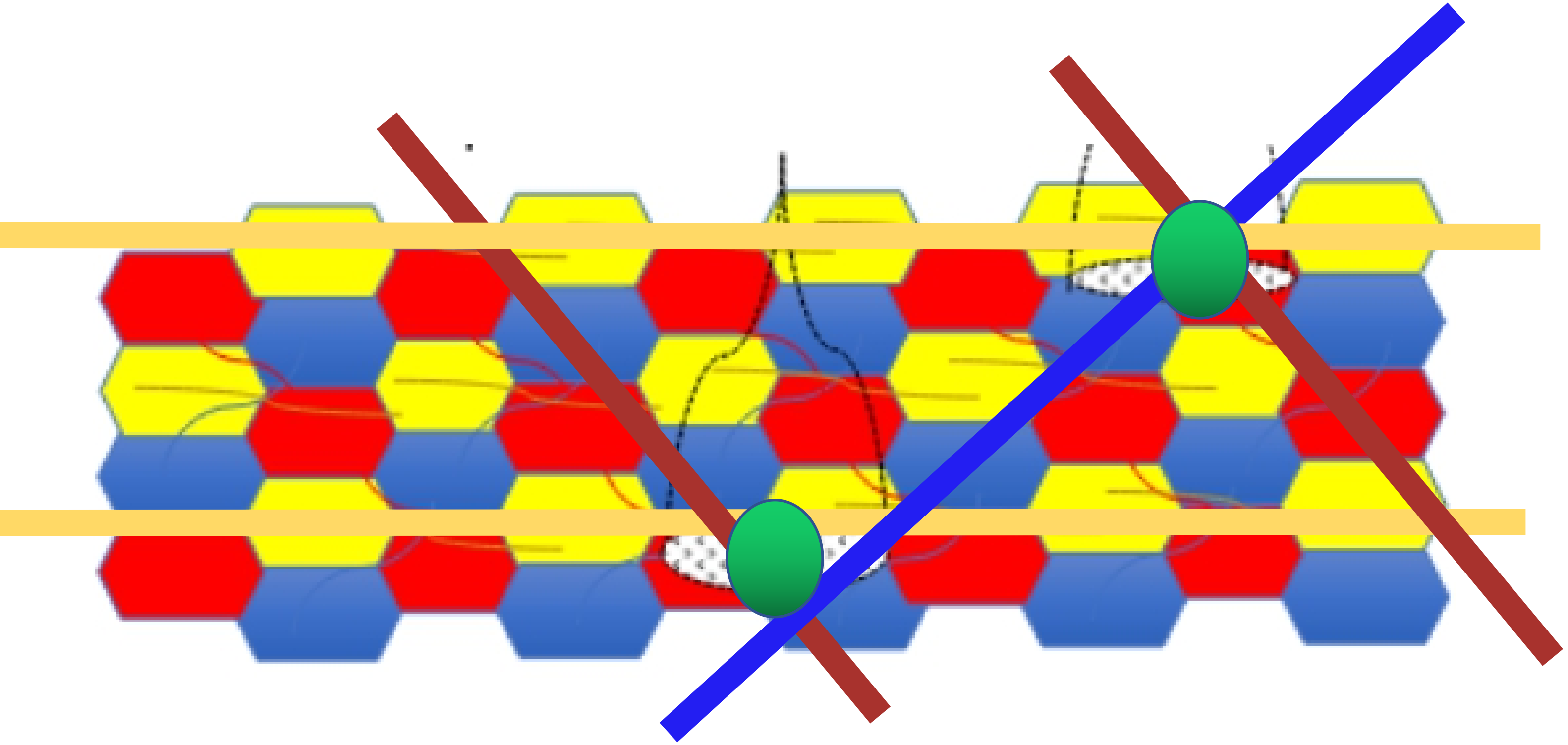


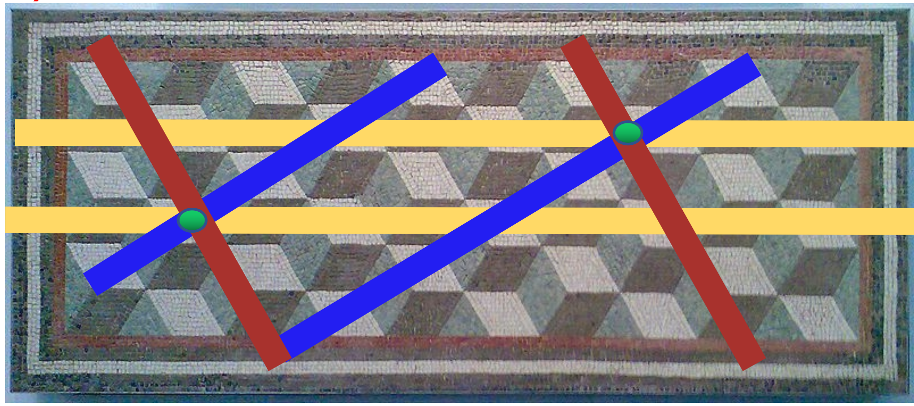
- 40cm×30cm
- Paint with a surface resistivity in the range 1-10MΩ/□

Woven strips

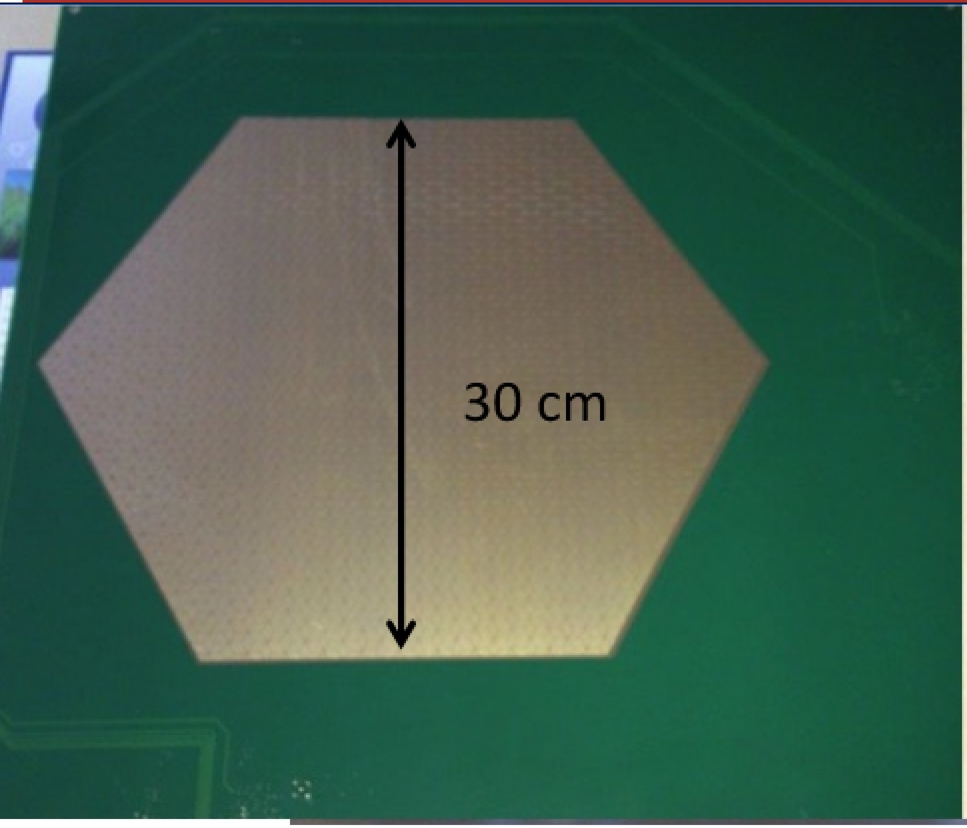
Patent: PCT/EP2018/053561

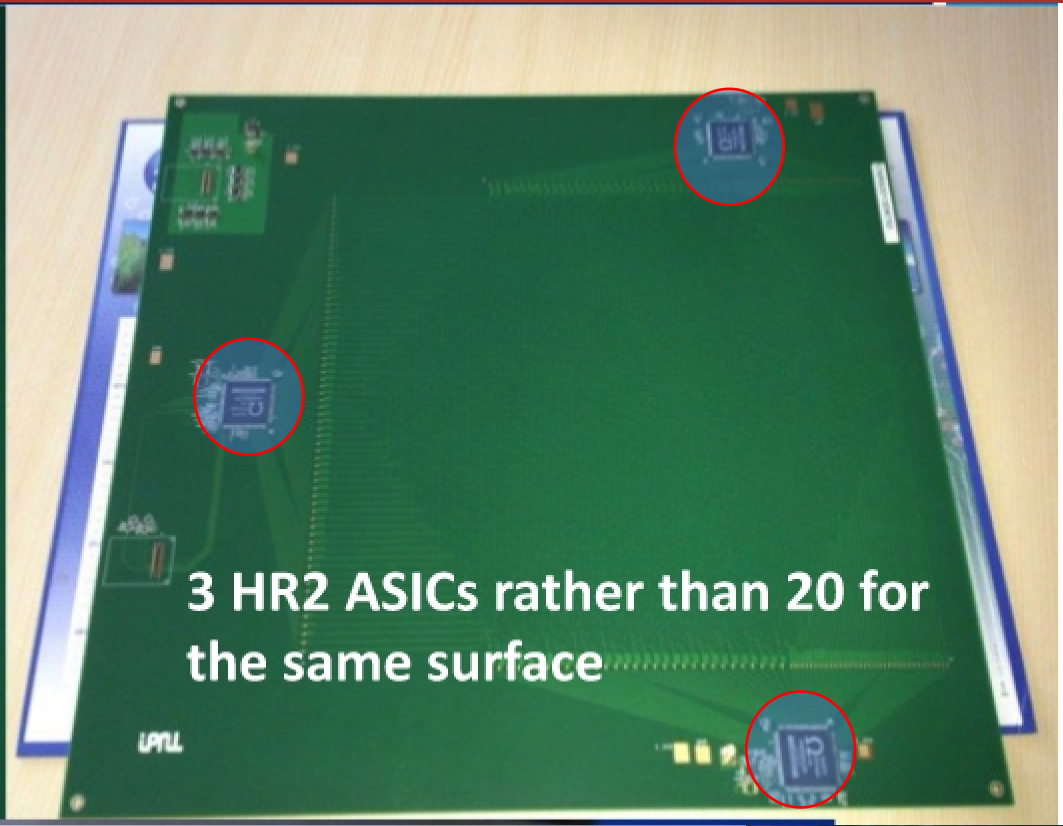
Pads : High granularity, cost, power, heat (cooling system, pulsed electronics)
Strips : ghost, less channels, less power consumption, ...

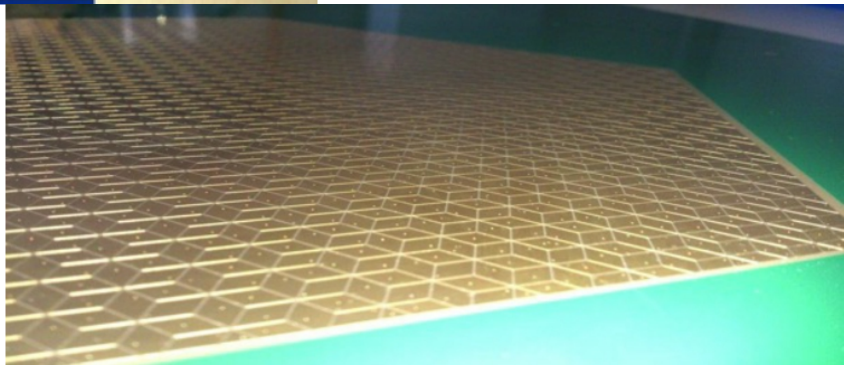




N*N to 3N : Reduction of electronic channels, power consumption and occupancy
Other tessellation possible !





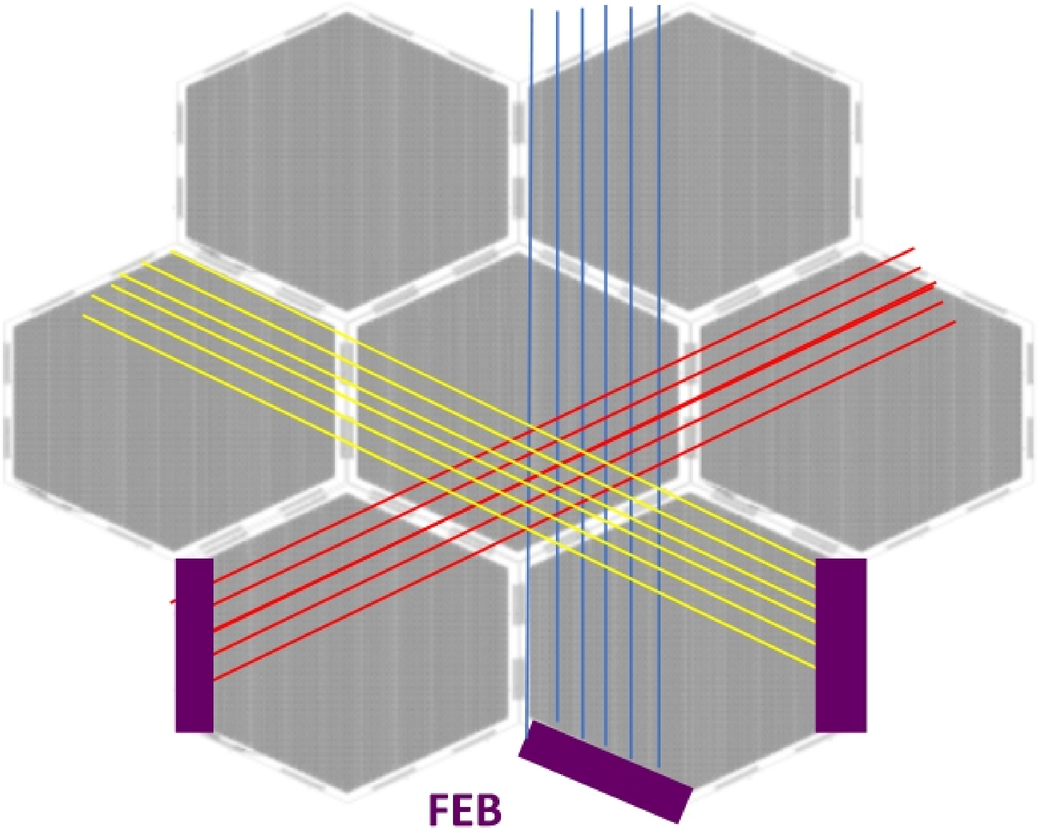


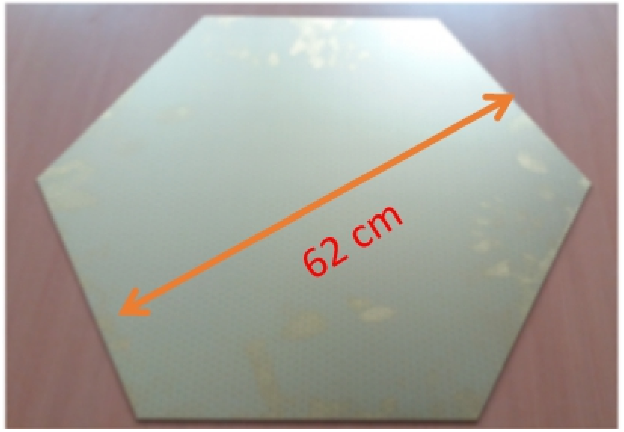
PCB with **lozenges-based** structure and 3 directions.

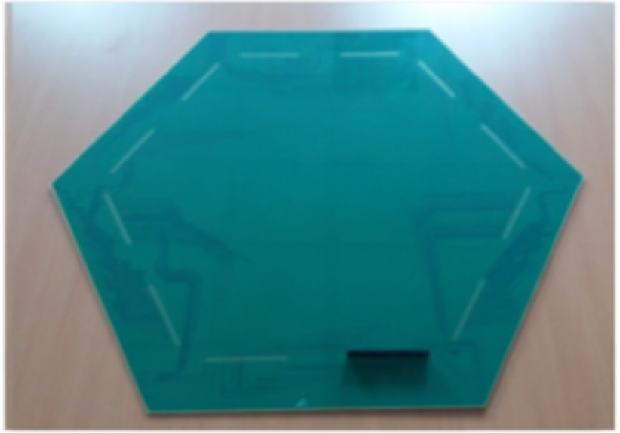
The readout electronics was set on the same PCB.
HARDROC2B ASICs (64-ch, 2-bit).

To large surface

To instrument very large gaseous detectors the readout electronics could not be part of the PCB. Separate strip panels from the readout electronics.



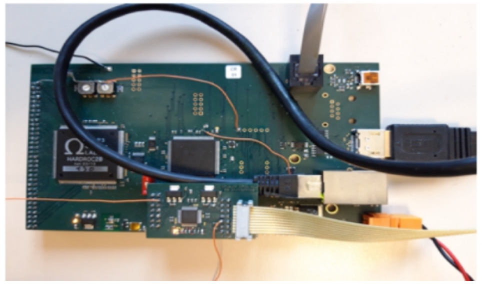




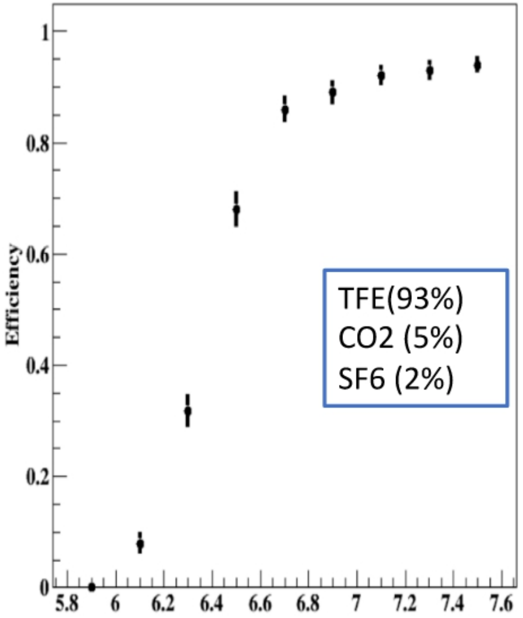
PCBs with only woven strips :

With connectors to transmit signal :

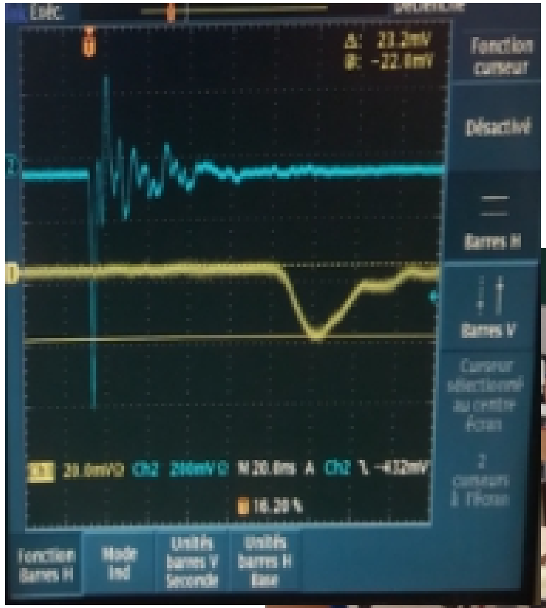
- Two adjacent PCBs
- The electronics board



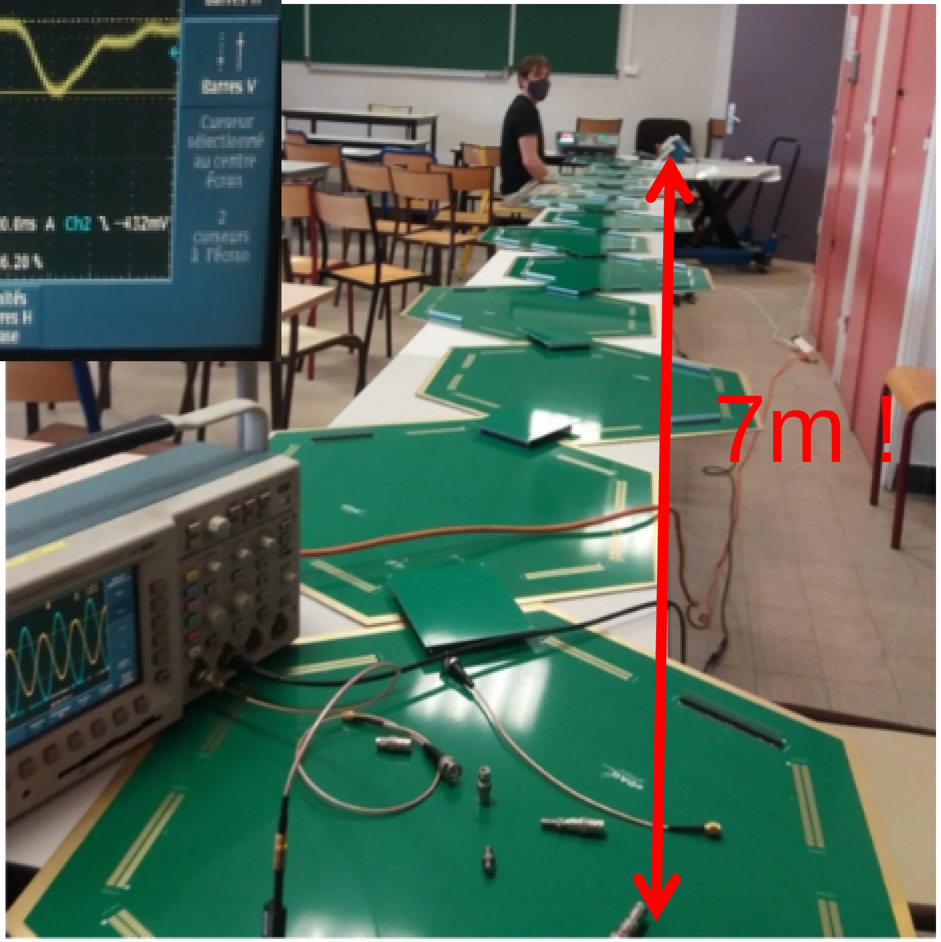
Plugged directly on the back of the PCB (64 channels)



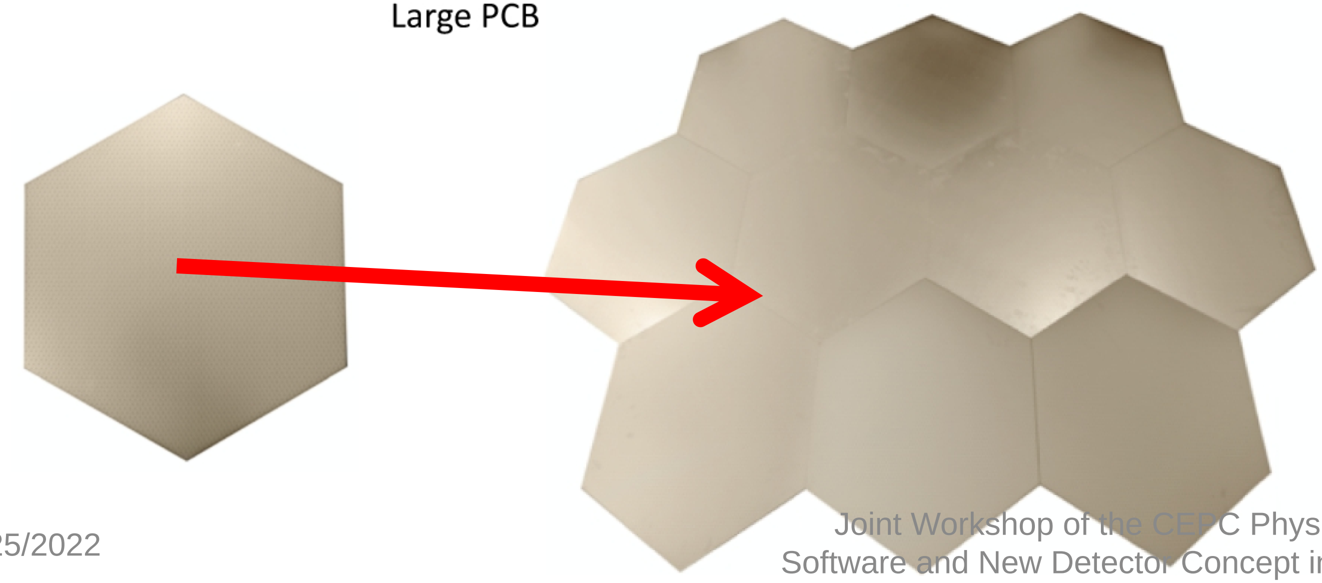
Setup with 8 detectors equipped with the new readout scheme



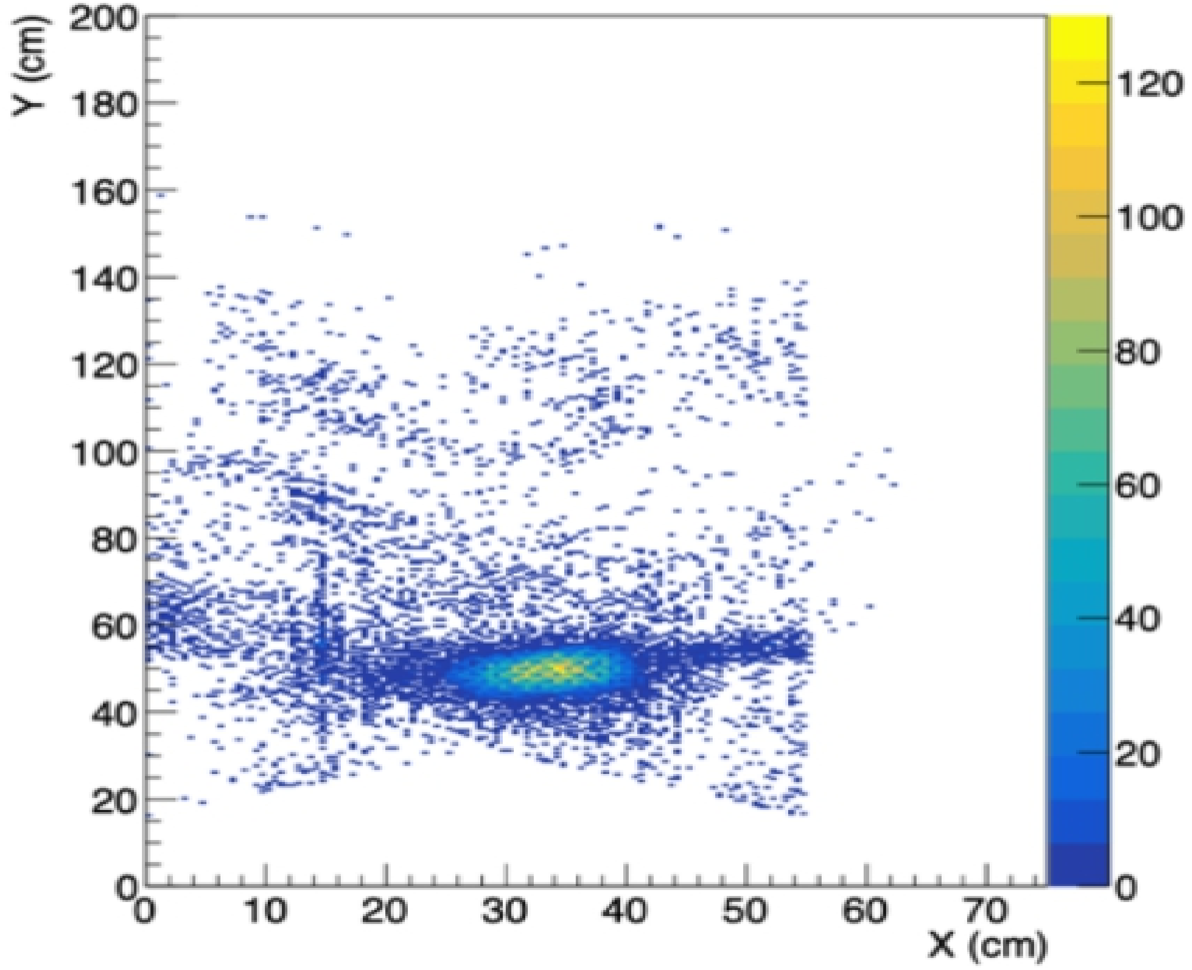
RPC-like signal shape injected on one end and detected on the opposite one is different but the charge loss is rather small.

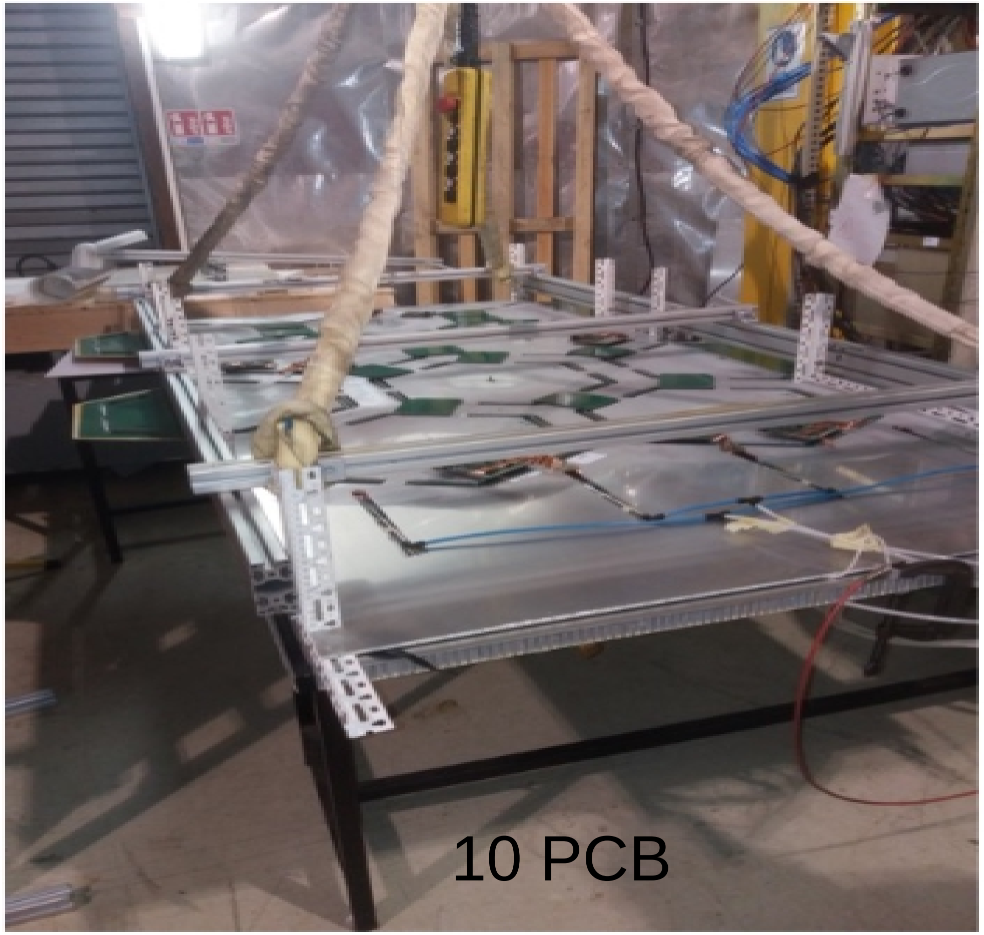


Large PCB



Tested on a large GRPC (2m x 1m) with several PCBs
Reconstruction efficiency (1 direction efficiency is not included) is around 90%



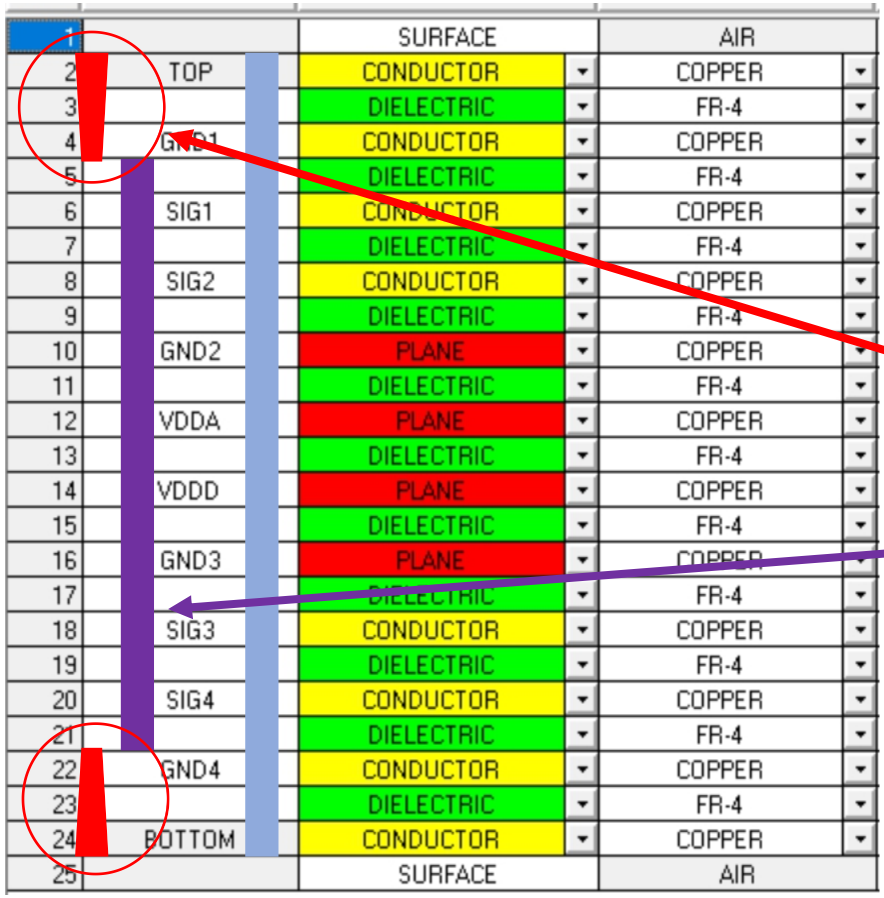


Summary

- SDHCAL has good linearity and energy resolution
- Real size prototype has been built
- New electronics are under study to use timing information.
- Woven strips electronics are studied
- Improvements on RPCs (gas flow,spacer configuration)

Backup

Design of Front-end Board

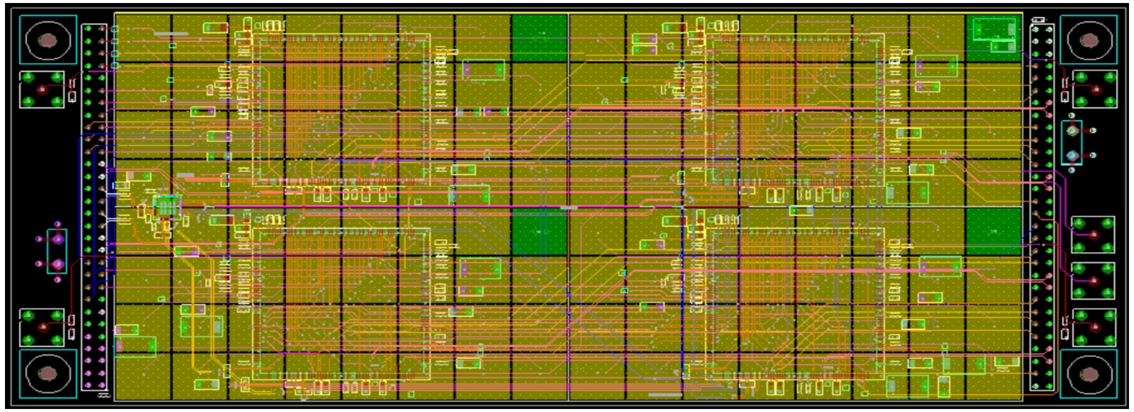


1		SURFACE	AIR
2	TOP	CONDUCTOR	COPPER
3		DIELECTRIC	FR-4
4	GND1	CONDUCTOR	COPPER
5		DIELECTRIC	FR-4
6	SIG1	CONDUCTOR	COPPER
7		DIELECTRIC	FR-4
8	SIG2	CONDUCTOR	COPPER
9		DIELECTRIC	FR-4
10	GND2	PLANE	COPPER
11		DIELECTRIC	FR-4
12	VDDA	PLANE	COPPER
13		DIELECTRIC	FR-4
14	VDDD	PLANE	COPPER
15		DIELECTRIC	FR-4
16	GND3	PLANE	COPPER
17		DIELECTRIC	FR-4
18	SIG3	CONDUCTOR	COPPER
19		DIELECTRIC	FR-4
20	SIG4	CONDUCTOR	COPPER
21		DIELECTRIC	FR-4
22	GND4	CONDUCTOR	COPPER
23		DIELECTRIC	FR-4
24	BOTTOM	CONDUCTOR	COPPER
25		SURFACE	AIR

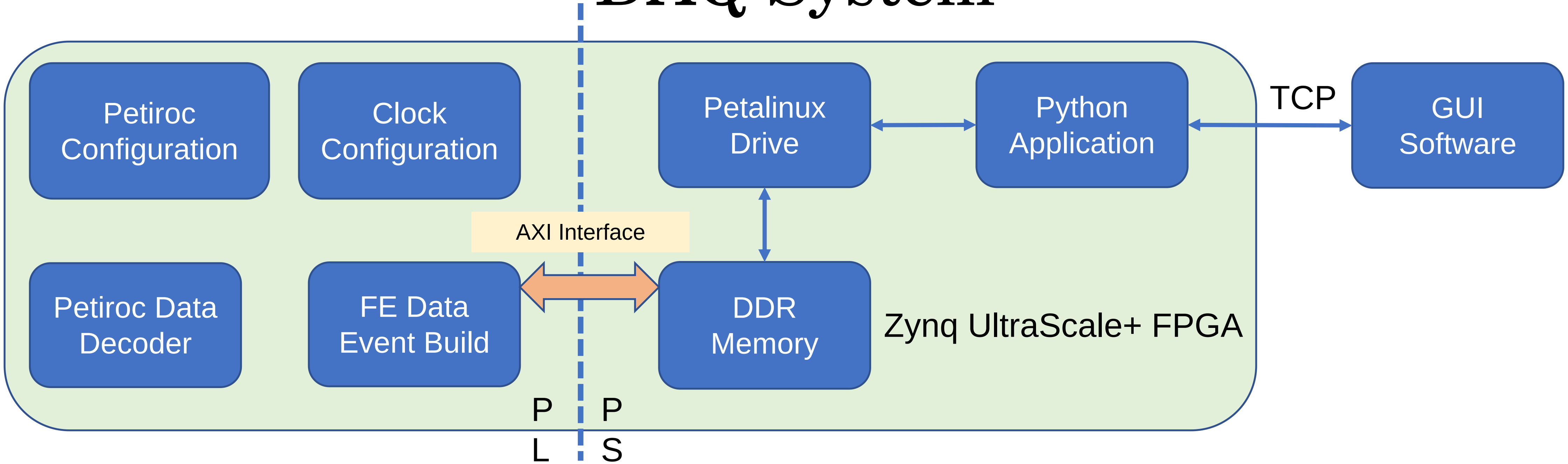
Stack-up and via design

- 12 layers PCB
- Many induction units are at the bottom

- Laser-drilled Via Technology (small size: ~0.1mm) between outside two layers
- Buried Vias with the size 0.3mm



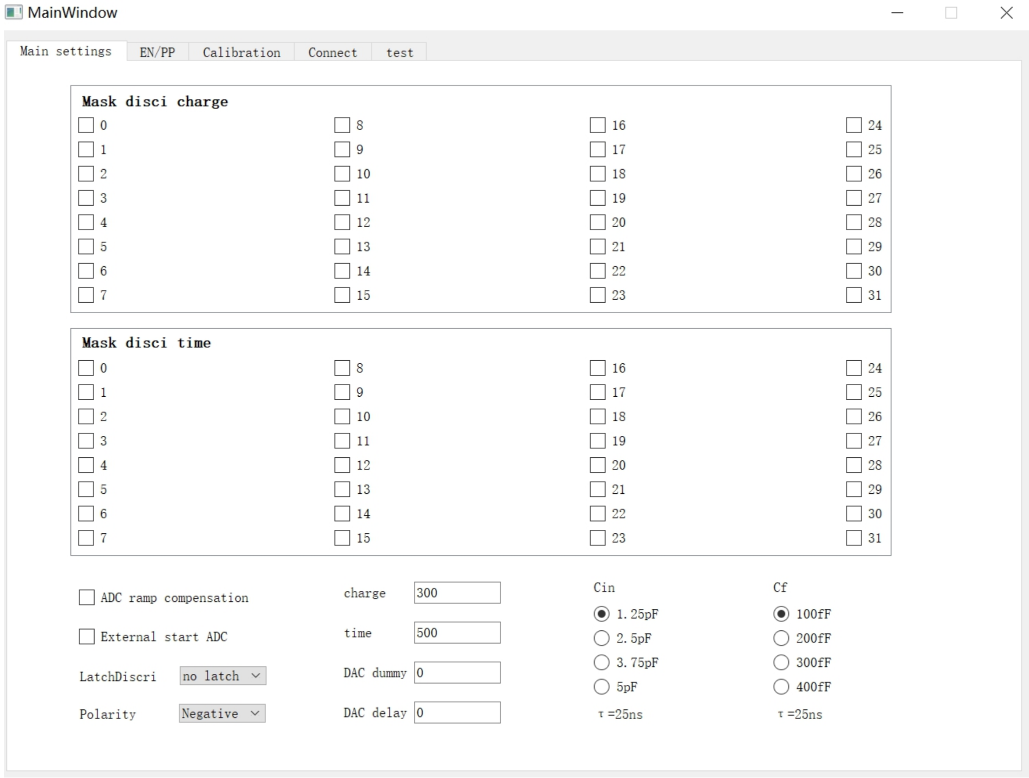
DAQ System



- Front-end interface: Petiroc configuration and data output decoder
- AXI interface between PL and PS, through DDR memory
- The PetaLinux tools allows to customize embedded Linux solutions on Xilinx processing systems.
- Python application access PS memory via linux driver, and communicates with PC via ethernet

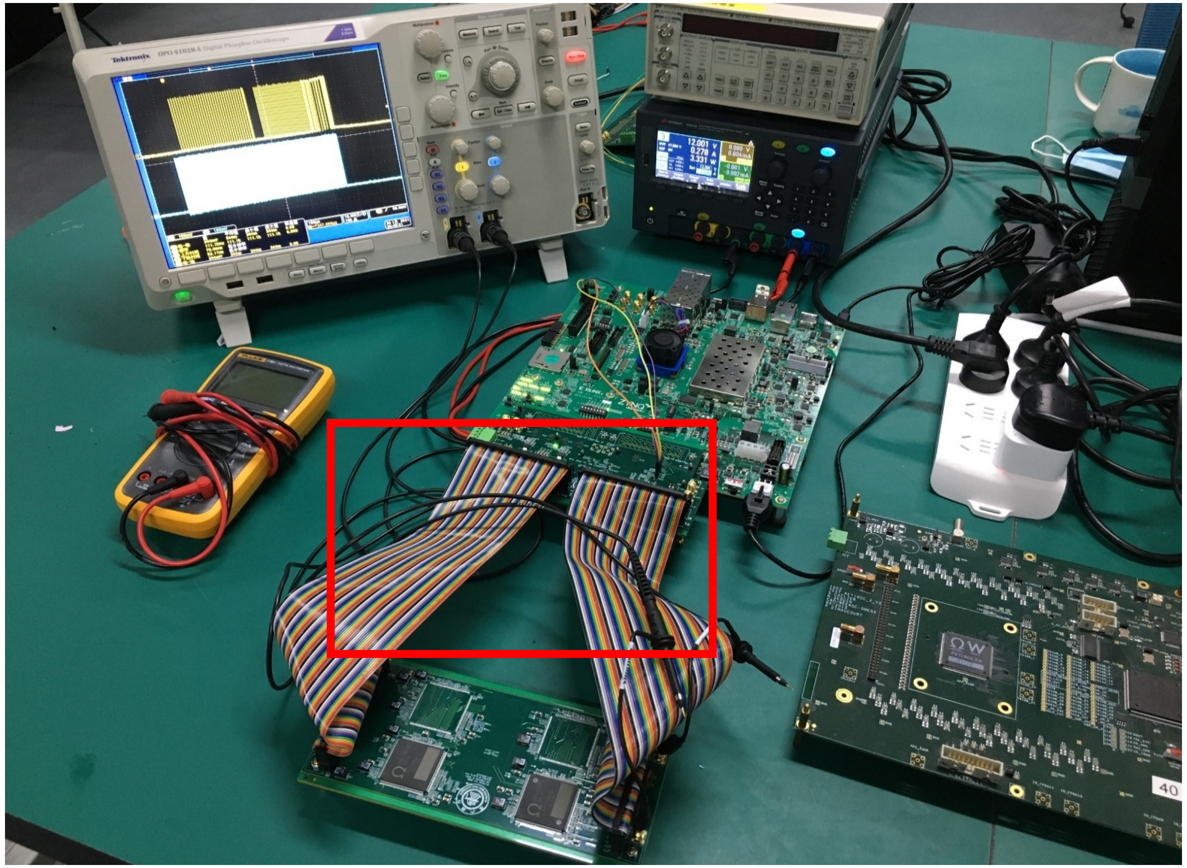
DAQ Software

- The DAQ software is a Python GUI application.
  - The GUI is designed via QT designer, which is set of cross-platform C++ libraries that implement high-level APIs.
  - PyQt5 modules binding with QT v5.



Status of System Test

```
===========================10 bit step============================
Ch0 : 64 Coarsetime: 1100011101, Decode: 100001011 ==> Counter: 267, Hit: 1
Ch1 : 65 Coarsetime: 1000010110, Decode: 111110010 ==> Counter: 498, Hit: 0
Ch2 : 66 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch3 : 67 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch4 : 68 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch5 : 69 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch6 : 70 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch7 : 71 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch8 : 72 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch9 : 73 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch10: 74 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch11: 75 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch12: 76 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch13: 77 Coarsetime: 1001011110, Decode: 111001010 ==> Counter: 458, Hit: 0
Ch14: 78 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch15: 79 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch16: 80 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch17: 81 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch18: 82 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch19: 83 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch20: 84 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch21: 85 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch22: 86 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch23: 87 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch24: 88 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch25: 89 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch26: 90 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch27: 91 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch28: 92 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch29: 93 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch30: 94 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch31: 95 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
```



- Crosstalk exists in the injection test

Summary

- Timing information helps to identify neutrons and separate close-by showers.
- MRPC detector is being built, which has an improved timing performance.
- A front-end prototype and a interface card has been designed and tested.
- The Xilinx ZCU102 board is used as the DAQ system.
  - The firmware and software of DAQ system has been developed.
- A new version of hardware has been designed, and will be fabricated soon.
- The larger prototype is being developed.

Introduction of PETIROC chip

- Time measurement with 10bits TDC interpolating 40MHz coarse time
- Charge measurement (Q>50fC) with 10bits DAC
- Voltage input amplifier, 200Ohm matching
- High bandwidth preamp (GBWP> 1.2 GHz)
- PETIROC parameters:
  - One chip with 32-channels and mixed analog/digital
  - The 32chs input connected with PAD (detector unit)
  - One channel split into two parts, respectively for charge and time measurement
  - Internal DAC for each channel to adjust the amplitude of the input signal
  - Lower power consumption (~6mW/channel)
  - Jitter ~18 ps RMS on trigger output (4 photoelectrons injected)