中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Status of pixel sensor prototypes for the CEPC vertex detector

Yunpeng Lu and Ying ZHANG
On behalf of the pixel sensor design teams
2022-5-23

Joint Workshop of the CEPC Physics, Software and New Detector Concept in 2022

Outline

- Overview of pixel sensors developed for CEPC VTX
- Progress of the JadePix chips
- Progress of the TaichuPix chips
- Progress of the SOI-3D chips
- Summary and outlook

CEPC Vertex detector requirements

Circular Electron Positron Collider (CEPC) proposed as a Higgs factory.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

  ➔ Impact parameter resolution,

$$\sigma_{r\emptyset} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$

Physics driven requirements		Running constraints	Sensor specifications	
$\sigma_{s.p.}$	2.8 μm		Small pixel	***~16 μm***
Material budget	0.15% X_0/layer		Thinning to	***50 μm***
		Air cooling	low power	***50 mW/cm²***
r of Inner most layer	16 mm	beam-related background	fast readout	***~1 μs***
		radiation damage	radiation tolerance	***≤3.4 Mrad/ year***
				≤6.2×10¹²n_{eq}/ (cm² year)

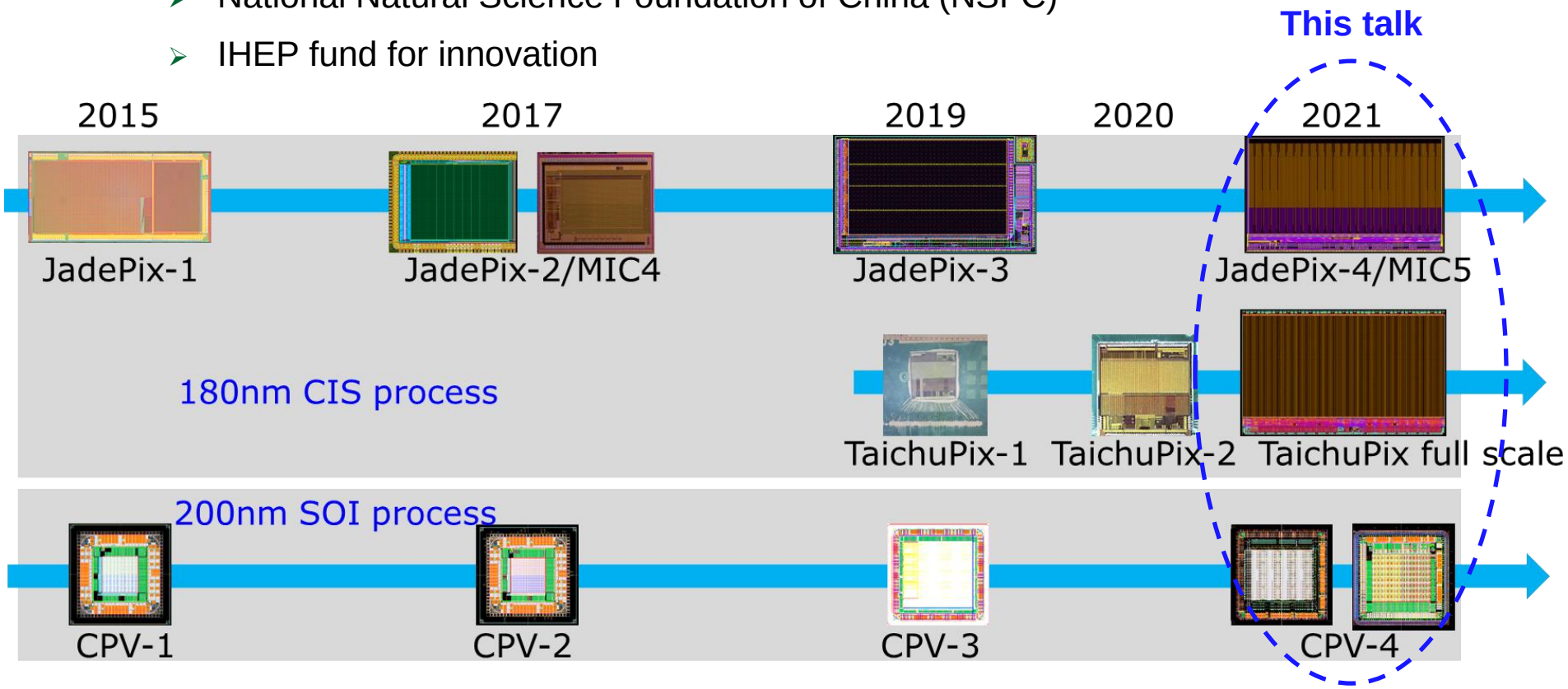
Baseline design parameters for CEPC vertex detector

	R (mm)	$\lvert z \rvert$ (mm)	$\lvert \cos\theta \rvert$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Overview of pixel sensors in China for CEPC VTX

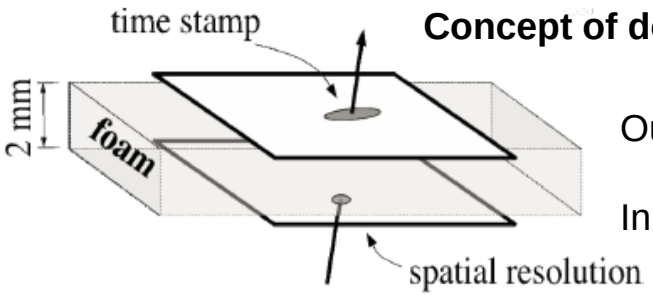
- **Development of pixel sensors for CEPC VTX supported by**
  - Ministry of Science and Technology of China (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation



Ref: “Status report on MAPS in China”, 2021 CEPC workshop, Yunpeng Lu

Update on JadePix chips

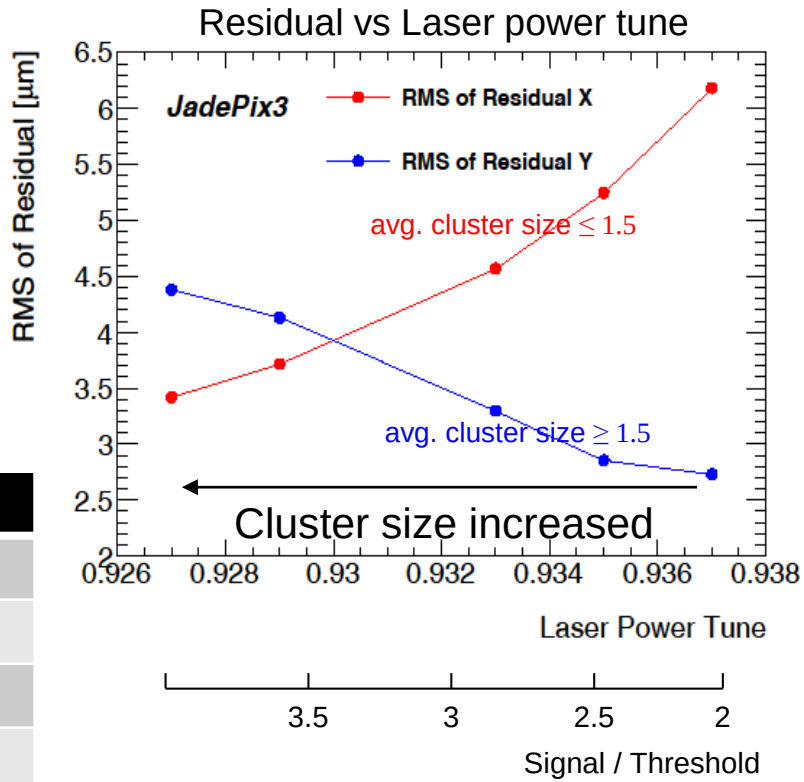
- **JadePix concerns the concept of double-sided layer**
  - Fine pitch & low power sensor for spatial resolution
    - Laser test on JadePix-3 indicates **s.p. < 3 μm achievable**
  - A faster sensor to provide time-stamp
    - **JadePix-4 in fabrication**



Concept of double-sided layer

Outside

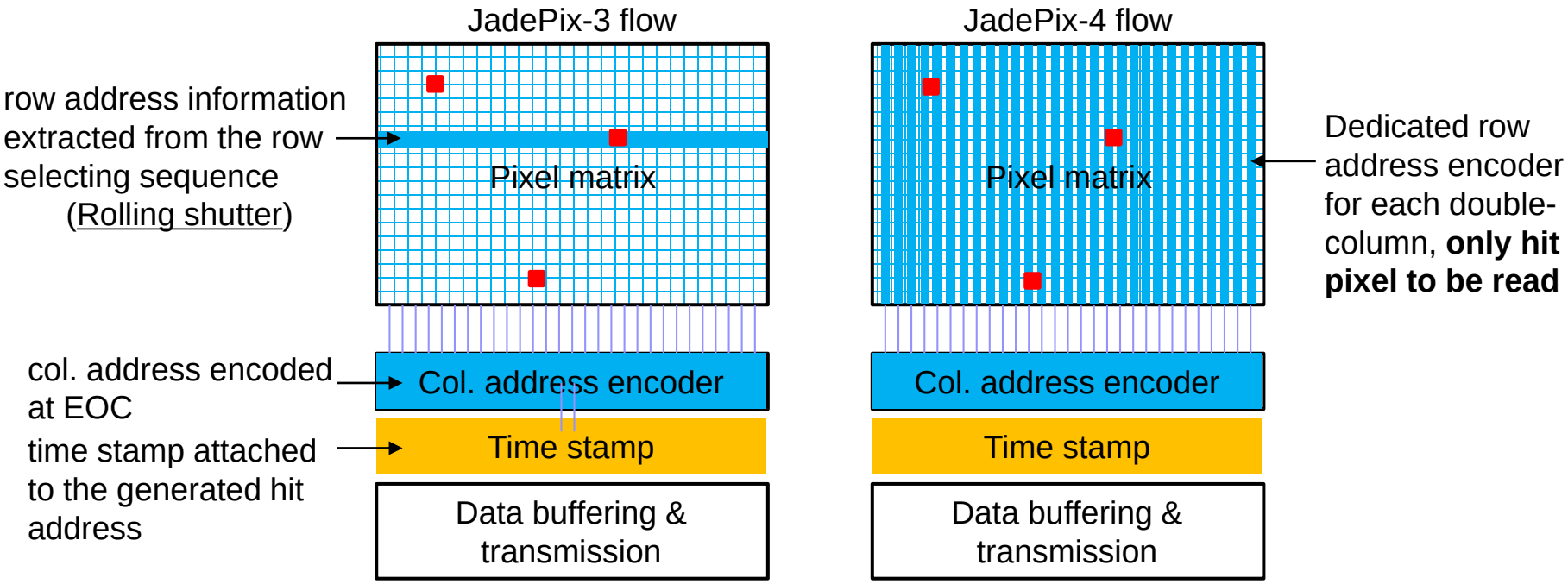
Inner side



	JadePix-3	JadePix-4/MIC5
Pixel size	16 μm × 23.1 μm	20 μm × 29 μm
Integration time	98.3 μs	**~ 1 μs**
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	356 row × 498 col.
Die size	10.4 mm × 6.1 mm	14.8 mm × 8.6 mm
Readout mode	Rolling shutter	Data-driven

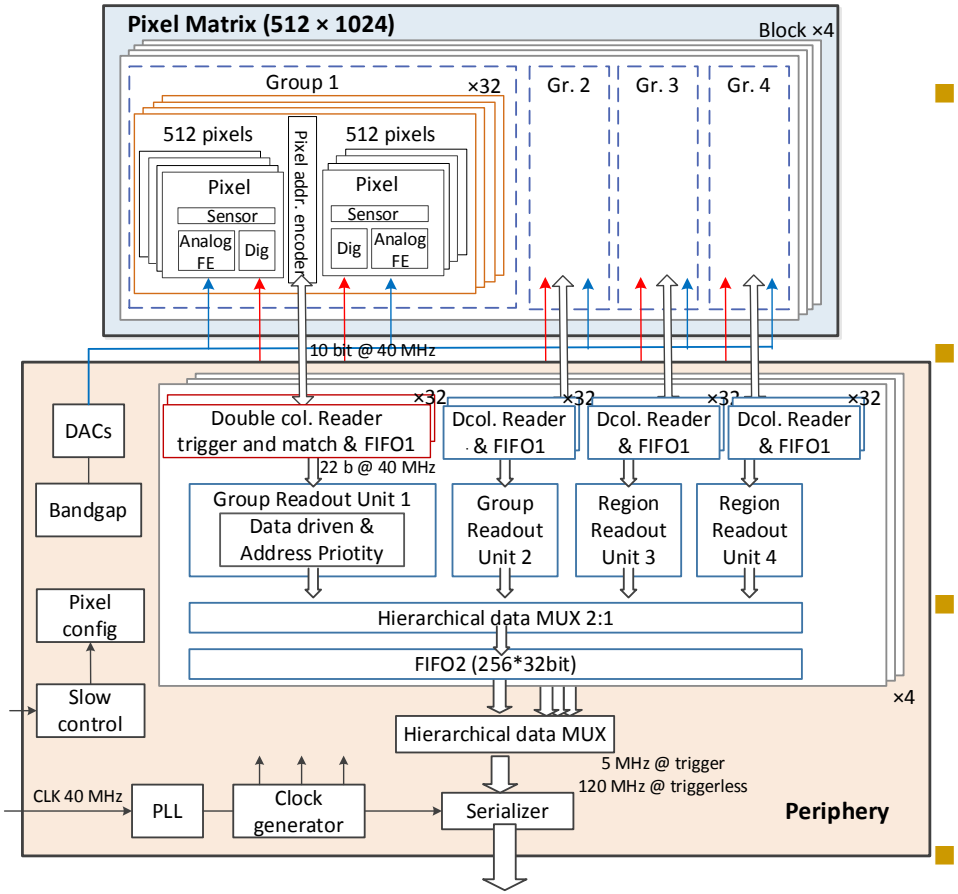
Hit processing flow of JadePix-3/4

- **Hit registered in each pixel needs fast processing**
  - Hit position (col. and row address) to be encoded
  - Time stamp to be attached
  - Register to be reset for the next hit
- **A major modification on the hit processing flow**
  - Row address encoding embedded into the active pixel matrix, which is much faster



TaichuPix architecture

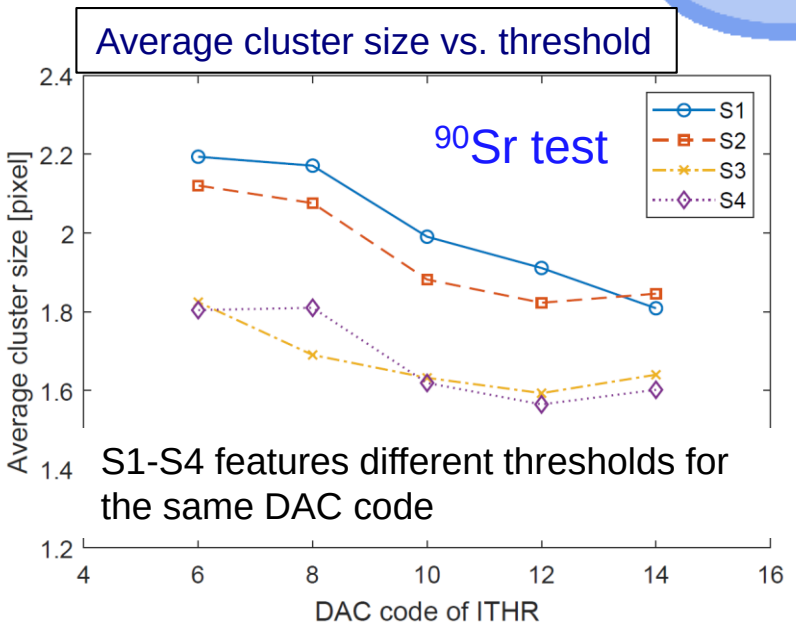
Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype



- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - **Time stamp added at EOC**
  - **Readout time**: **50 ns** for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 4.48 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

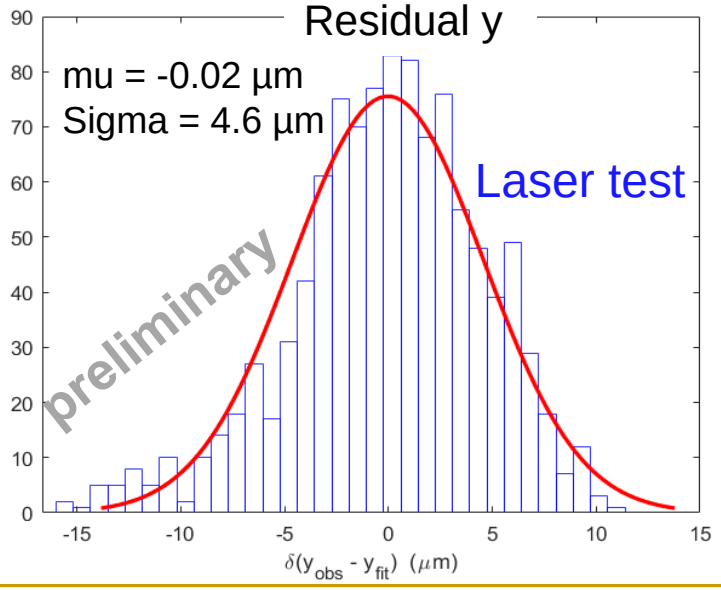
Update on TaichuPix chips

- **TaichuPix2 test with ^{90}Sr**
  - Average cluster size decreases with threshold as expected
  - **Cluster size < 3** indicates the estimated maximum hit rate (36 MHz/cm^2) reasonable
  - **Cluster size > 1** could benefit the spatial resolution (better than $\boldsymbol{pitch}/\sqrt{\mathbf{12}}$ = 7.2 μm)



S1-S4 features different thresholds for the same DAC code

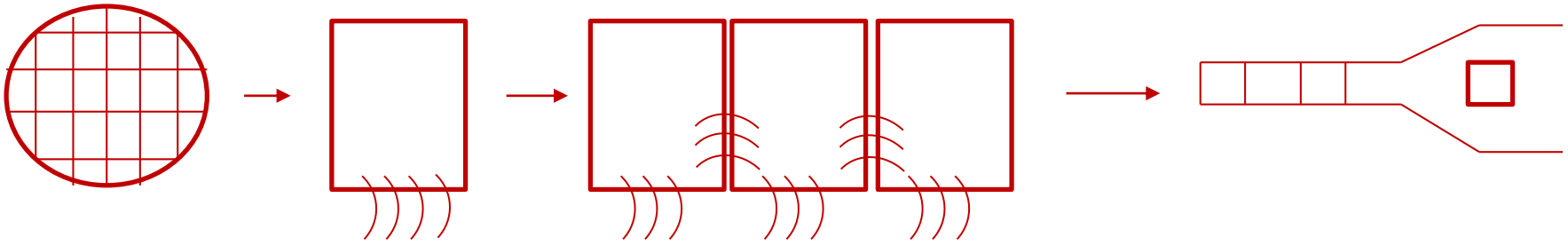
- **Laser test**
  - Laser diode with 658 nm wavelength
  - One dimension laser scan on the test chip with fixed step of 1 μm
  - Preliminary result indicates a resolution **less than 5 μm**
  - Further investigation ongoing
    - Laser 1064 nm
    - With different laser power and/or diff. pixel threshold



Update on TaichuPix chips

- **First full-scale protype in fabrication, to be received in June**
  - Die size 25.7 mm × 15.9 mm
  - Pixel cell inherited from MPW + scaled logic with new layout Periphery + debugged/improved blocks + enhanced power network
  - 12 wafers ordered, expected to be assembled on the ladder prototype

- **Preparation for chip & ladder test in progress**
  - Probe card customized for the wafer test
  - Single chip test board designed and fabricated
  - Ladder readout electronics and DAQ designed



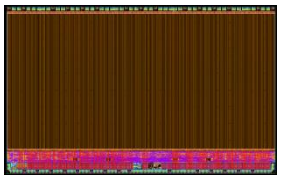
Ladder readout design

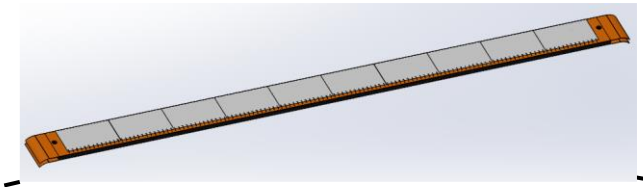
- **Detector ladder required for detector assembly**
  - Sensor chips, readout electronics, mechanical support, etc.

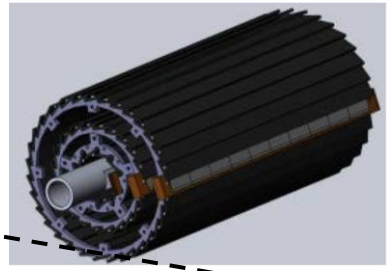
CMOS imaging sensor prototype

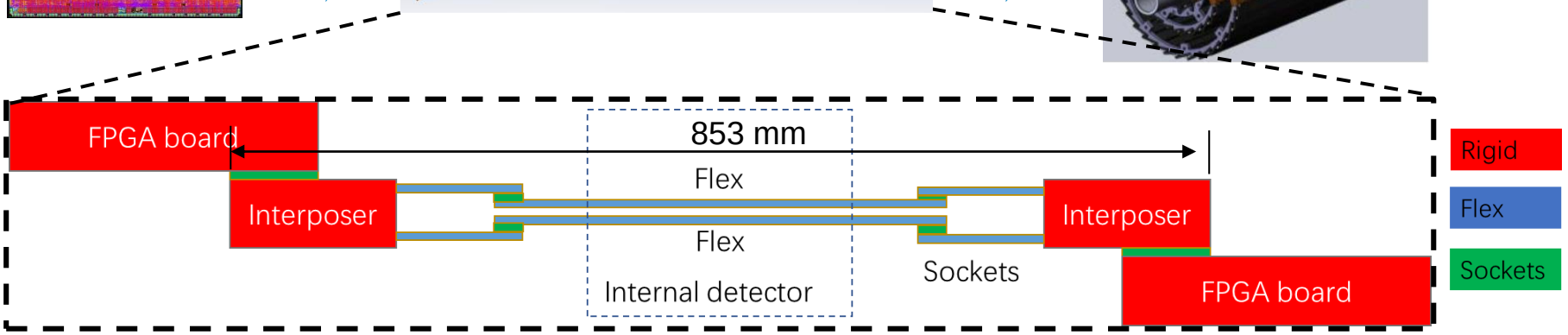
Detector module (ladder) prototype

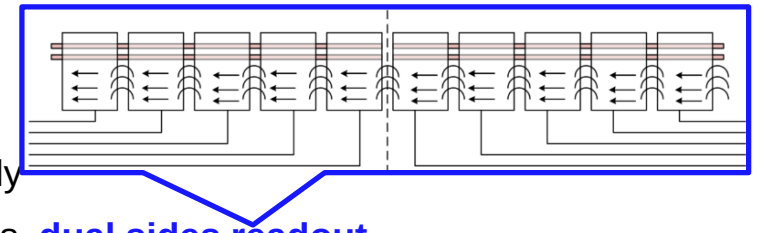
Full size vertex detector Prototype







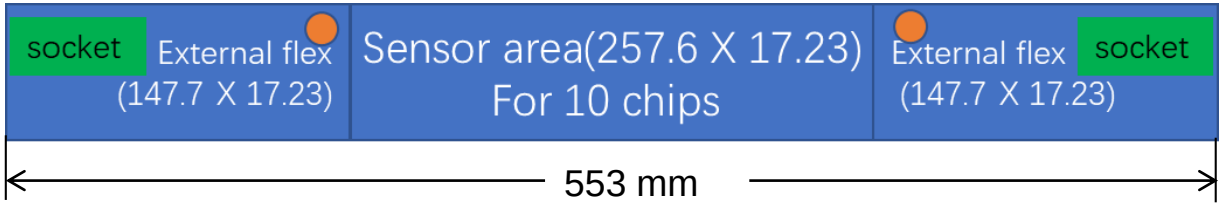




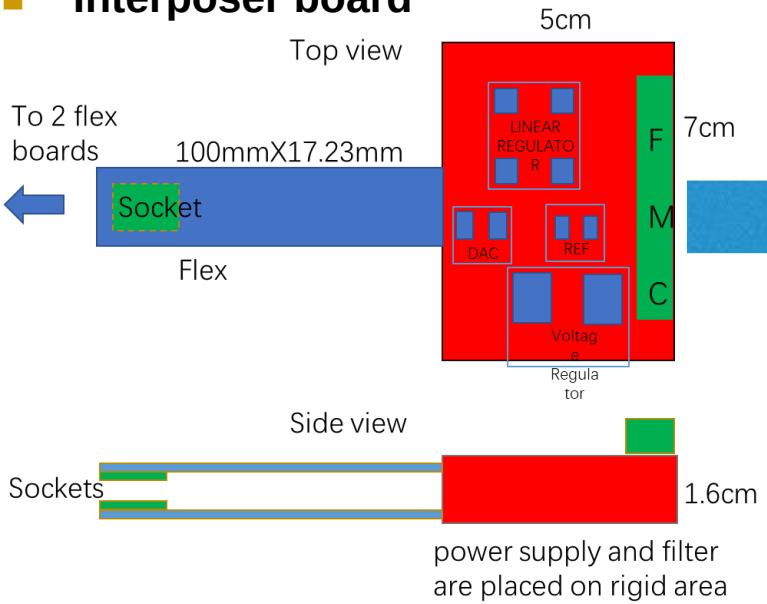
- **Ladder readout structure**
  - Containing 3 boards for easier production & assembly
    - Flex board：Assembled with 10 TaichuPix chips, **dual sides readout**
    - Interposer board：FMC mezzanine rigid and flex board, in production
    - FPGA board：FMC carrier board, available in the lab

Ladder readout design

- **Two versions of flex board designed**
  - Version 1 (baseline): 2 layers, **less material**, limited layout space leads to **worse signal integrity**, thickness ~0.2 mm, in production
  - Version 2: 4 layers, **more material** dedicated GND and power plane gain **better signal integrity,** thickness ~0.4 mm, production done



- **Interposer board**

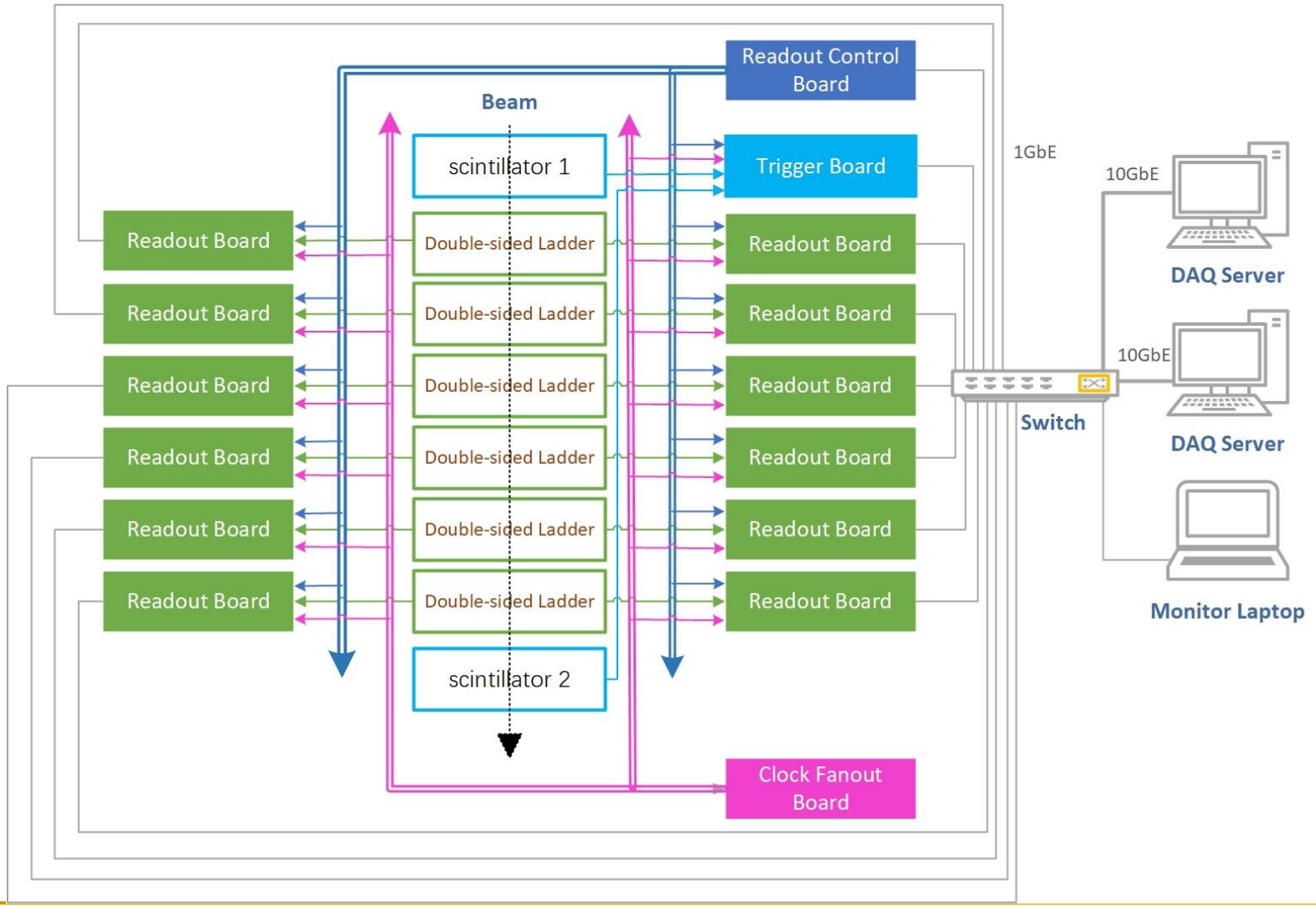


- **FPGA board**

  - Communication with chips
  - Data processing and package data
  - Readout to PC via 1Gbps Ethernet
  - Capability of 6 Gbps readout and 2GB internal DDR memory

Design of DAQ

- **Considering 6 double-sided ladders**

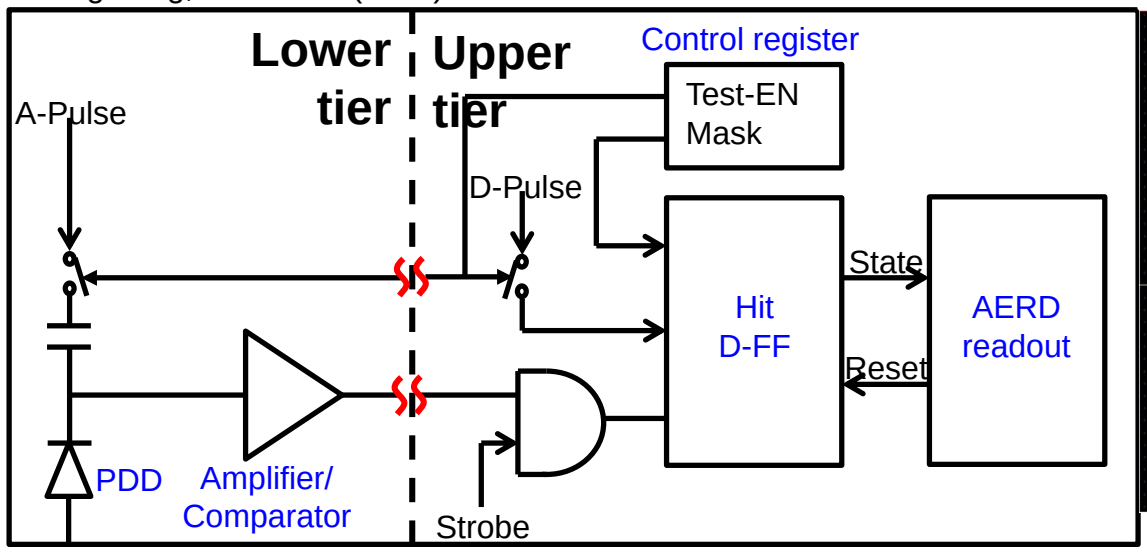


Status of SOI prototypes

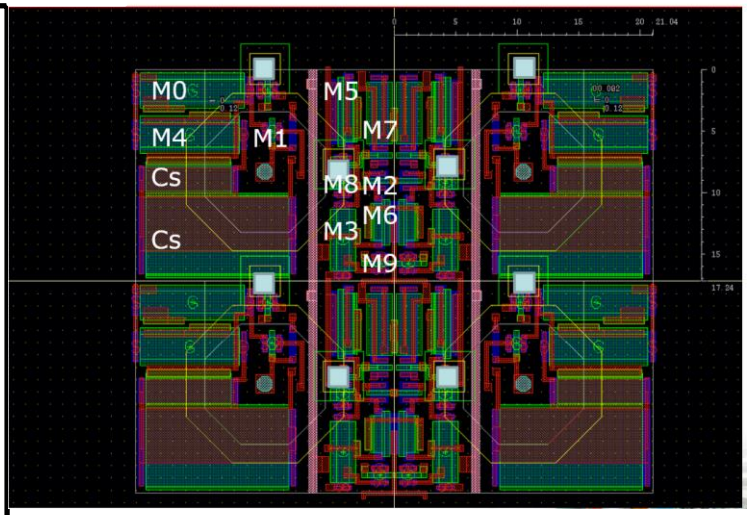
Exploring the 3D technology on CPV4 design

- **2 tiers to accommodate the full-functioned pixel: 17.24 × 21.04 μm² on each**
  - Lower tier: PDD (Pinned Depleted Diode) sensing diode + amplifier/comparator
  - Upper tier: Hit D-Flipflop + Control register + AERD readout*
- **2 vertical connections in each pixel: comparator output and test switch**
  - Power / ground connection implemented in the I/O pad ring
- **Critical to make the PDD and analog front-end compatible**
  - $V_{thr.}$ shift by -70 mV/PMOS, 50 mV/NMOS as the PDD depleted (-4 V)

*Ping Yang, NIMA 785 (2015) 61-69



3D bumps marked with

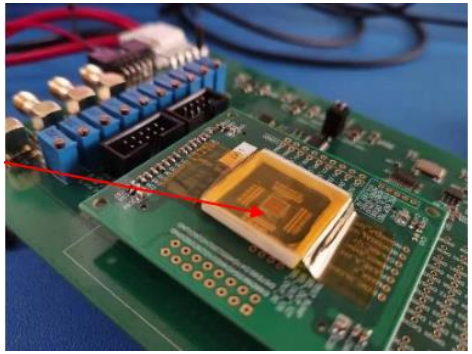


4 pixels arranged in 2 columns

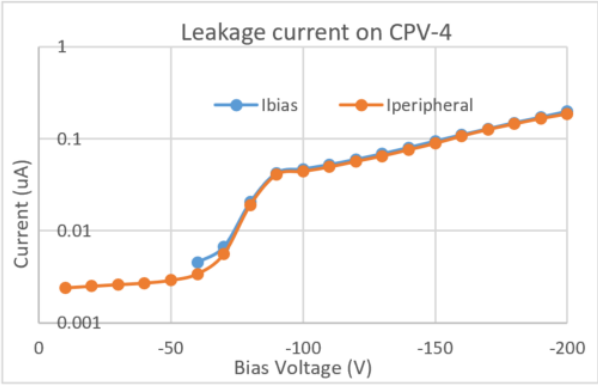
Status of SOI prototypes

Functional verification of CPV-4 before 3D integration

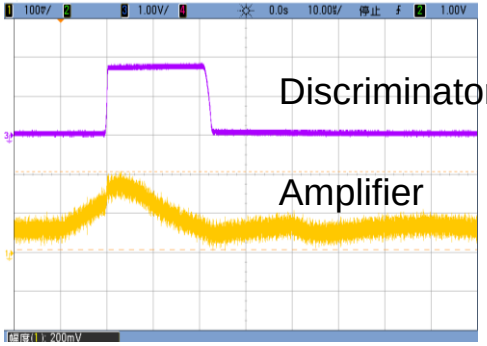
- **Quick test on the Lower and upper tier separately**
  - Checkpoint before the 3D integration
- **Leakage current reduced successfully by**
  - Optimization of PDD implant dose
  - 1 Bias Ring + 4 Guard Ring + 1 Current Collecting Ring
- **Analog front-end operated with the PDD sensor**
  - Analog waveform inspected on oscilloscope
- **Digital logic functions validated**



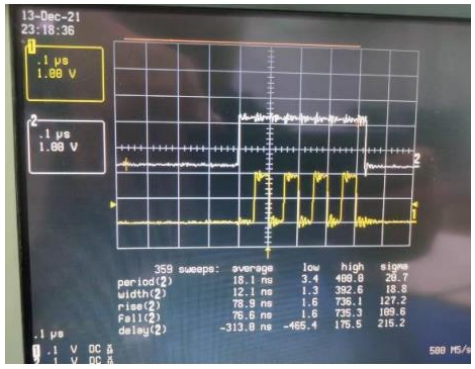
CPV4 digital sensor bonded on test board



The analog sensor can be biased at -200 V



Analog frontend with PDD
Test charge injected ~ 750 e^-

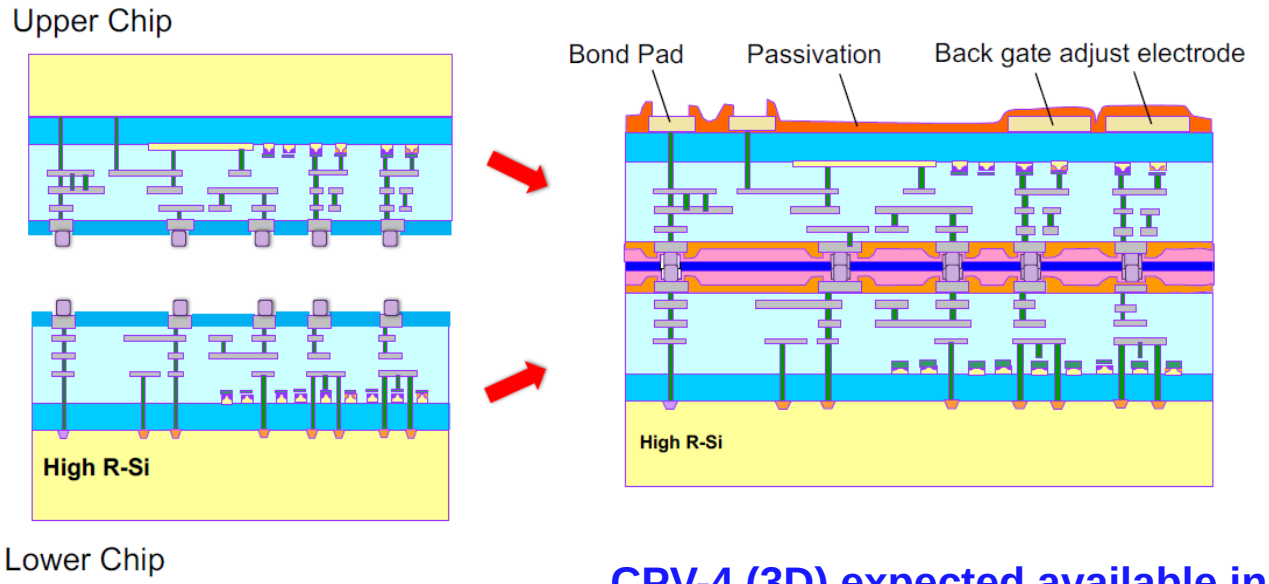


Pulse injection test of digital sensor
white line: valid signal, representing hit occurs
Yellow line: reset signal after read the pixel

SOI-3D integration ongoing

- **3D integration by foundry in Japan in progress**
  - The bulk of upper tier removed by wet-etching
    - 260 μm → 10 μm thick
  - Lower tier can be thinned as a conventional sensor
    - 75 μm in SOI case and 50 μm in CMOS case (lower tier not necessarily an SOI sensor)

  * Currently SOI-3D demonstrated on a lower tier of 260 μm thick



CPV-4 (3D) expected available in August

- **Test and DAQ system being developed**

Summary and outlook

- **Progress made on the JadePix and TaichuPix development**
  - JadePix-4 featuring a fast readout designed as a complementary to the JadePix-3, in fabrication
  - The first full-scale TaichuPix prototype designed based on the TaichuPix-2 results, in fabrication
  - The Ladder assembled with TaichuPix chips being designed
    - Readout electronics, DAQ, mechanics, etc.
  - 6 double-sided ladder expected available in November
  - Beam test @ DESY planned in December

- **Exploration of SOI-3D has started with the first design of CPV4-3D**
  - Targeting on the full specs of pixel sensors
  - To examine the scheme, implementation and yield of SOI-3D
  - Quick test on the Lower and upper tier separately
    - Functionality verification done, promising result obtained
  - 3D-integration prototype expected available in August
  - 2 ~3 MPW run planned in 5 years

- **Exploration of next generation of CMOS pixel sensor technology ongoing**
  - A 55 nm CMOS technology provided by Chinese foundry is being evaluated

Pixel sensor teams

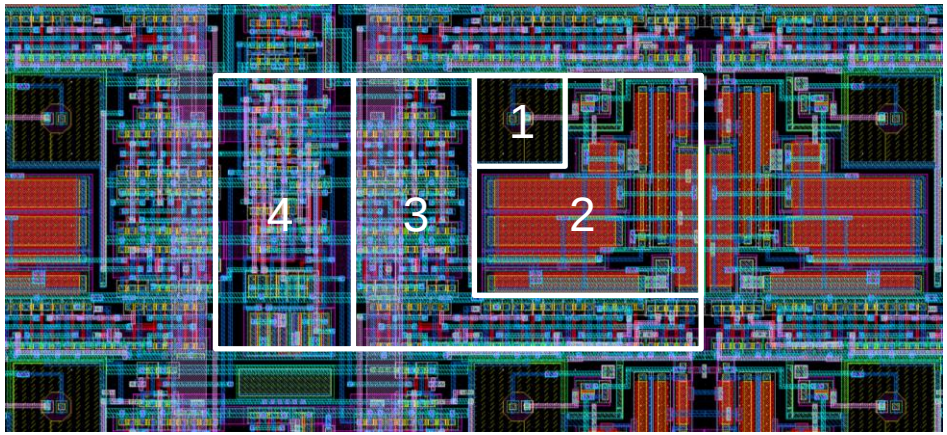
- **JadePix-3/4**
  - IHEP: Ying Zhang, Yang Zhou, Zhigang Wu (graduated), Jing, Dong, Wenhao Dong/ USTC, Chunhao Tian/ USTC, Yunpeng Lu, Qun Ouyang
  - CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng (graduated), Anyang Xu (graduated), Sheng Dong, Hulin Wang, Xiangming Sun
  - SDU: Liang Zhang
  - Dalian Minzu Unv: Zhan Shi
- **TaichuPix**
  - IHEP: Wei Wei, Ying Zhang, Xiaoting Li, Jun Hu, Hongyu Zhang, Zhijun Liang, Joao Guimaraes da Costa
  - CCNU/ IFAE: Tianya Wu, Raimon Casanova, Sebastian Grinstein
  - NWPU: Xiaomin Wei, Jia Wang
  - SDU: Liang Zhang, Jianing Dong, Long Li
- **SOI**
  - IHEP: Yupeng Lu, Yang Zhou, Jia Zhou, Jing Dong, Mingyi Dong, Hongyu Zhang, Qun Ouyang

Thank you very much for your attention!

Backup slides

Design of JadePix-4/MIC5

- **Key component verified and reused from JadePix-3**
  - Diode
  - Analog frontend
  - Hit register
- **Asynchronized Encoder and Reset Decoder (AERD) ***
  - Generating col. and row address from hit pixel
  - Tracing back to reset hit pixel
- **Final layout of pixel matrix**
  - pixel array: 356 row × 498 col.
  - Pixel size: 20 μm × 29 μm

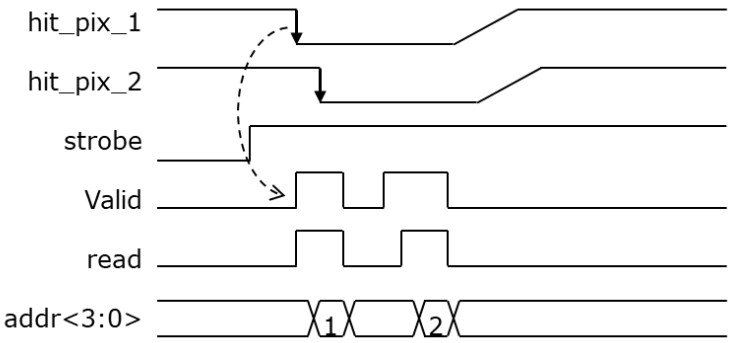


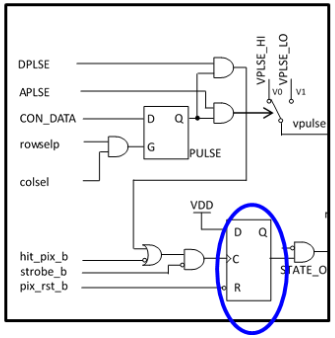
JadePix-4 pixel layout
(MET4 and above not shown)
1. Diode
2. Analog frontend
3. Digital logic
4. AERD shared by 2 col.

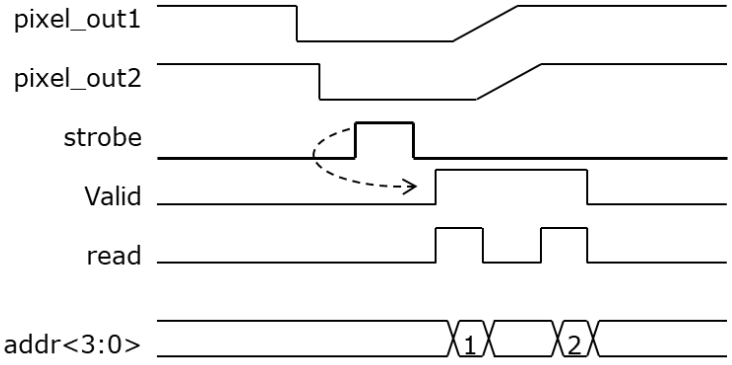
*P. Yang, etc., NIMA 785 (2015) 61-69

Readout of JadePix-4/MIC5

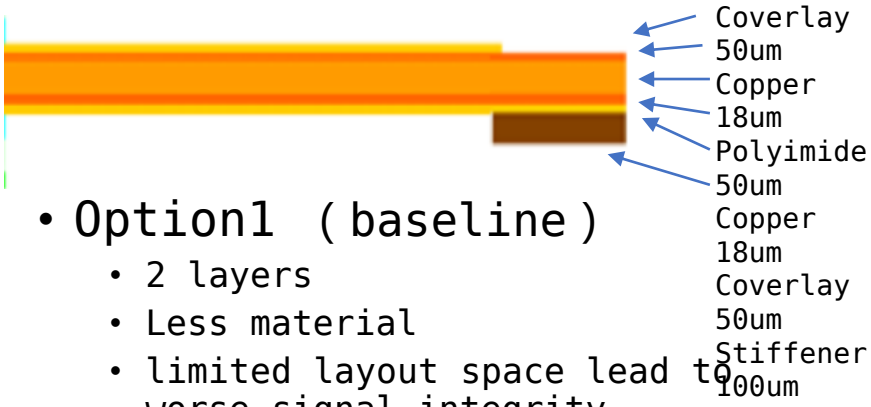
- **Triggerless mode**
  - Global gate signal, **strobe==1**
  - All hits registered at their leading edge
  - 0.2 hits/μs per double col. with the estimated hit density of inner most layer
  - Occupancy 0.02% @ integration time = 1 μs
- **Trigger mode**
  - Global gate **controlled by trigger signal**
  - Hits registered only when overlapped with a trigger (analog buffer)
  - Capable to handle very high hit density with a dead time for readout, 50 ns/hit







Layer Stackup



- Option1 （baseline）
  - 2 layers
  - Less material
  - limited layout space lead to worse signal integrity
    - Crosstalk
    - Large voltage drop
    - Ground bounce
  - Thickness: ~0.2mm （+0.1mm stiffener）

- Option2
  - 4 layers
  - Dedicated GND and power plane gain better signal integrity
  - More material
  - Thickness: ~0.38mm （+ 0.1mm stiffener ）
  - For study the ASIC chips and electronics performance

  The design of the 2 options is similar，and the production has been started at the same time.