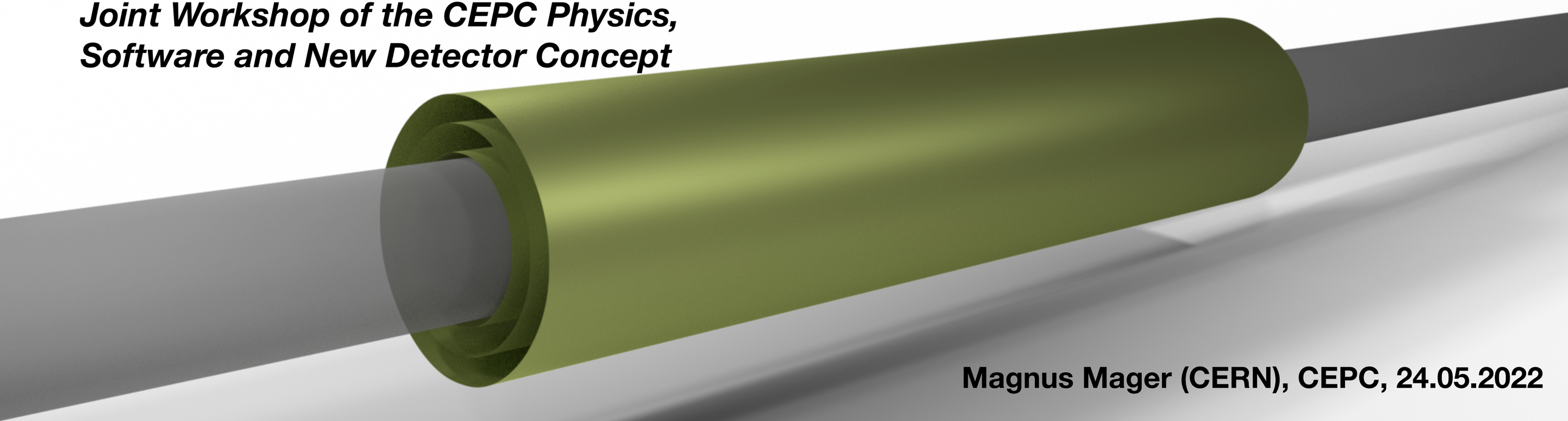
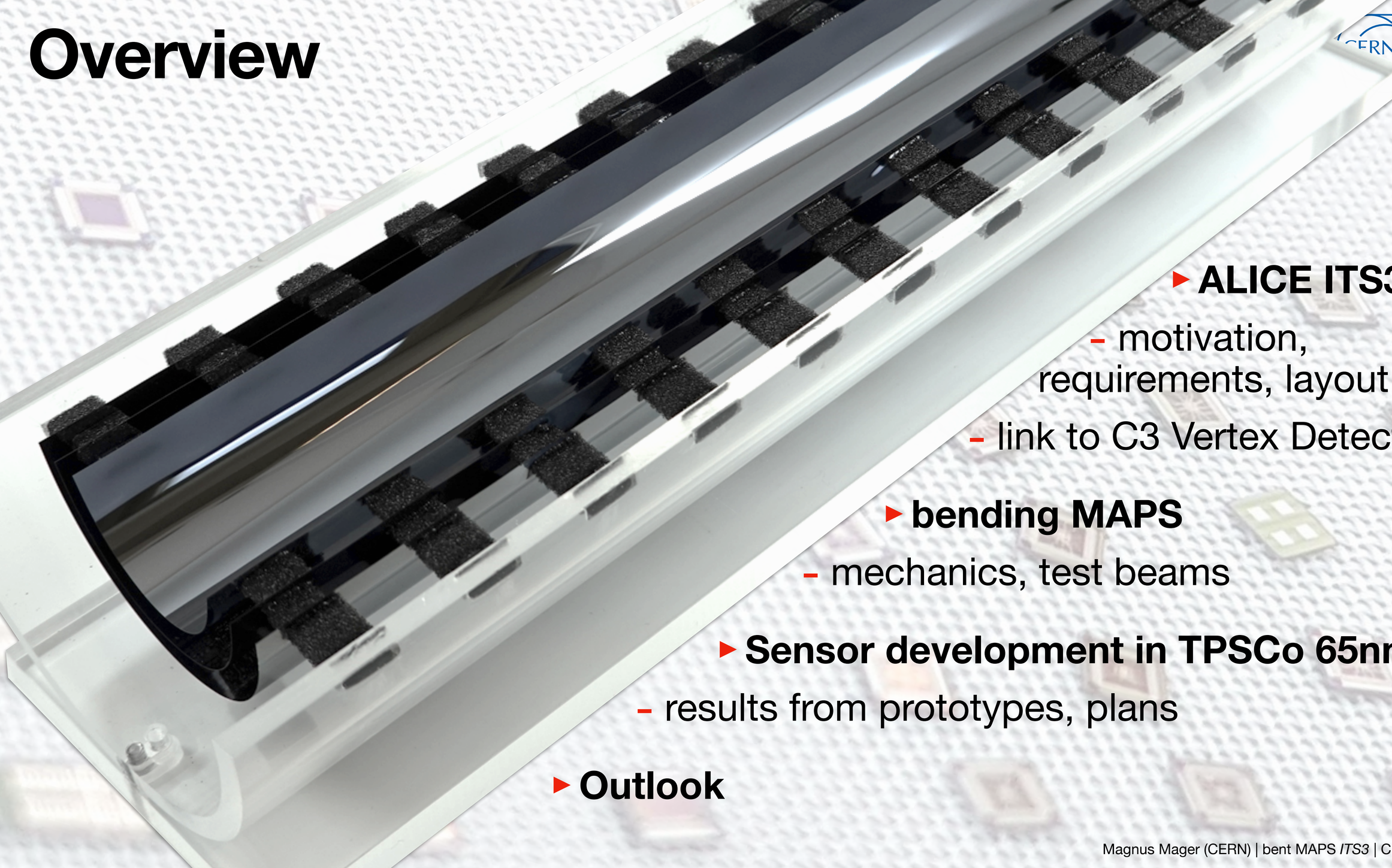
Bent CMOS sensor R&D for next-generation vertex detector *ALICE ITS3*

Magnus Mager (CERN)
on behalf of the ALICE collaboration
Joint Workshop of the CEPC Physics, Software and New Detector Concept



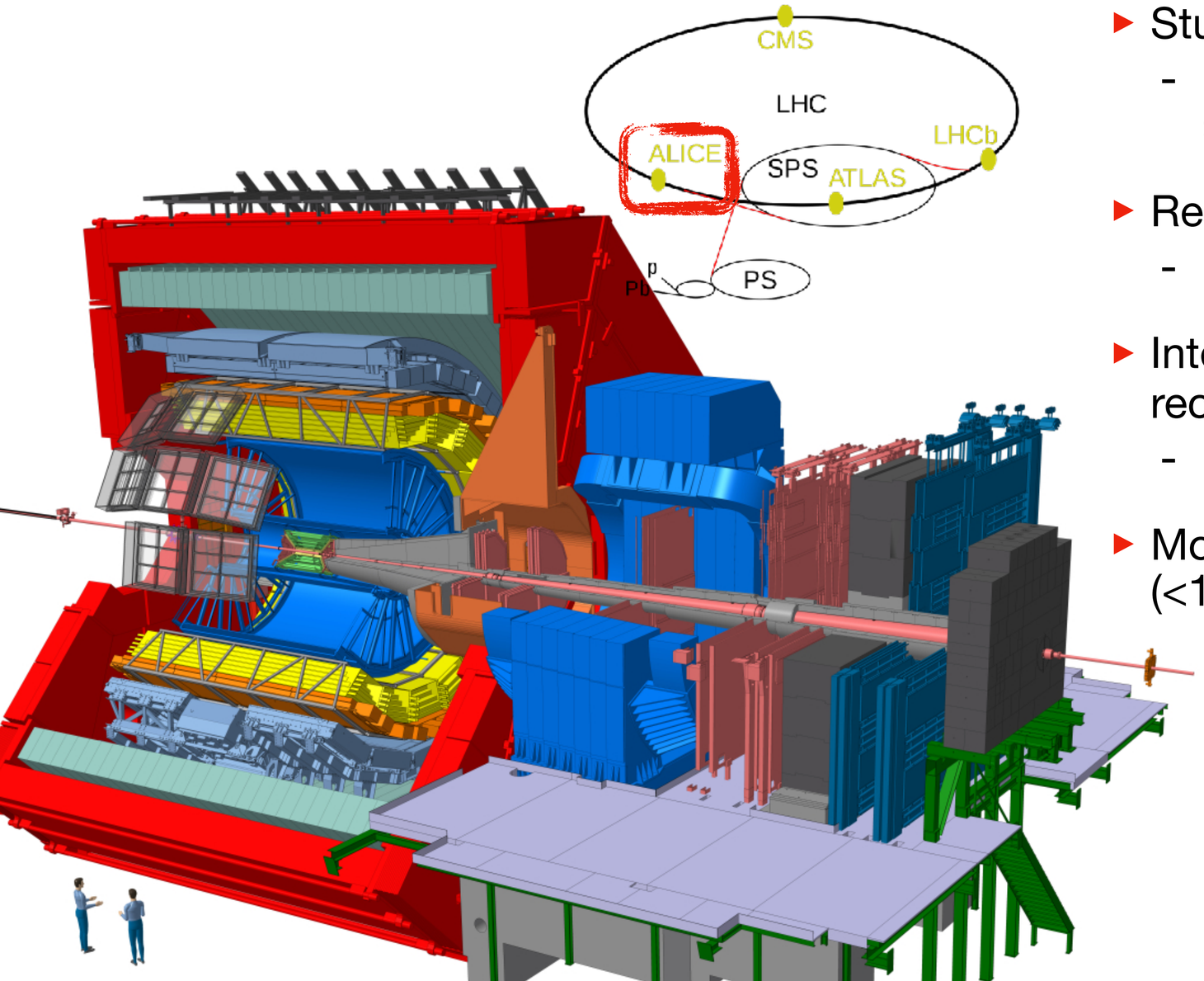
Overview



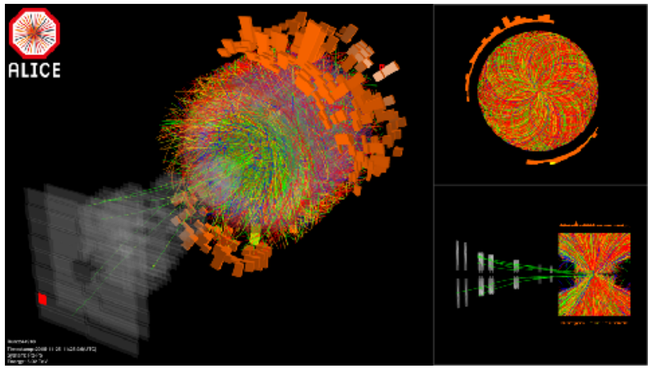
- **ALICE ITS3**
  - motivation, requirements, layout
  - link to C3 Vertex Detector
- **bending MAPS**
  - mechanics, test beams
- **Sensor development in TPSCo 65nm CIS**
  - results from prototypes, plans
- **Outlook**

ALICE

Detector and main goals

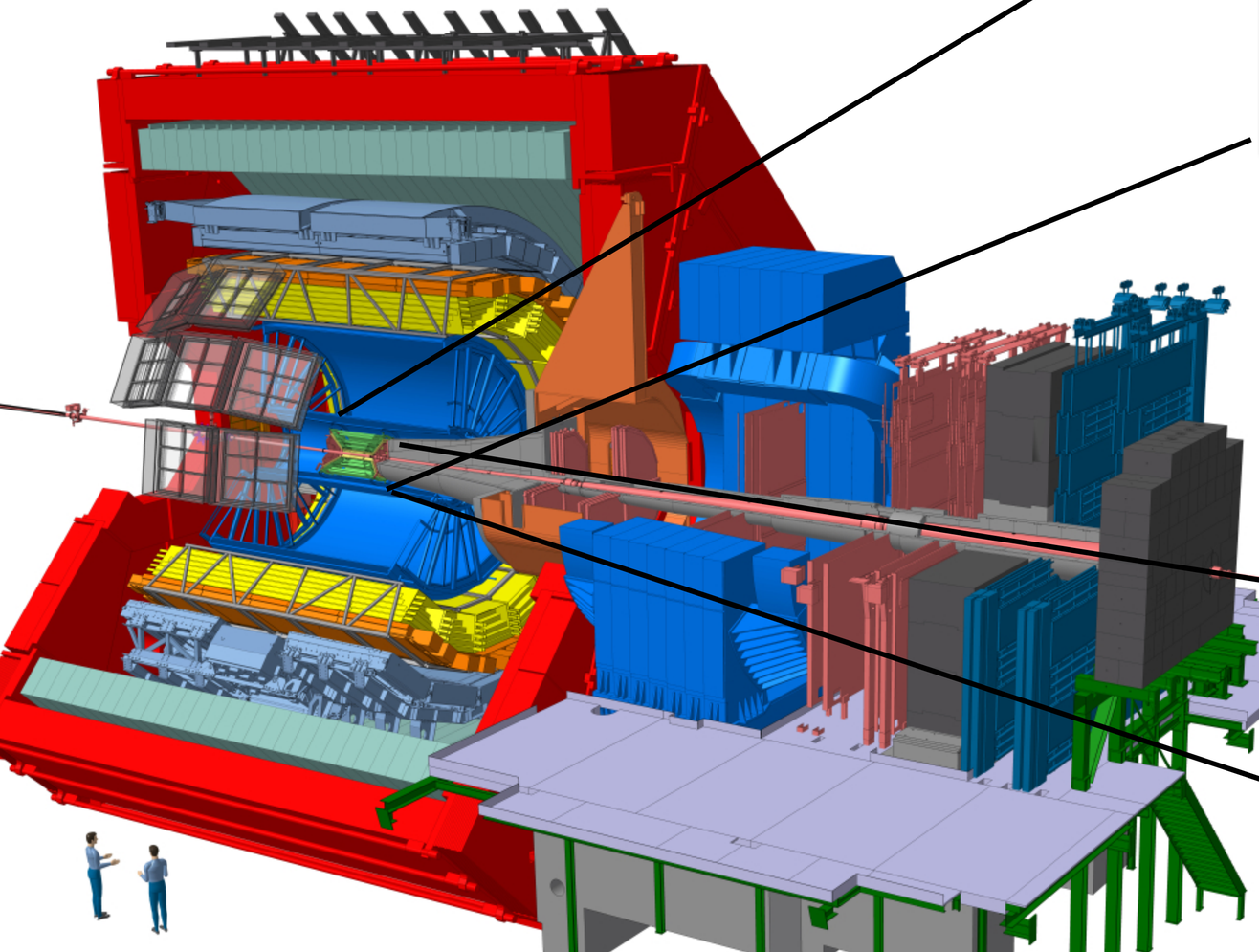


- Study of QGP in heavy-ion collisions at LHC
  - i.e. up to O(10k) particles to be tracked in a single event
- Reconstruction of charm and beauty hadrons
  - requires precise inner tracker
- Interest in low momentum (≲1 GeV/c) particle reconstruction
  - requires low material budgets
- Moderate radiation environment (<10^{14} 1MeV n_{eq}/cm^2 NIEL)

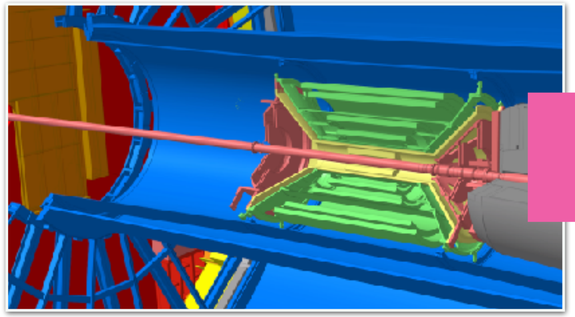


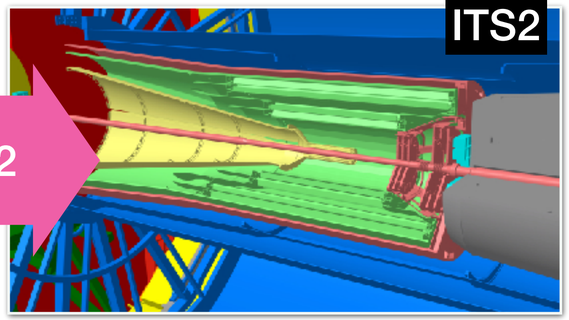
ALICE

LS2 upgrades with Monolithic Active Pixel Sensors (MAPS)



Inner Tracking System





LS2

6 layers:
- 2 hybrid silicon pixel
- 2 silicon drift
- 2 silicon strip

Inner-most layer:
- radial distance: 39 mm
- material: $X/X_0 = 1.14\%$
- pitch: $50 \times 425\ \mu m^2$

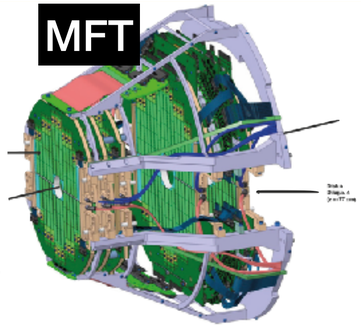
rate capability: 1 kHz

7 layers:
- all MAPS
- 10 m^2, 24k chips, 12.5 Giga-Pixels

Inner-most layer:
- radial distance: 23 mm
- material: $X/X_0 = 0.35\%$
- pitch: $29 \times 27\ \mu m^2$

rate capability: 100 kHz (Pb-Pb)

Muon Forward Tracker



new detector

5 discs, double sided:
- based on same technology as ITS2

ALICE

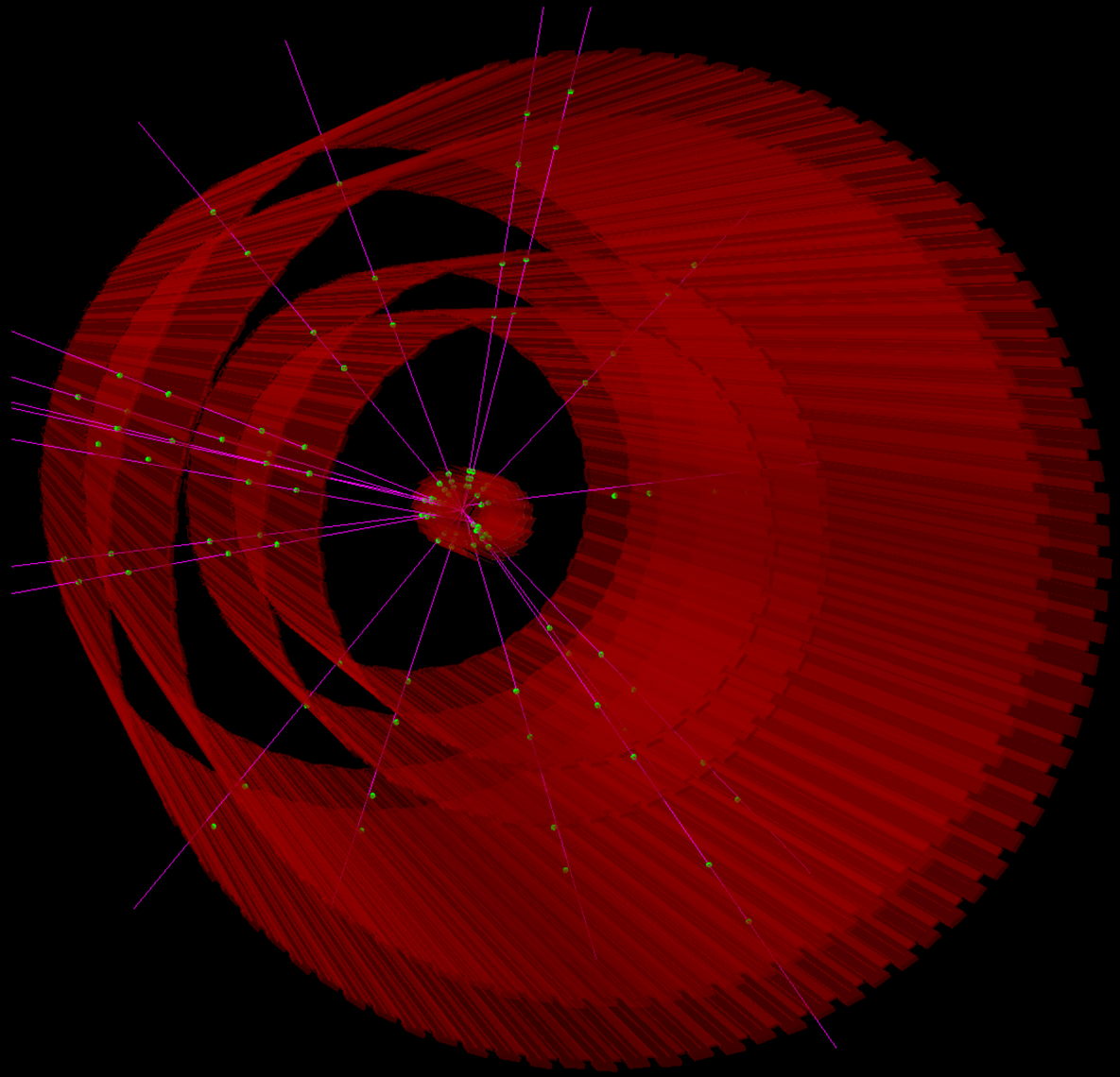
LS2 upgrade

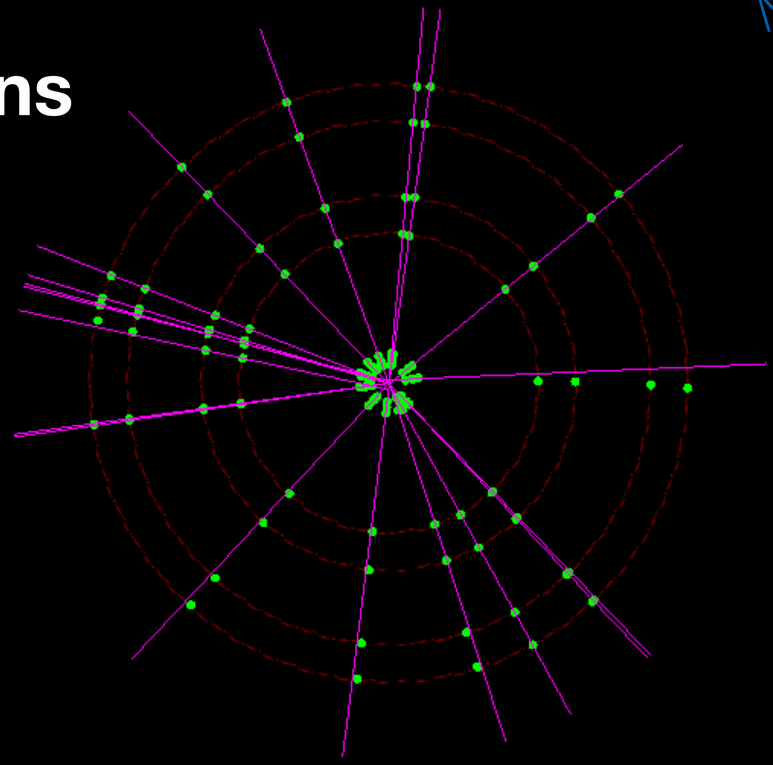
Active Pixel

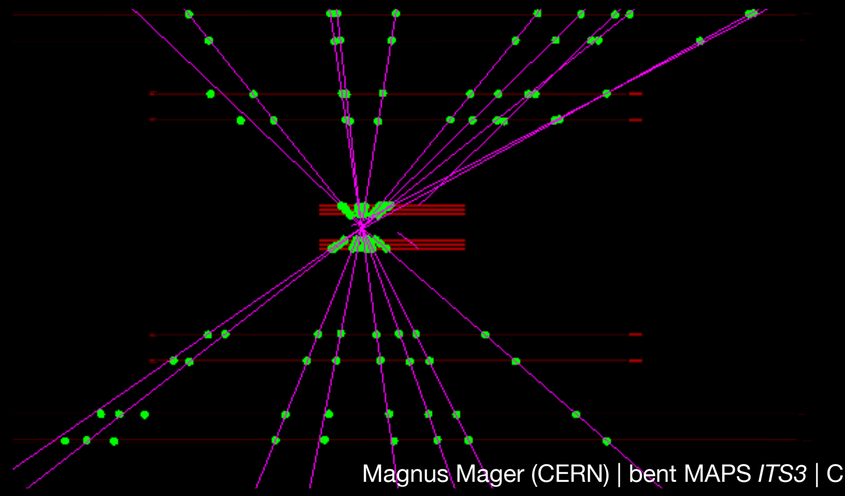
~ 10 years of R&D and C&I

LHC pilot beam results

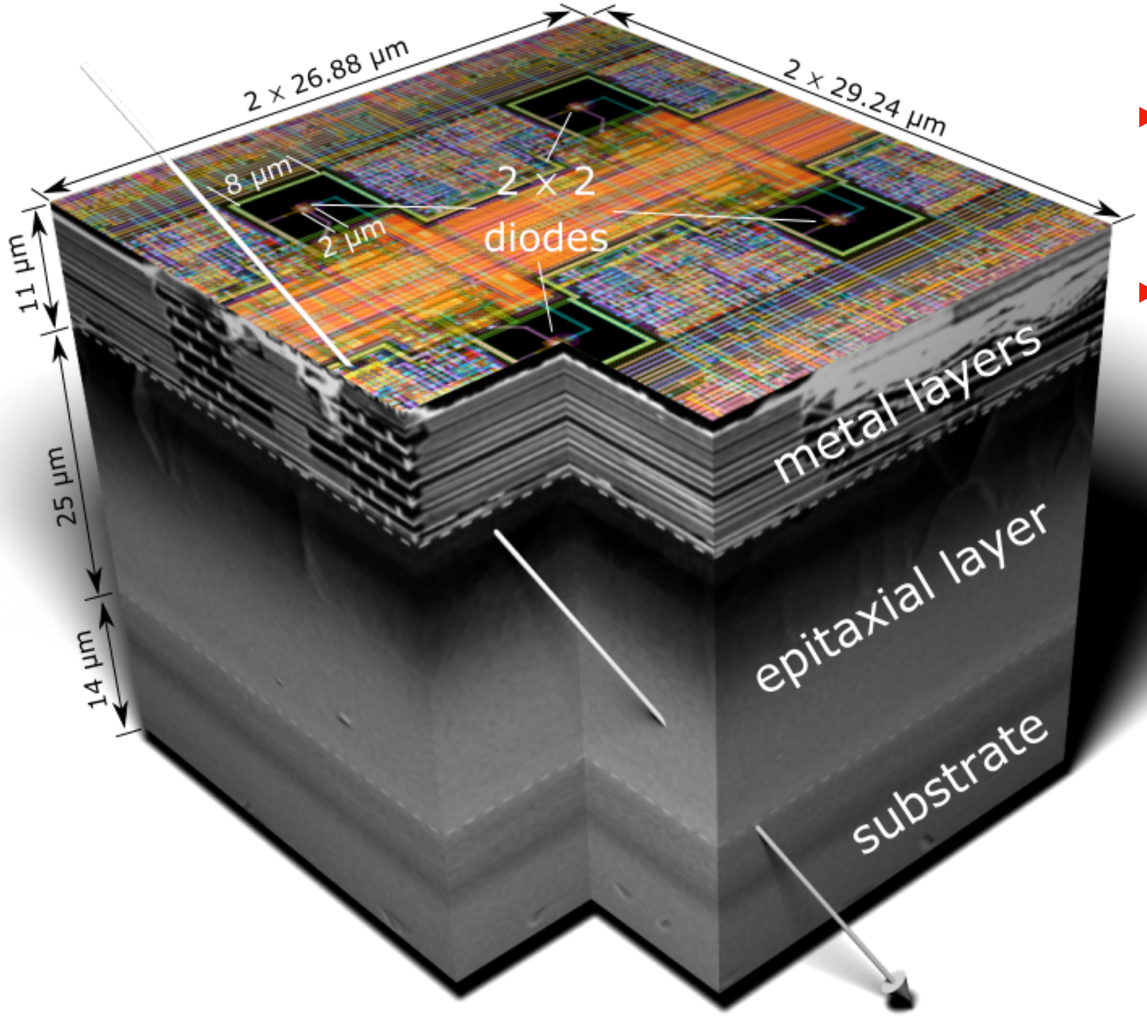
September 2021, 900 GeV proton collisions



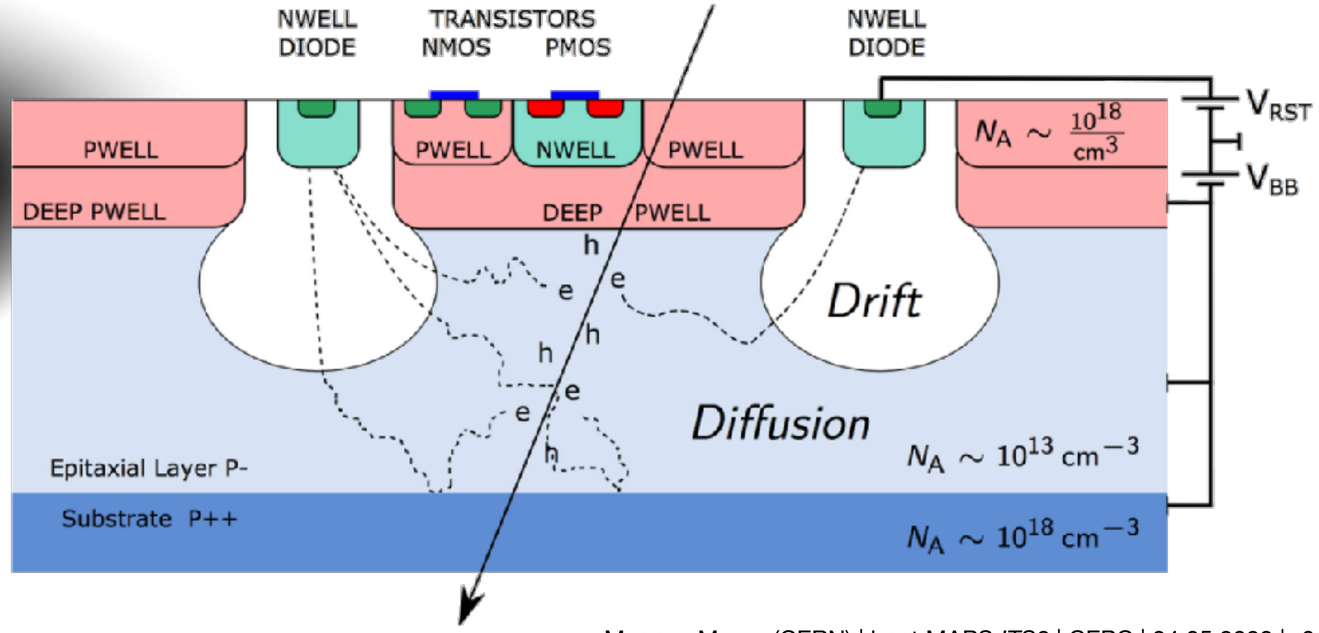




ALPIDE
Technology

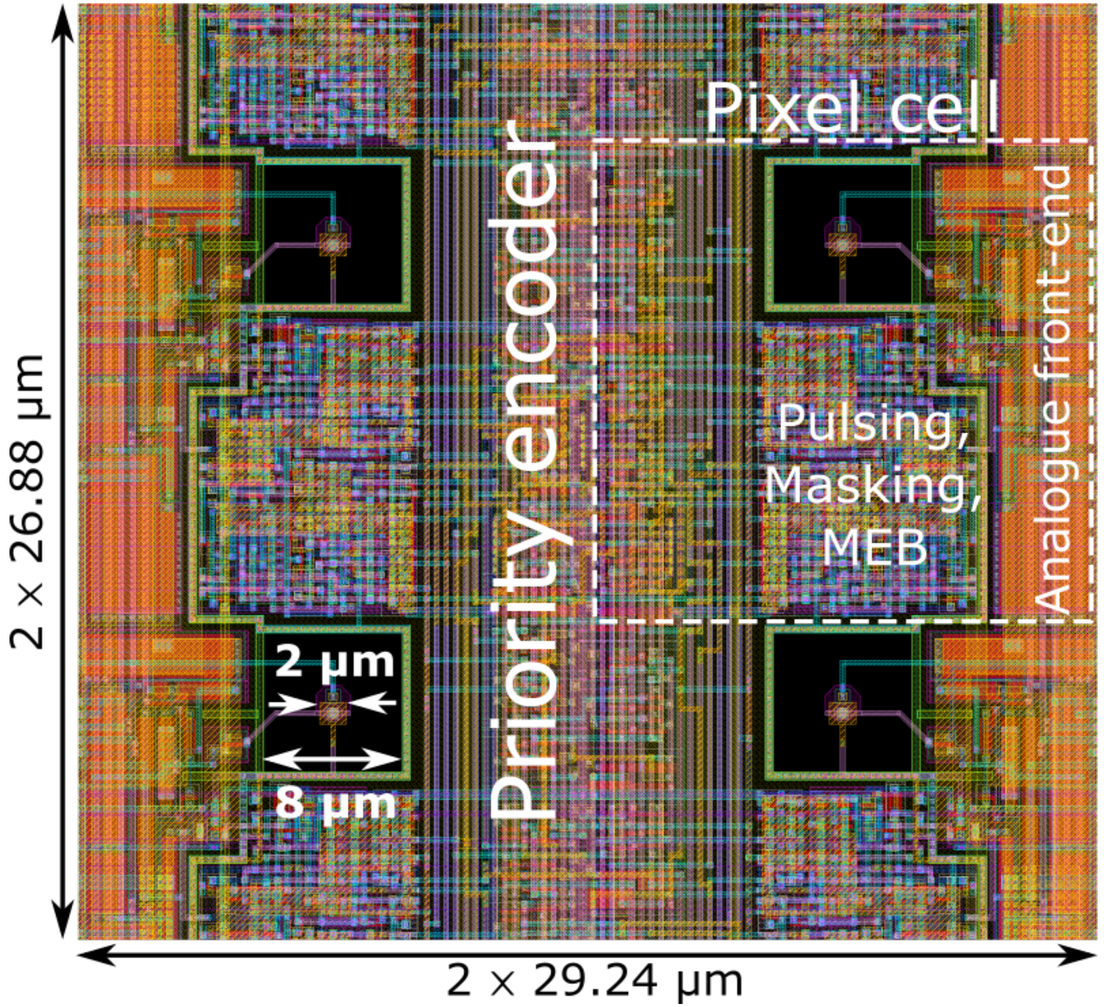


- **Process:** Tower Semiconductor 180 nm CIS
  - deep p-well to allow CMOS circuitry inside matrix
  - reverse-substrate bias
- **Detection layer:** 25 µm high-resistive (>1 kΩcm) epitaxial layer
- **Thickness:** 100 µm (OB) or 50 µm (IB)



ALPIDE

Pixel functionality

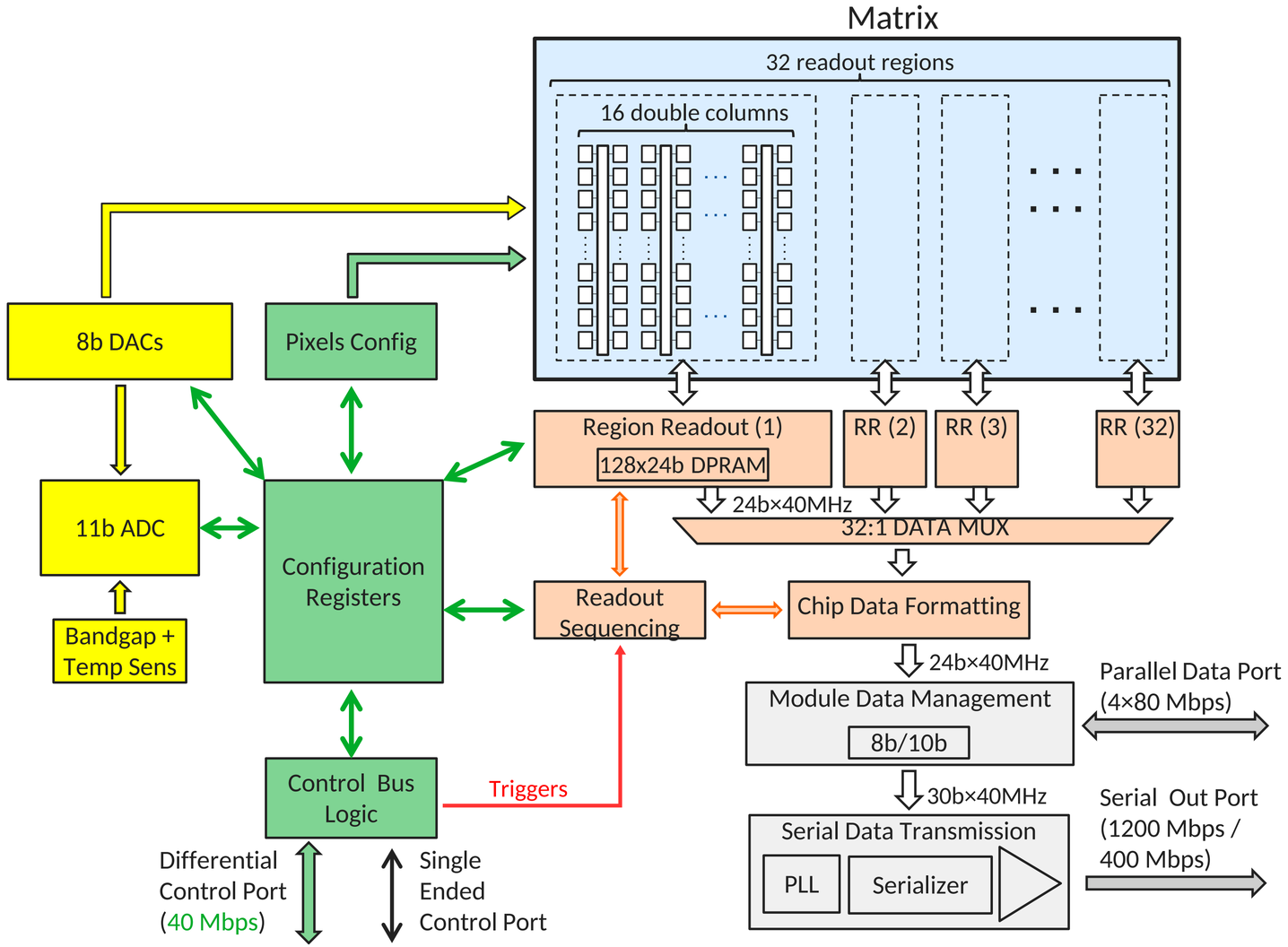


- **Front-end:**
  (9 transistors, full-custom)
  - continuously active
  - shaping time: < 10 µs
  - power consumption: 40 nW
- **Multiple-event memory:** 3 stages
  (62 transistors, full-custom)
- **Configuration:** pulsing & masking registers
  (31 transistors, full-custom)
- **Testing:** analogue and digital test pulse circuitry
  (17 transistors, full-custom)
- **Readout:** priority encoder, asynchronous, hit-driven

O(200) transistors / pixel (wrt. 3T/4T)

ALPIDE

Global architecture



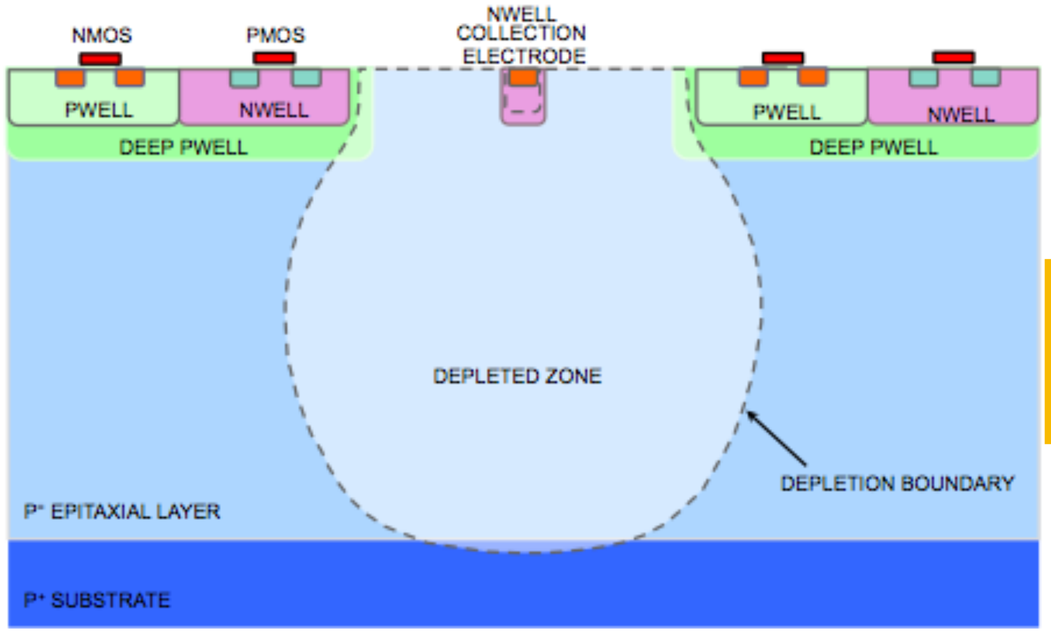
- **Fully integrated:**
  - next active circuit ≳ 8 m away off-detector
- **Strobing:**
  - global shutter
  - either triggered or in continuous sequence
- **Data interface:**
  - high-speed serial link using copper cables

MAPS are highly integrated devices: reducing material budget + integration complexity

Process modification

Fully depleted MAPS — ITS2 “side project”

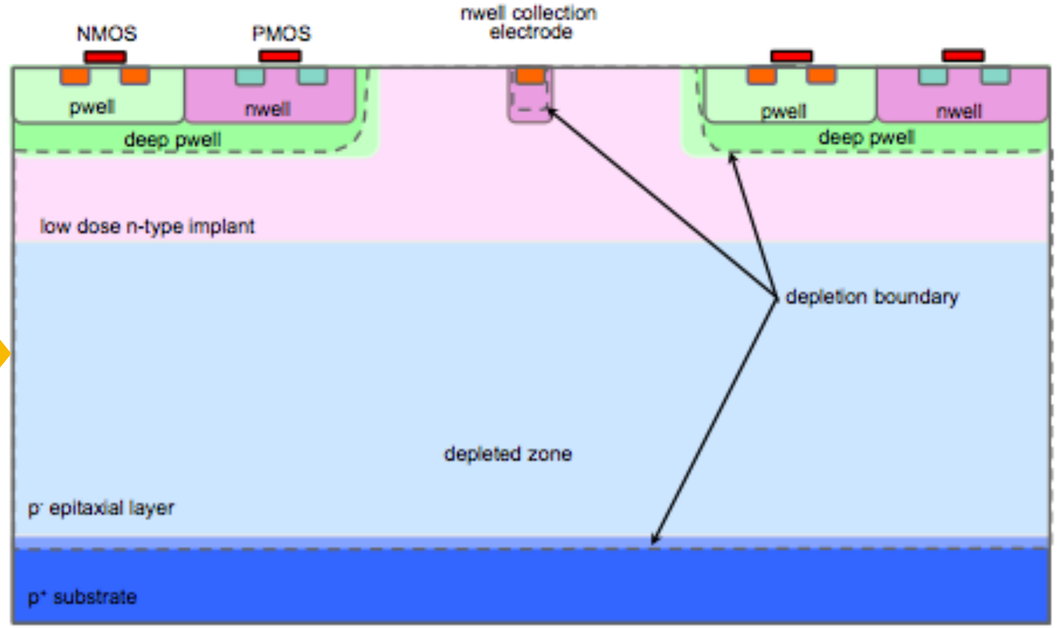
Foundry standard process



Partially depleted epitaxial layer
Charge collection time < 30 ns
Operational up to 10^{14} 1 MeV n_{eq}/cm^2

Developed and prototyped within ALPIDE R&D

Modified process CERN/Tower



Fully depleted epitaxial layer
Charge collection time < 1 ns
Operational up to 10^{15} 1 MeV n_{eq}/cm^2

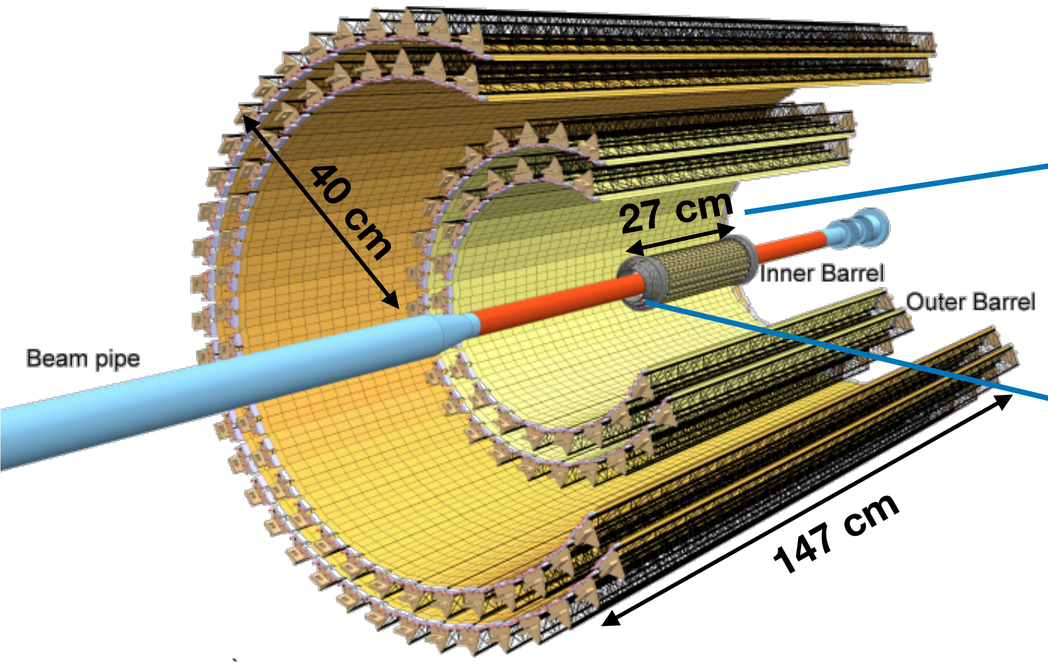
Excellent co-operation with foundry!

Now being further pursued with MALTA, CLICpix, FastPix, …

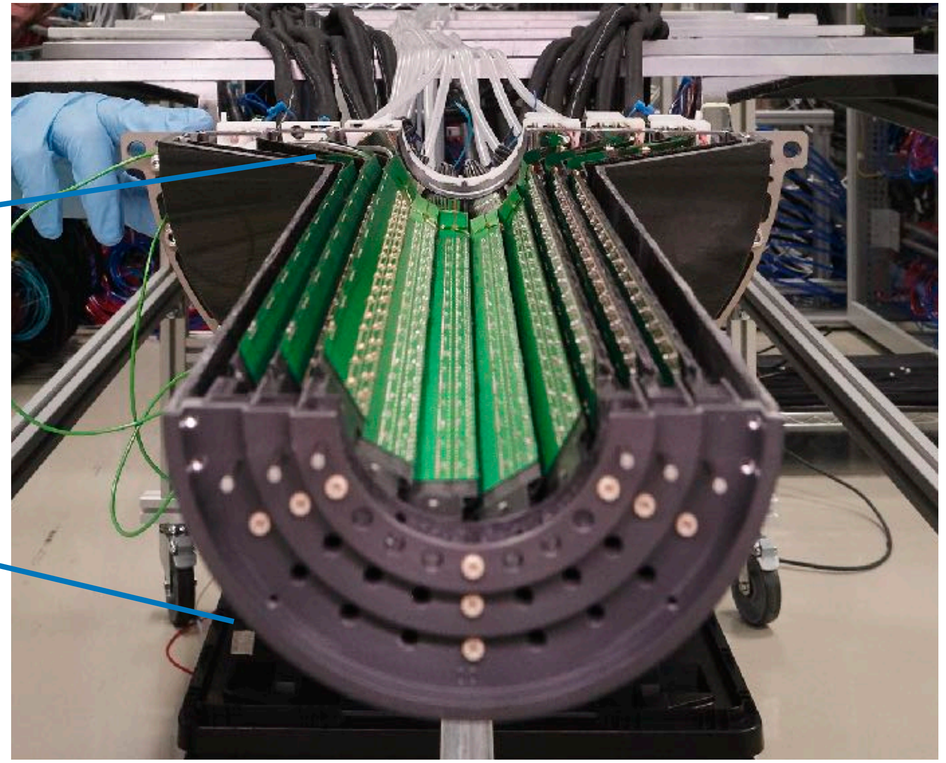
More details:
NIM **A871** (2017) 90-96
https://doi.org/10.1016/j.nima.2017.07.046

ITS2 inner barrel

Layout



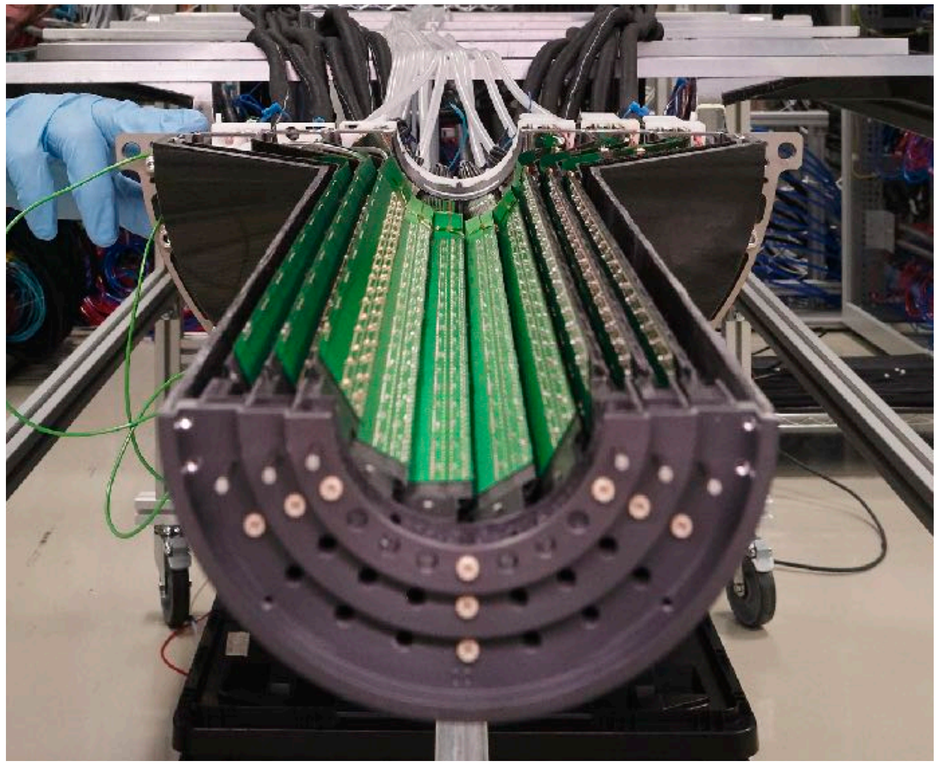
ITS2: assembled three inner-most half-layers



- ITS2 is expected to perform according to specifications or even better
- The Inner Barrel is ultra-light but rather packed → further improvements seem possible
- **Key questions: Can we get closer to the IP? Can we reduce the material further?**

ITS2 → ITS3

idea

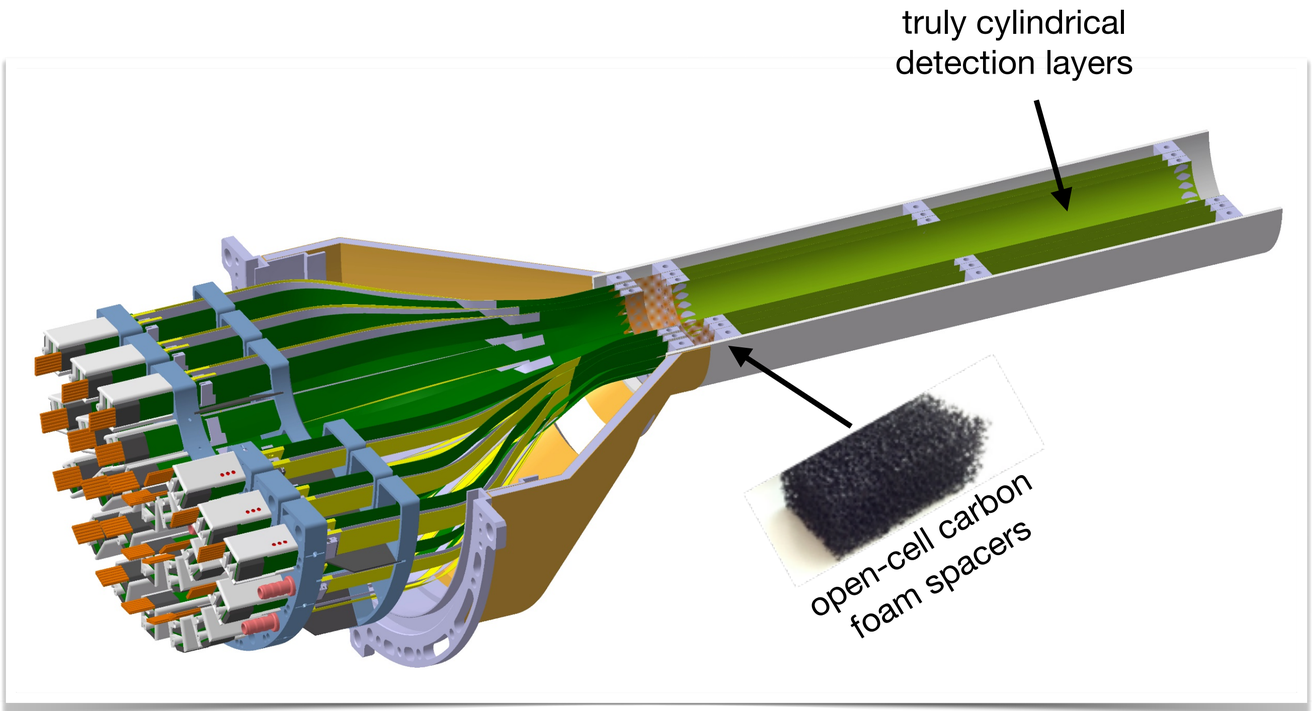


- By employing wafer-scale, bent sensors it can be improved on:
  - material budget (~ factor 7)
  - distance to interaction point (no “turbo” geometry)

ITS3 Letter of Intent [CERN-LHCC-2019-018 ; LHCC-I-034]

The idea is simple, but requires quite some R&D — which we started in Dec 2019!

ITS3 detector concept



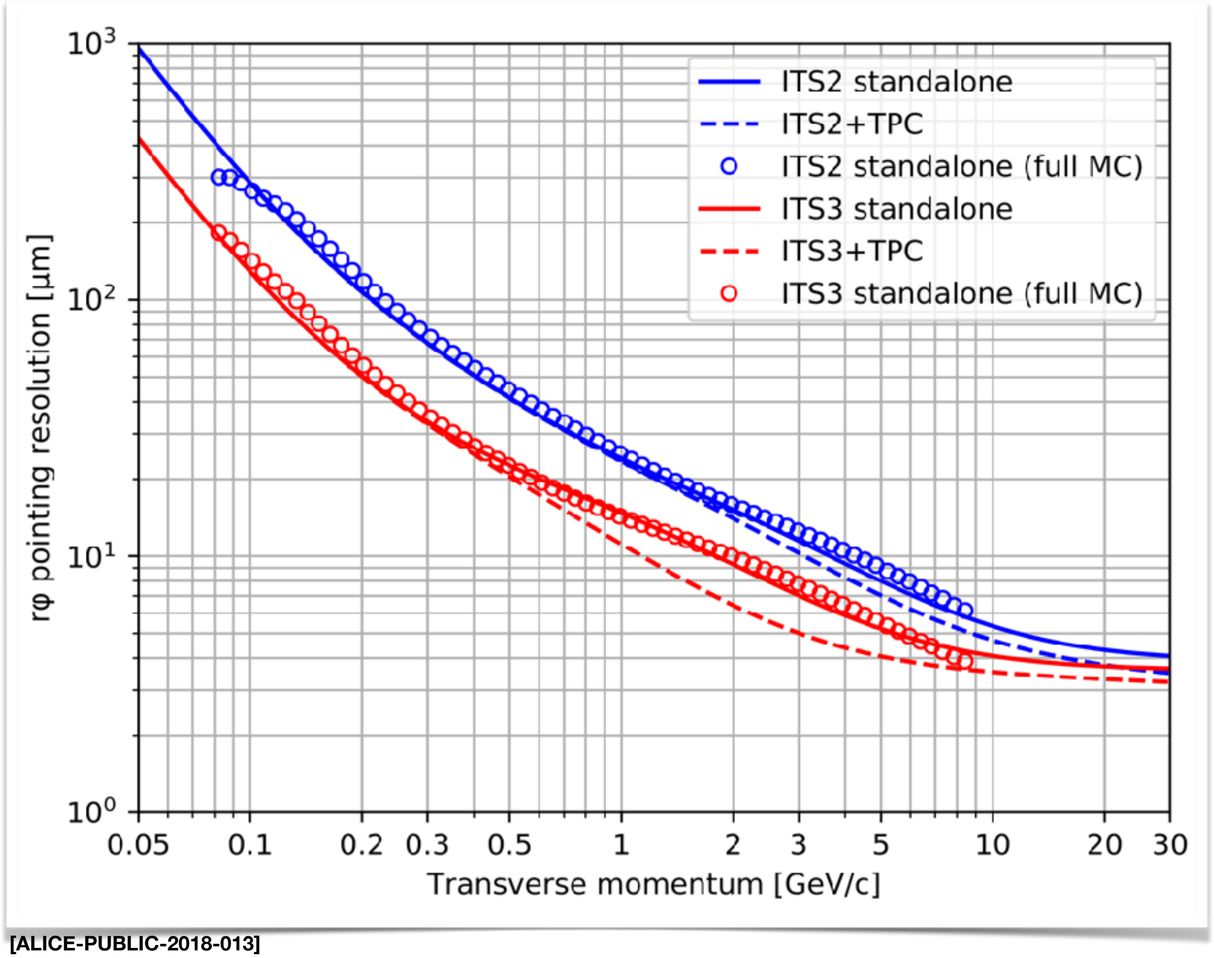
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- Key ingredients:
  - 300 mm wafer-scale sensors, fabricated using stitching
  - thinned down to 20-40 µm (0.02-0.04% X_0), making them flexible
  - bent to the target radii
  - mechanically held in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X_0 (beampipe: 500 µm Be: 0.14% X_0)
  - homogeneous material distribution: negligible systematic error from material distribution

The whole detector will consist of six (!) sensors (current ITS IB: 432) – and barely anything else

ITS3 performance figures

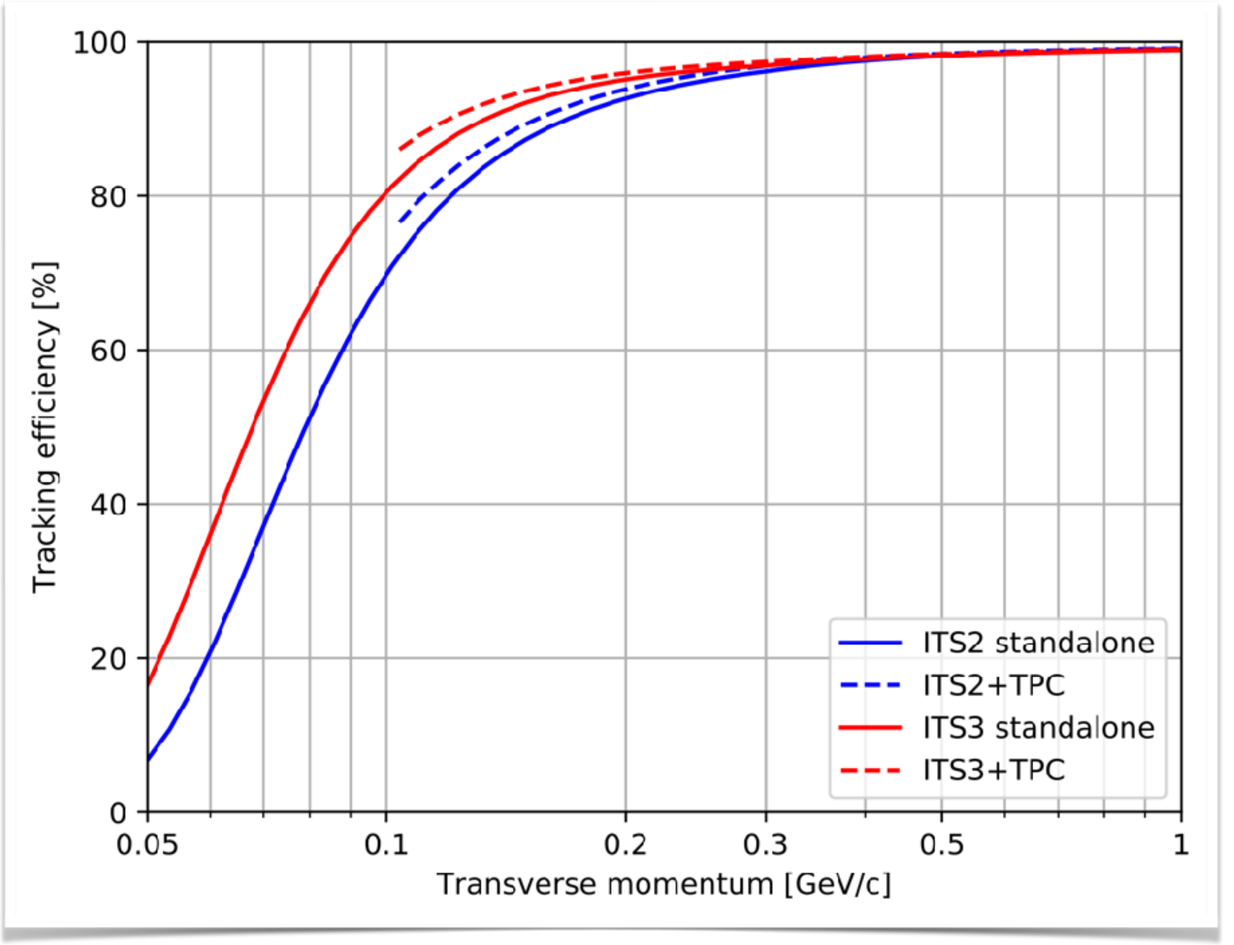
pointing resolution



[ALICE-PUBLIC-2018-013]

improvement of factor 2 over all momenta

tracking efficiency

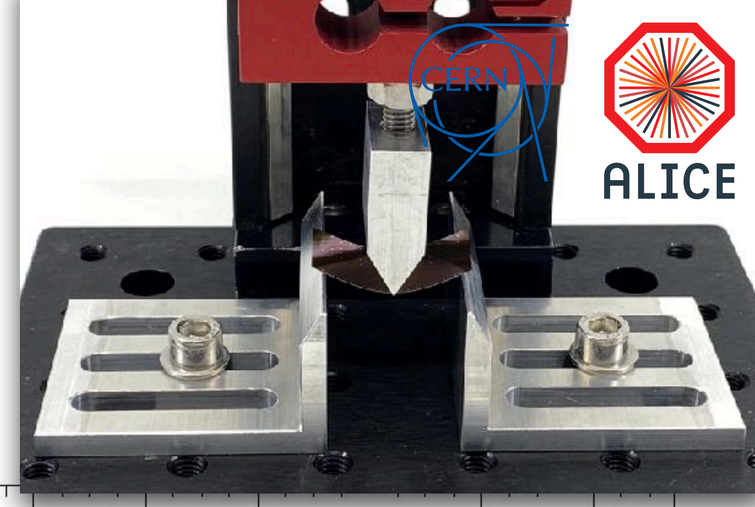


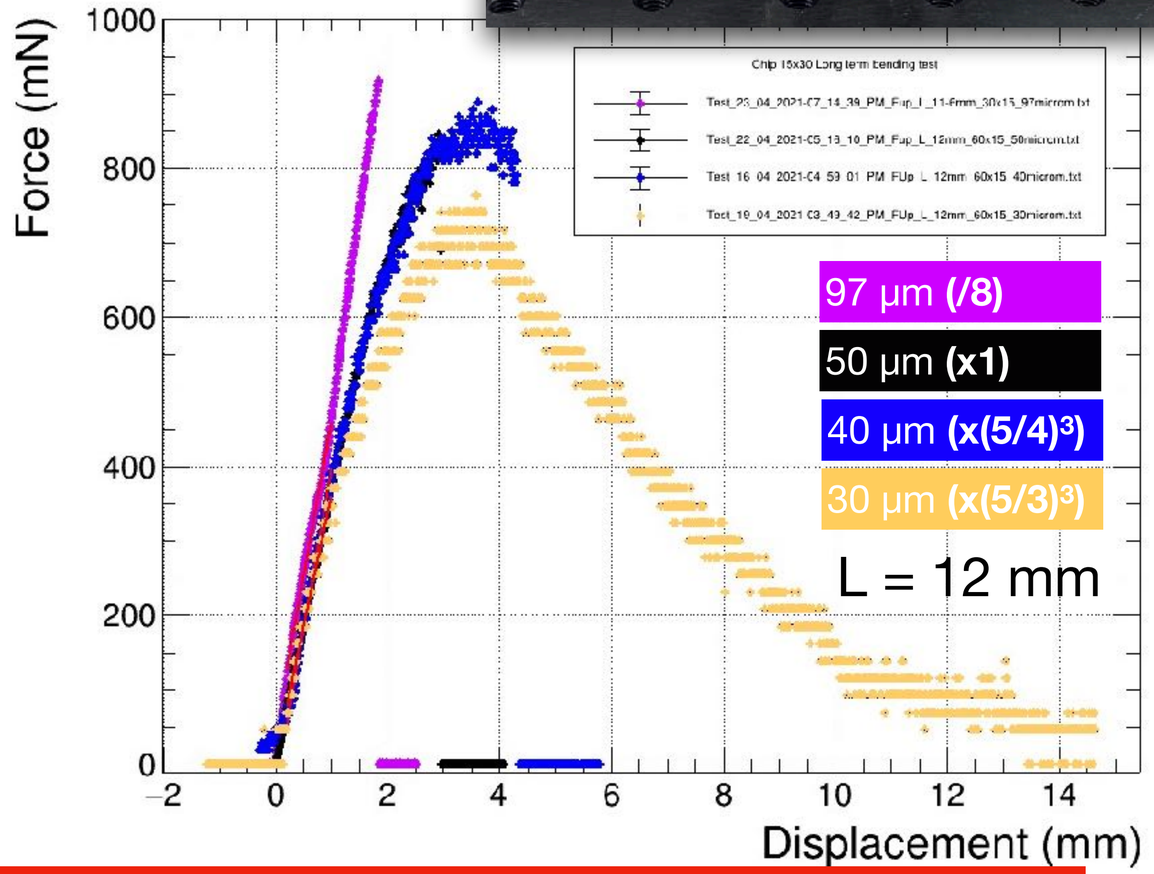
large improvement for low transverse momenta

Bending MAPS

Flexibility of silicon

- **Monolithic** Active Pixel Sensors are quite flexible
  - already at thicknesses that are used for current detectors
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors
- Breakage at smaller radii for thinner chips
  - again benefit from thinner sensors
- **Our target values are very feasible!**

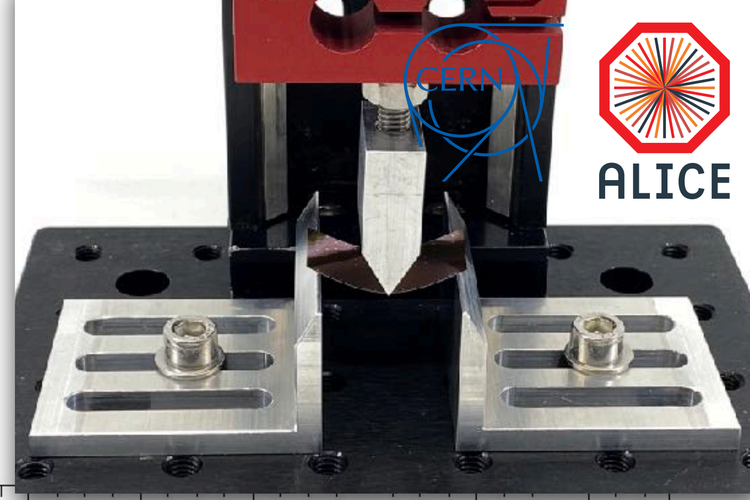


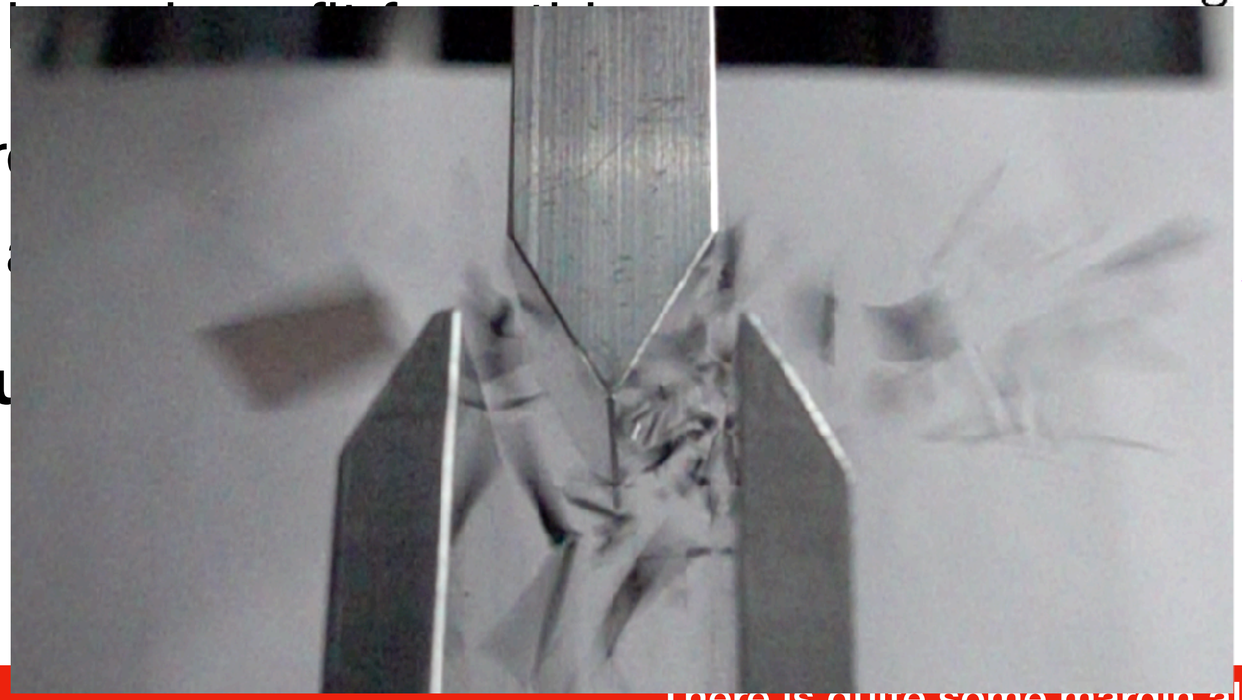


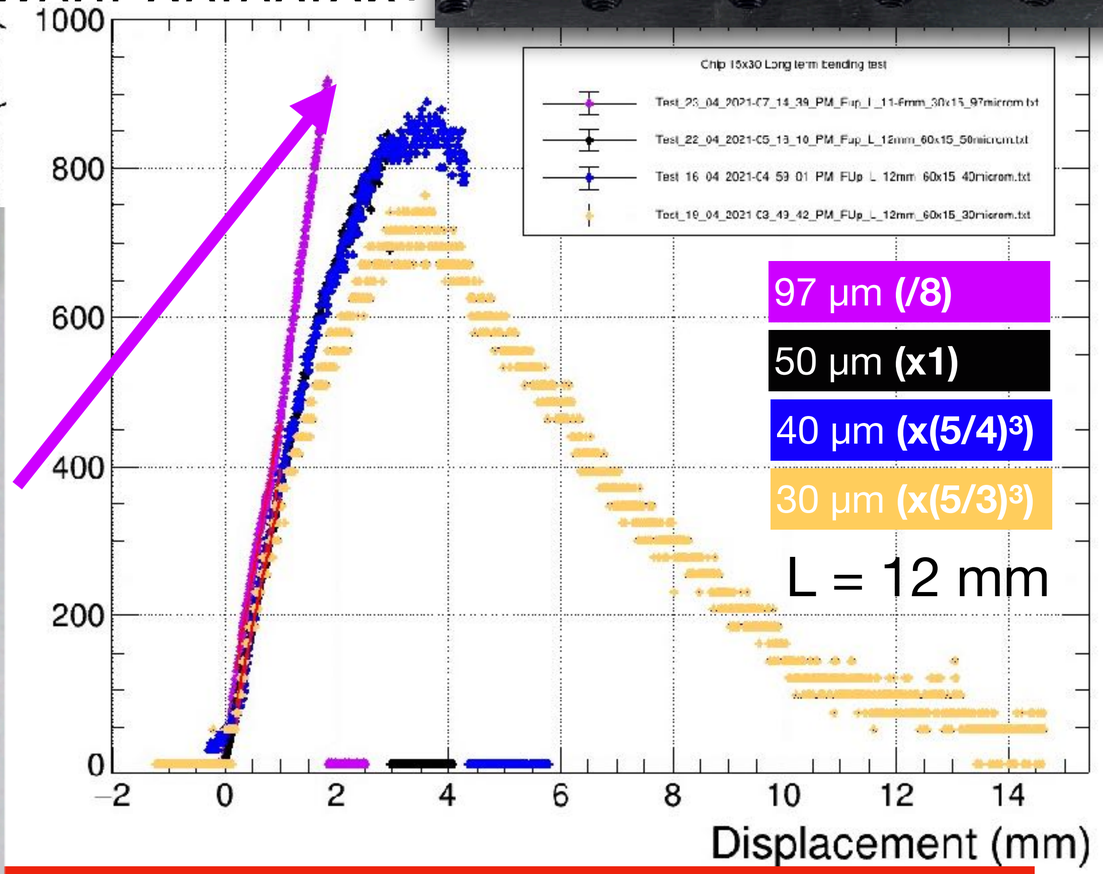
There is quite some margin already at 50 µm!

Flexibility of silicon

- **Monolithic** Active Pixel Sensors are quite flexible
  - already at thicknesses that are used for current detectors
- Bending force scales as (thickness)$^{-3}$
  -
- Br
  -
- **Ou**

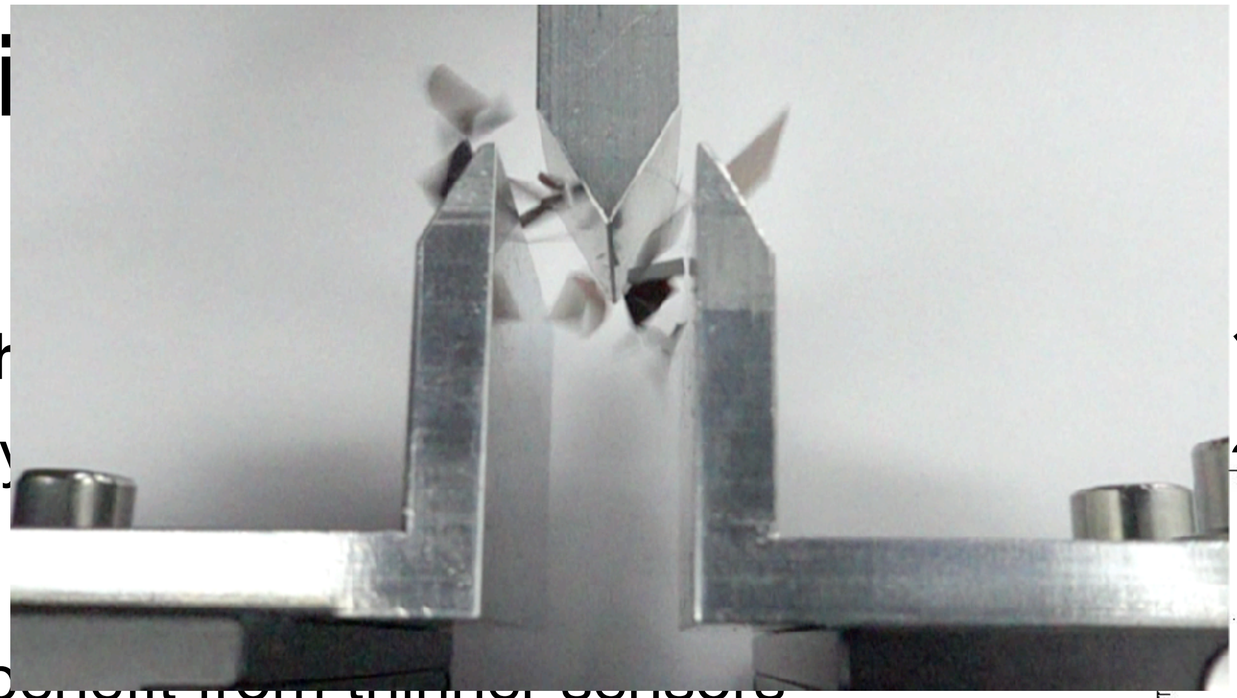


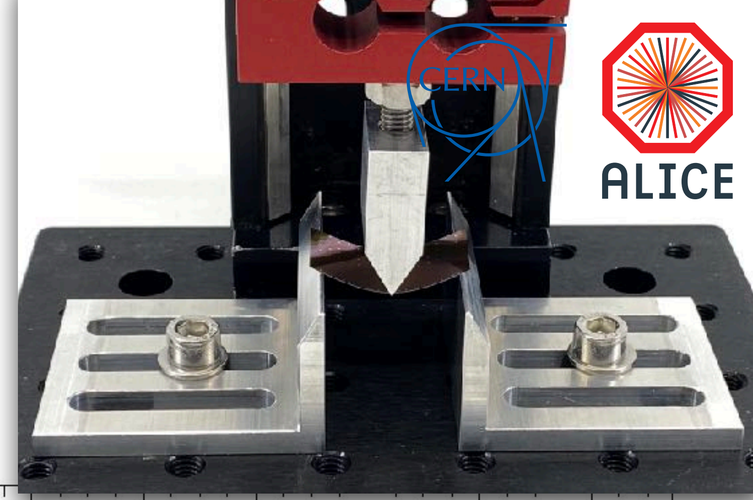




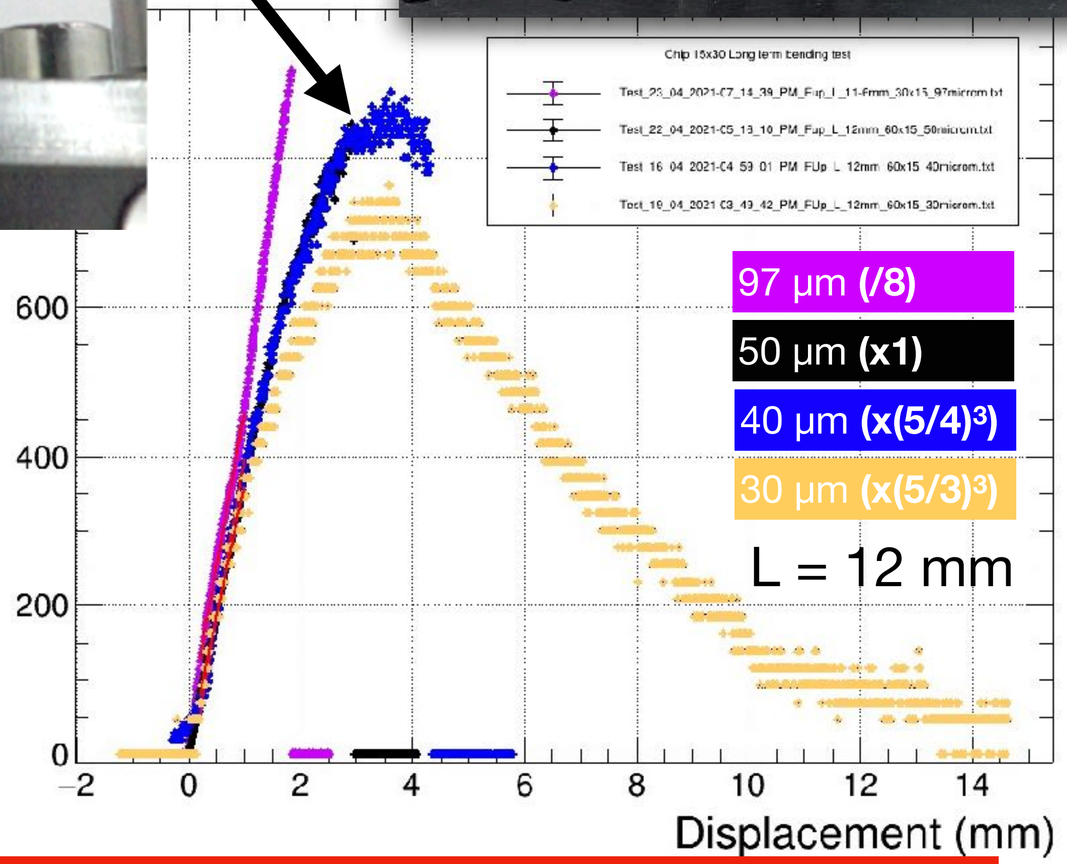
There is quite some margin already at 50 µm!

Flexibi





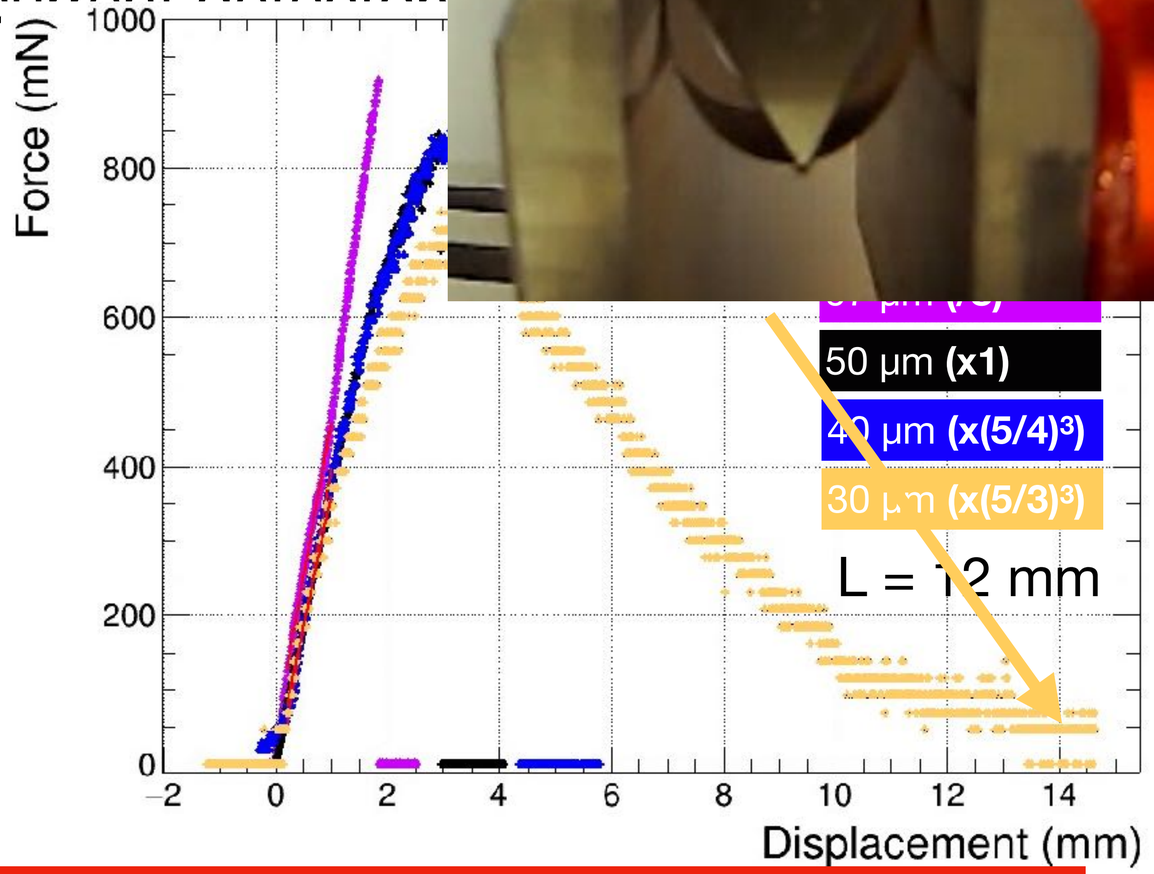
- **Monolith**
  - already
- Bending
  - large b
- Breakage at smaller radii for thinner chips
  - again benefit from thinner sensors
- **Our target values are very feasible!**



There is quite some margin already at 50 µm!

Flexibility of silicon

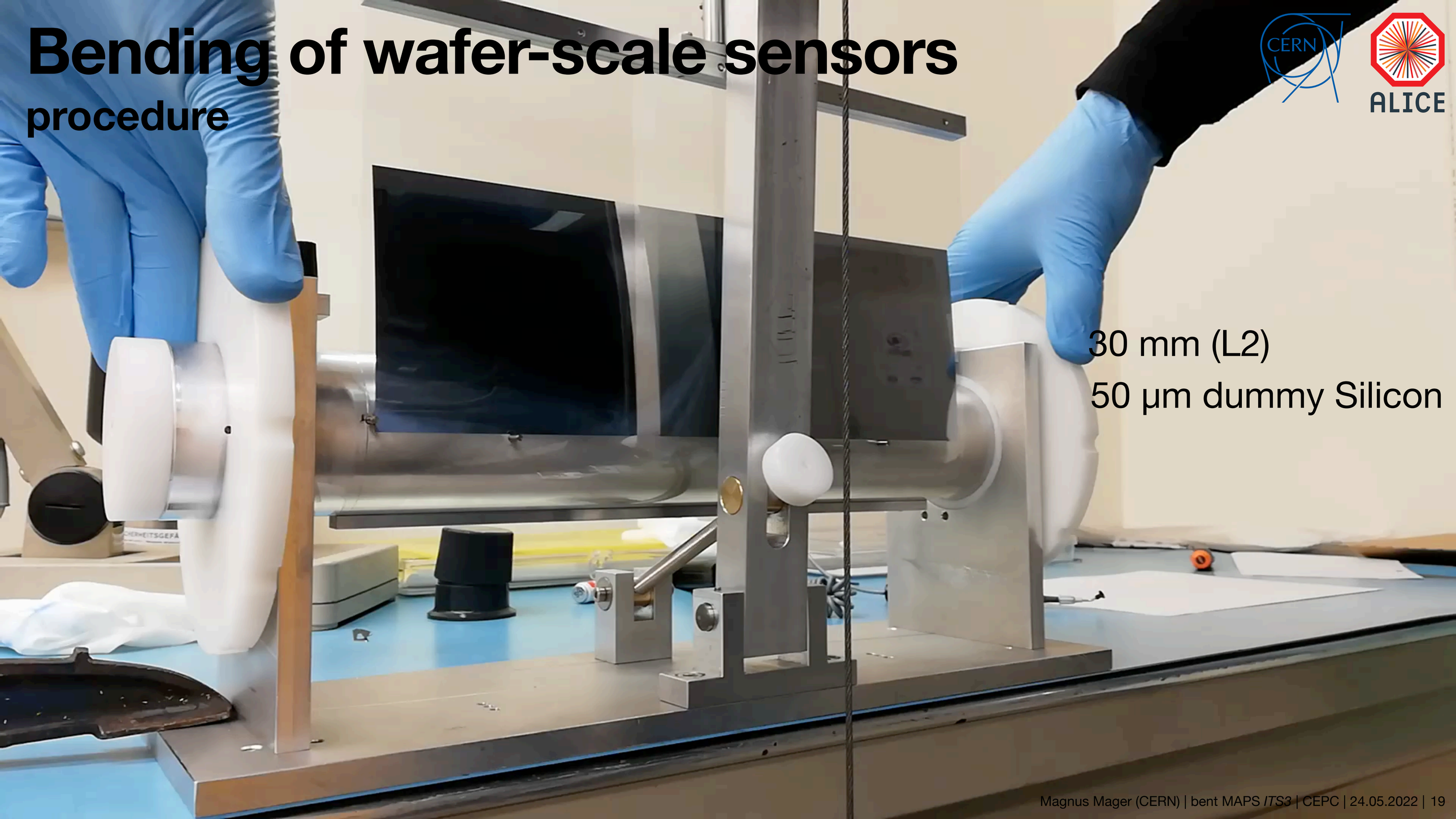
- **Monolithic** Active Pixel Sensors are quite flexible
  - already at thicknesses that are used for current detectors
- Bending force scales as (thickness)$^{-3}$
  - large benefit from thinner sensors
- Breakage at smaller radii for thinner chips
  - again benefit from thinner sensors
- **Our target values are very feasible!**



There is quite some margin already at 50 µm!

Bending of wafer-scale sensors

procedure

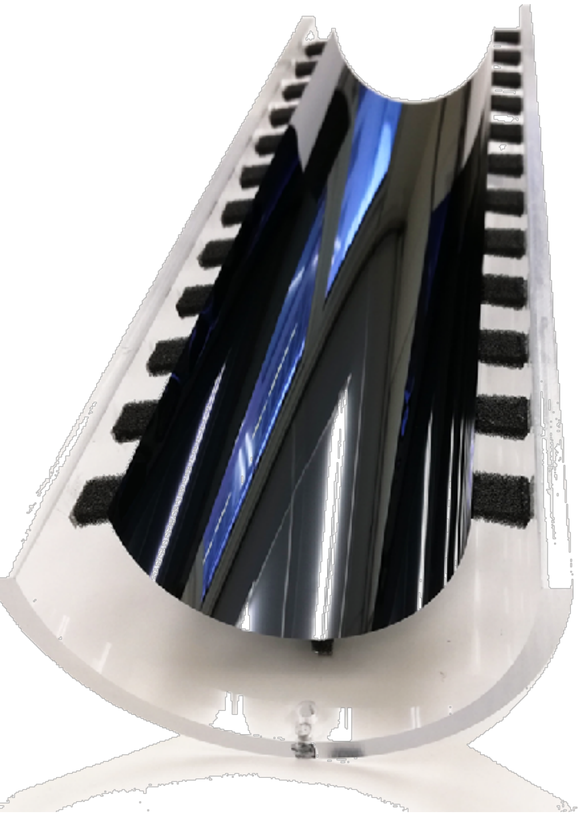


30 mm (L2)

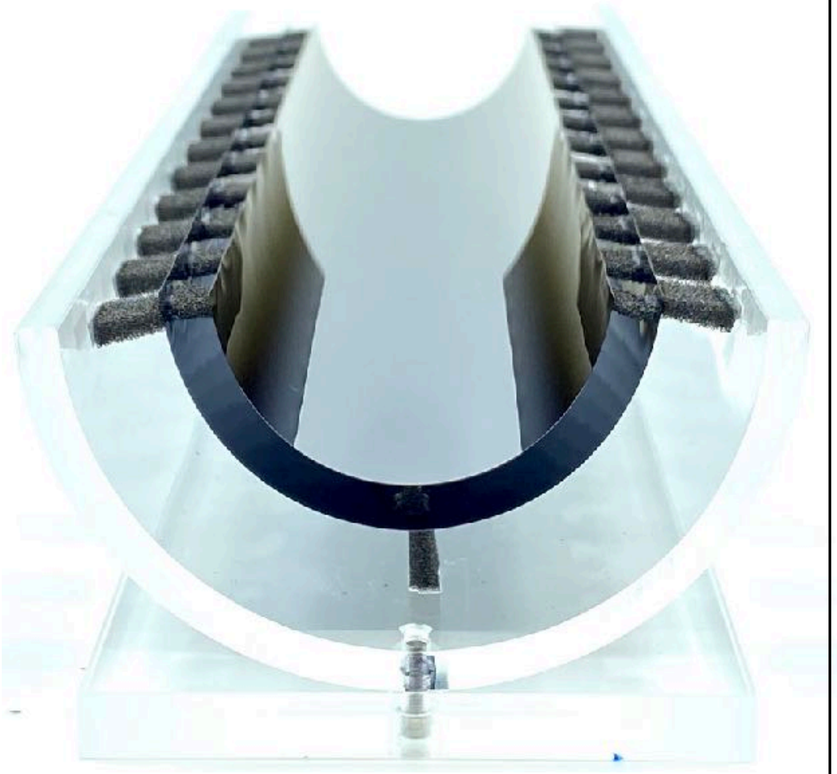
50 µm dummy Silicon

Layer assembly

Layer 2



Layers 2+1

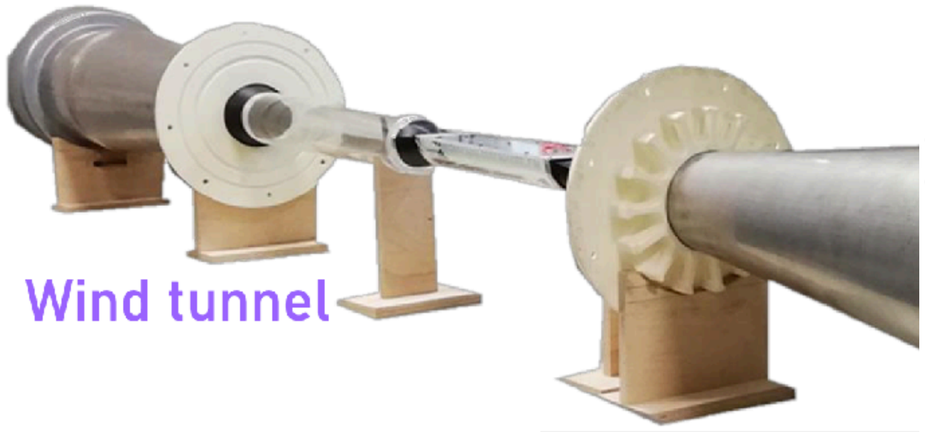


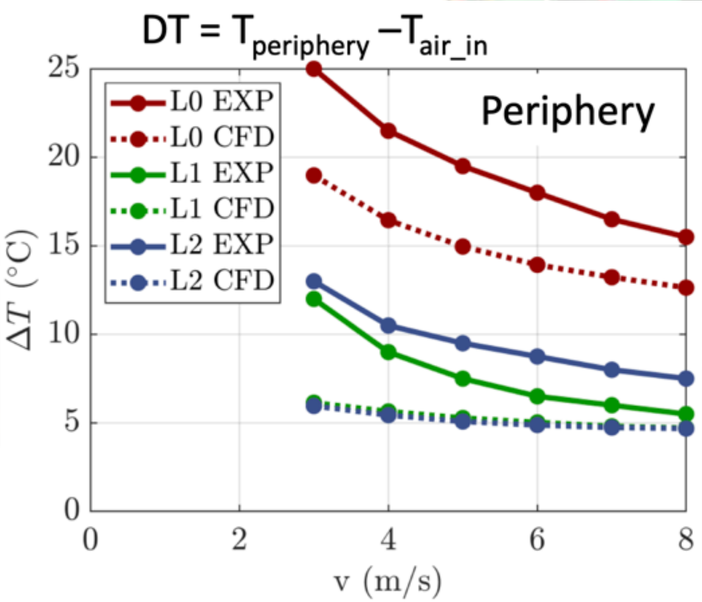
Layers 2+1+0

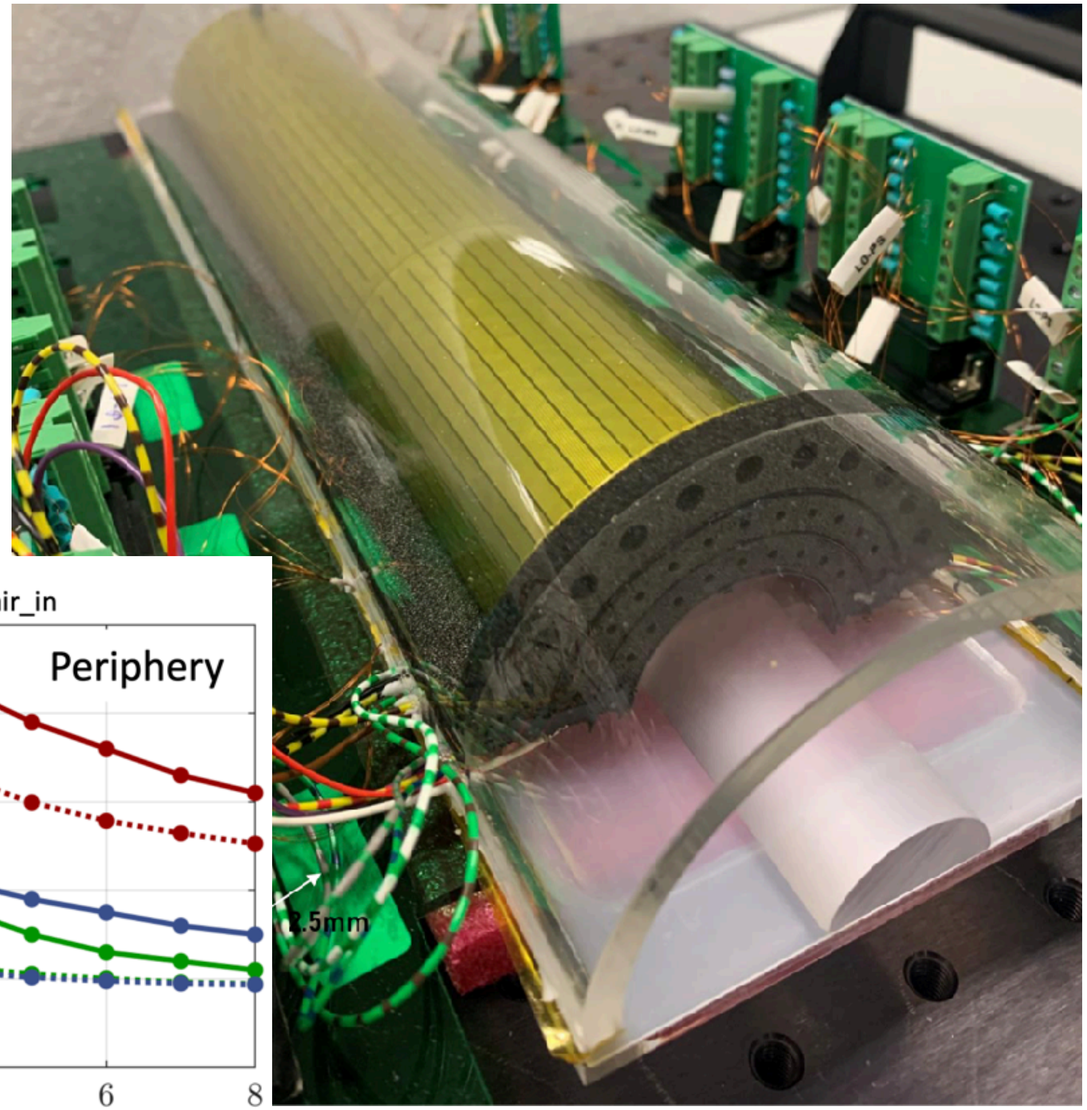
3-layer integration successful!

R&D on air cooling

- A set of bread board models based on heating elements are being developed
- Placed in a custom wind tunnel, thermal and mechanical properties are studied

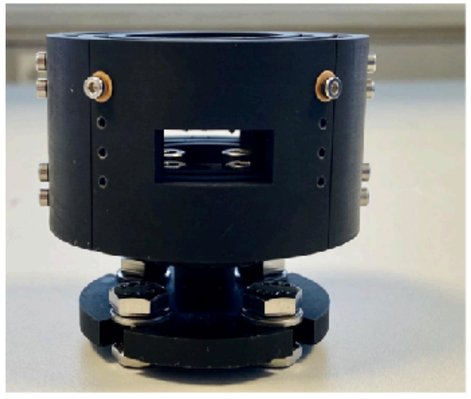


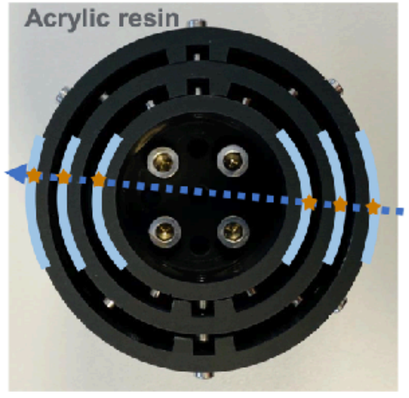


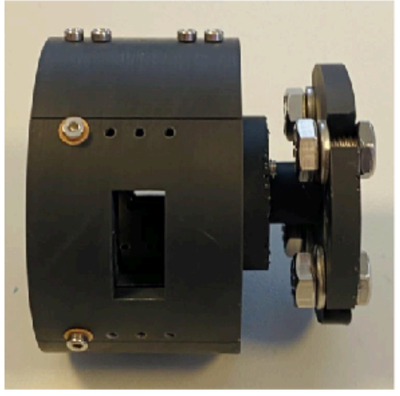


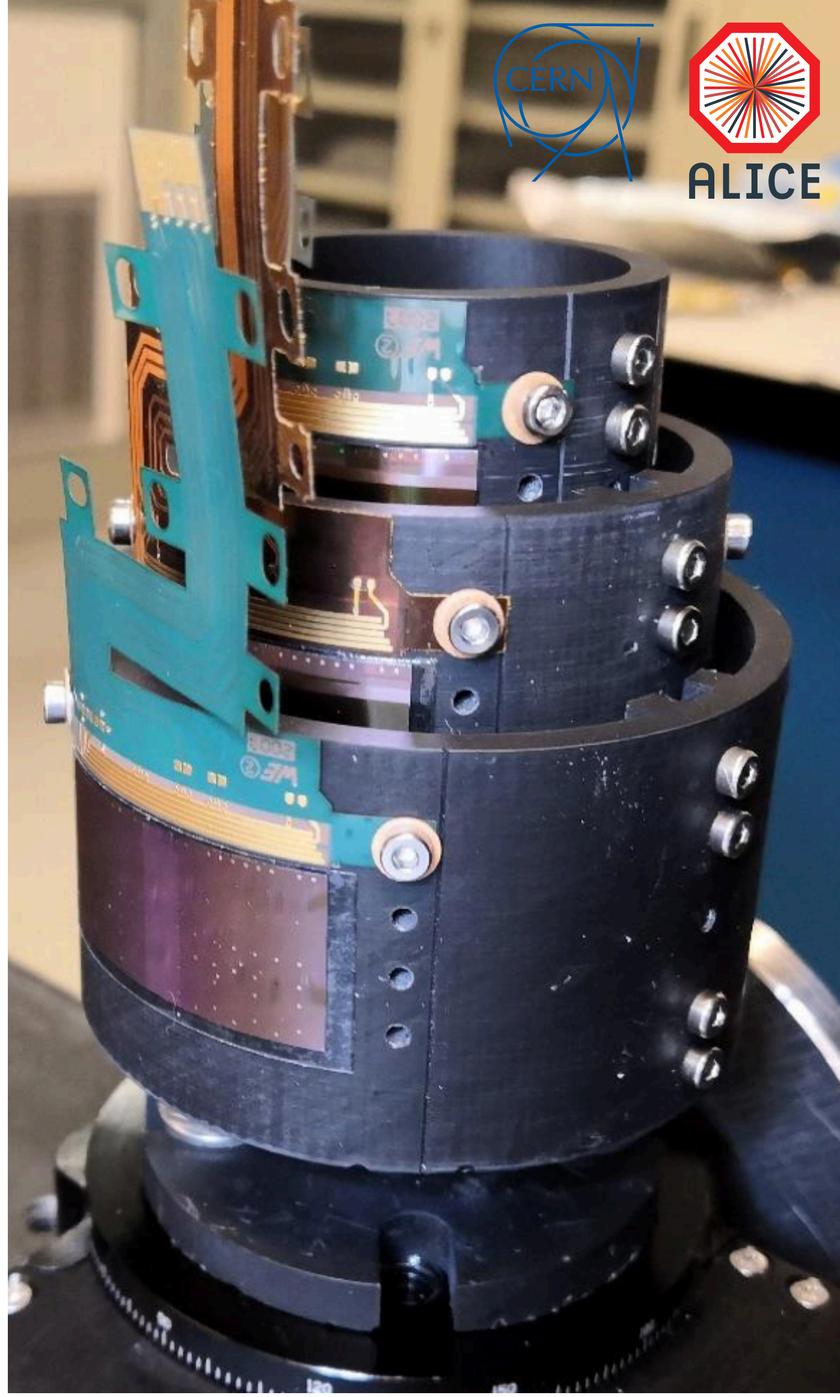
Bent ALPIDEs

- A number of prototypes with bent ALPIDEs were produced
  - several different ways were explored
    (bending before bonding, or vice versa, different jigs)
  - “feeling” for handling thin silicon was gained
- By now, we have a full mock-up of the final ITS3, called “µITS3”
  - 6 ALPIDE chips, bent to the target radii of ITS3









Beam tests

1st paper doi:10.1016/j.nima.2021.166280

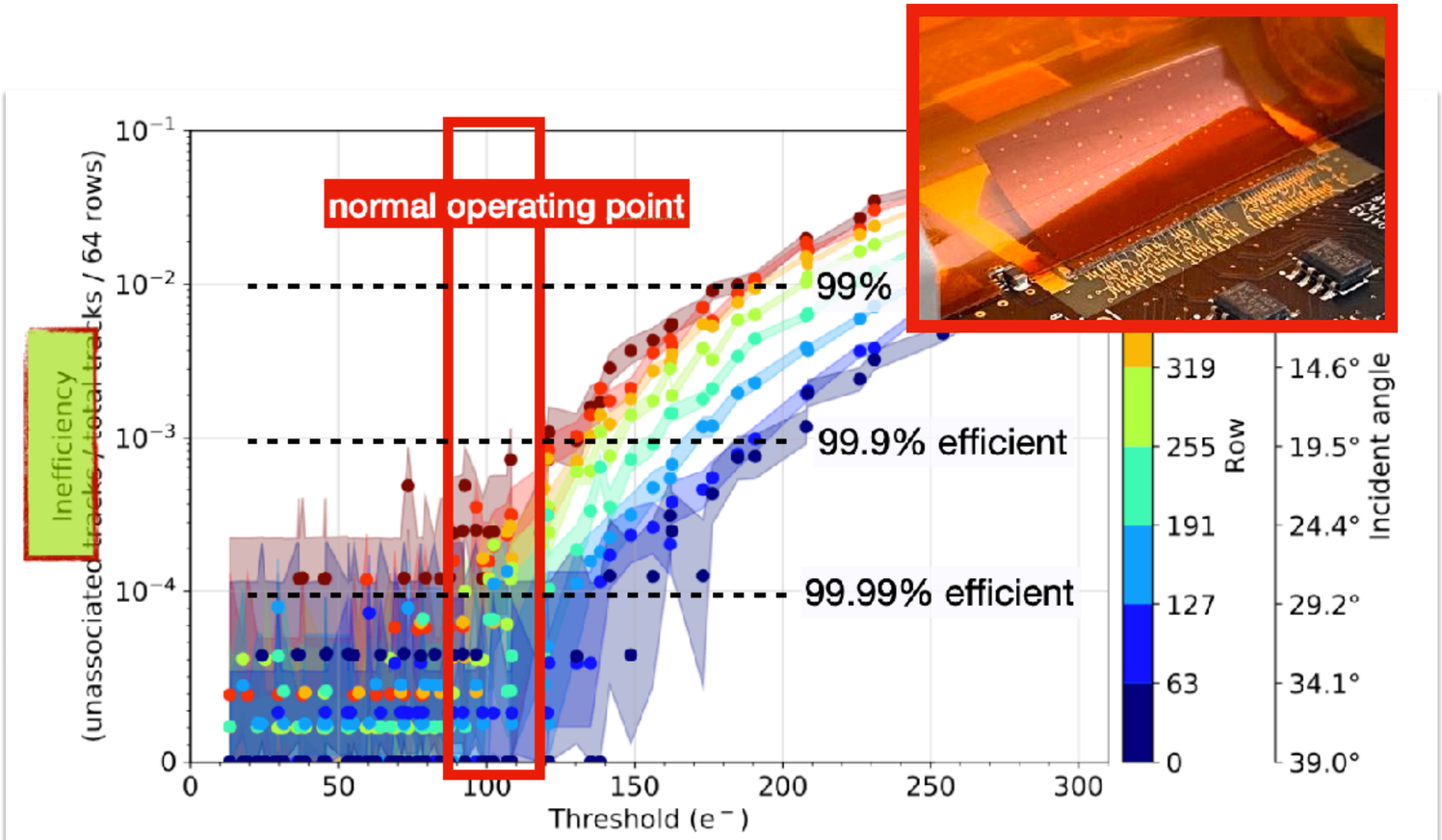


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

ELSEVIER

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

Available online 10 January 2022, 166280

In Press, Journal Pre-proof

First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS project [1]

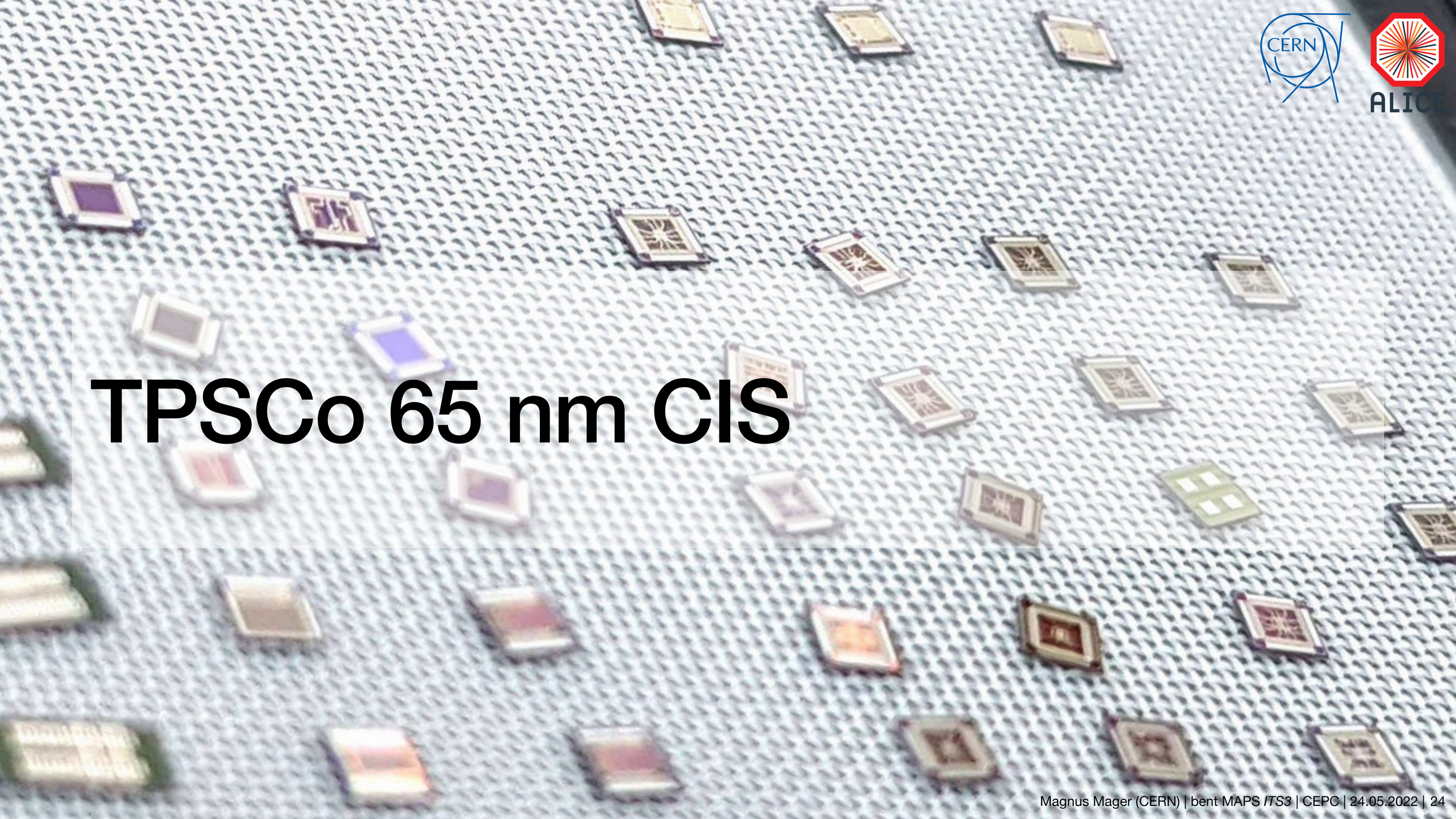
Show more

Share Cite

https://doi.org/10.1016/j.nima.2021.166280

Get rights and content

Clearly proving that bent MAPS are working!



TPSCo 65 nm CIS

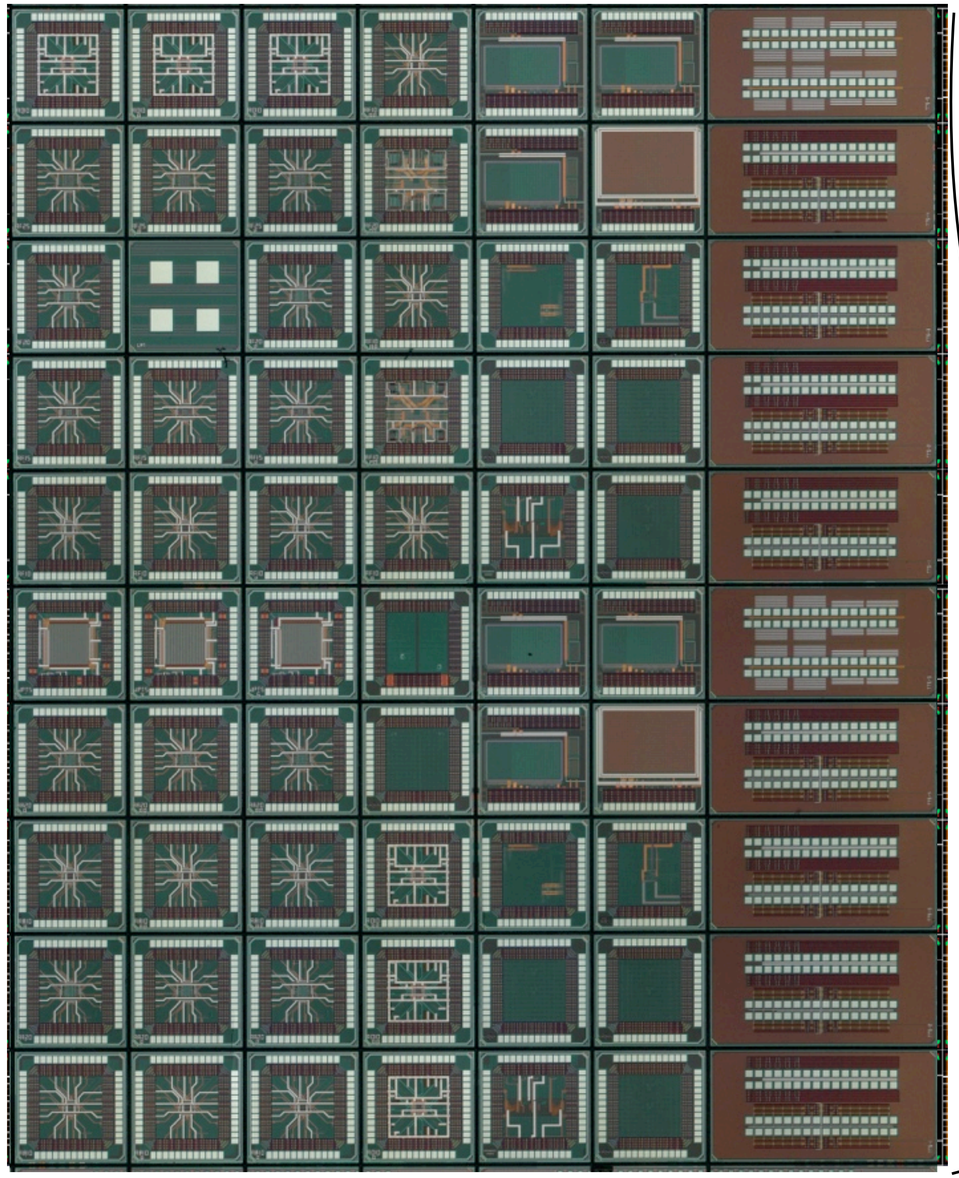
TPSCo 65 nm CIS

reasons for migration from TJ 180 nm CIS

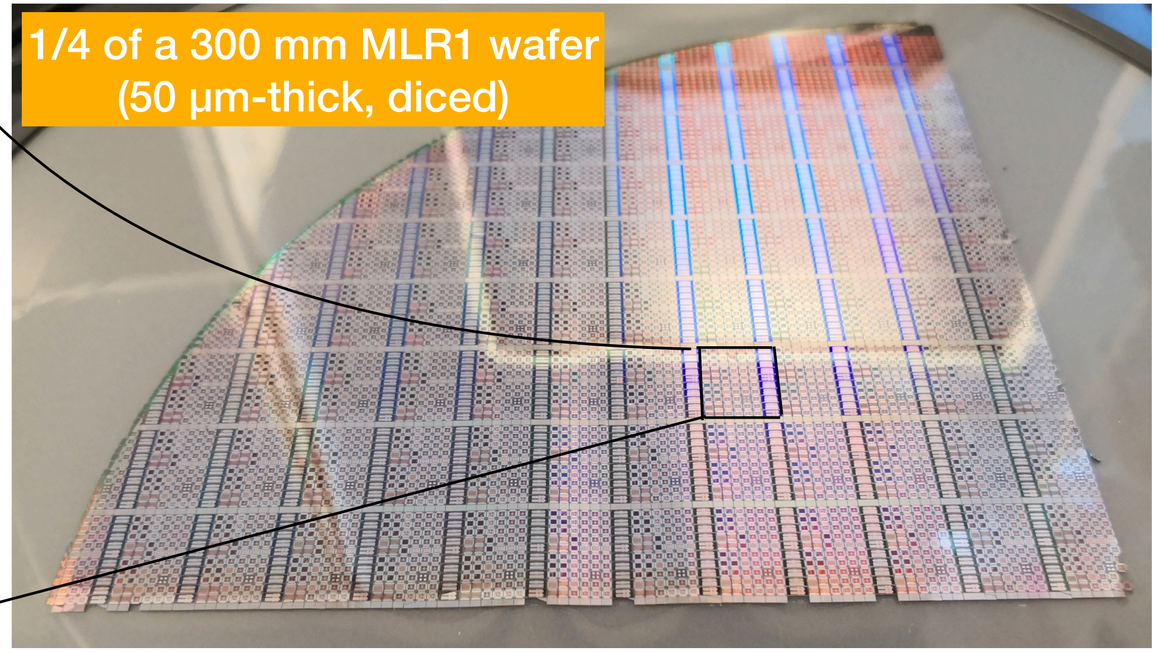
- ALICE by now long standing experience with **Tower Semiconductor** (aka “TowerJazz”), using their **180 nm** CIS process
  - we produced and tested >70k sensors for ITS2
  - we optimised the process together with the foundry to reach full depletion (not used for ITS3, but then followed up later by several groups)

- The **65 nm** CIS of **Tower Partners Semiconductor (TPSCo)** offers:
  - l**arger wafers:** 300 mm instead of 200 mm, single “chip” is enough to equip an ITS3 half-layer
  - **smaller structure sizes:** *potentially*
    - lowering power consumption
    - increasing spatial resolutions
    - increasing in-pixel circuitry
    - increasing yield

First submission in TPSCo 65 nm CIS



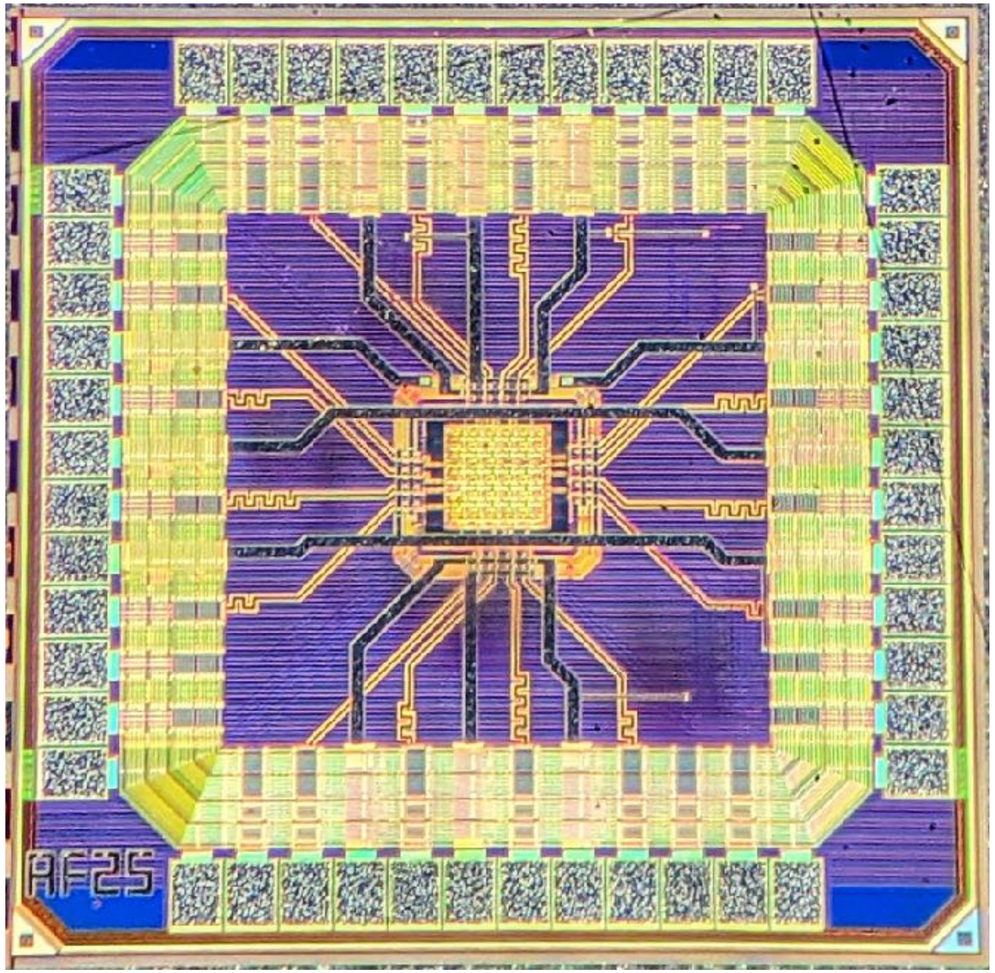
- Submission together with CERN EP R&D WP 1.2
  - contains many test chips (transistor test structures, DACs, analog pixel matrices, digital pixel matrices, …)
- Fully processed wafers available since summer 2021
- Chips are now thinning/diced/picked in large quantities
- Tests are ongoing at several institutes and groups



Analog Pixel Test Structure (APTS)

overview

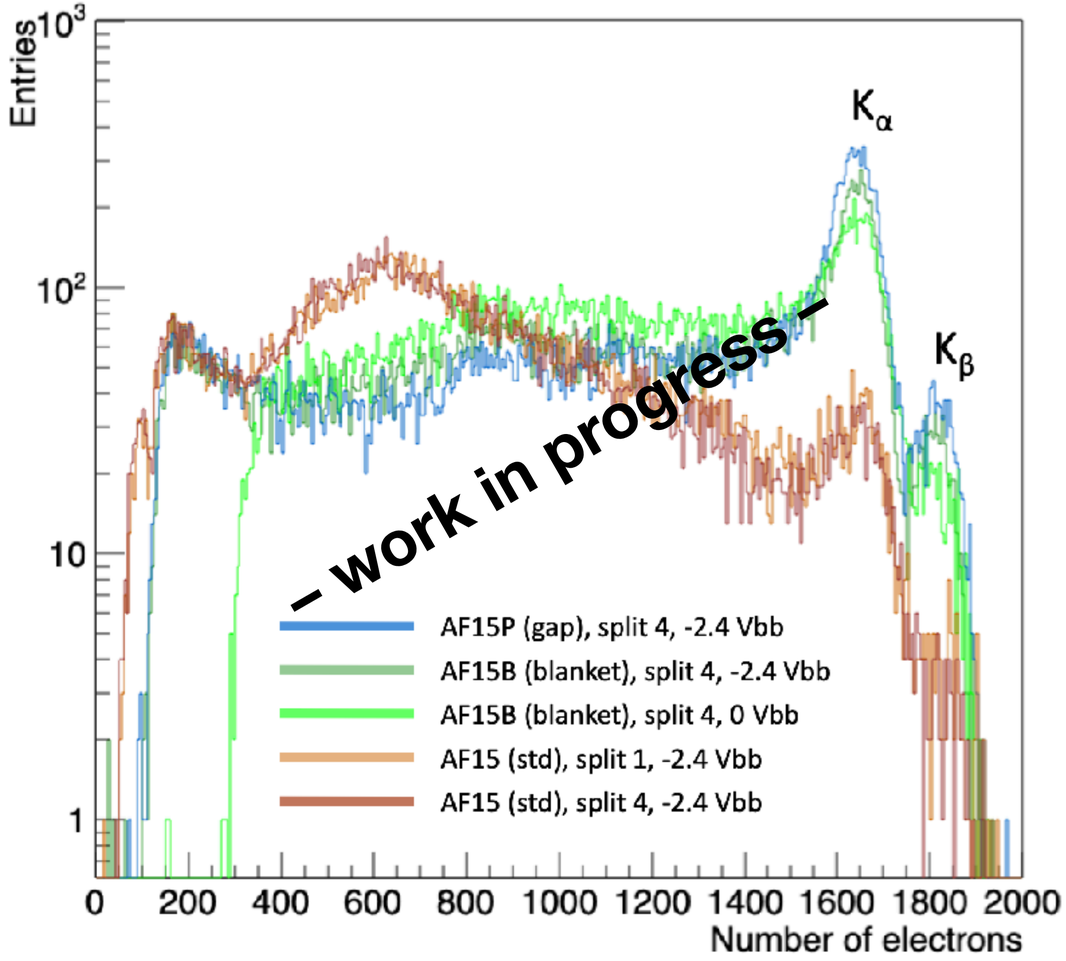
- The analog pixel test structure (APTS)
  - 6x6 pixels (central 4x4 read out)
  - different pitches: **10, 15, 20, 25 µm**
  - different implant geometries
  - different output drivers
- Allows for very detailed mapping of parameters space
  - important e.g. in view of larger pixels
  - also key to verify and tune simulation models



APTS lab results

process optimisation: charge collection/sharing

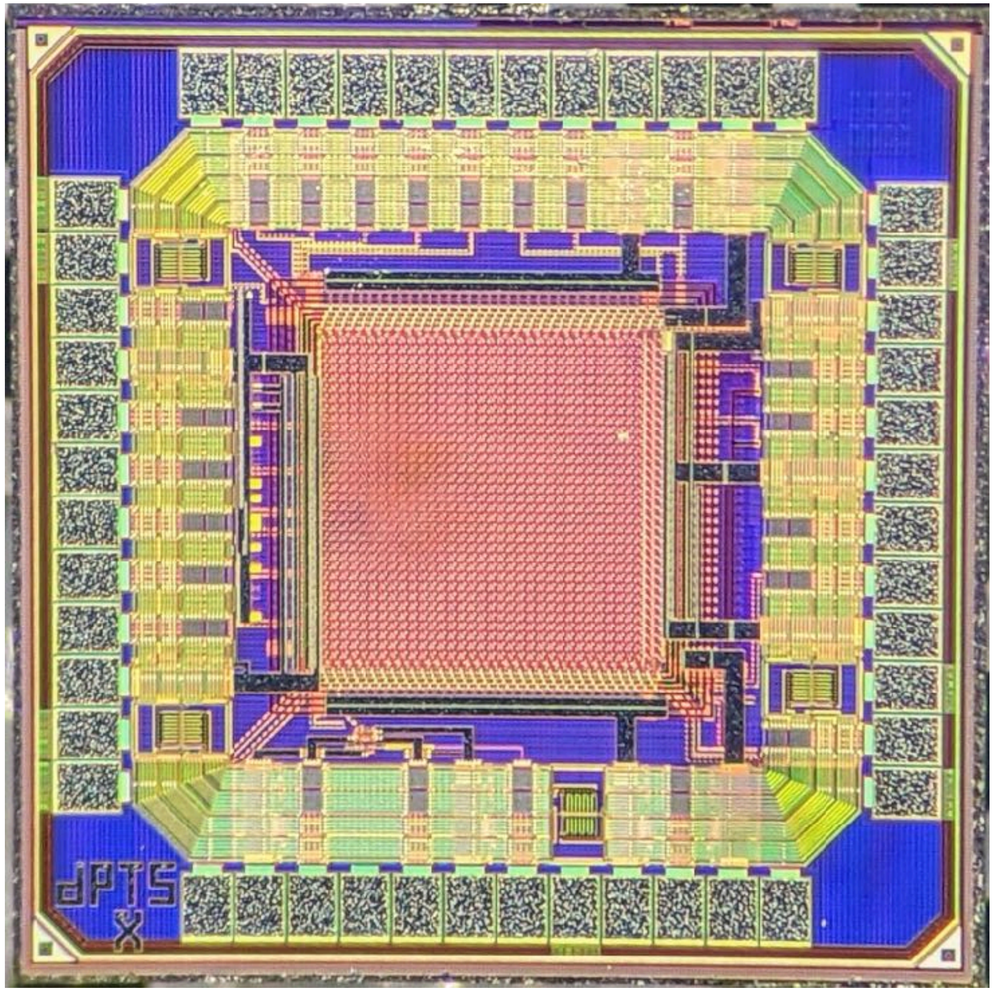
- Already in the first run in 65 nm process modifications were done together with the foundry
  - excellent collaboration with the foundry
  - this took several years in the 180 nm
- This allows to engineer/tune the charge charing and collection times to some extent
- A detailed study will allow to choose the best trade-off for the vertex detector, outer tracker



Digital Pixel Test Strucutre (DPTS)

overview

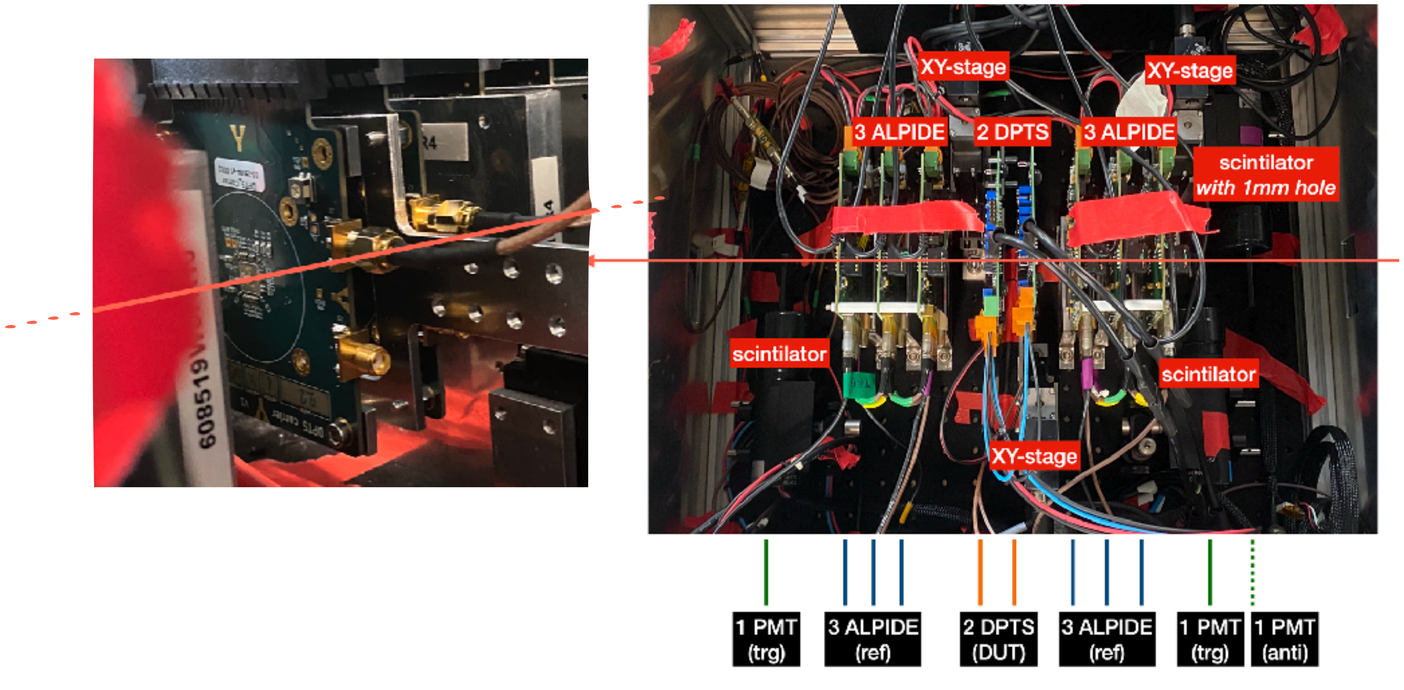
- The digital pixel test structure (DPTS)
  - 32x32 15 µm pitch pixels
- Includes full digital front-end and readout
- Studied now in detail, shows excellent performance parameters (**preliminary**):
  - Efficiency: >99%
  - Time resolution: O(10ns)
  - Radiation hardness: OK for ALICE
  - Spatial resolution: O(3-4 µm)
- Silicon-proven building block for larger chips!

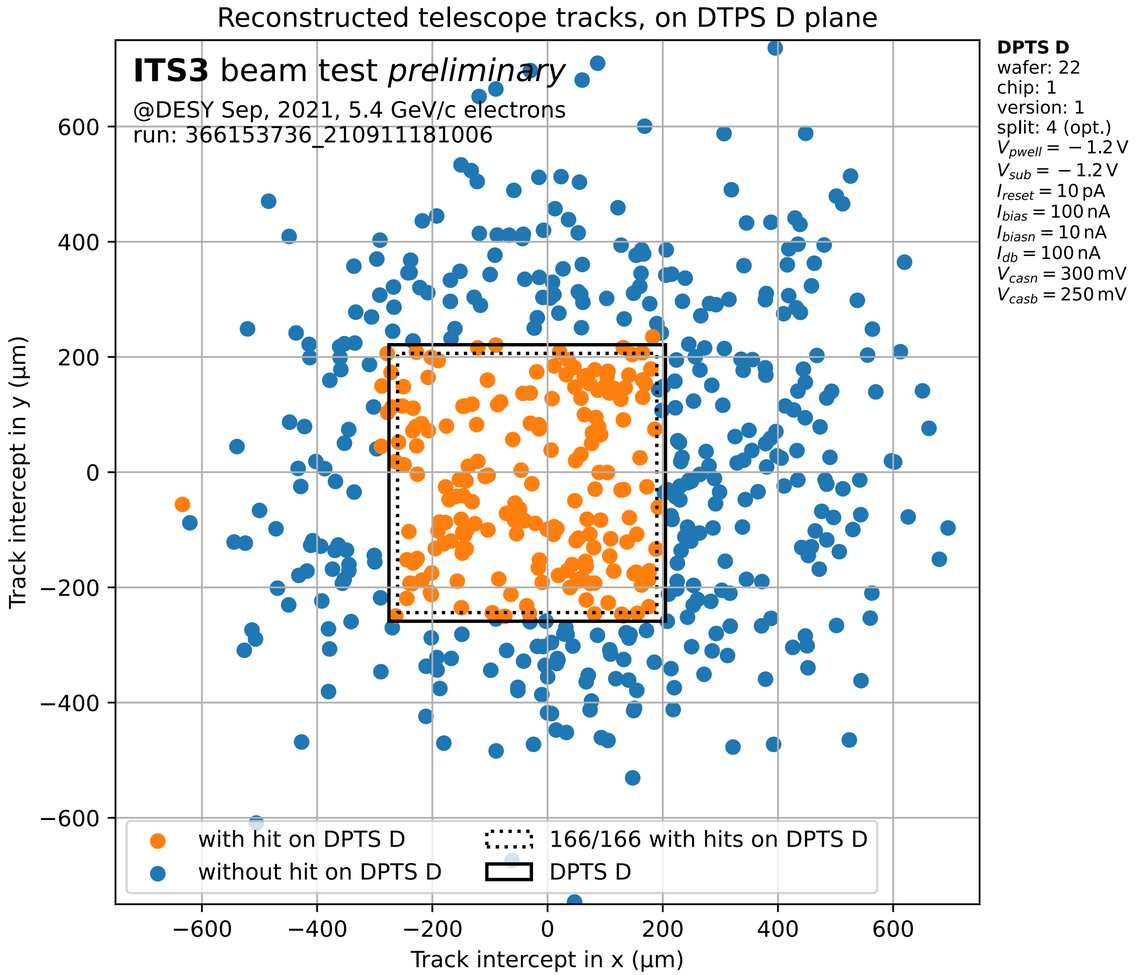


DPTS test beam results

detection efficiency

- 100% detection efficiency at first shot
- by now validated at >5 beams campaigns
- including irradiated samples (preliminary)

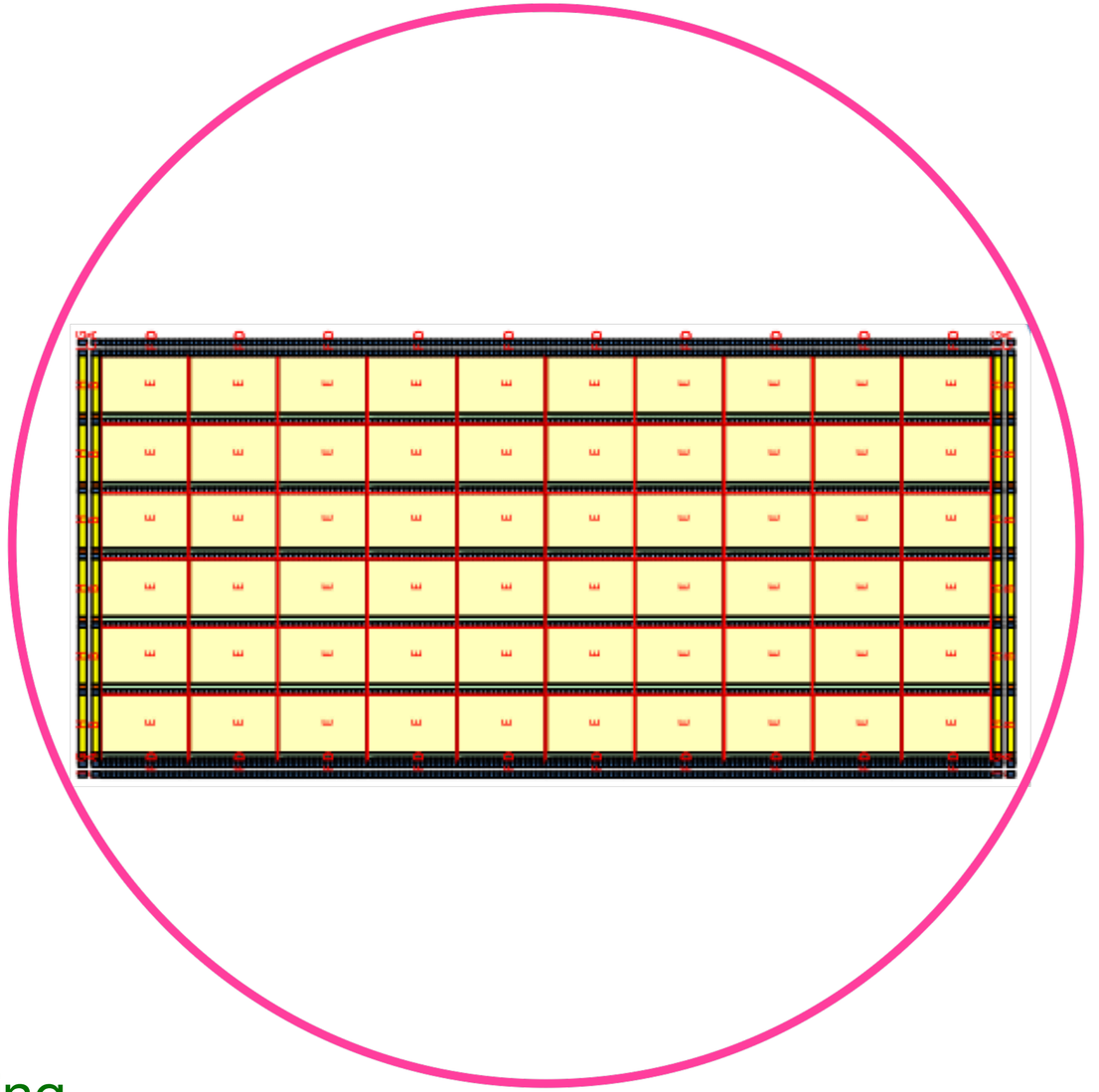




Towards the final sensor

next submission “ER1”

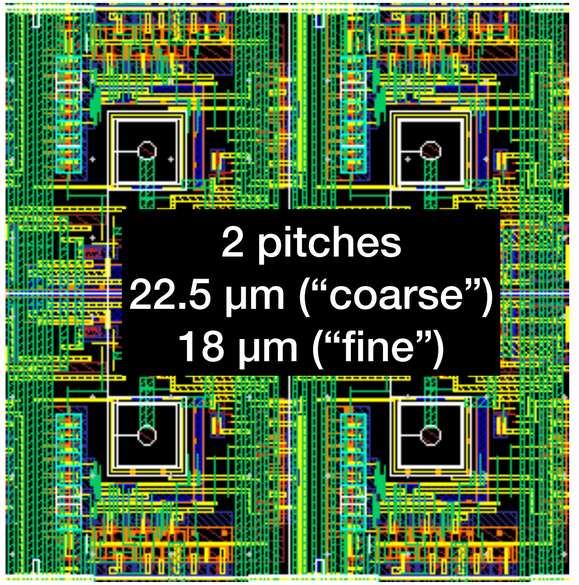
- **Floor plan** compatible with stitching worked out in close collaboration with foundry
- **Mock submission** happened Dec 2021
  - crucial step to verify stitching constraints
- **Designs** (ITS3 + CERN EP R&D WP1.2) include:
  - the large **ITS3 stitching demonstrator** (“MOSS”)
  - an alternative stitching architecture (“MOST”)
  - several small chips with building blocks and pixel and radiation test structures
- Designs are converging:
  - plan to **submit** before summer 2022
- Preparations for **post-processing** and **testing** ongoing

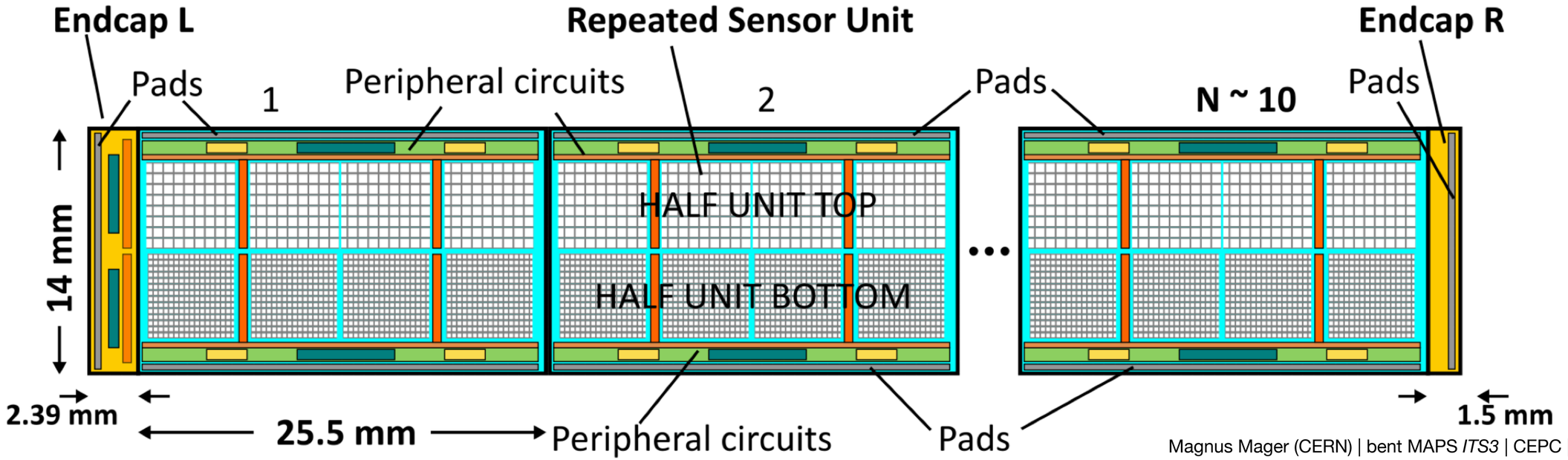


ER1

MOSS: ITS3 stitching demonstrator

- Fully functional sensor (with diodes, front-end, readout)
  - taking advantage of Si-proven parts from MLR1
  - but not integrating all building blocks and functionality of final sensor, yet
- Different densities (pitches) to study impact onto yield
- Several testing options to study voltage drops and possible defects

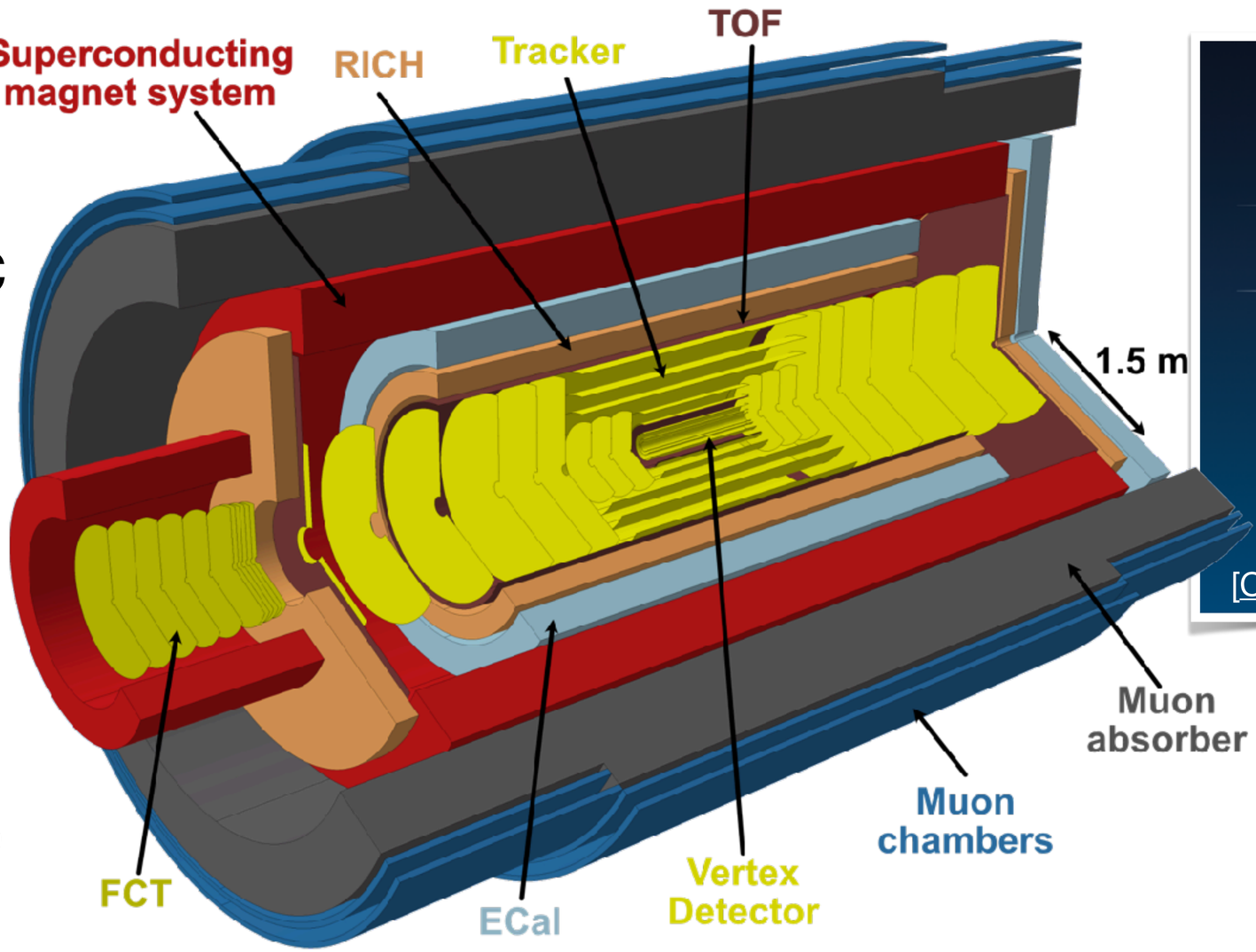


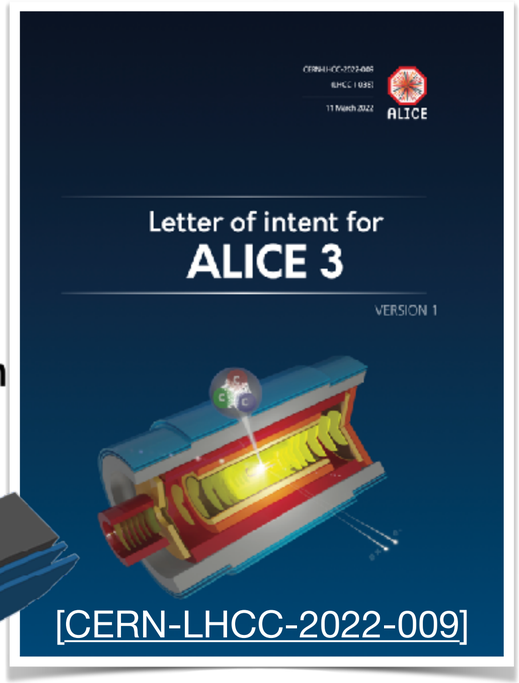


Outlook

ALICE 3

- ALICE proposes to build a completely new detector in LHC LS4 (2033-34)
- It will heavily rely on silicon detectors
- Central part:
  a 60 m² MAPS tracker
  - with **in-beampipe** vertex layers





Letter of Intent very positively evaluated by LHCC → R&D programme ramping up!

Summary

- **ALICE** has a history in developing MAPS and will continue to do so:
  - **ITS2** (10 m^2, 12.5 GPixel) is installed and taking data
  - R&D for **ITS3** is ongoing and well on track
  - **ALICE 3** will scale the effort up by another order of magnitude
- Requirements for a **Lepton Collider** are very similar to those for ALICE **ITS3**
  - ITS3 can be seen as the demonstrator/prototype/concept detector for lepton facilities
  - even better: ITS3 will be a real full-scale detector facing and addressing integration issues
- Very **exciting times** for MAPS are ahead of us!

Thank you!