WASA: A Low power consumption ASIC for TPC

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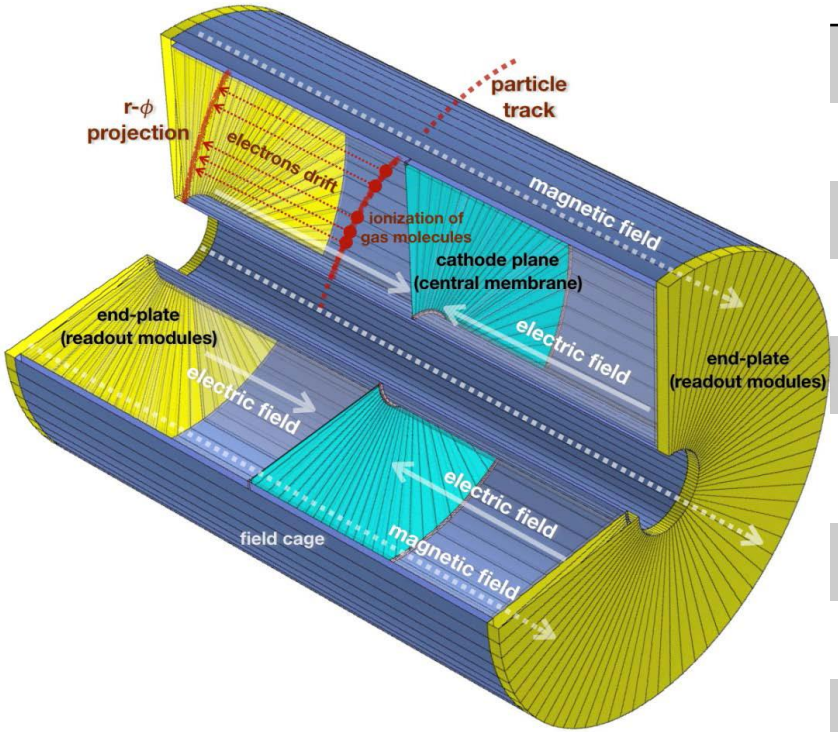
Outline

- Introduction
- The Progress of WASA V1
- The Progress of WASA V2
- Summary & Future Plan

Introduction

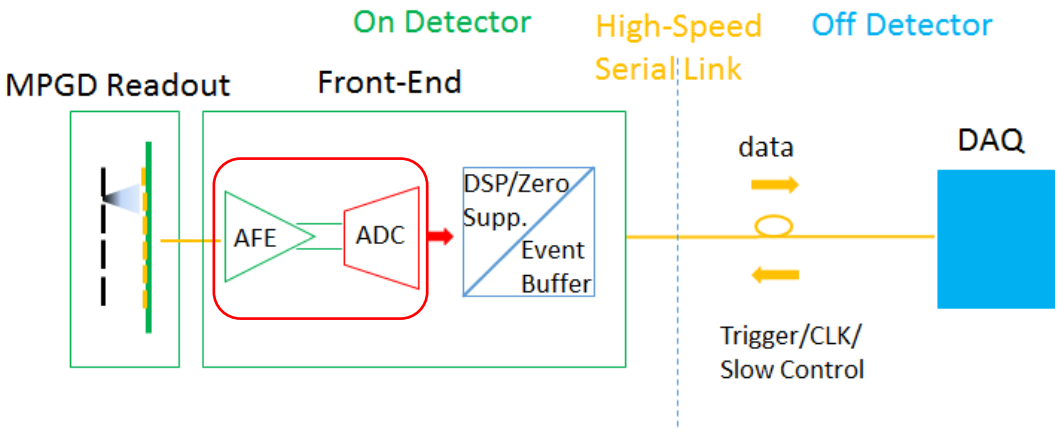


Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm × (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6mm) are needed, resulting ~1 million channel of readout electronics
- Need low power consumption readout electronics working at continuous mode

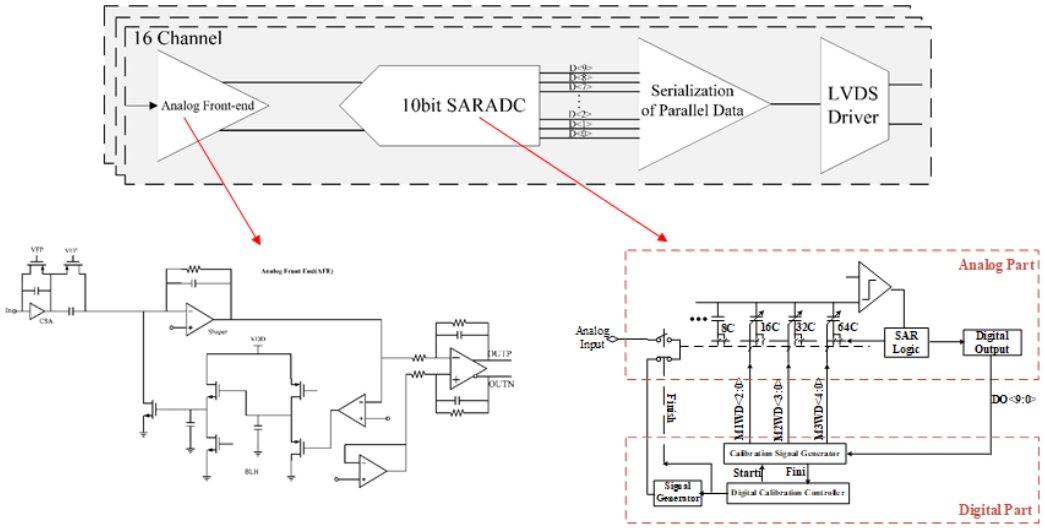
Chip Architecture

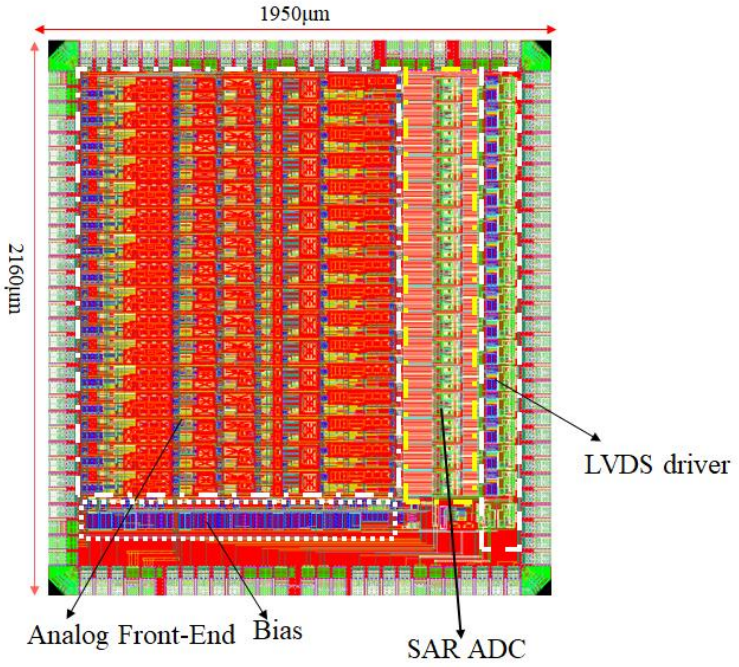
- In order to reduce the power consumption:
  - Using more advanced 65 nm CMOS process favoring digital logics
  - Reducing analog circuits:
    - CR-$(RC)^n$ →CR-RC, moving high order shaping to digital domain
    - ADC structure : pipeline → SAR (Successive Approximation Register)



WASA: WAveform SAmpling FE ASIC for TPC

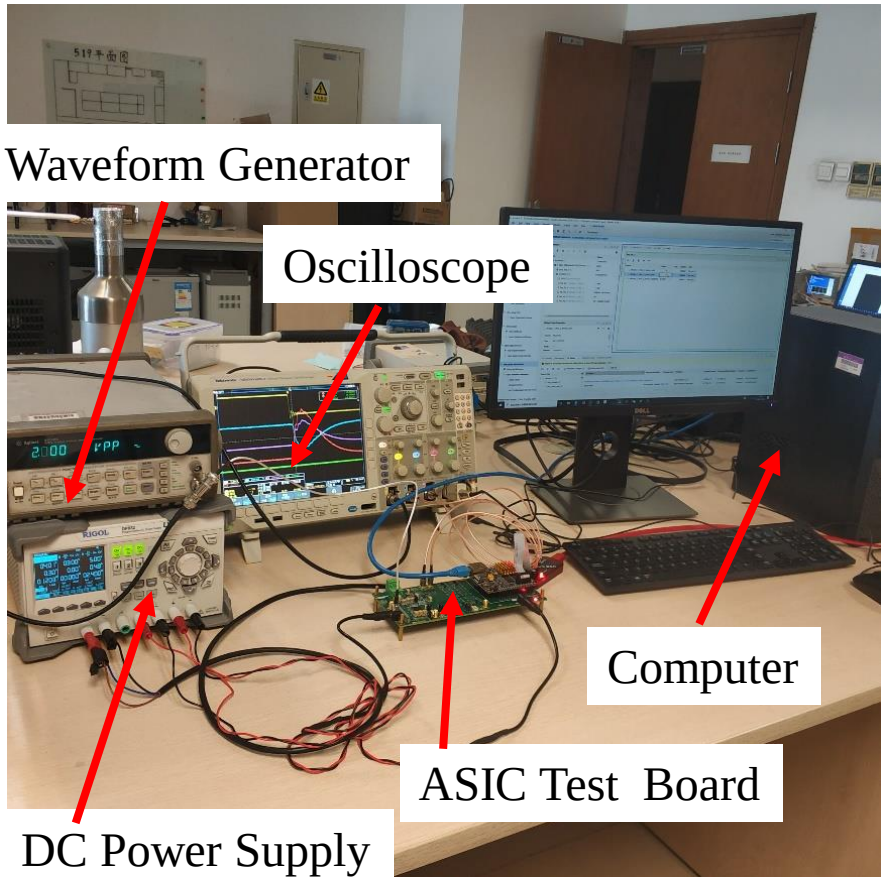
- WASA V1 :
  - 16 channel AFE+ADC+LVDS data output
  - The Power consumption: AFE in 1.4 mW/ch and ADC in 1 mW/ch
  - Die size in 1950 μm x 2160 μm
  - Submitted in Dec, 2019



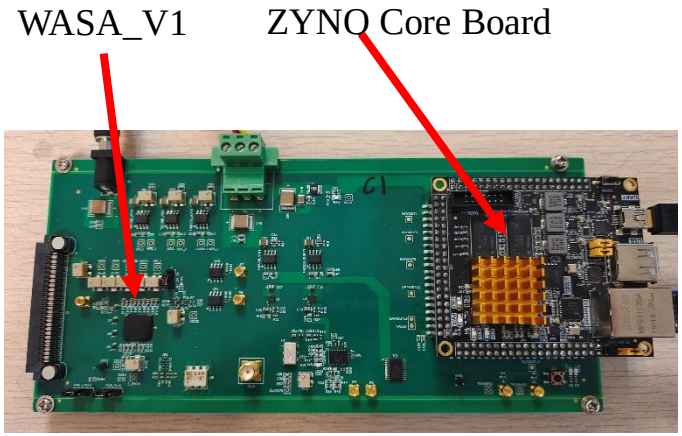


Test Setup

- Test Setup

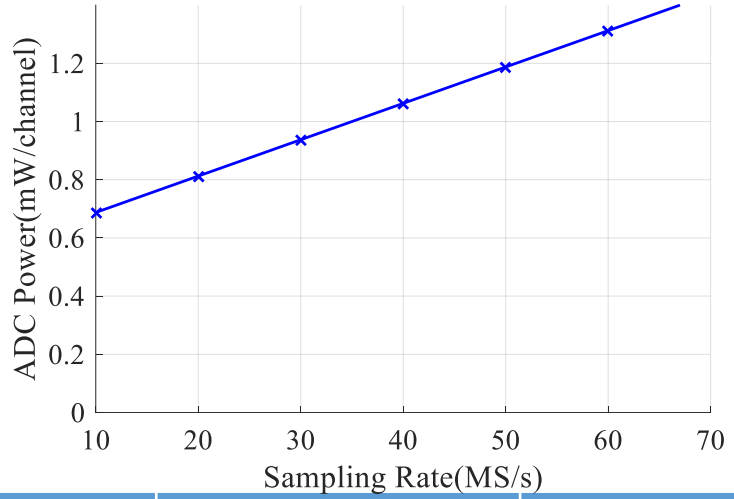


- ASIC Test Board



Test Results: Power Consumption

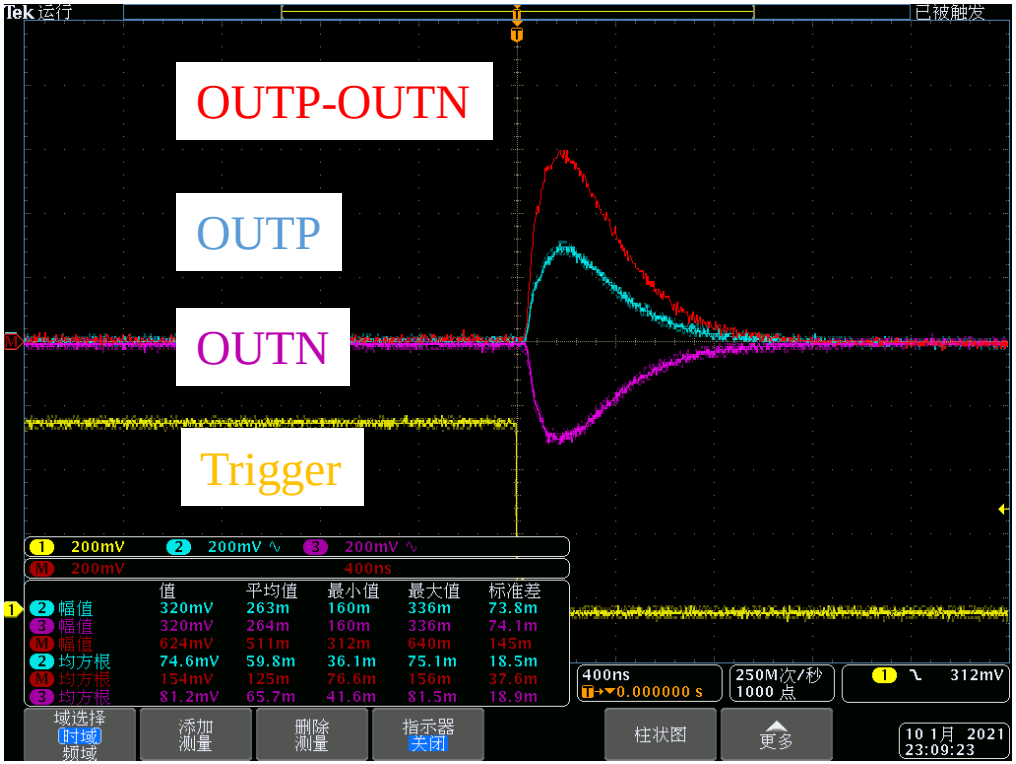
- The power consumption of the AFE: **1.43 mW/ch** (1.40 mW/ch sim.)
- The power consumption of the ADC increases as the sampling rate



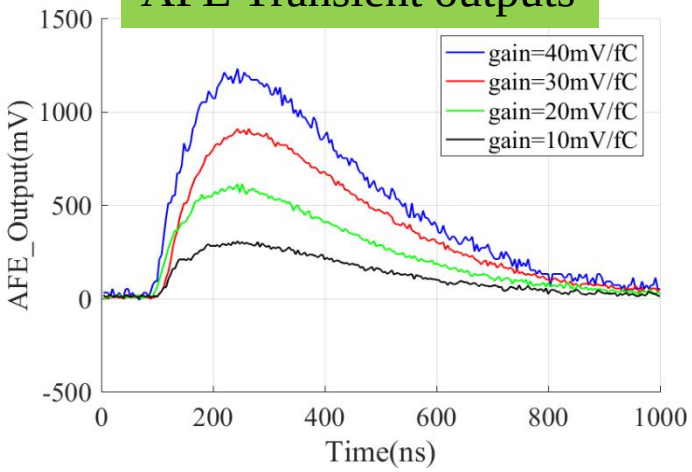
	AFE (mW/ch)	ADC (mW/ch)	Total (mW/ch)
WASA_V0 (simulation)	1.93	1.0	2.93
WASA_V0(measured)	2.02	1.0	3.02
WASA_V1 (simulation)	1.40	1.0	2.40
WASA_V1 (measured)	1.43	1.06 @40MS/s	2.49

Test Results: Transient waveforms

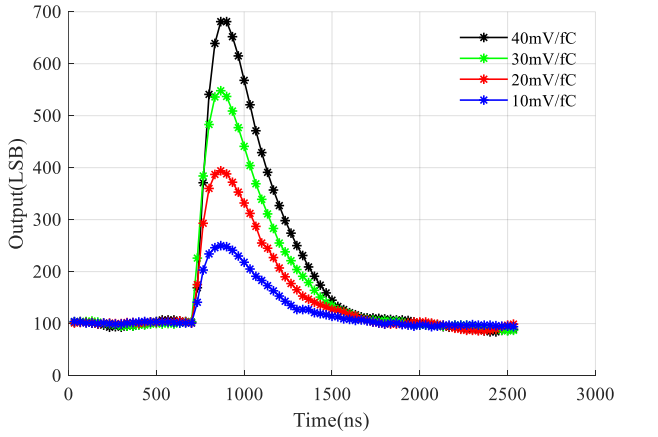
- Transient outputs
  - Differential baseline can be externally adjusted



AFE Transient outputs

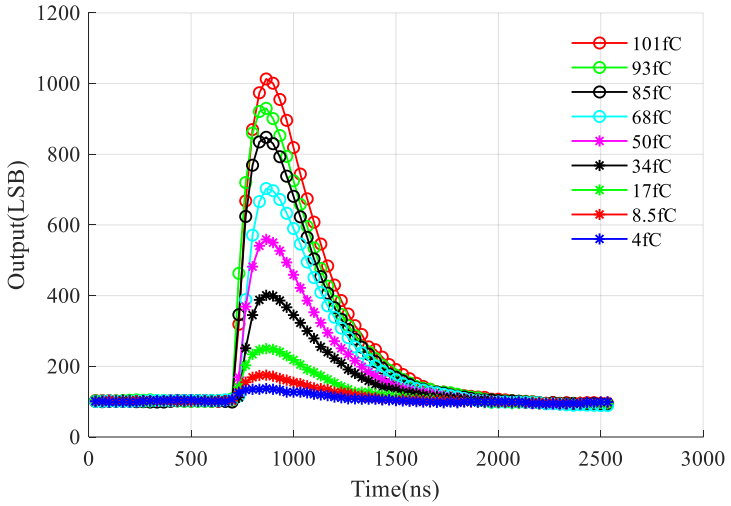


ADC Transient outputs @ 30MSPS

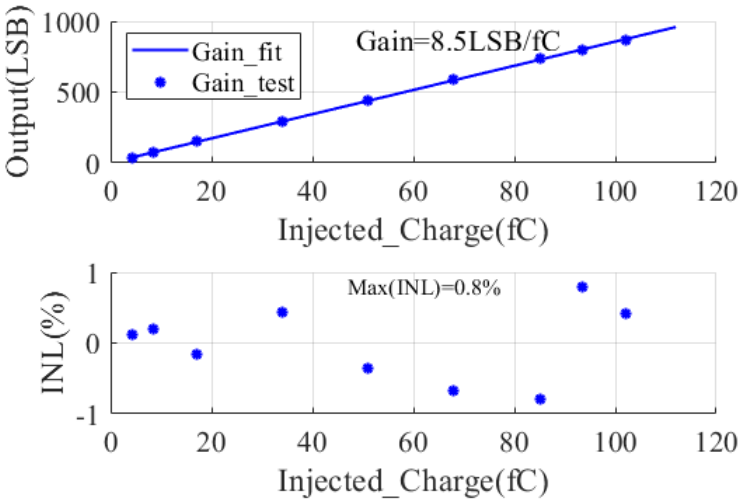


Test Results: Non-Linearity

- Transient outputs



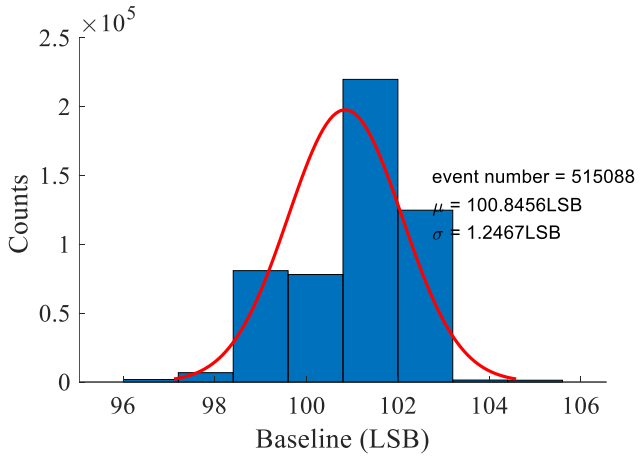
- The linearity @ gain = 10 mV/fC



Gain = 8.5 LSB/fC = 8.5 x 1.3 mV/fC = 11.05 mV/fC

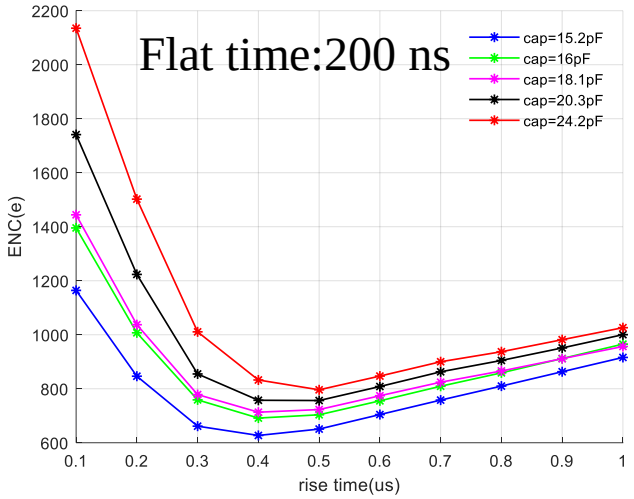
Test Results: Noise

- Baseline distribution @8.5 LSB/fC， C_{in}=15.2 pF



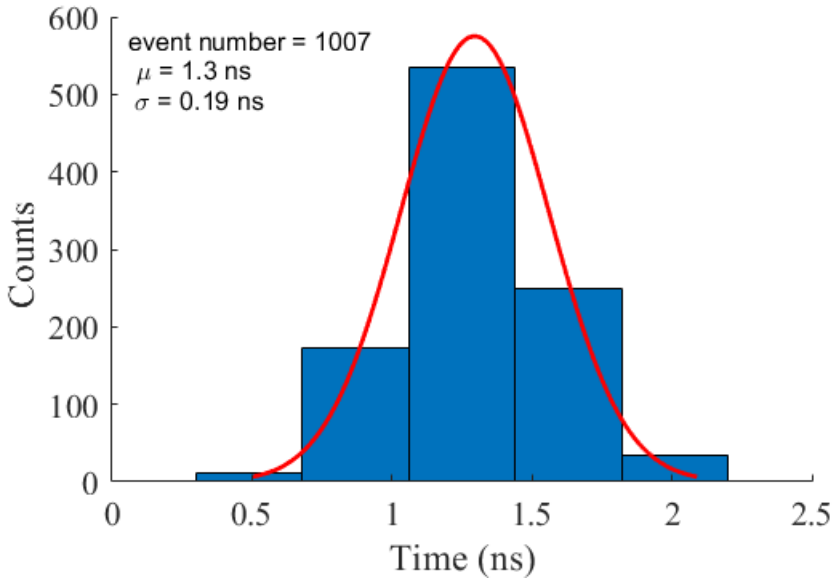
ENC:1.24/8.5*6250=911.76 e

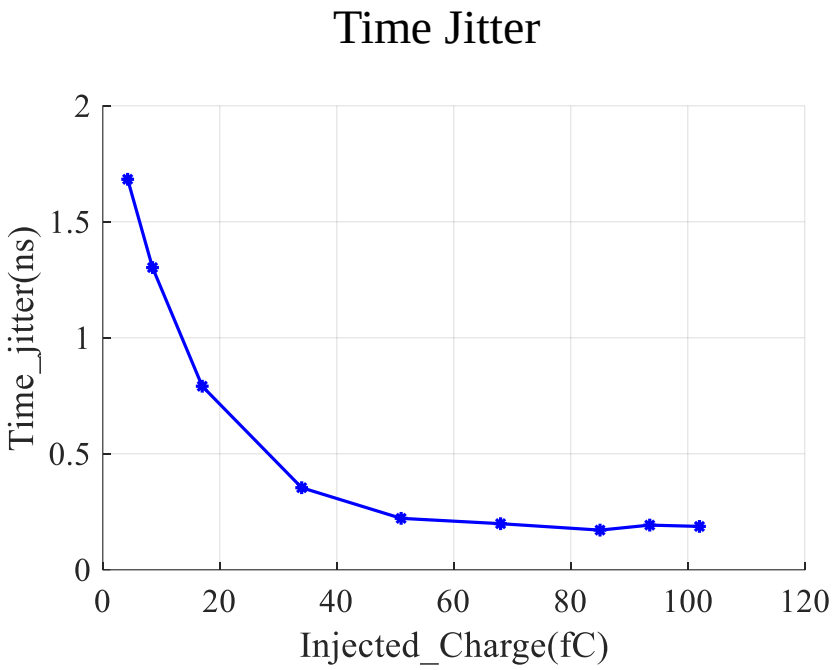
- ENC after digital trapezoidal filter in MATLAB



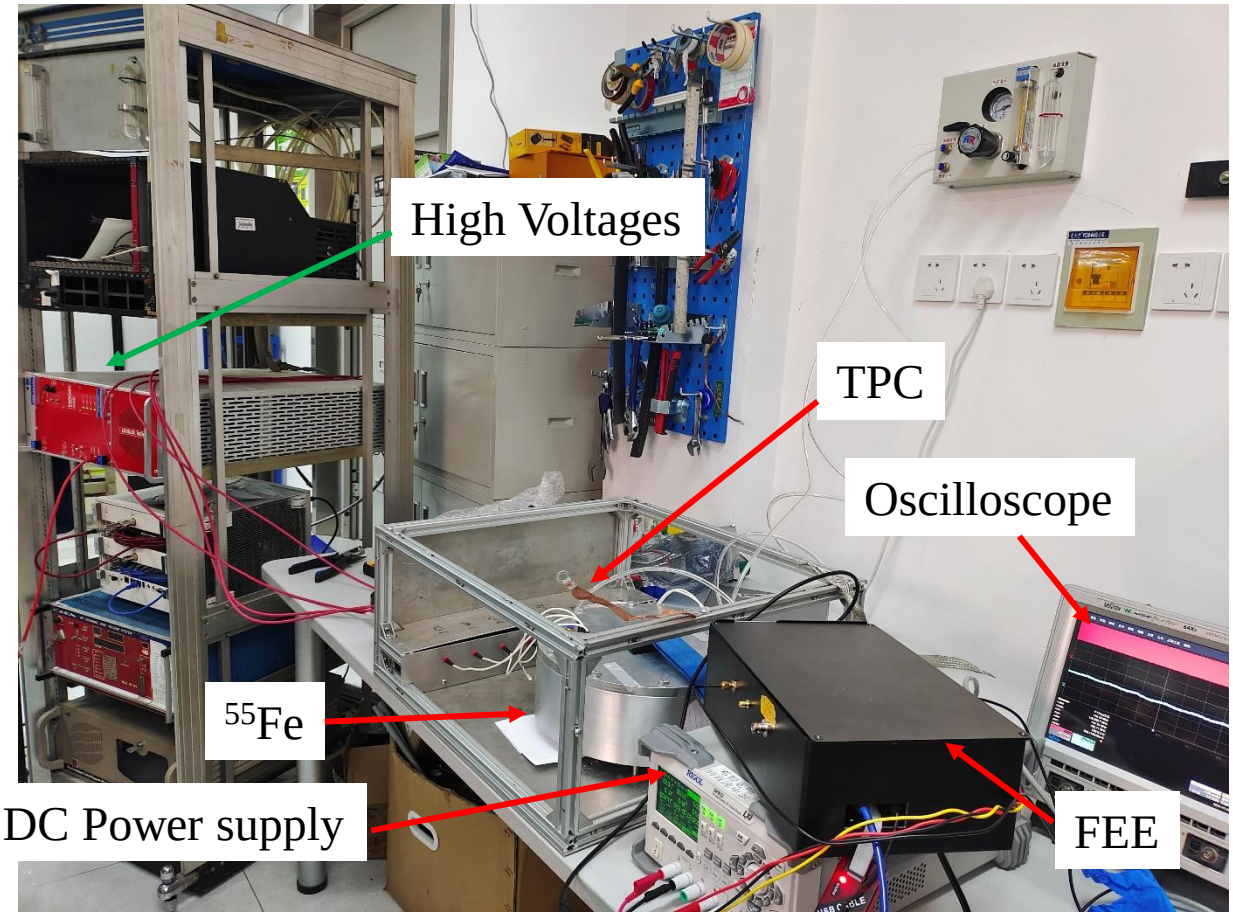
Test Results: Timing @ 30 MS/s

- Constant fraction time distribution @ Q_{in}=100 fC,10 mV/fC



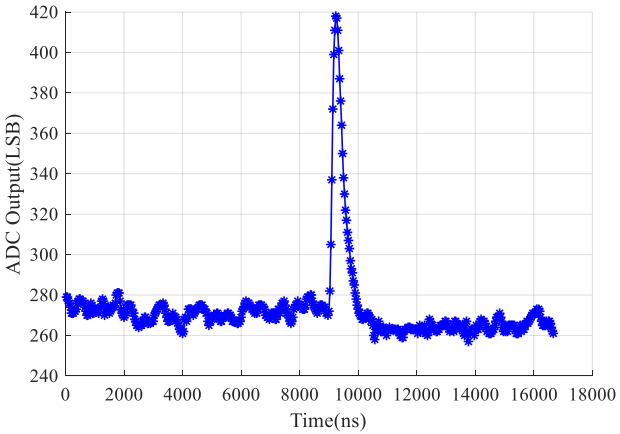


Test Results: Fe-55

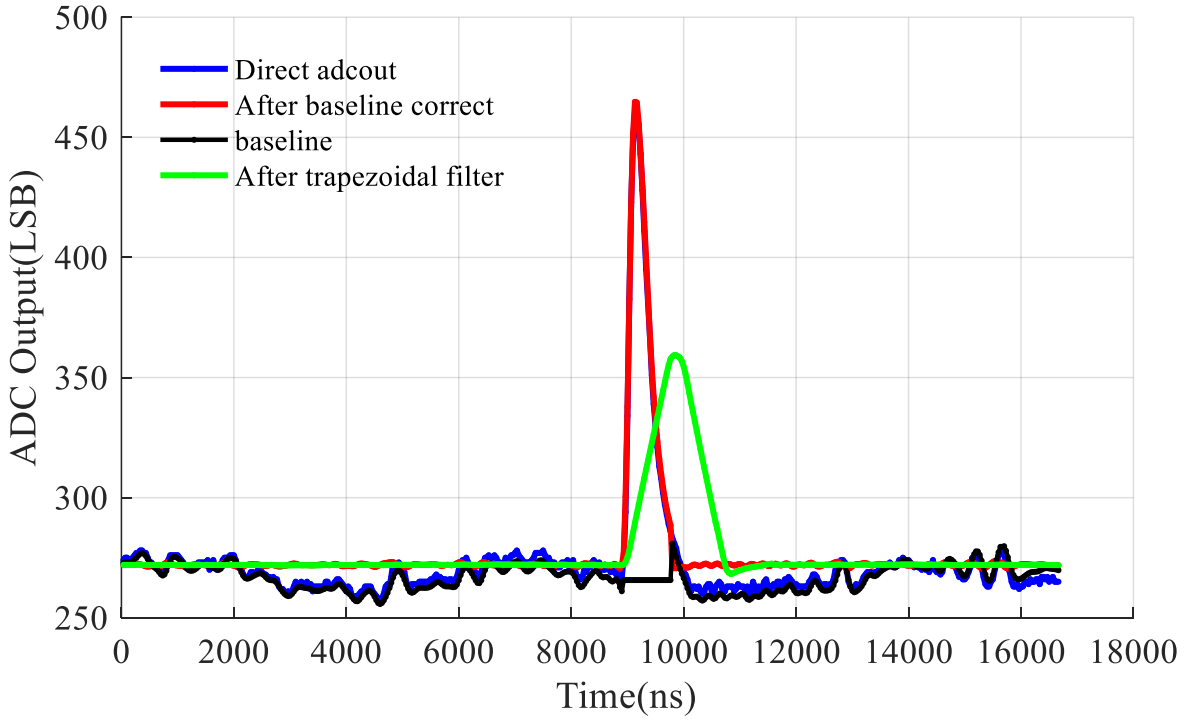


TPC Work Conditions:

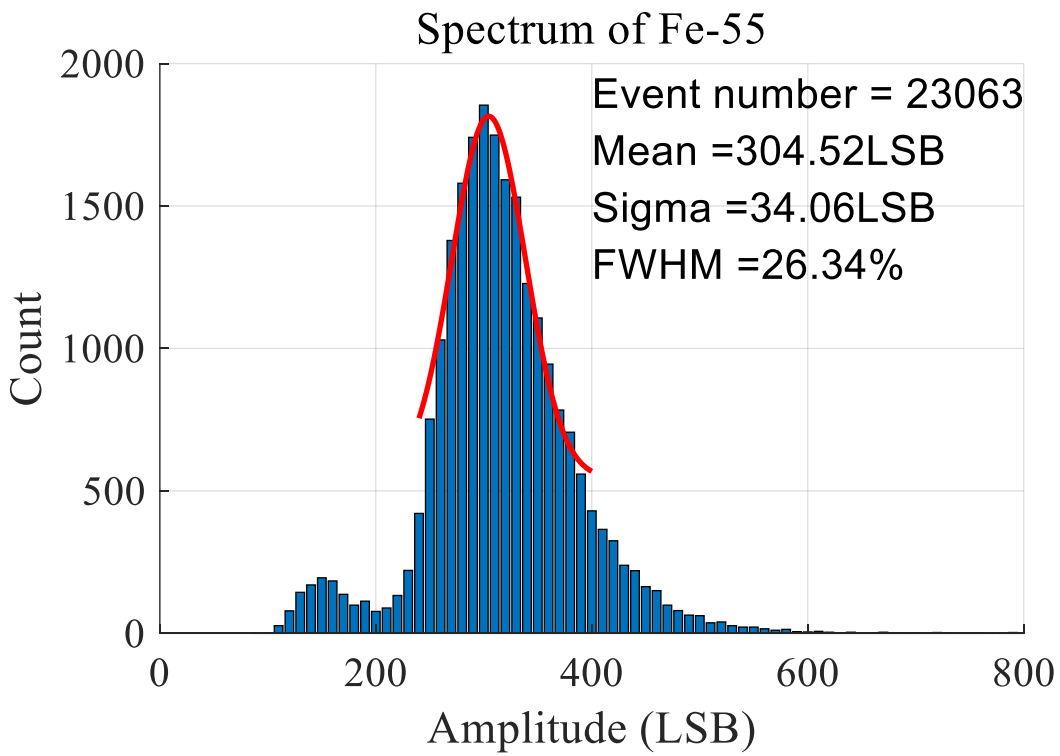
- GEM: 280 V
- Drift Field: 323 V/cm
- Gas: Ar/CF_4/iC_4H_{10} 95/3/2 (T2K)



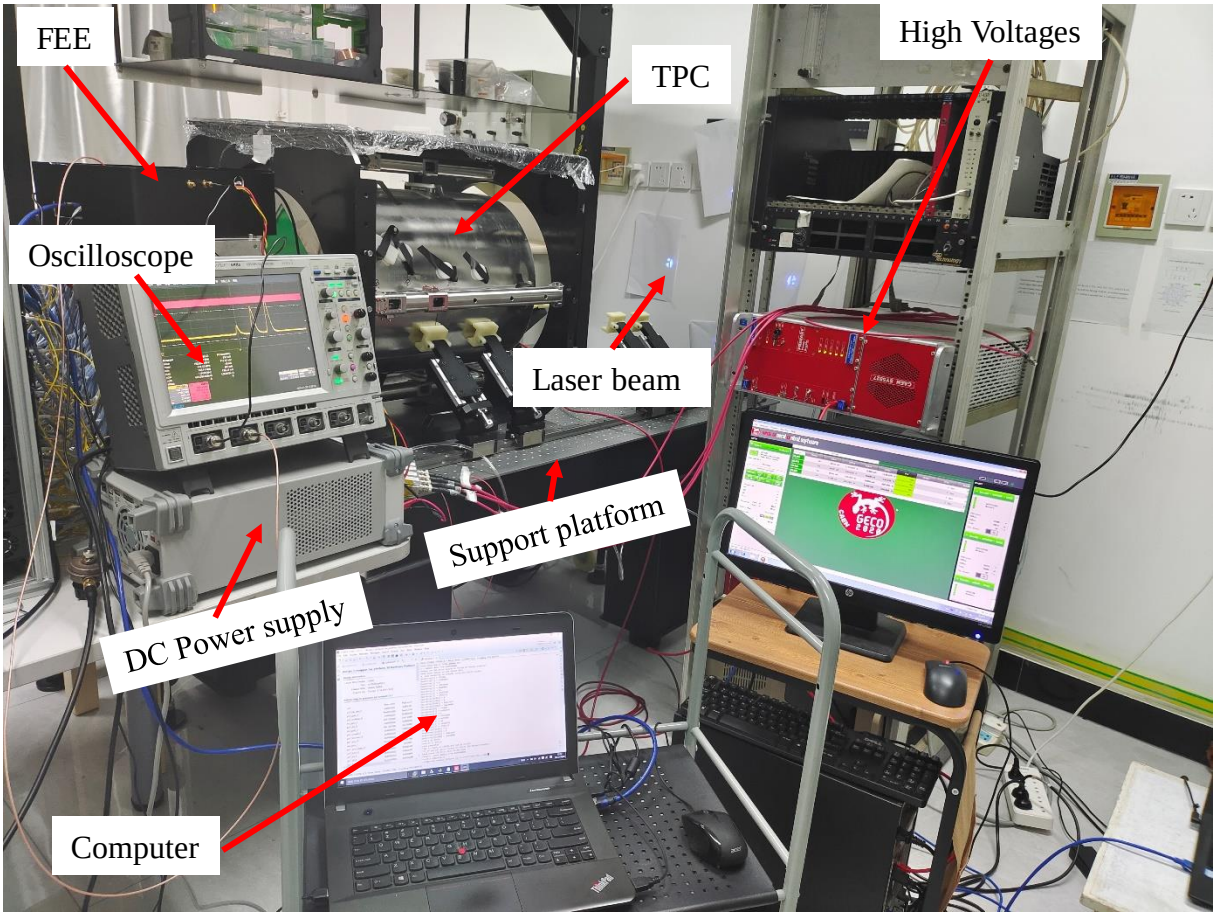
Transient Waveforms After Digital Filter



Fe-55 Energy Spectrum

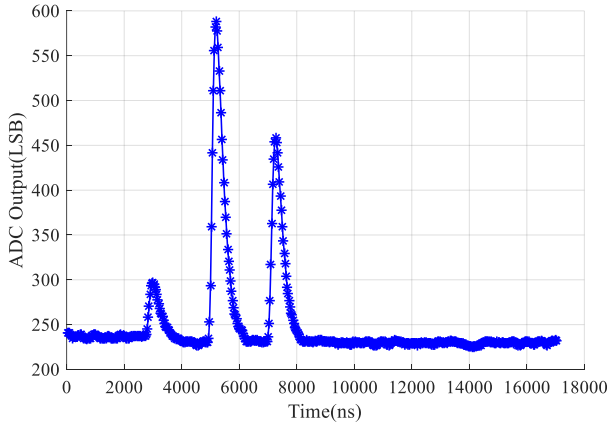


Test Results: Laser Tracks



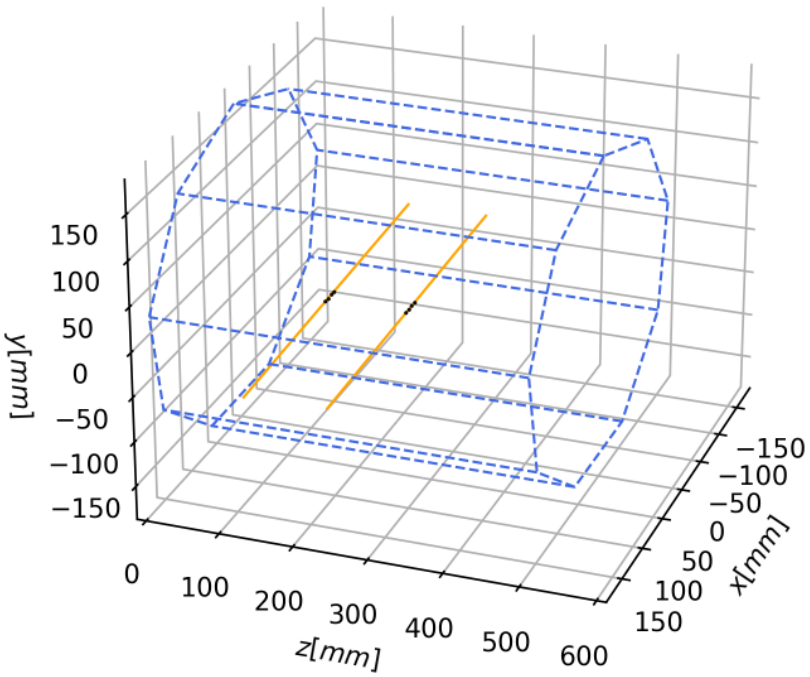
TPC Work Conditions:

- GEM: 280 V
- Drift Field: 9000 V/50 cm = 180 V/cm
- Gas: Ar/CF_4/iC_4H_{10} 95/3/2 (T2K)
- Laser: 7.2 mJ @20 Hz
- Sampling Rate: 30 MS/s

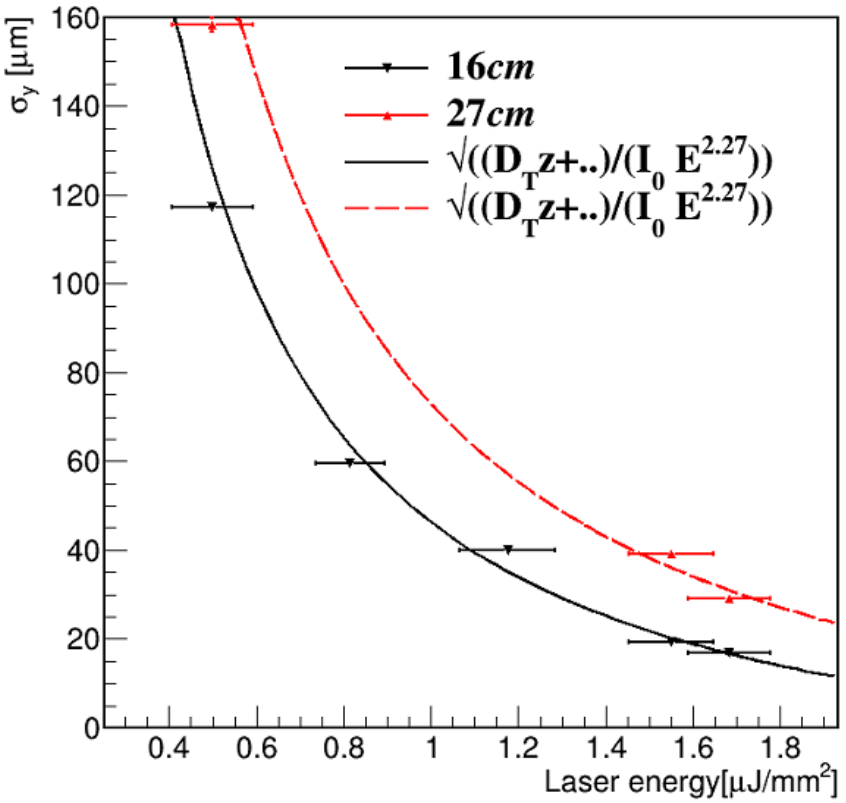


Track & Position Resolution (Preliminary)

- Laser Tracks

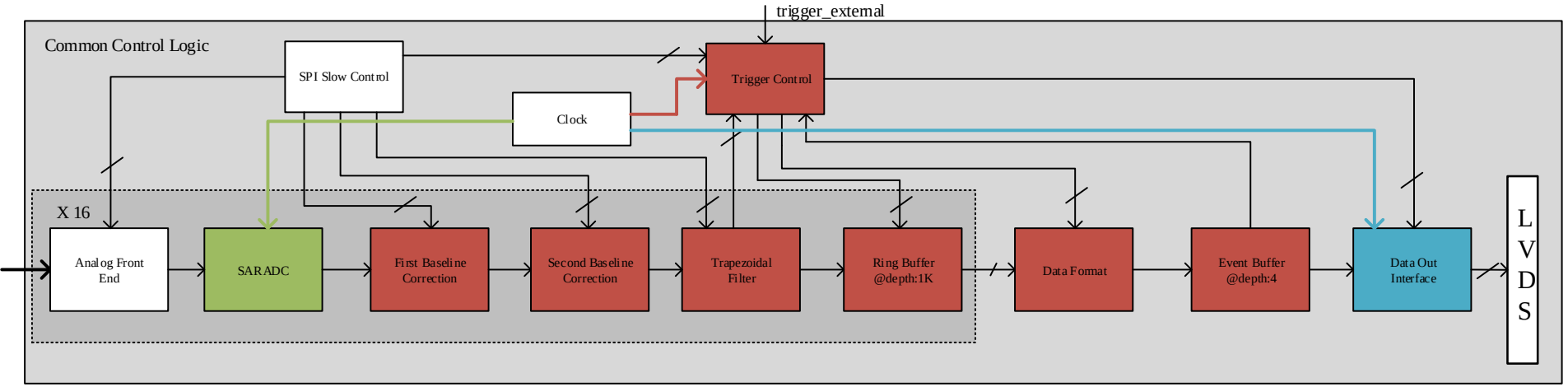


- Position Resolution

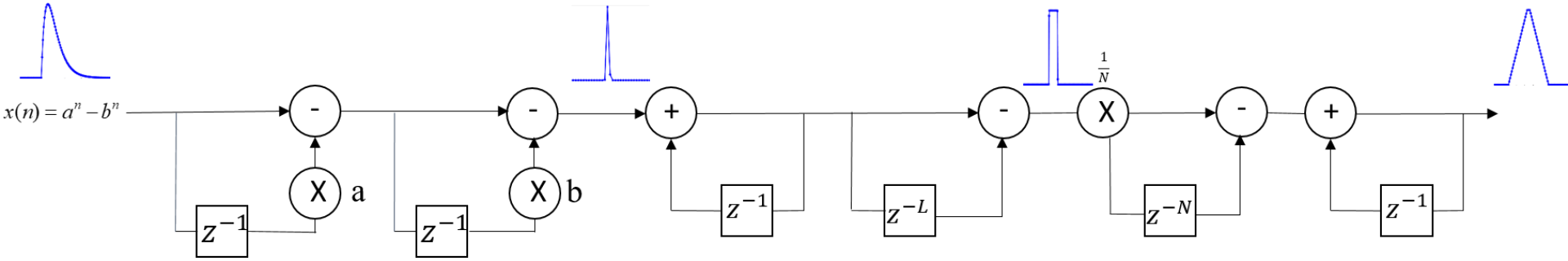


WASA V2

- Digital signal processing:
  - Two stage baseline corrections, learnt from SAMPA
  - Digital trapezoidal filter, to make pulse shape symmetric and shorter
- Trigger logics with two stage data buffer (ring buffer and event buffer)

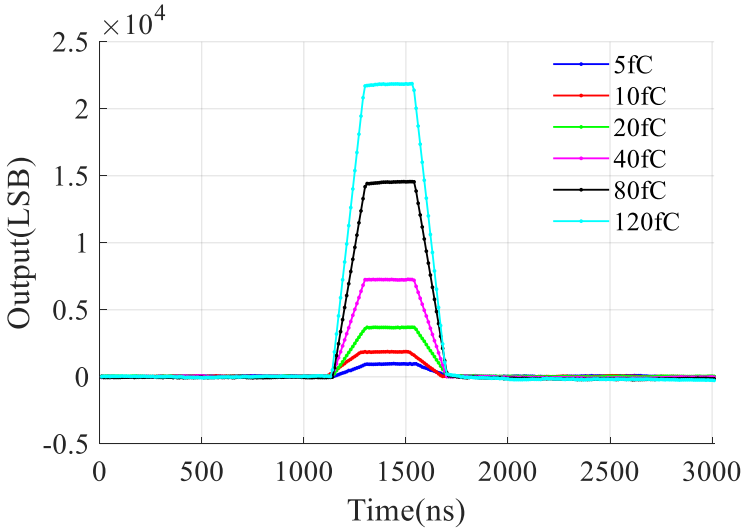


Integrated Digital Trapezoid Filter

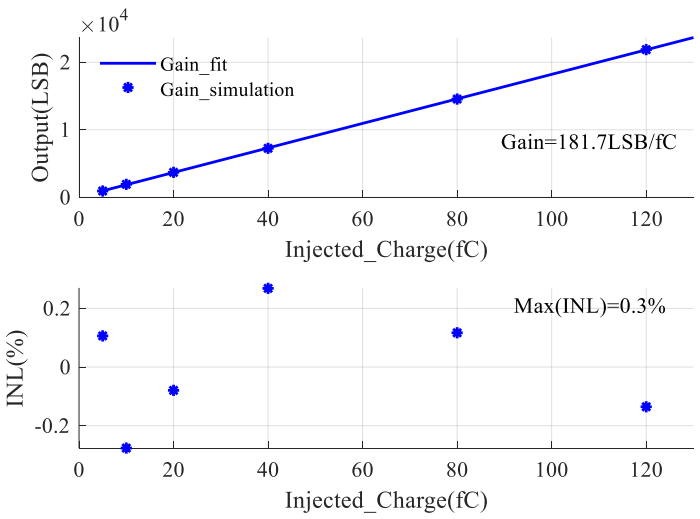


Valentin T. Jordanov, Unfolding-synthesis technique for digital pulse processing. Part 1: Unfolding, NIMA Vol 805, 2016，63-71

- Transient Outputs



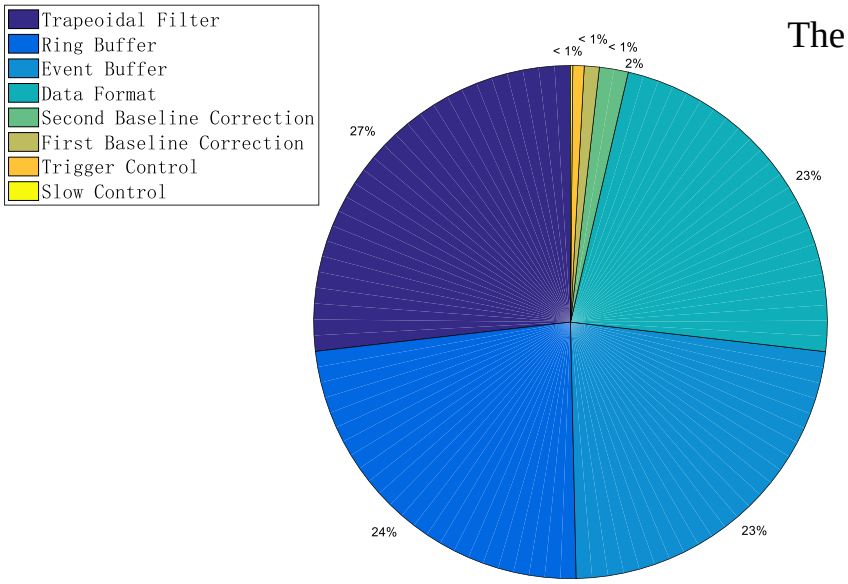
- Linearity



Power Consumption Estimation

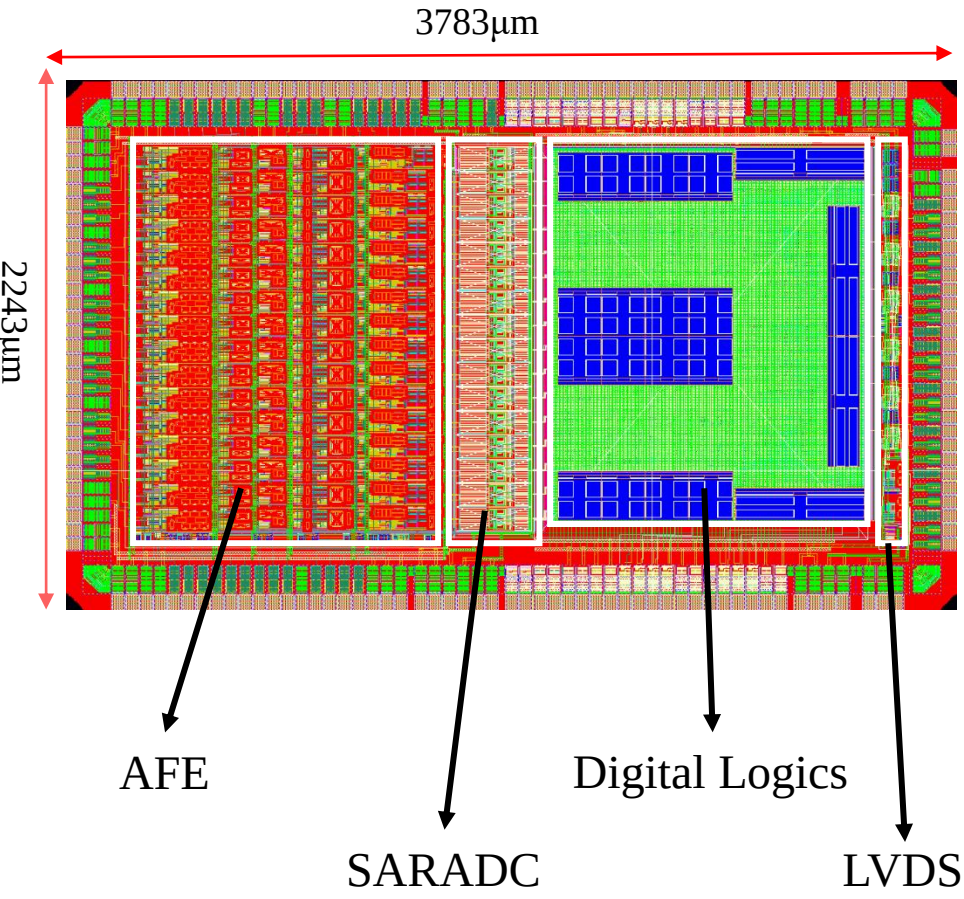
- The simulation settings of digital logics @ 1.2 V, tt, 25 C, switch activity = 10% (**Conservatively**)
- The power consumption: 3.36 mW+0.078 mW/MHz x sampling rate in MHz

Sampling Rate MS/s	10	20	30	40	50	60	70	80	90	100
Digital logics: mW/ch	2.03	2.69	3.34	4.0	4.62	5.28	5.90	6.55	7.20	7.85
ADC: mW/ch	0.69	0.81	0.94	1.06	1.19	1.31	1.44	--	--	--



The Power Distribution

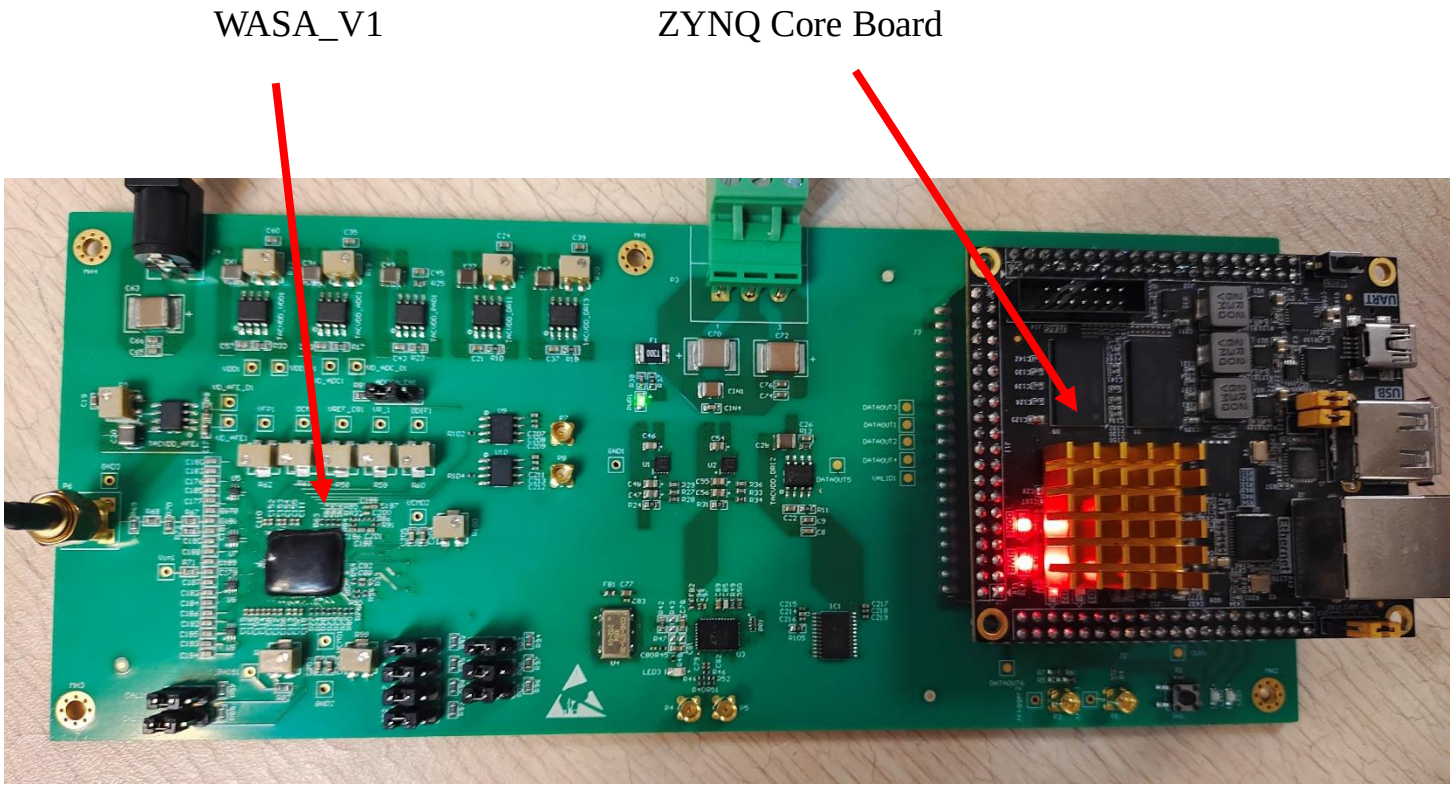
The Layout of WASA V2



- The floor plan in layout:
  - The die size： 3783 μm x 2243 μm
  - Analog Front-End, SAR ADC, Digital Logics, LVDS driver are supplied by separate power
  - Analog Front-End, SAR ADC, Digital logics, LVDS driver are separated by guarding ring
- The ASIC have been taped out in Jan 12 ,2022 and is being evaluated.

The Layout of WASA V2

- ASIC Test Board

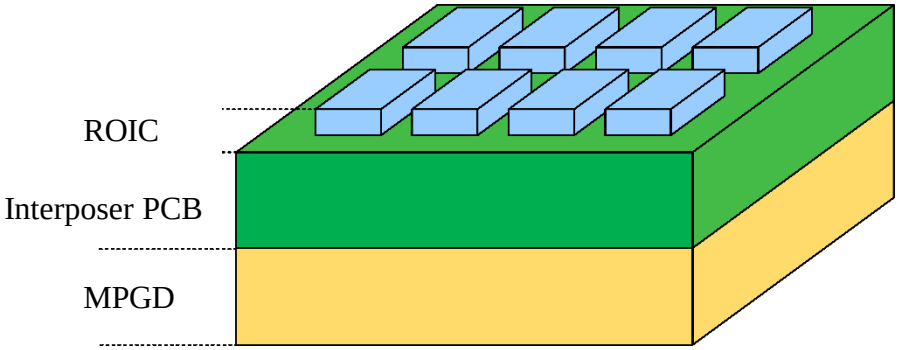


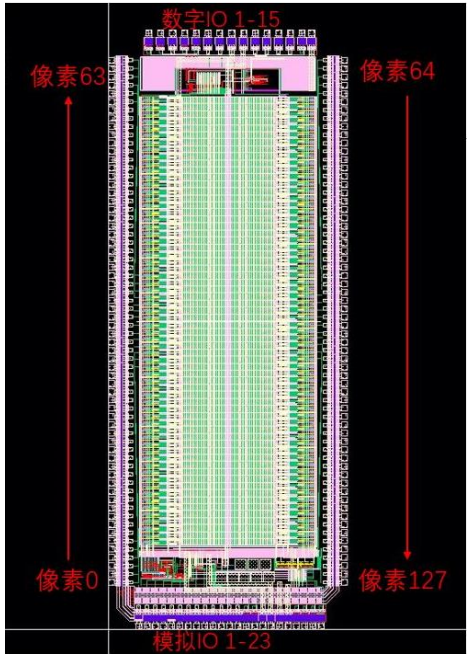
Summary

- A 16 channel low power readout ASIC WASA V1 has been developed and evaluated
  - The power consumption is 2.49 mW/channel
    - P_{AFE}=1.43 mW/channel
    - P_{ADC} = 1.06 mW/channel @ 40MS/s
  - ENC = 911.7 e @ Cin=15.2 pF, gain=10 mV/fC and can be reduced to 627 e using digital trapezoidal filter
  - Tested with TPC detector at IHEP: OK, more tests with more readout channels
- The second iteration of WASA V2 has also been designed
  - Two stage BC, digital trapezoidal filter, and trigger logics with two stage data buffer are implemented on chip
  - The ASIC have been taped out and is being evaluated.

Future Plan

- Large Pixel Readout
  - 1mm x 6 mm → 0.3~0.5 mm pixel
  - Higher precision, higher rate
  - Potential for dN/dx
- Concept Design
  - ROIC +Interposer PCB as RDL
  - High metal coverage, 4-side buttable
  - Low power Energy/Timing measurement ASIC
    - ~100 e noise
    - 5 ns drift time resolution
    - <100 mW/cm2





Thank You