Status of CPEC Vertex Detector Prototype Elec& DAQ readout design

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On behalf of the CEPC MOST2 Vertex detector design group

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Outline

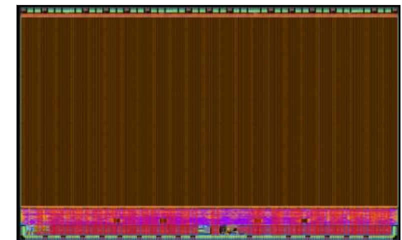
- Overview of MOST2 vertex detector R&D
- Design of electronics readout
- Design of DAQ
- Schedule

Overview

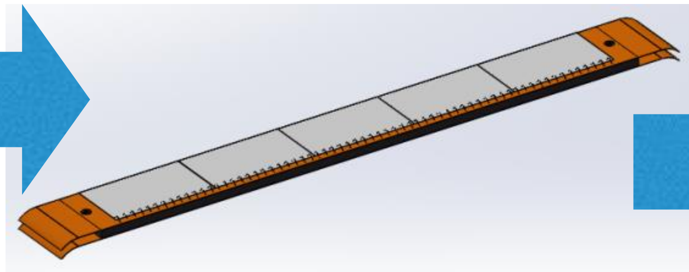
Zhijun Liang

- MOST2 vertex detector R&D can break down into sub-tasks:
  - CMOS imaging sensor chip R&D
  - Detector layout optimization, Ladder and vertex detector support structure R&D
  - Detector assembly
  - Data acquisition system R&D

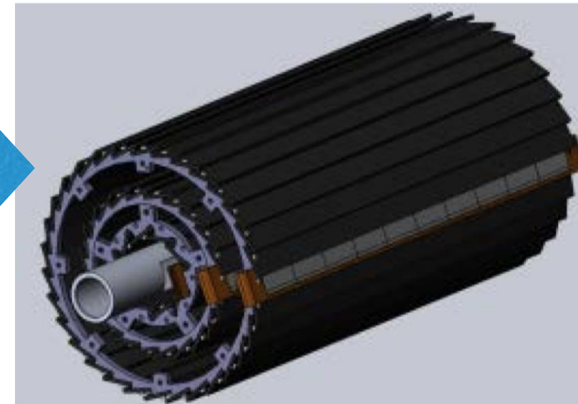
CMOS imaging sensor prototyping



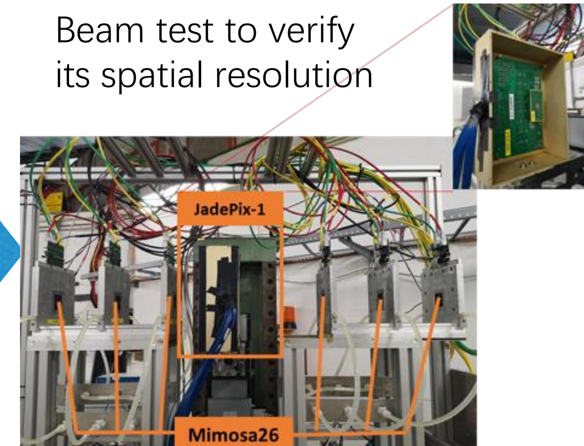
Detector module (ladder) Prototyping

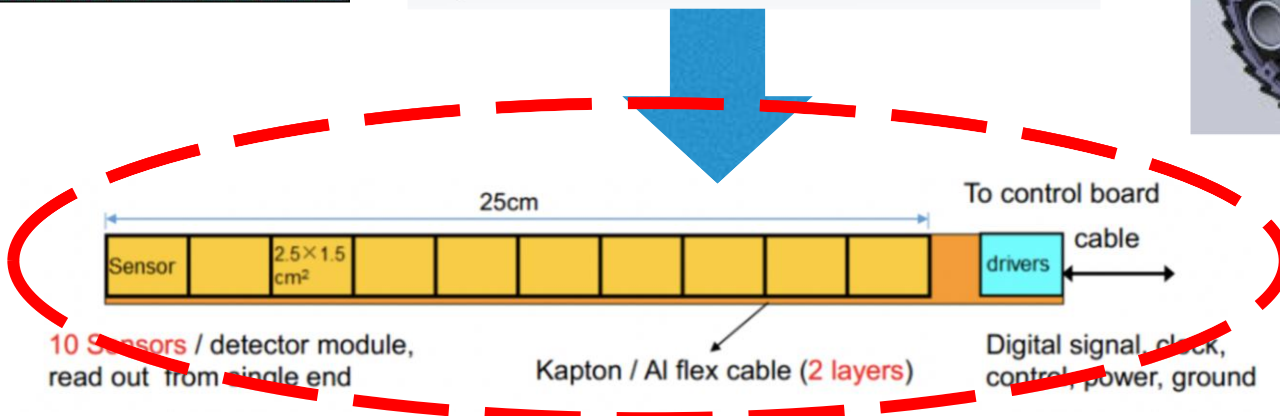


Full size vertex detector Prototype

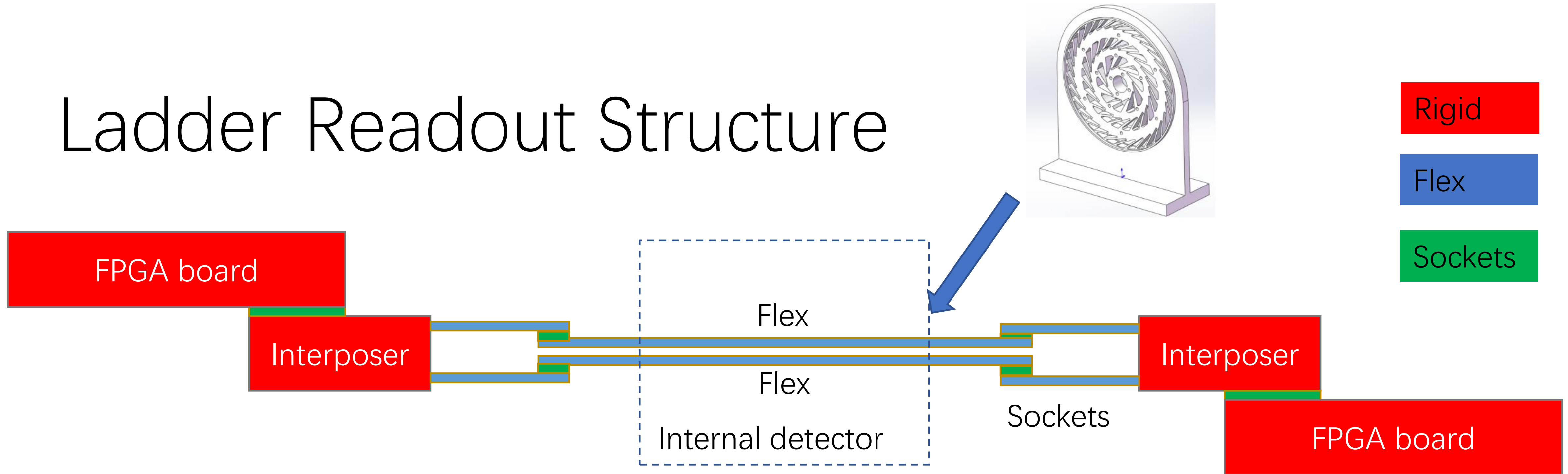


Beam test to verify its spatial resolution



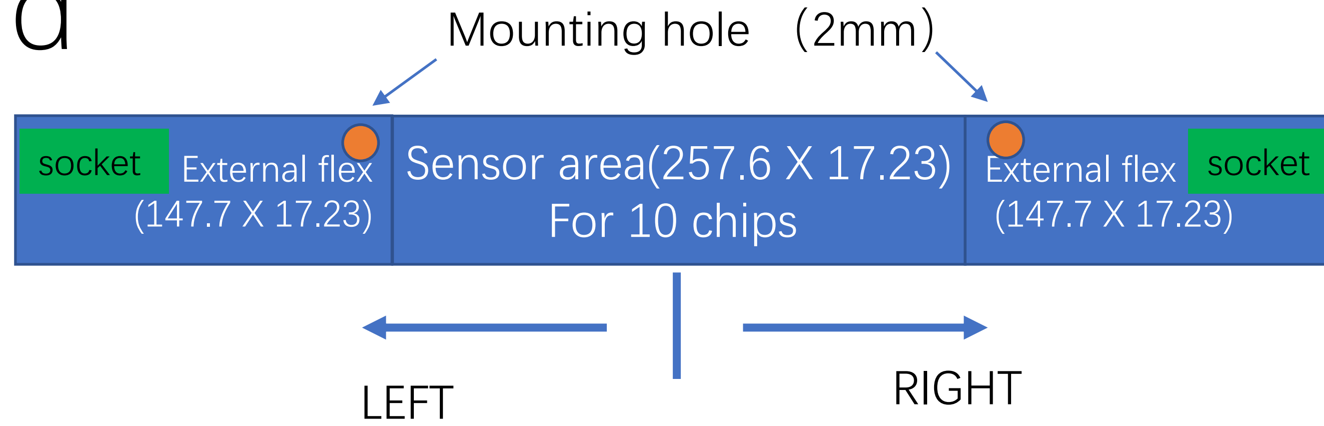


Ladder Readout Structure



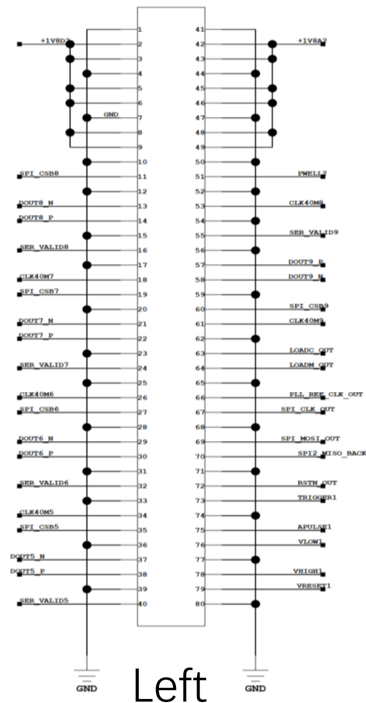
- 3 boards
  - Flex board： Assembled with 10 TAICHU chips, Dual sides readout
  - Interposer board： FMC mezzanine rigid and flex board
  - FPGA board： FMC carrier board
- Easier production, easier assembly

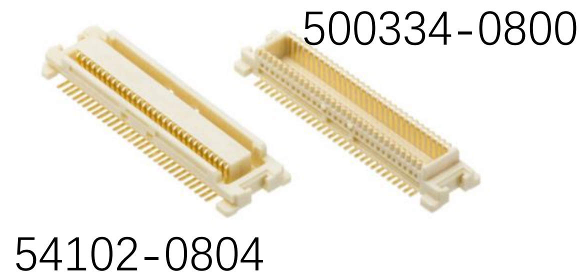
Flex board

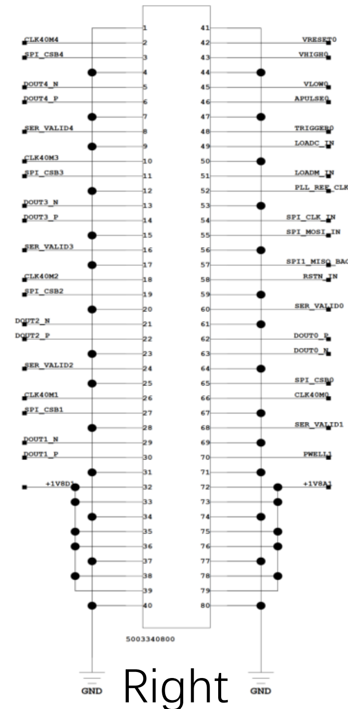


553mm length in total

Socket signal definition

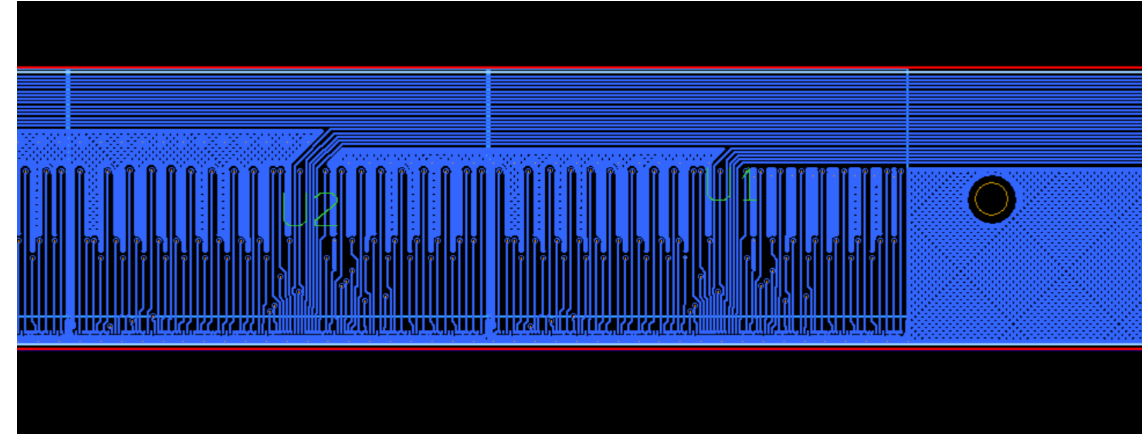




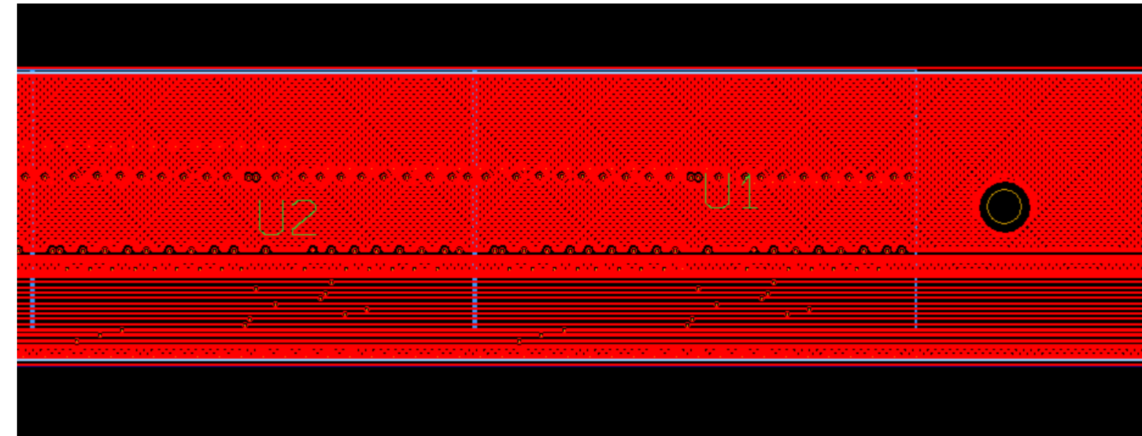


PCB Layout

- Independent signals（Bonding side）：
  - CLK40M, SPI_CSB, DOUT_P, DOUT_N, SER_VALID
- Shared signals（Bottom side）：
  - APULSE, TRIGGER, VRESET, VHIGH, VLOW, 7 SPI signals
- Power supply
  - VDDD, VDDA, PWELL, GND

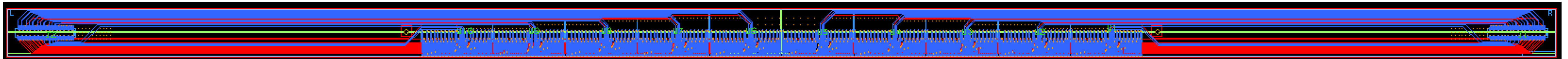


Bonding side



Bottom side

553mm X 17.23mm



Full layout

Layer Stackup

- Option1 （baseline)
  - 2 layers
  - Less material
  - limited layout space lead to worse signal integrity
    - Crosstalk
    - Large voltage drop
    - Ground bounce
  - Thickness: ~0.2mm （+0.1mm stiffener)

- Option2
  - 4 layers
  - Dedicated GND and power plane gain better signal integrity
  - More material
  - Thickness: ~0.38mm （+ 0.1mm stiffener ）
  - For study the ASIC chips and electronics performance

Vdrop: estimate 0.03Ω = (1mmX25.6mmX0.5oz)

VDDD 6mm width, 0.21A * 0.03 / 6 *12.5 = 13mV
VDDA 4mm width, 0.21A * 0.03 / 4 * 12.5 = 20mV
GND 2mm width, 0.42A * 0.03 / 2 *12.5 = 79mV

The design of the 2 options is similar, and the production has been started at the same time.

Interposer board

- Power supply requirement:
  - 1.8VDDA ≈ 0.21A
  - 1.8VDDD ≈ 0.21A
  - PWELL (-6V – 0)
  - VRESET, VHIGH, VLOW from DAC

Top view

5cm

7cm

To 2 flex boards

100mmX17.23mm

Socket

Flex

LINEAR REGULATOR

DAC

REF

Voltage Regulator

FMC

To FPGA board

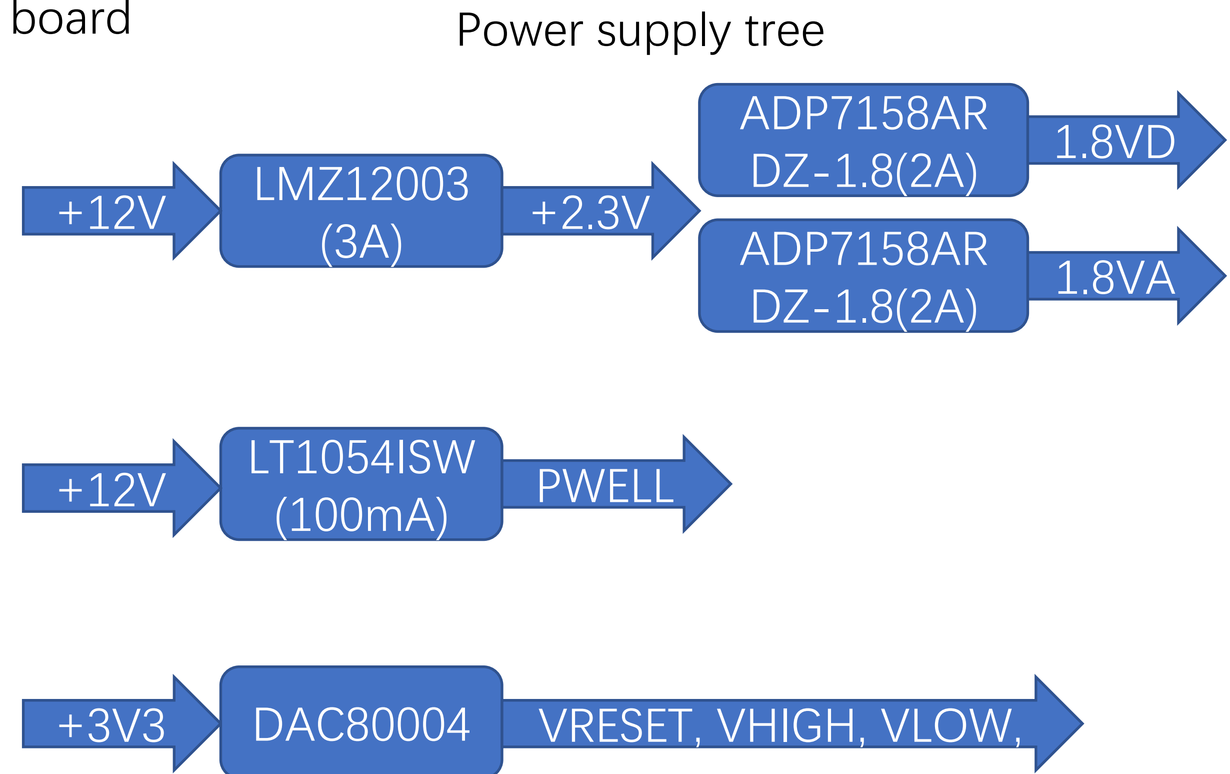
Side view

Sockets

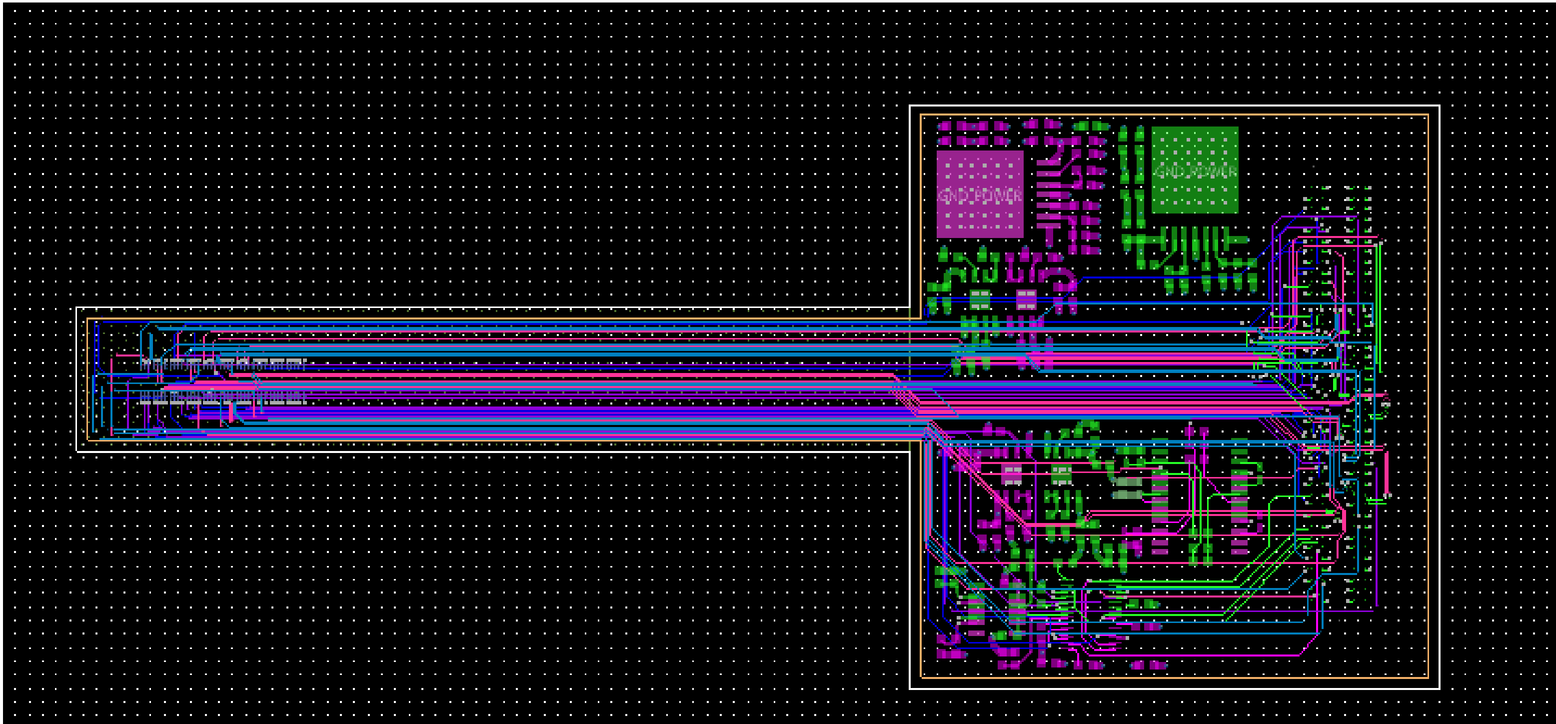
1.6cm

power supply and filter are placed on rigid area

Power supply tree



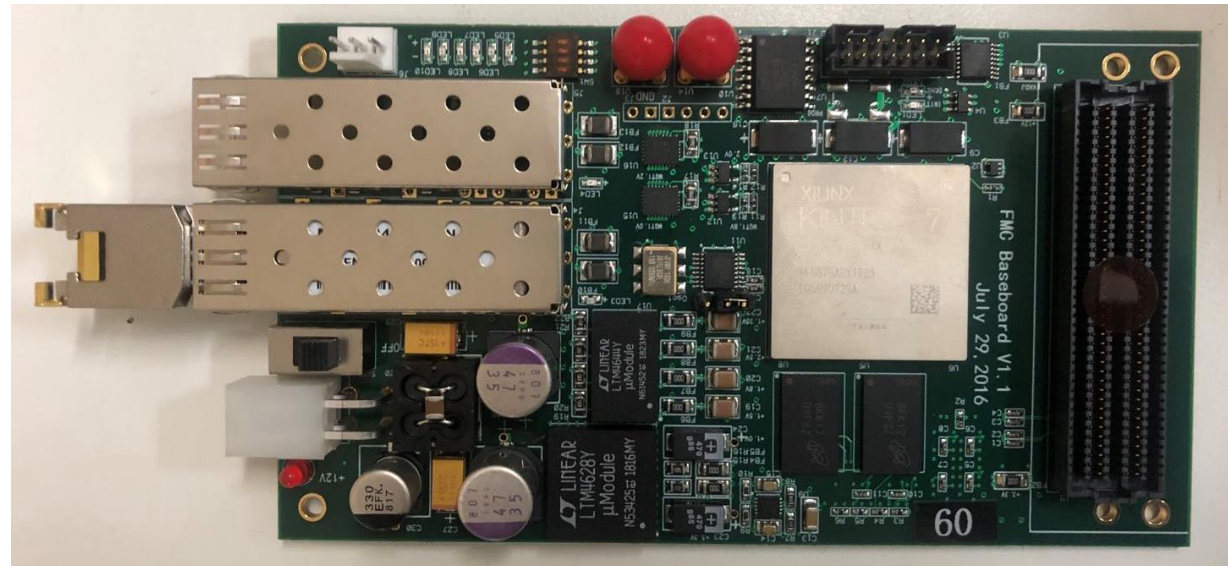
PCB Layout



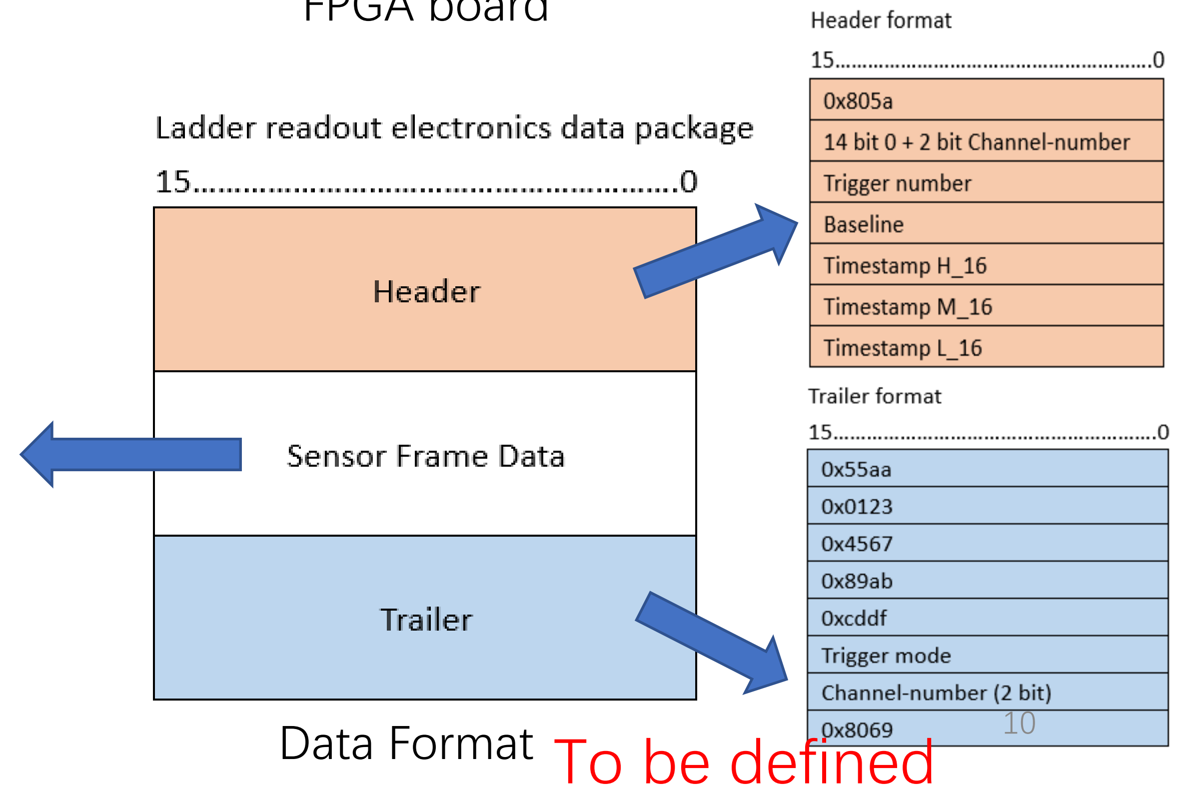
- 14 layer rigid +
- 4 layer flex X2

FPGA board

- Features
  - Communication with chips
    - Configure the chips via SPI bus
    - Readout from chips via LVDS
    - Provide main power 12V， 3.3V
  - Data processing and package data
  - Readout to PC via 1Gbps Ethernet
    - Data Readout： TCP/IP
    - Configuration： UDP
  - FMC standard
    - ASP-134606-01: 8.5mm height
  - Capability of 6Gbps max readout and 2GB internal DDR memory



FPGA board



Data Format

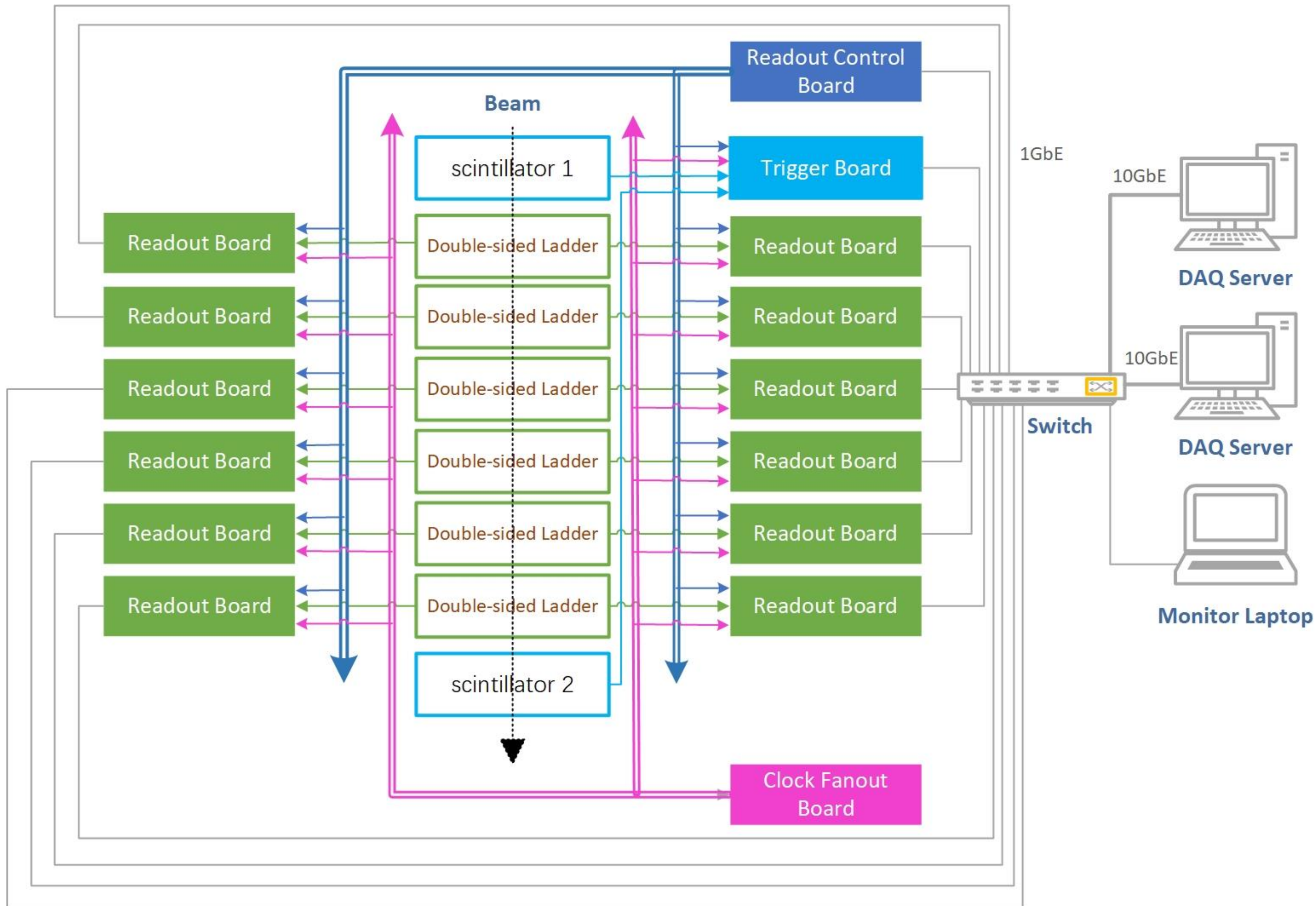
To be defined

Bandwidth calculation

- For 1 chip
  - Triggerless: 4G bps
  - With external trigger:
    - 160Mbps @ CEPC maximum
    - ~Mbps @Beam test
- For 1 FPGA board （10 chips）
  - 1 Gbps Ethernet is enough for beam test
  - Support CEPC trigger mode by updating the SFP to optical link
  - Need reconsidering the structure for triggerless

Design of DAQ

Hongyu Zhang



Front End Electronics:

- Readout Board: x12
  - Readout Ladder electronics data
- Clock Fan-out Board: x1
  - Fan-out common clock signal to each readout board
- Readout Control Board: x1
  - Fan-out common reset / common start / common stop signals to each readout board
  - Synchronize global timestamps of each readout board
- Trigger Board: x1
  - Provide timestamp of Scintillator trigger signal

Schedule

- Flex boards(2 options):
  - Design finished
  - In production ~ 2-3 weeks
- Interposer boards:
  - Design finished
  - In production ~ 3 weeks
- FPGA boards and fanout boards:
  - 18 FPGA boards and 3 fanout boards are available.

- Test of Ladder
  - In September

Thank you

- May: Flex cable available
- May: Test of wire bonding and gluing on carbon support
- July: ASICs arrive to IHEP
- August: Wafer level test of ASICs
- September: Single chip and module testing
- September: Assembly of ladders with chips

- June: Production of installation tooling
- June: Installation mock-up
- July: Barrel support parts fabricated
- End September: Assembly first barrels
- October: Assembly of multiple ladders and readout tests
- Earlier November: Finish assembly of prototype
- November: Cosmic ray testing or BEPC beam test
- End November/December: DESY test beam