The design of LGAD readout electronics system

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Outline

- Background
- Readout electronics system
  - AFE based on Altiroc
  - AFE based on discrete device
  - Digital readout part
- Summary and future plan

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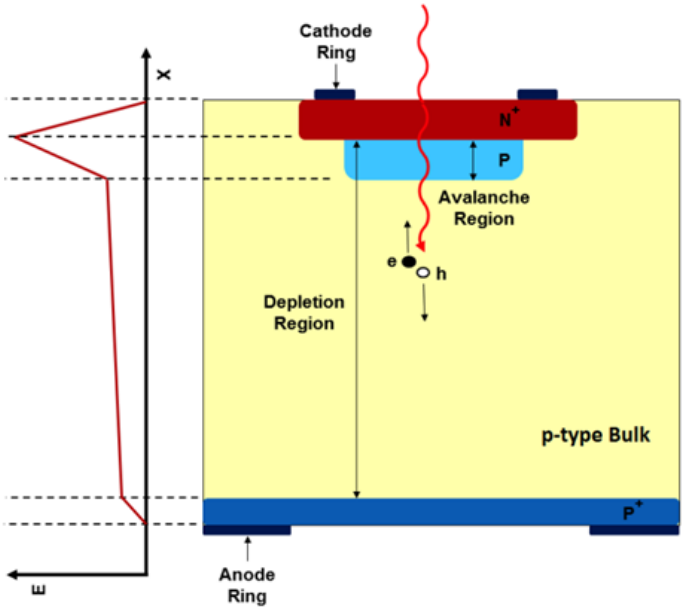
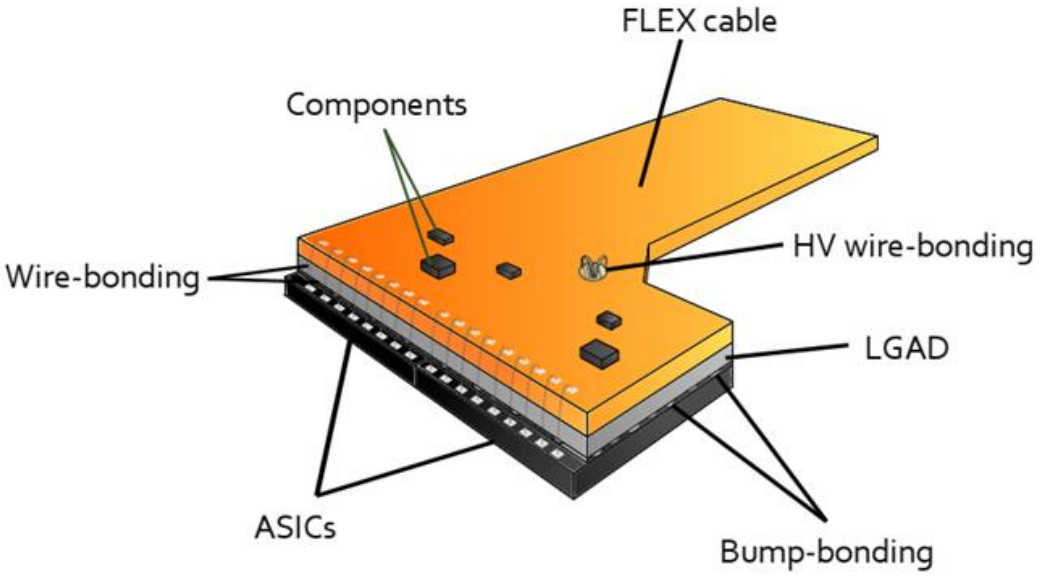
Background

- Low Gain Avalanche Detectors (LGAD).
  - chosen for the HGTD sensors.
- LGAD is connected to ASICs by bump-bonding



LGAD



LGAD-ASIC module

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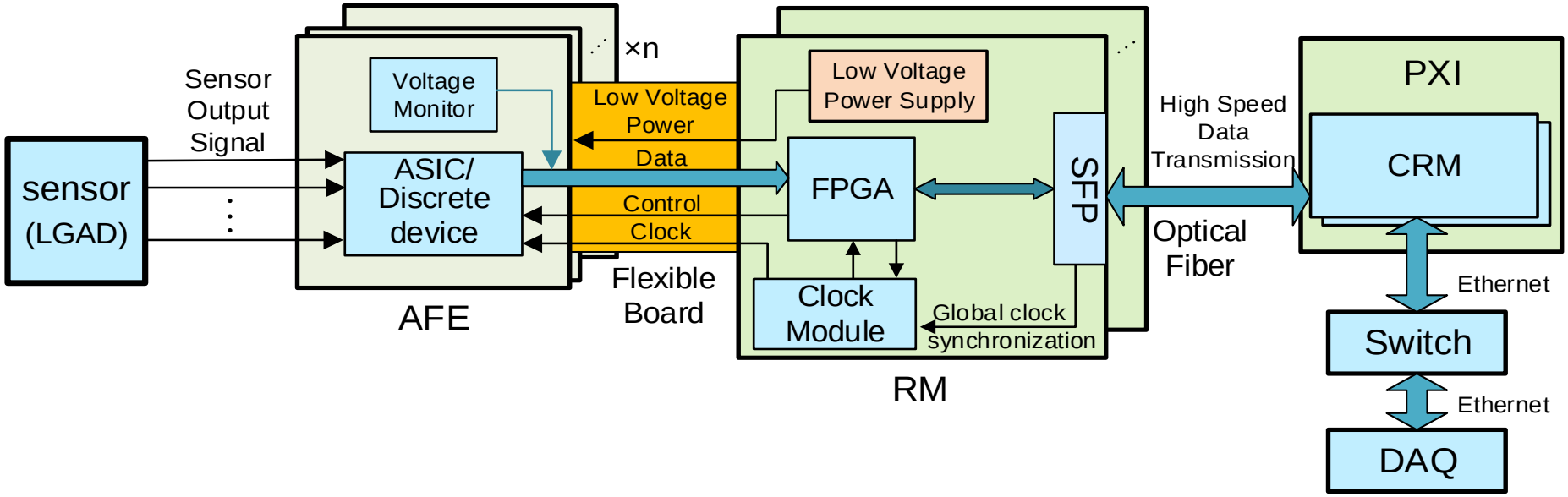
LGAD readout electronics system



- LGAD readout electronics is designed for the verification of USTC LGAD.
- Analog front-end electronics(AFE) is based on Altiroc2 or discrete device.
- Readout modules (RMs) transfer data from AFEs to the CRM.
- Common readout module (CRM) collects data and sends them to DAQ.

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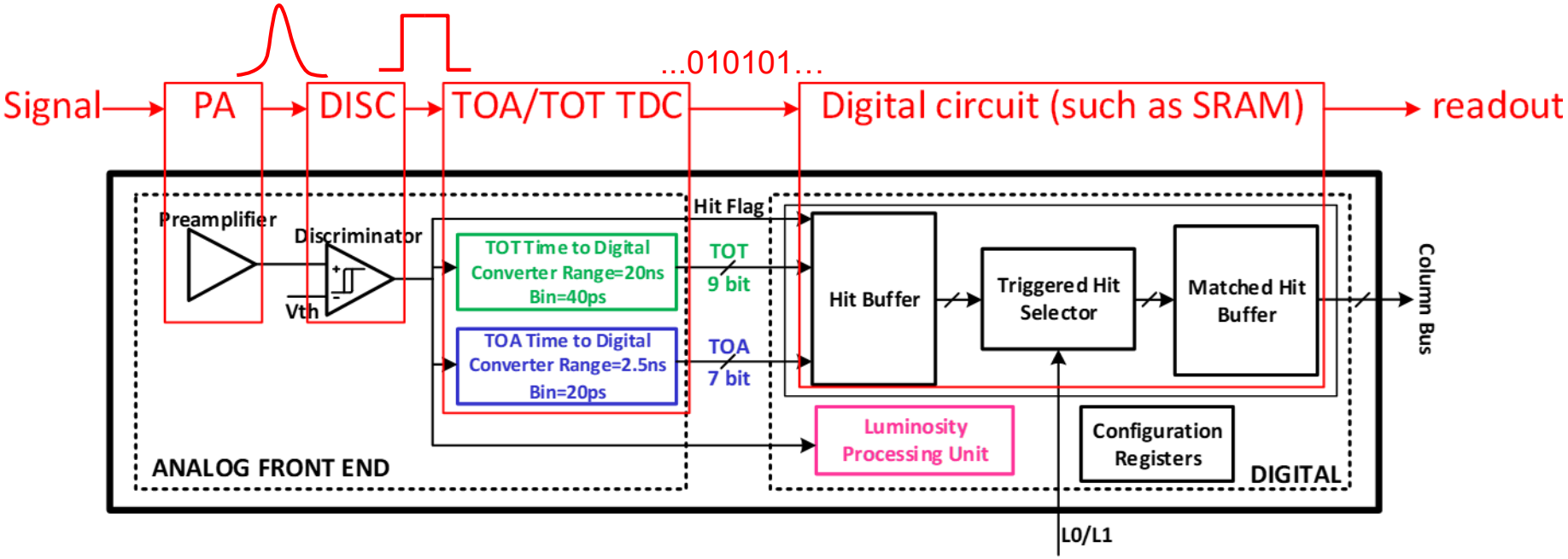
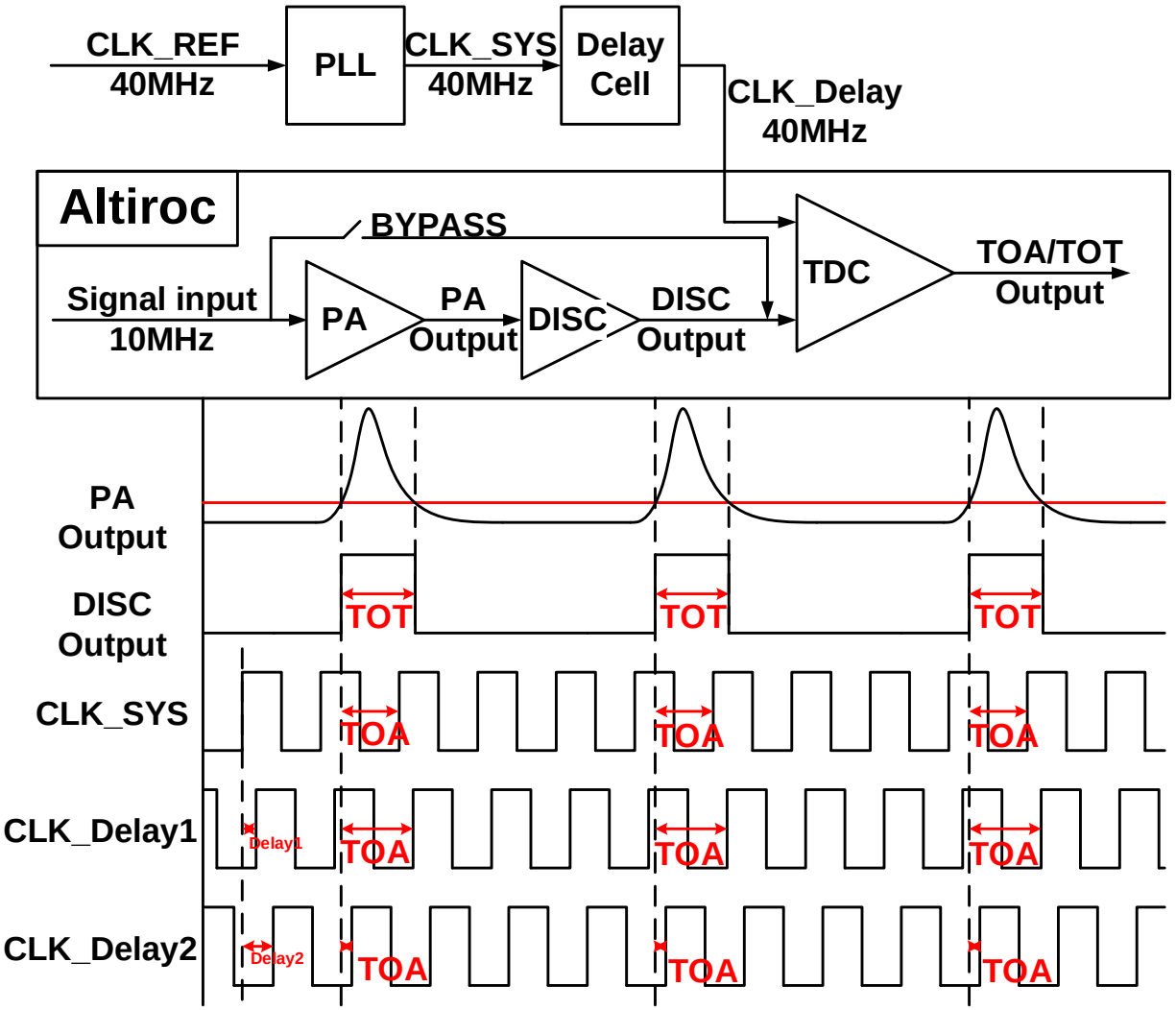
Altiroc

- ATLAS LGAD Timing Integrated Readout Chip
- Altiroc is a front-end electronics, low-noise custom ASIC used for LGAD readout.
- Altiroc has developed to the second generation.



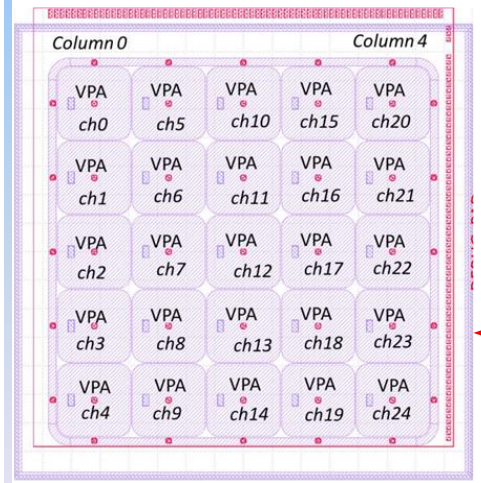
Altiroc test



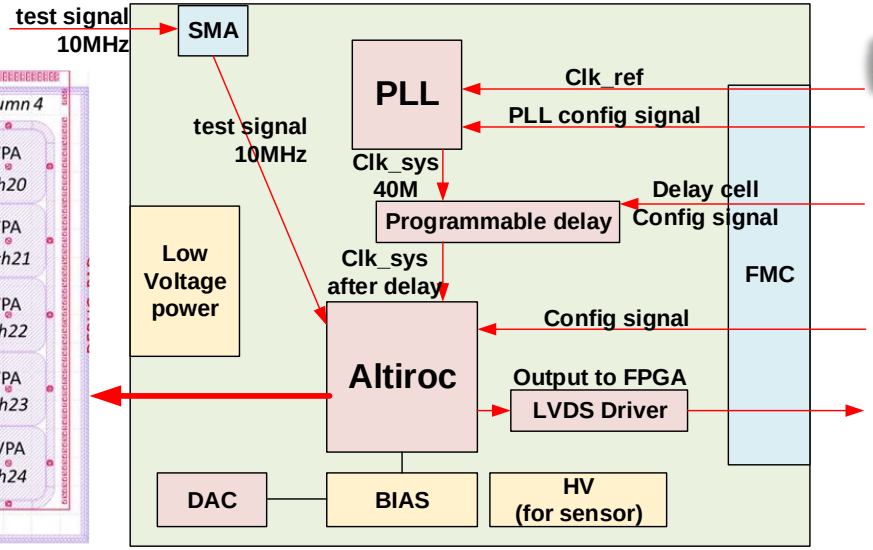
obtain the performance of Altiroc from TOA and TOT

Altiroc1

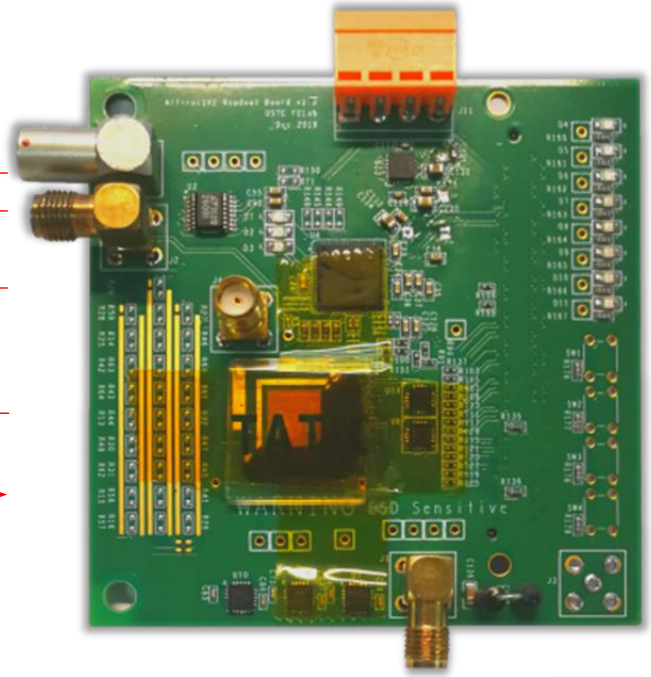
- Altiroc1 contains 25 channels (5 x 5)
- Test Altiroc1 with the test board we design
- TOA test and some other tests (etc. TOT, Vth, Charge)



Altiroc1 5x5 channels



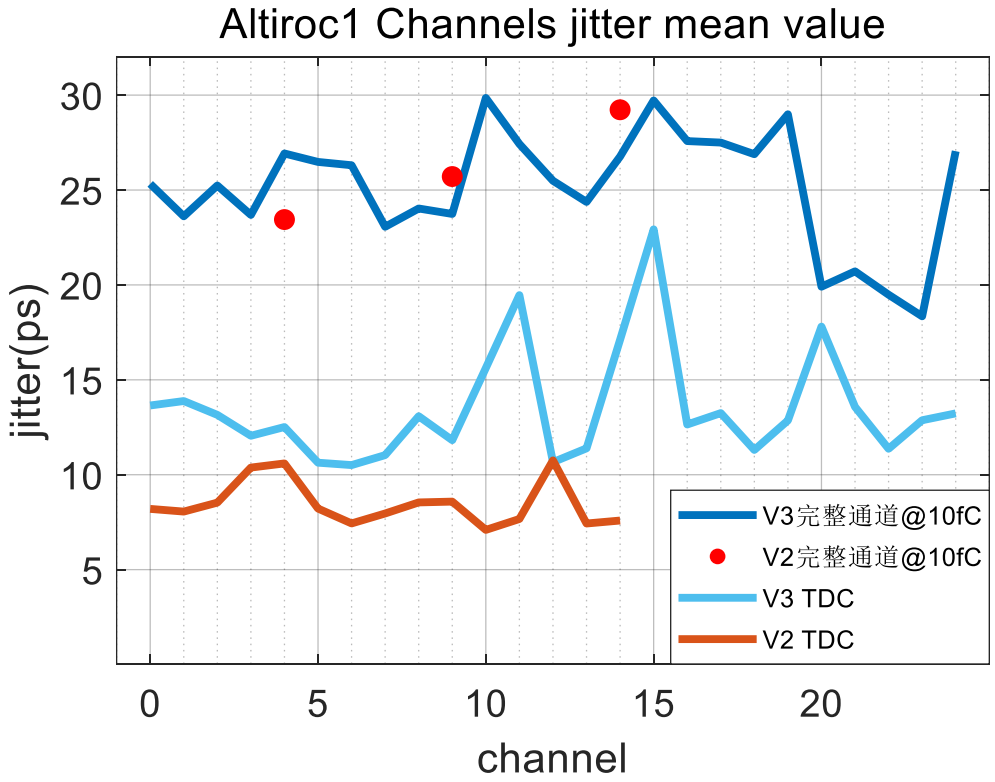
Altiroc1 test board



Altiroc1 test board

Altiroc1 test

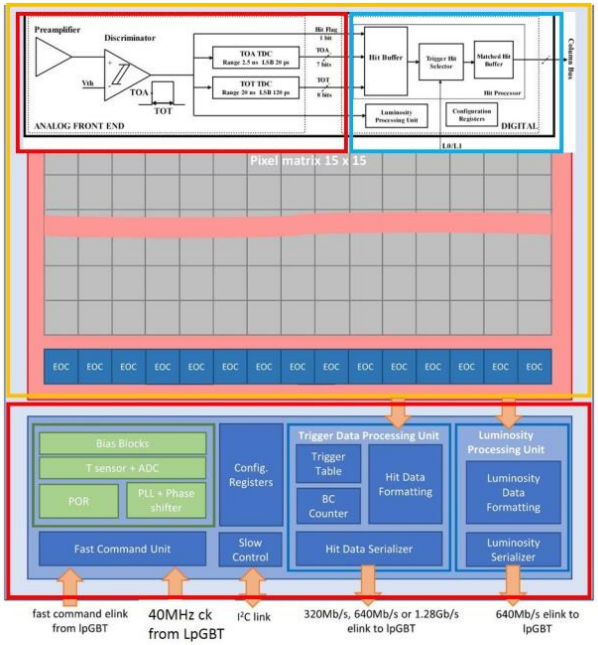
- Some channels cannot be tested
- TOA jitter of Altiroc1 is around 25 ps



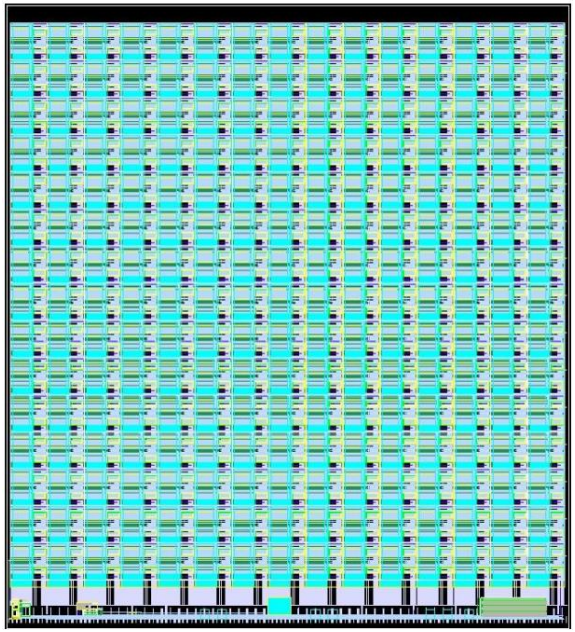
Altiroc1 TOA test results

Altiroc2

- Altiroc2 is the latest version of the Altiroc series.
- Altiroc2 contain 225 channels (15 x 15) and complete readout function.

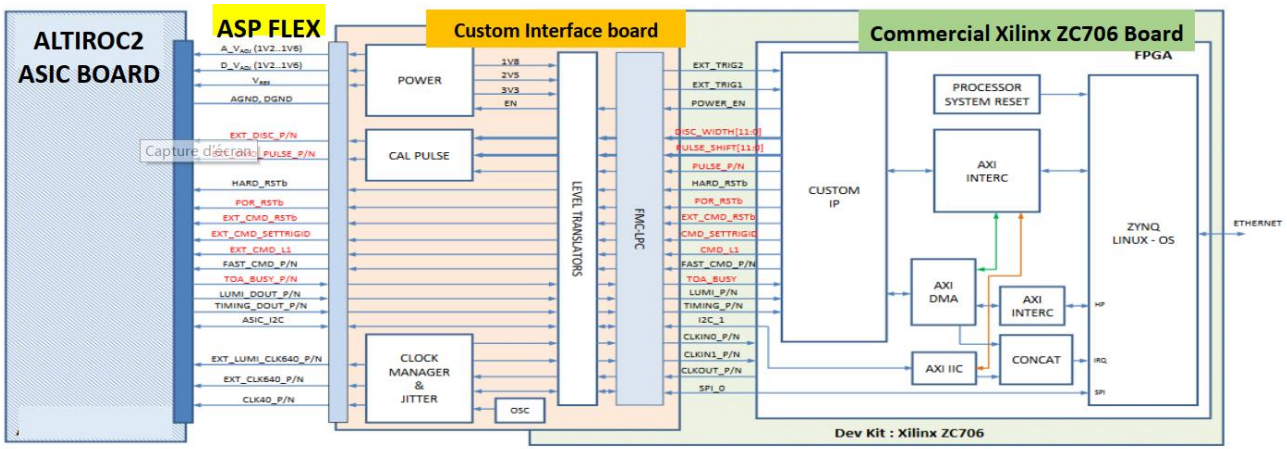


Altiroc2 general structure

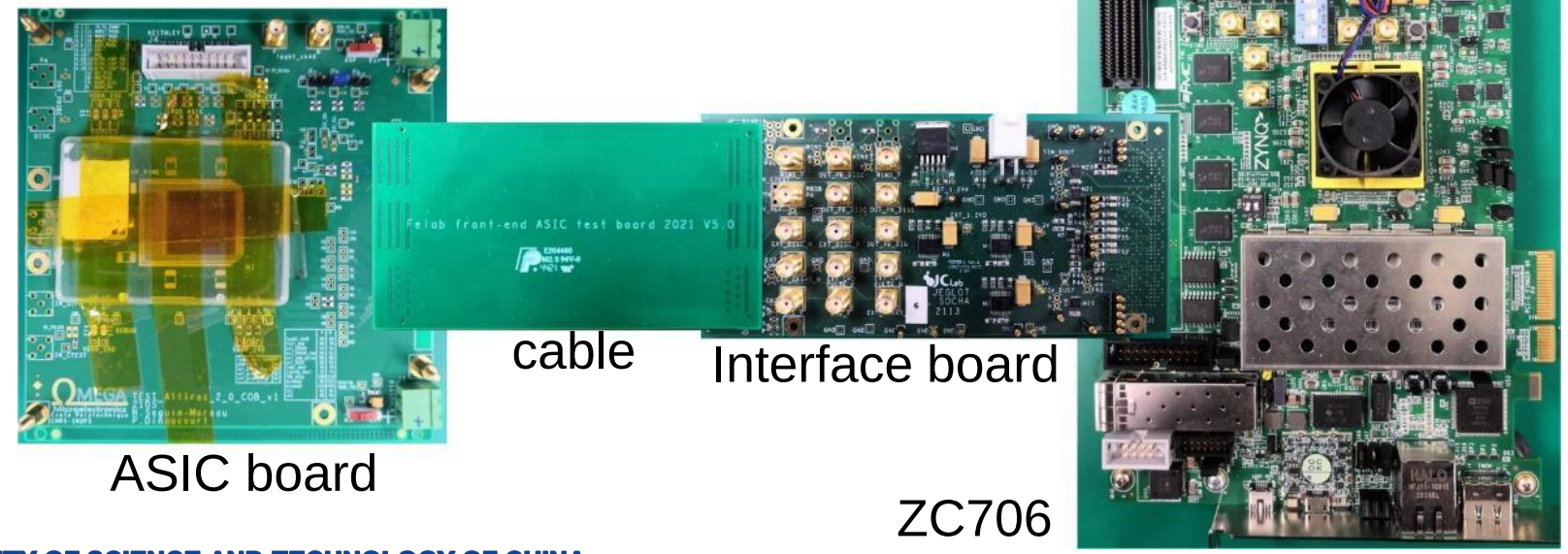


Altiroc2 15x15 channels

Altiroc2 test



Altiroc2 test system from OMEGA



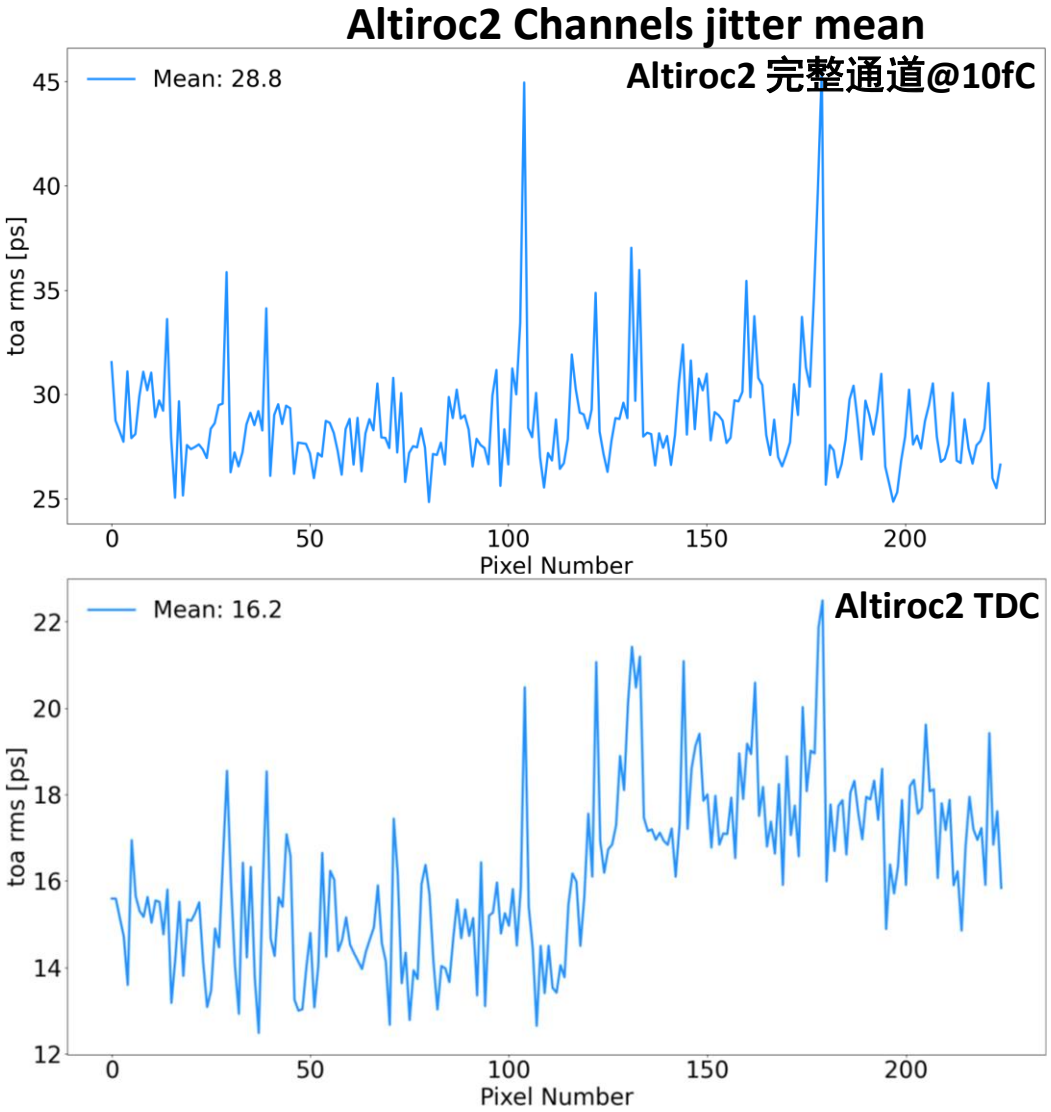
ASIC board

cable

Interface board

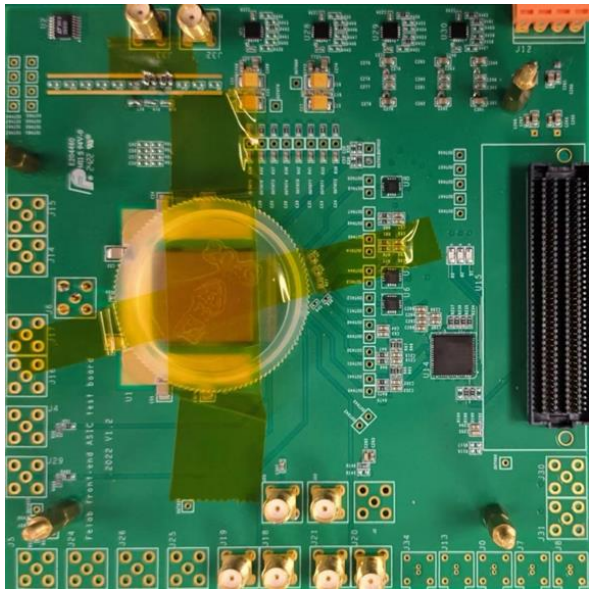
ZC706

Altiroc2 test

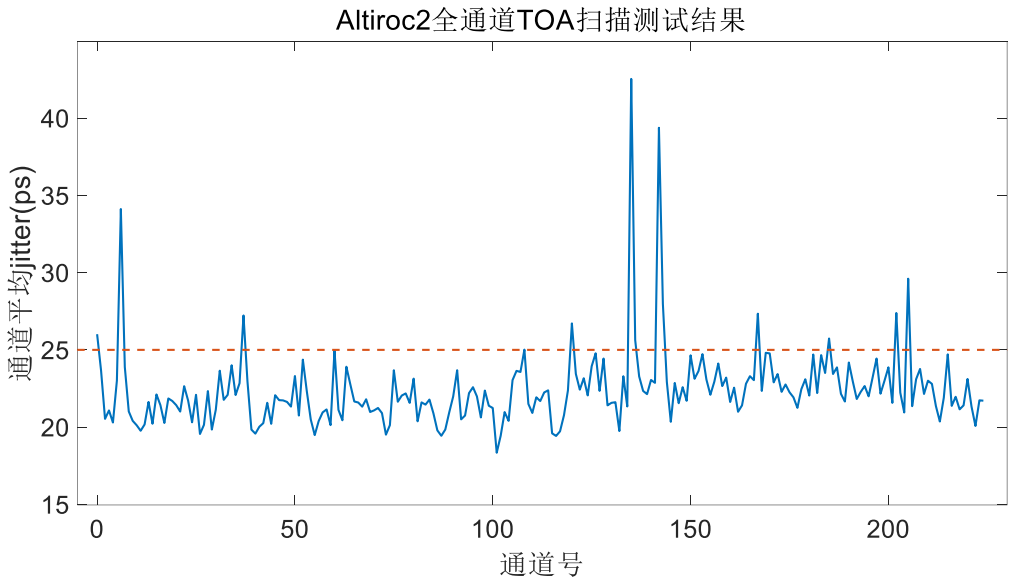


AFE based on Altiroc2

- AFE based on Altiroc2 has been designed
- The TOA jitter of most of channels is lower than 25ps
- Meet difficulties in bump-bonding and be waiting for more LGAD-Altiroc2 modules now



AFE based on Altiroc2



Altiroc2 test results

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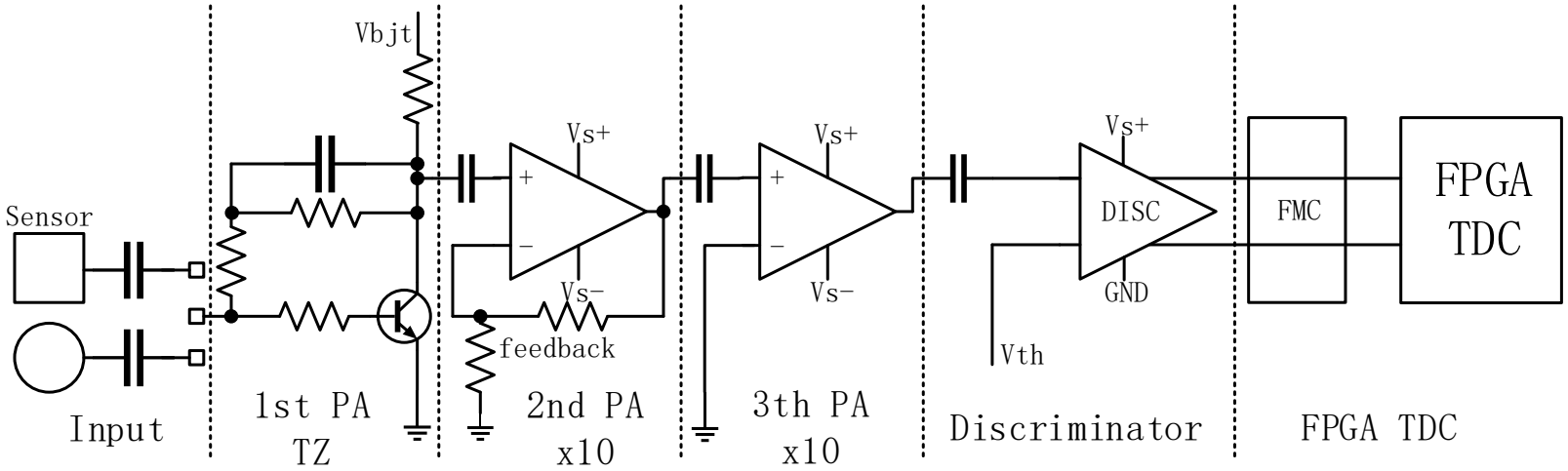
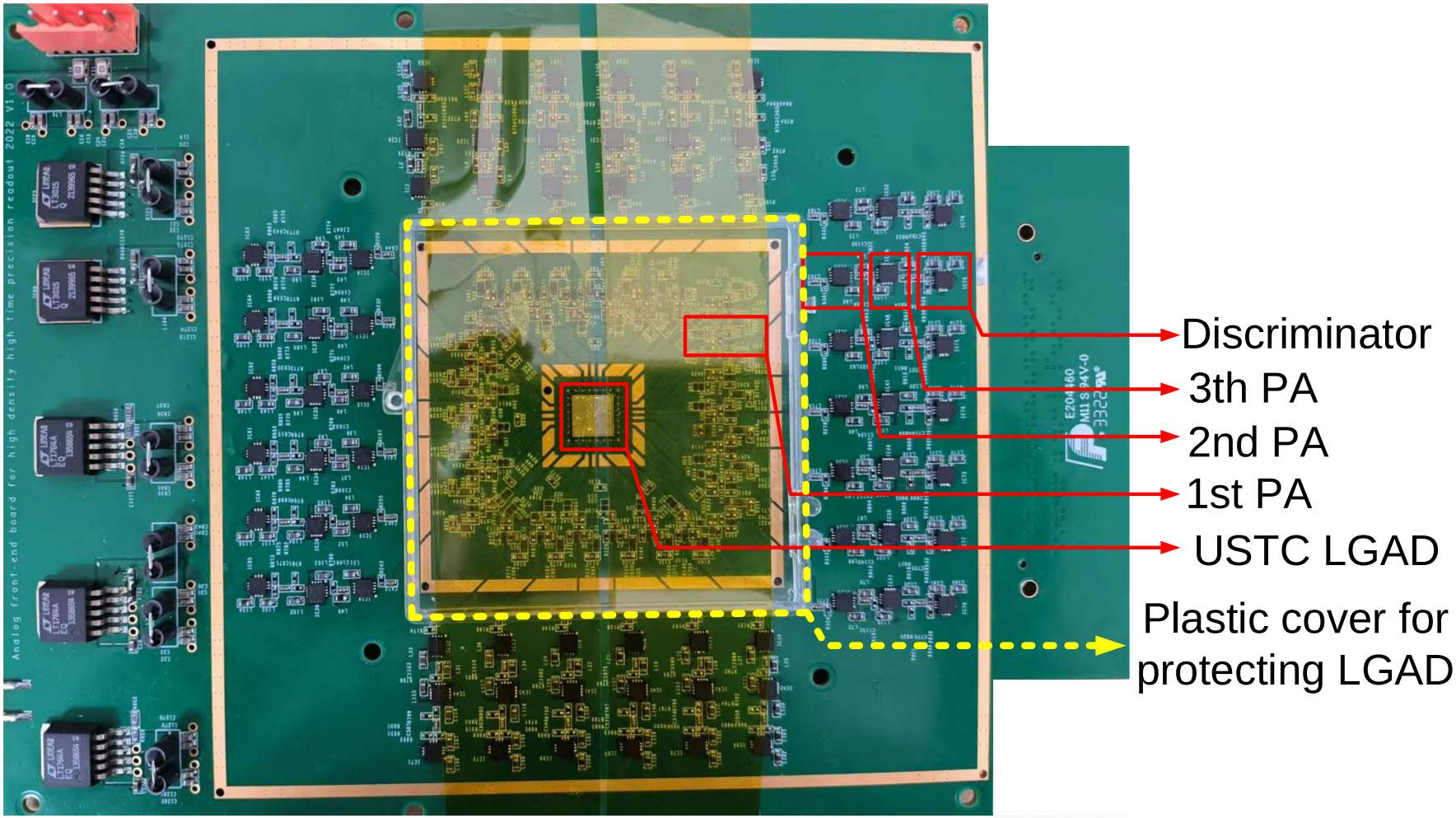
AFE based on discrete device

- Waiting for more LGAD-ASIC modules
  - Design AFE based on discrete devices as an alternative
- Overall design
  - 5 x 5 USTC LGAD
  - Amplifier and discriminator composed by discrete devices
  - FPGA TDC

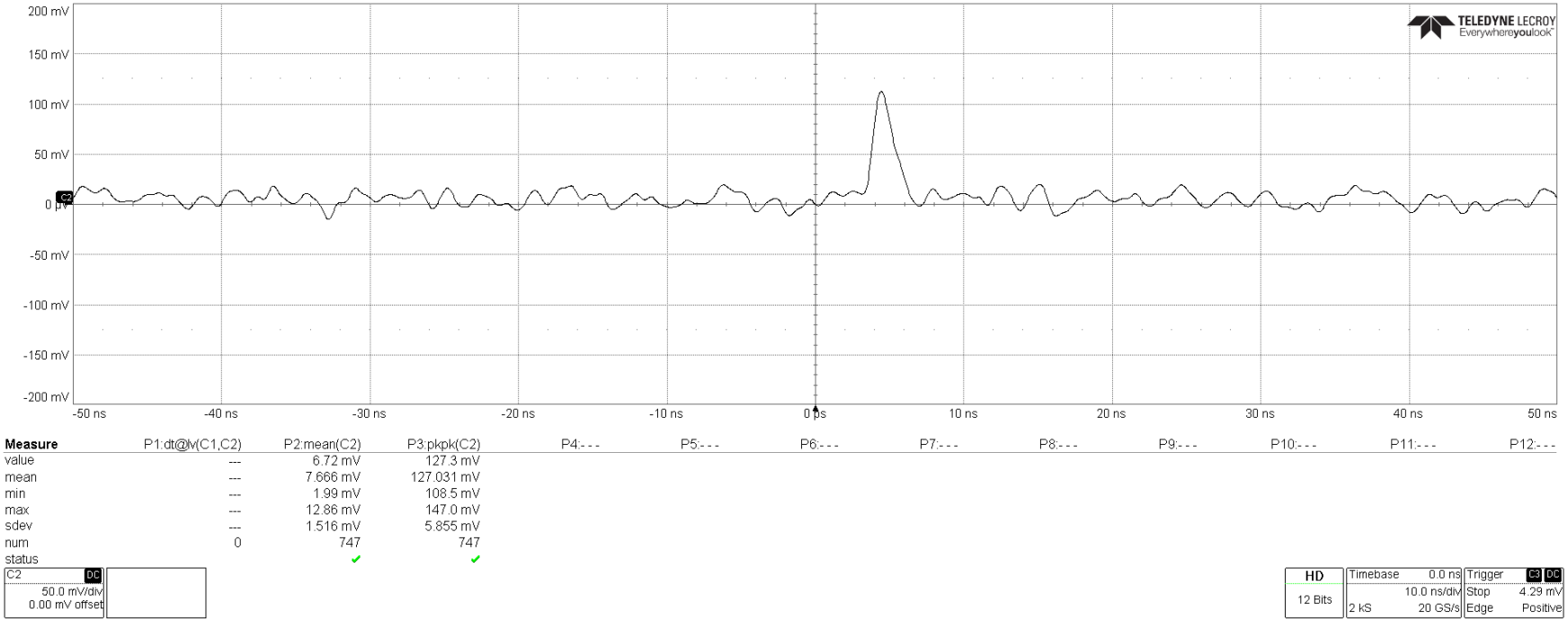


AFE based on discrete device



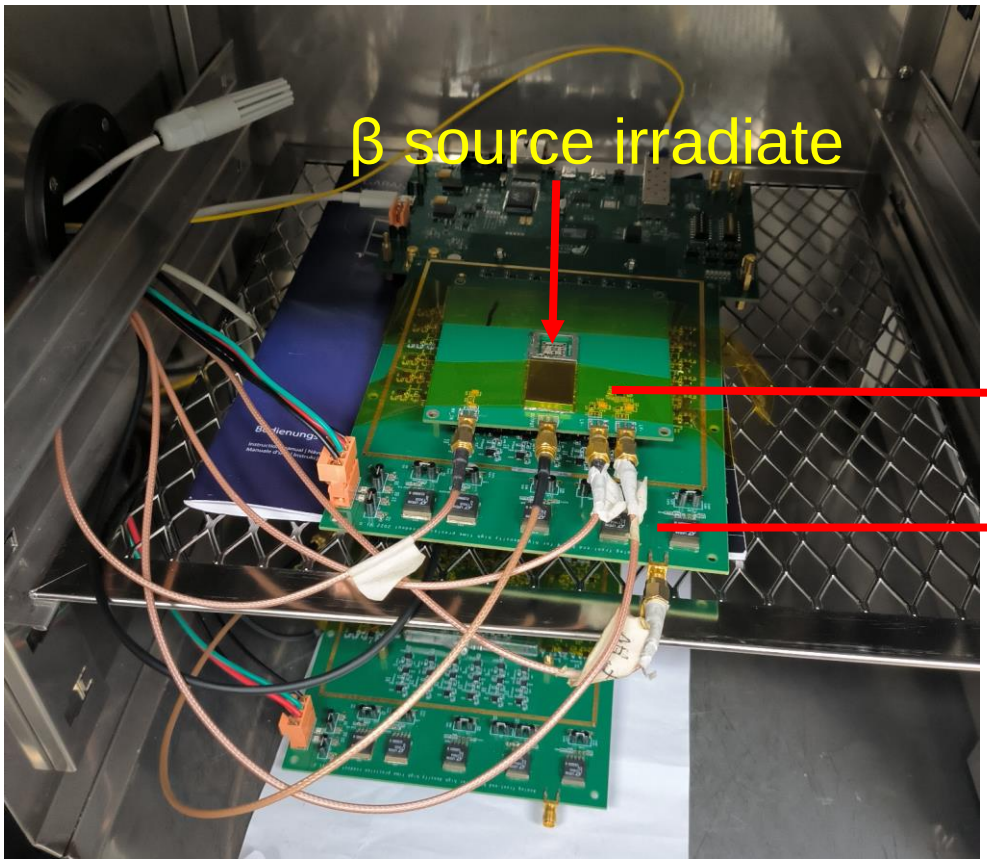
Electronics Test

- Input external signal from signal generator to simulate the signal from LGAD
- The jitter of electronics channels is 15~17ps



AFE based on discrete device

- Test AFE by measurement of Time of Flight



T0 output from a LGAD test board after calibration

T1 output from the AFE based on discrete device

AFE based on discrete device

- The TOF jitter of AFE with LGAD is lower than 43ps

	1	2	3	4	5
1	42.19	41.13	41.59	41.66	42
2	42.23	41.94	41.9	40.84	42
3	41.76	41.58	41.42	41.32	41.9
4	40.47	40.3	41.2	41.27	41.01
5	42.31	39.97	39.95	41.6	41.2

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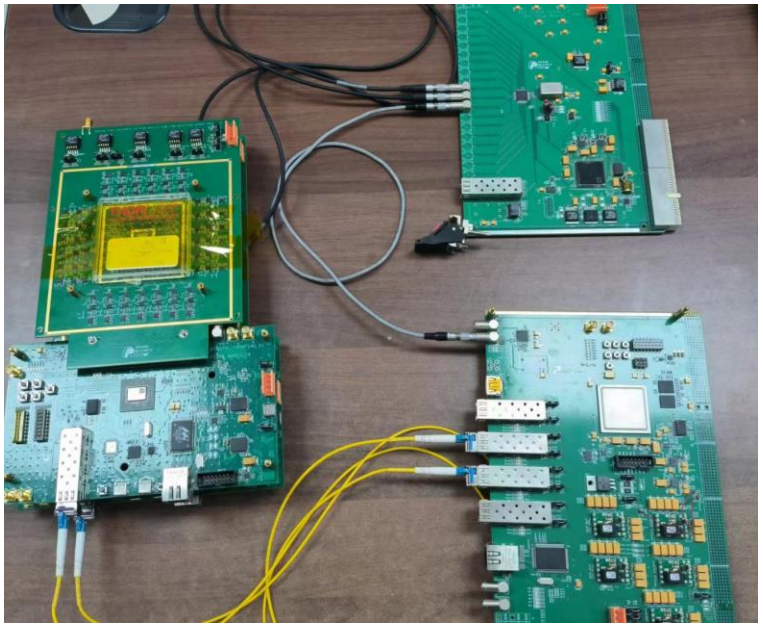
Digital readout part

- For transfer the timing data from TDC to DAQ, we also design CRM
  - Collect and package data
  - Receive external clock and trigger
  - Distribute clock and trigger to RMs



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Summary and future plan

- Summary
  - AFE based on Altiroc2 :
    - The TOA jitter of most of channels is lower than 25ps
  - AFE based on discrete device
    - The TOF jitter of AFE with LGAD is lower than 43ps
  - CRM
    - Transfer the data and enable to connect 4 RMs

- Future plan
  - USTC LGAD-Altiroc2 bump bonding module
  - Complete LGAD readout electronic system