Status of iRPC Trigger Backend system

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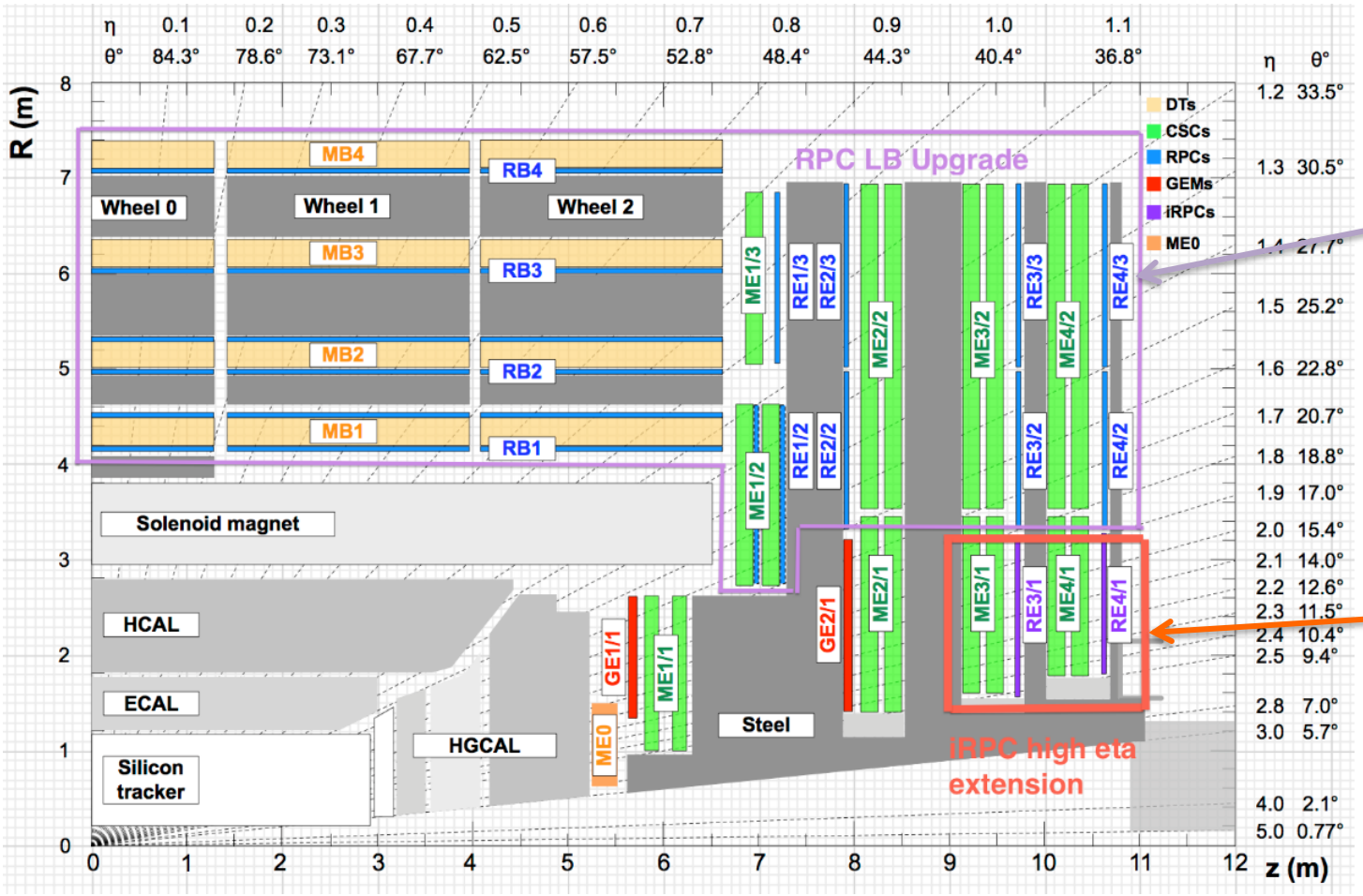
https://indico.ihep.ac.cn/event/16608/

Outline

- Overview of CMS RPC upgrade
- iRPC backend system development status
- Joint test in 904 and quick GIF++ result
- Next plan
- Summary

Phase-II RPC Upgrade Project Overview



Upgrade of Link System to improve timing resolution for existing RPC (**|η| < 1.9**)

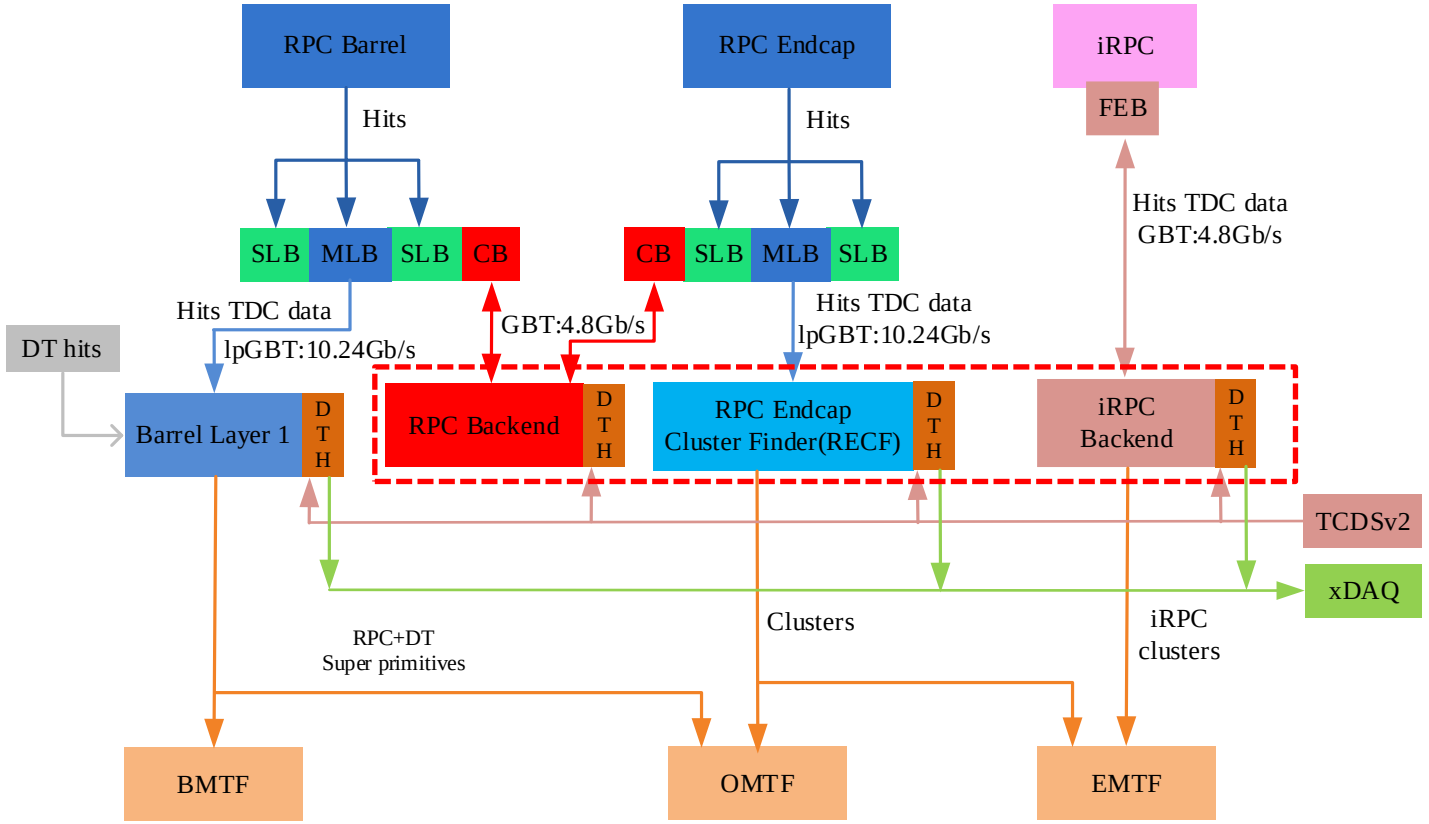
Extend the RPC coverage up to |η| = 2.4 to increase redundancy in high eta region in stations 3 and 4

iRPC/RPC backend and Endcap Trigger Primitive(TP) task

1. **iRPC backend:**
   - Fast/Slow control,
   - Monitor,
   - Data readout,
   - Trigger Primitive(Cluster) Generation

2. **RPC Endcap Cluster Finder(RECF):**
   - Data readout,
   - Trigger Primitive(Cluster) Generation,
   - TP data Fanout

3. **RPC backend:**
   - Fast control,
   - Slow control,
   - monitor,



Schedule and progress

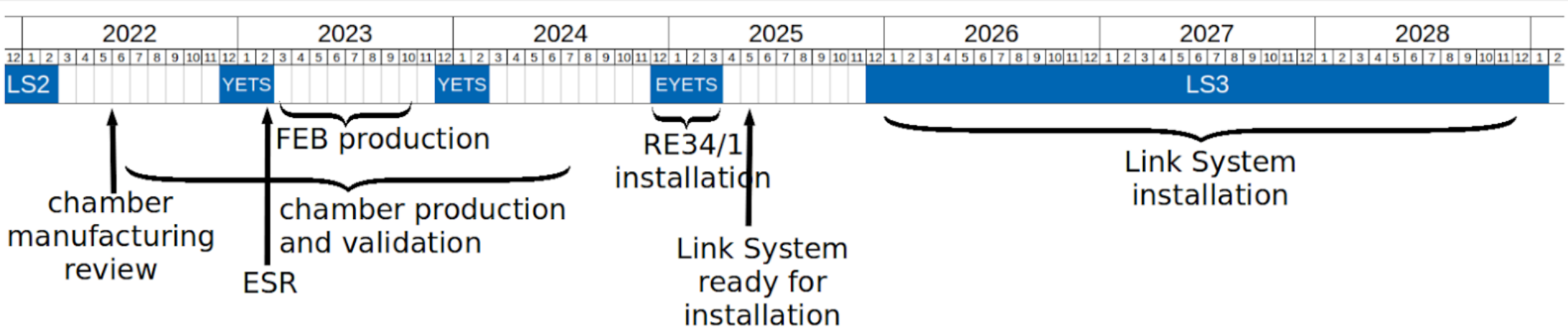
1. iRPC backend and TP

- 2022-2023: iRPC BE µTCA Demonstrator(current work)
- 2024-2025: iRPC BE ATCA installation

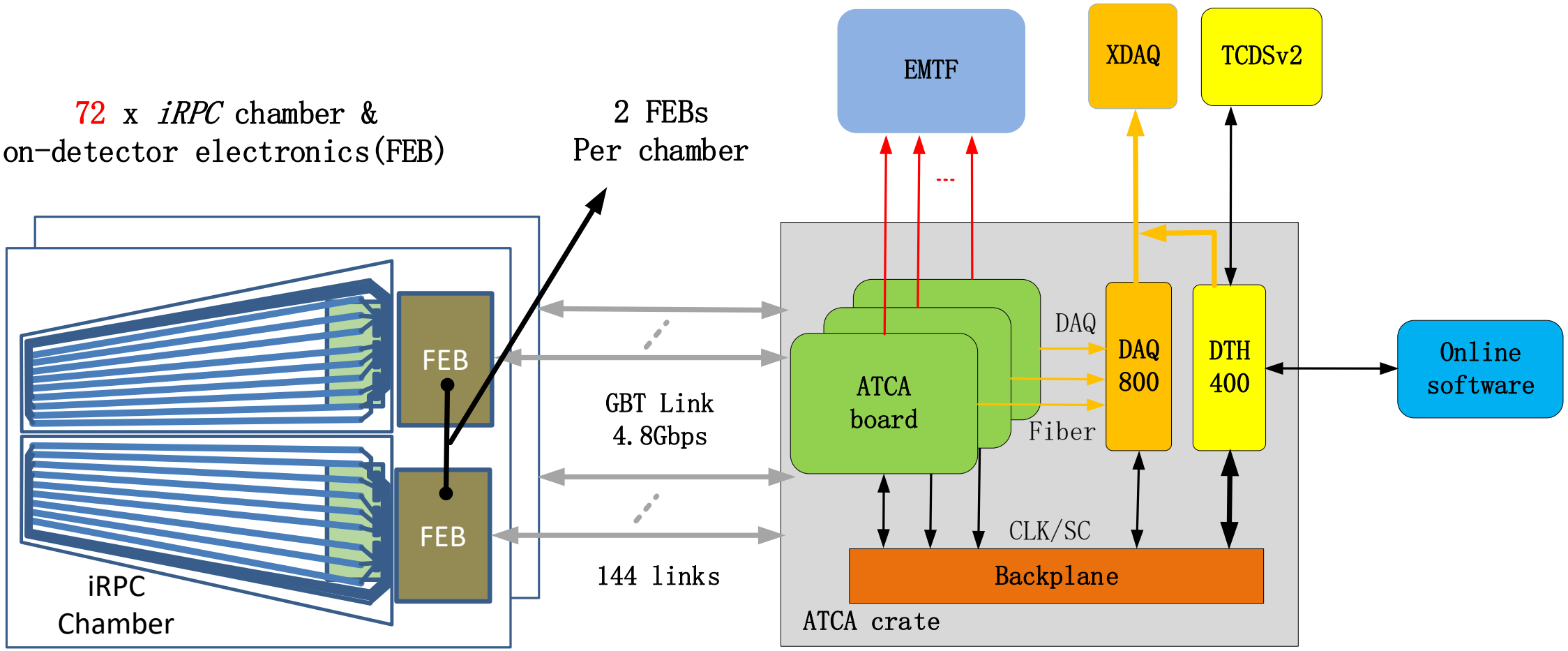
2.(3.)RECF and Backend:

- 2025-2027: RPC RECF and BE ATCA installation

- **Progress in 2022**
  - Joined serenity board design
    - In 2019 IHEP submitted CMS First ATCA prototype board. To keep minimize kinds of board for upgrade, RPC suggest IHEP TRG Group joined Serenity design.
  - iRPC BE Firmware development based on MTCA
  - Joint test with iRPC/FEB in 904
  - Beam test in GIF++



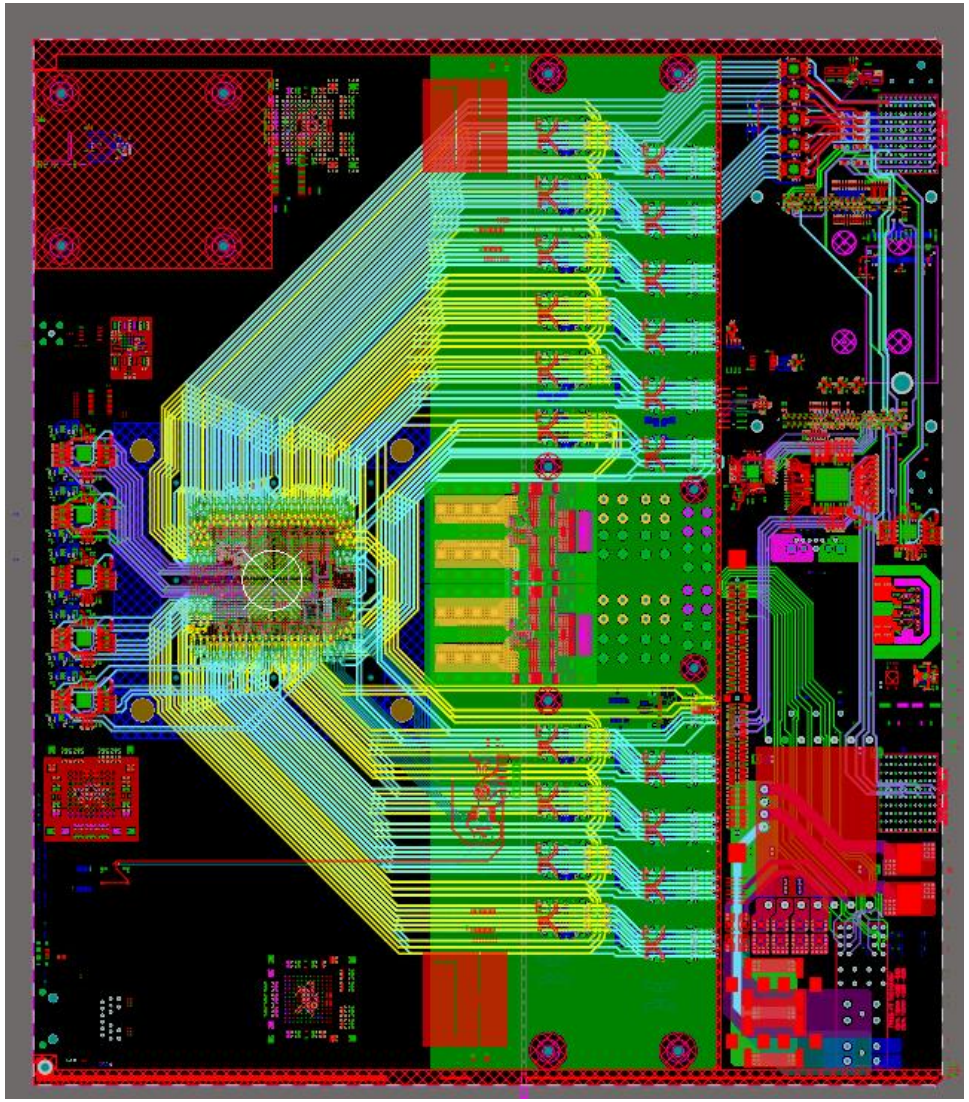
iRPC backend system



1 link including 1 tx and 1 rx

Status of Serenity Board

- Serenity(ATCA) is one of the two backend and trigger boards in CMS Phase-II upgrade, developed by European and Chinese team(IHEP).
- Zhen-An LIU is in Serenity Steering Group.
- Jingzhou ZHAO Joined Technical and Layout Group.
- IHEP team provided clock tree scheme and routing in progress in current stage.
- Final Serenity board in PCB layout phase.
  - Single FPGA design(Serenity-S1)
  - Supports VU13P-A2577 package,
  - 124 bi-dir links @25 Gbps
  - Working on basis 25Gbps 12ch Firefly transceivers will be validated.
  - New->Zynq functionality via Xilinx Kria SoM



iRPC Backend µTCA Demonstrator

iRPC backend µTCA Demonstrator

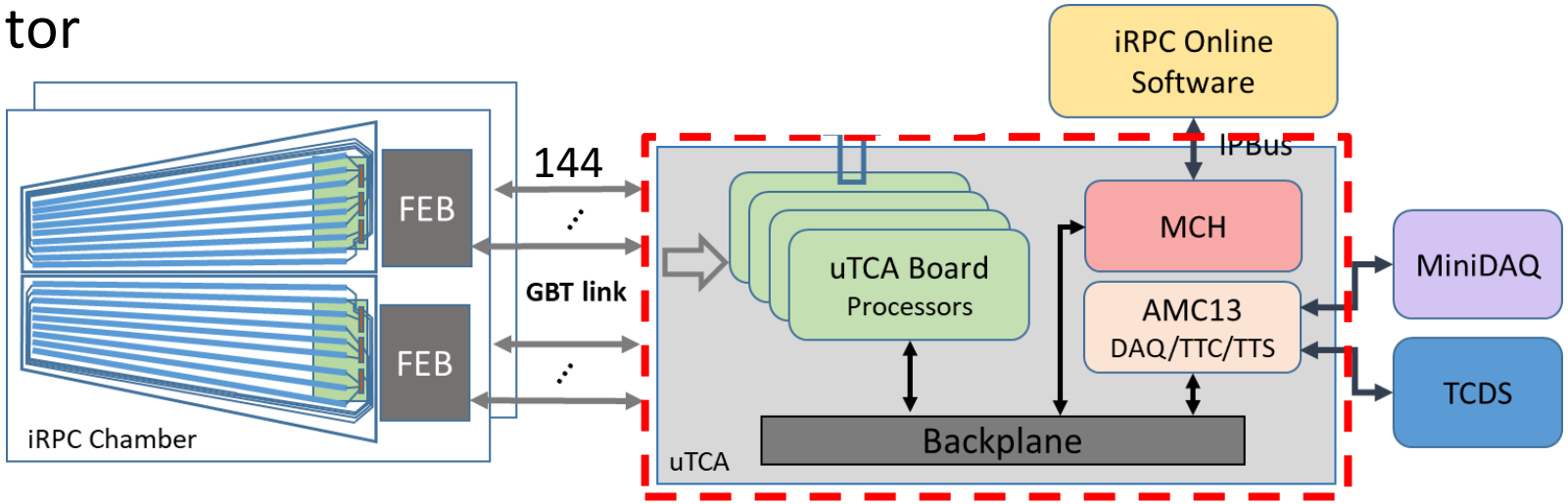
µTCA compliant BE boards
- core board

a µTCA crate,

an AMC13 card,
- system clock and fast control

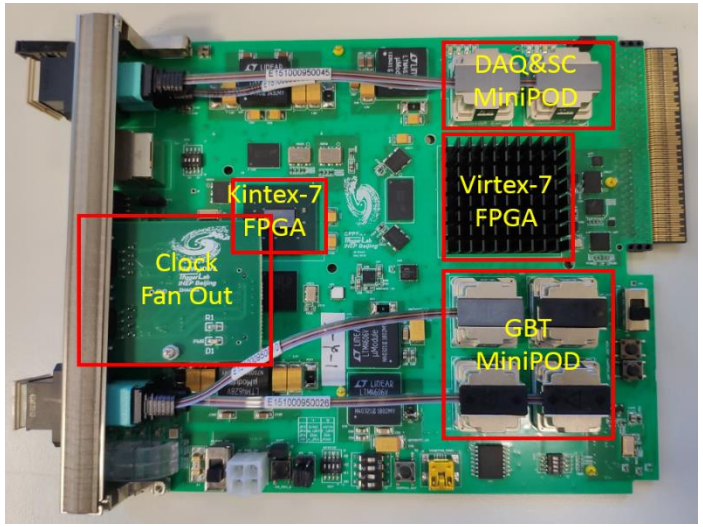
a µTCA Carrier Hub(MCH),
- manage the whole system

a sever PC.
- slow control and DAQ



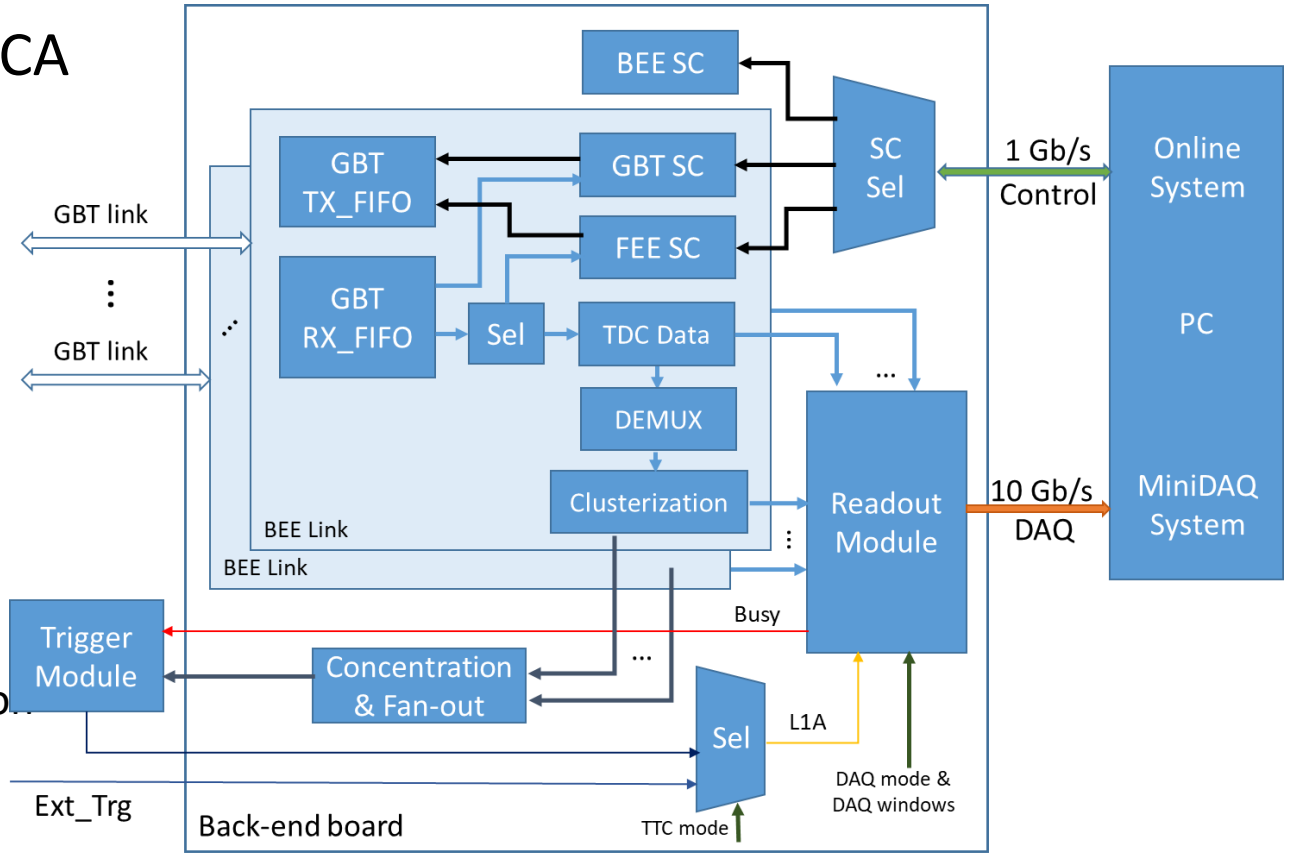
BE board

Virtex-7 FPGA： Core FPGA(GBT Communication with Feb + data processing);
Kintex-7 FPGA： Control FPGA(clock configuration , SC)

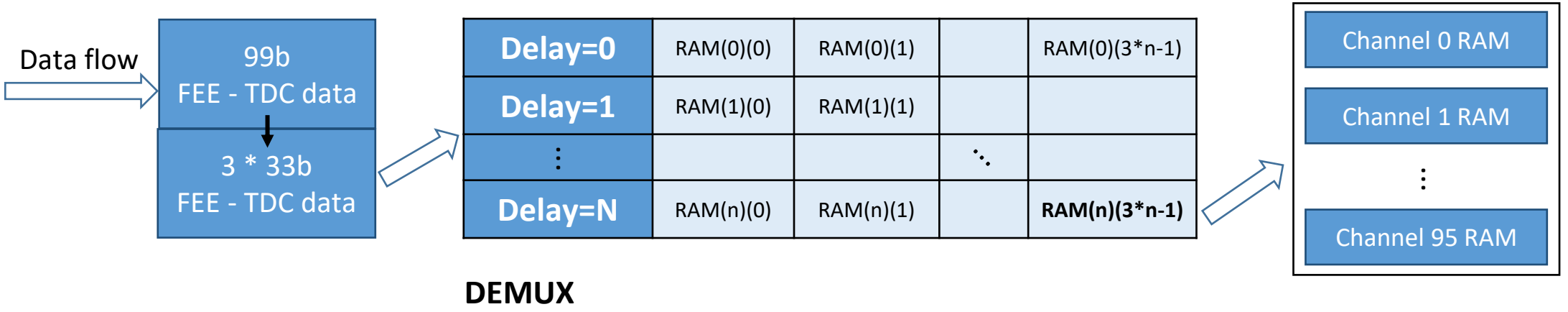


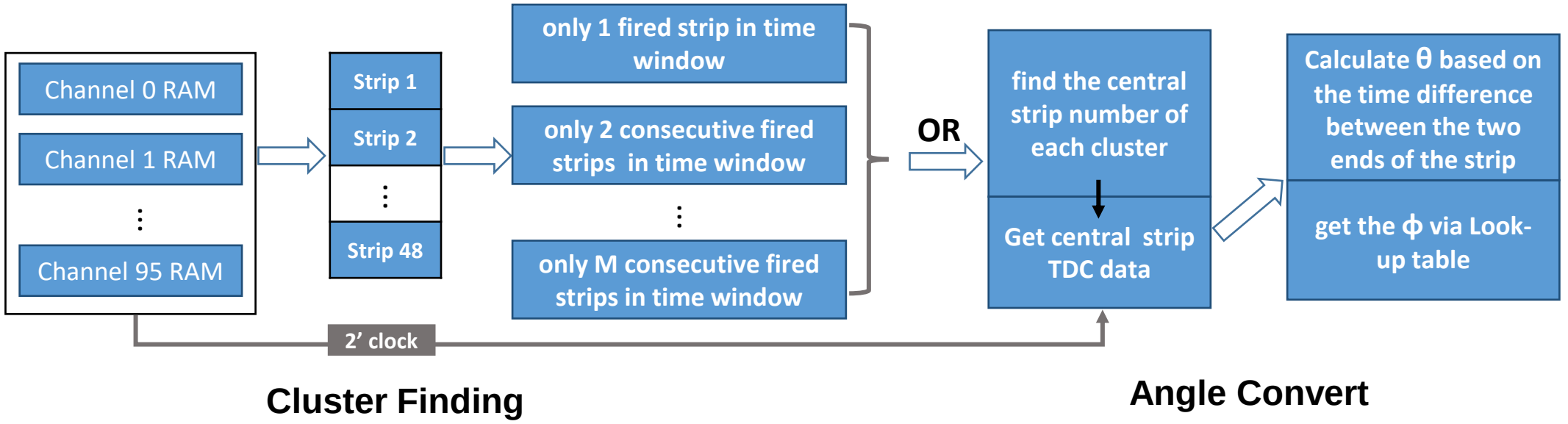
Currently iRPC BE function design

- BE firmware function based on MTCA
  - Transmission link
    - Bidirectional, 4.8Gb/s
  - Fast control
    - BC0/resync
  - Slow control
    - BEE-SC/FEE-SC/GBT-SCA
    - PC to BEB control link
    - 1Gb/s,
      - Sitcp protocol: for single board system
      - Ipbus: for P5 demonstrator system
  - Cluster finding algorithm
    - DEMUX/Cluster finding/Angle conversion
  - Readout algorithm
  - Backend board to PC DAQ link
    - 10Gb/s, TCP/IP



DEMUX, Cluster finding and angle convert flow



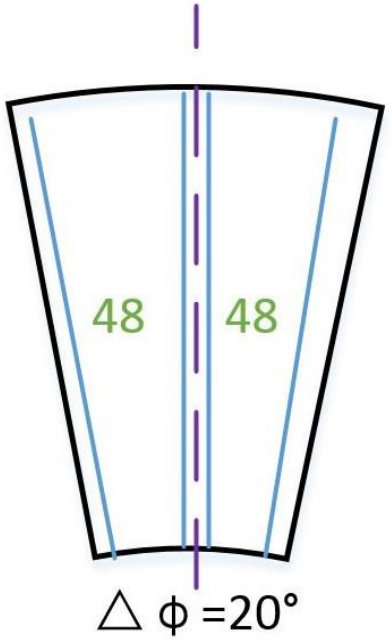


Trigger primitives - Cluster finding (preliminary)

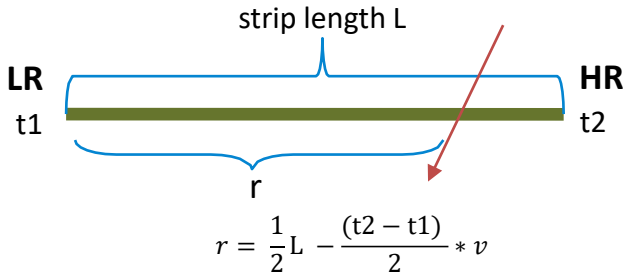
- **Cluster defined in current version of algorithm**
  - Strip with both end signals as fired strip.
  - One to 8 consecutive fired strips defined as a cluster.
  - Cluster center define:
    - If cluster size is odd: the strip in the center as the center of cluster.
    - If cluster size is even: choose the smaller number of the middle two strip as the center of cluster.（This will be upgrade to calculate a center position）
- **Current preliminary cluster finding**
  - Cluster finding within half chamber strips(48 strips).
  - Hit signal are stretched to 2 clocks width.
  - Two clusters maximum for half chamber.

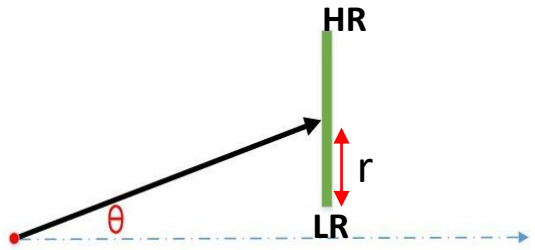
Trigger primitives - Angle conversion

- Angle conversion in current version is based in one chamber, 20 deg.
- Phi calculation for clusters:
  - Phi of center strip: lookup table, 10bits
  - Left to right, phi value increase
- R (theta) calculation for clusters:
  - Calculate the position (r) by the time difference between the both ends of the central strip.
  - R = r * 10 , 11bits



	Strip number	Strip to Phi	Phi value
Left chamber	1	0.1042	5
	2	0.3125	15
	…		
	48	9.8958	494
Right chamber	1	10.1042	505
	2	10.3125	515
	…		
	48	19.8958	994

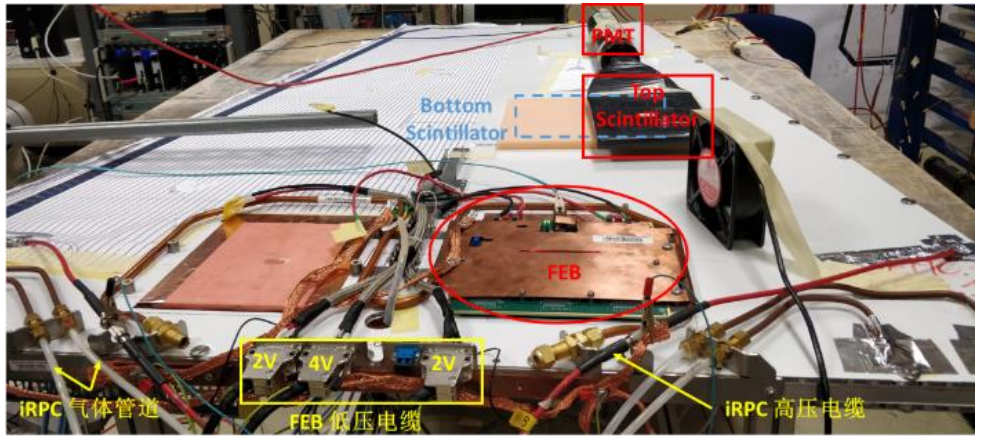


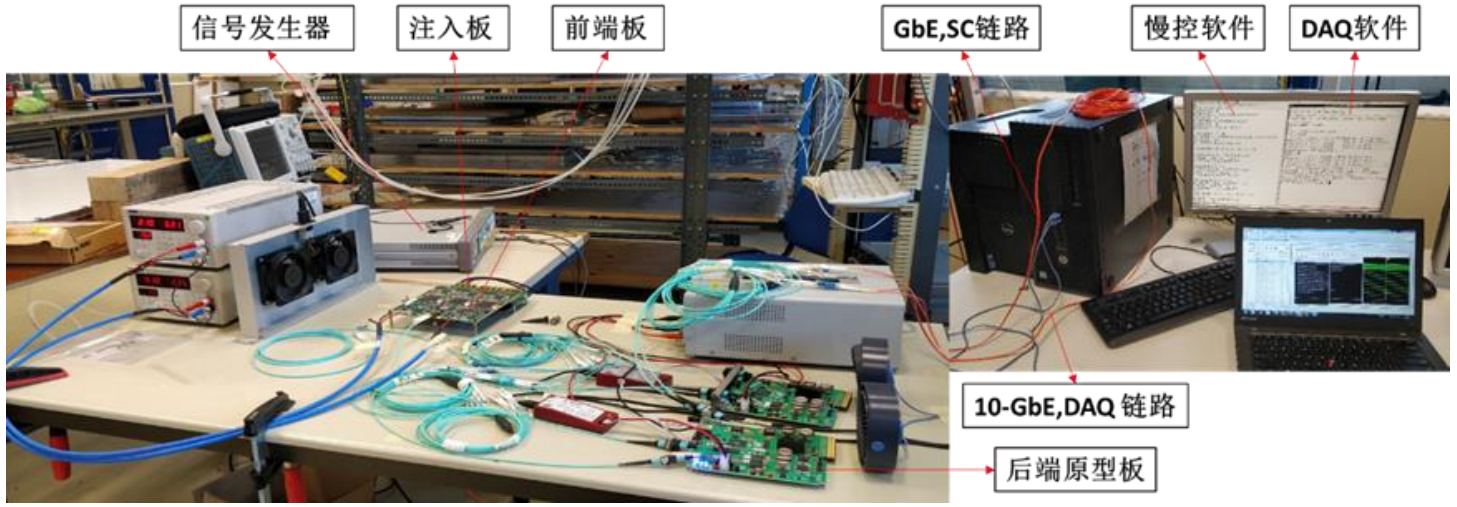


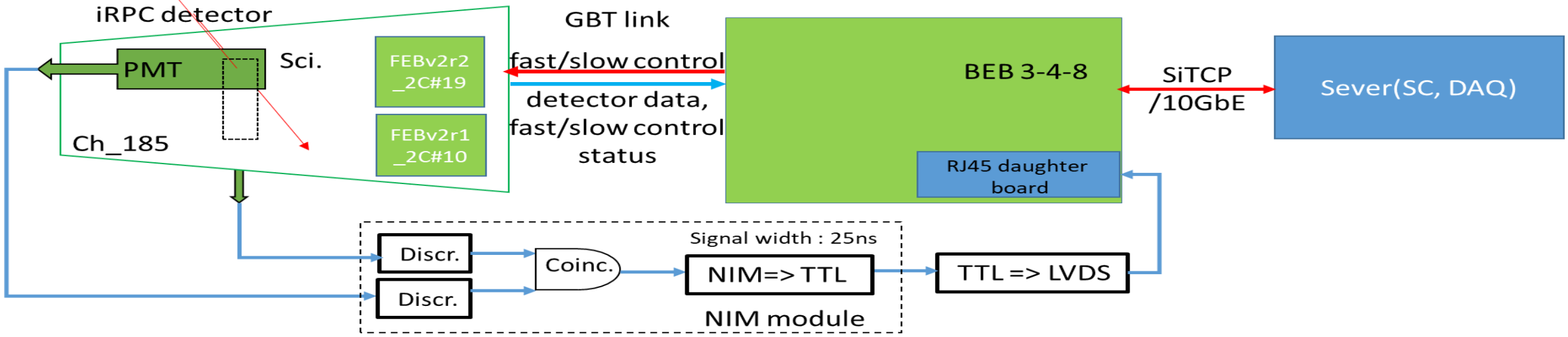
Suggestions to iRPC/FEB firmware

- **Modify unexpected transmission delay in FEB**
  - The TDC data of the FPGA0/2 are found with a delay compared to FPGA1. The delay is not fixed and measured to be 7-9BX(25ns) in the backend.
  - **Influence:** Enlarge readout window and latency on backend.
  - **IHEP suggestion** : remove the 7-9BX delay before transmission to the backend.
- **Check-Sort-Push data transmission mechanism**
  - FEB data sending algorithm: Data with smaller FPGA ID and channel ID have the higher priority to be transmitted.
  - **Influence:**
    - Data produced in same time in different channel will be transmitted with unexpected delay.
    - And when some channels have high occupancy, other channels will have no chance to send out data on time.
  - **IHEP suggestion :** "Check-Sort-Push" algorithm based on timing https://indico.cern.ch/event/967463/contributions/4071622/attachments/2126016/3579438/RPC_electronic_meeting_20201020.pdf

Joint test with FEB and chamber in 904







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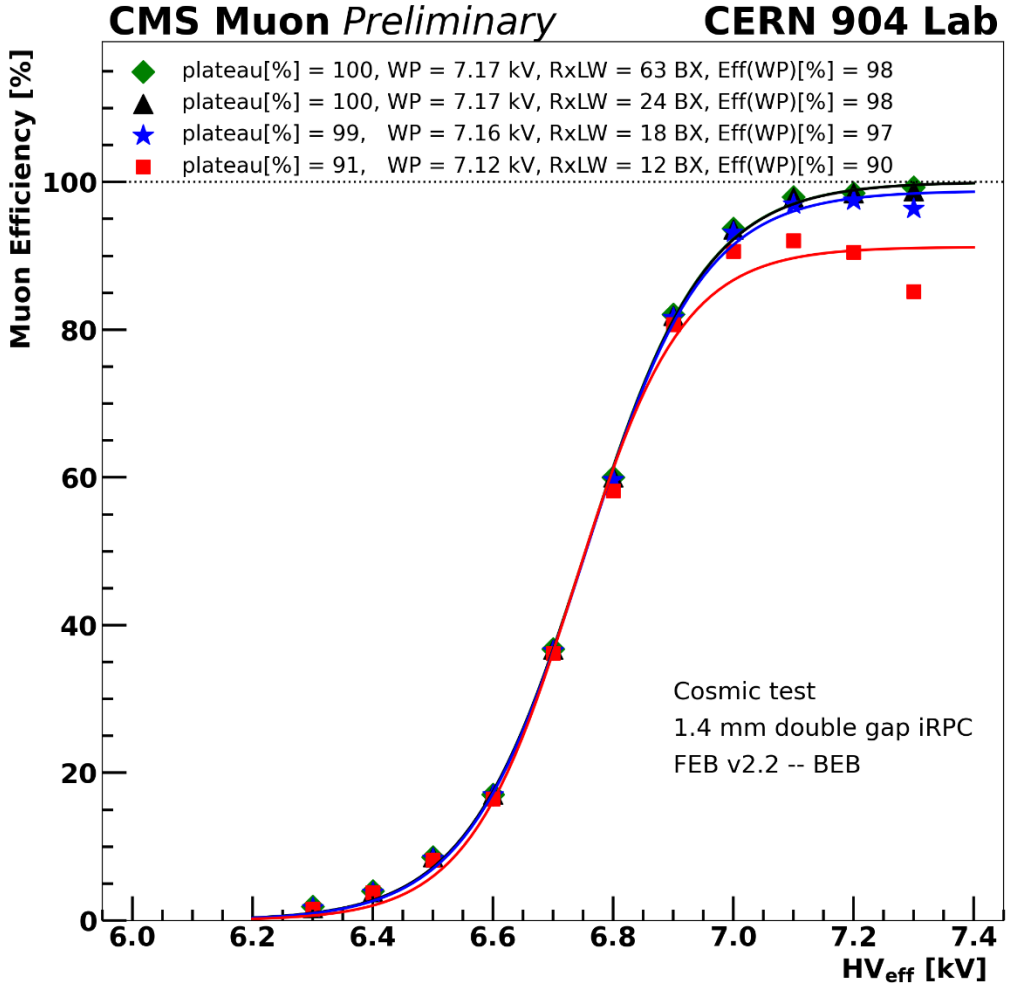
Joint test result --Efficiency scan

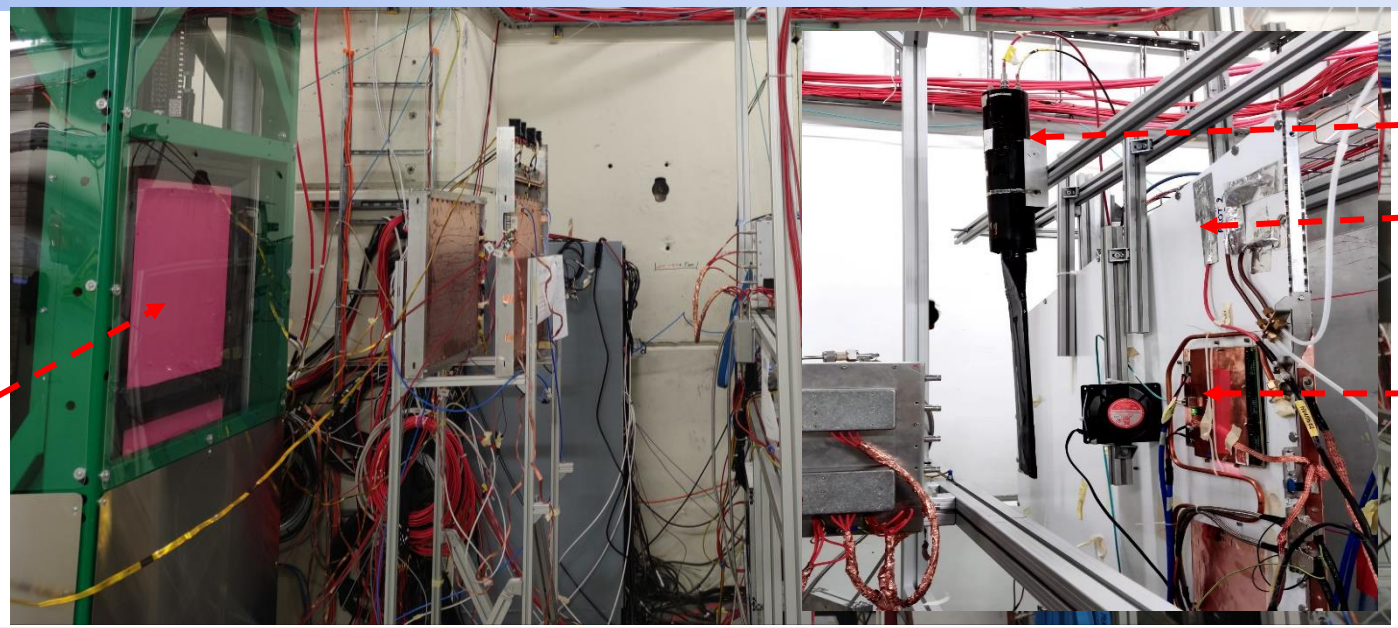
More results and details see HOU Qingfeng's and Weizhuo DIAO's reports.

- This result was acquired using the present FEE parameters and backend system in 904.
  - FEB firmware V1.8,
  - Pertiroc configuration: DAC = 10; CCOMP =14;
  - When RxLW = 12 BX(25ns), the efficiency was not high.
  - And it increases to 100% when the RxLW set as 63 BX(25ns) (Extreme test situation, at the cost of 1 link per BEB).
- Should be improved by implementing Check-Sort-Push mechanism in FEB.



GIF++ beam test system setup

2022.10.19-11.2



γ background source

Sci.(1/4)

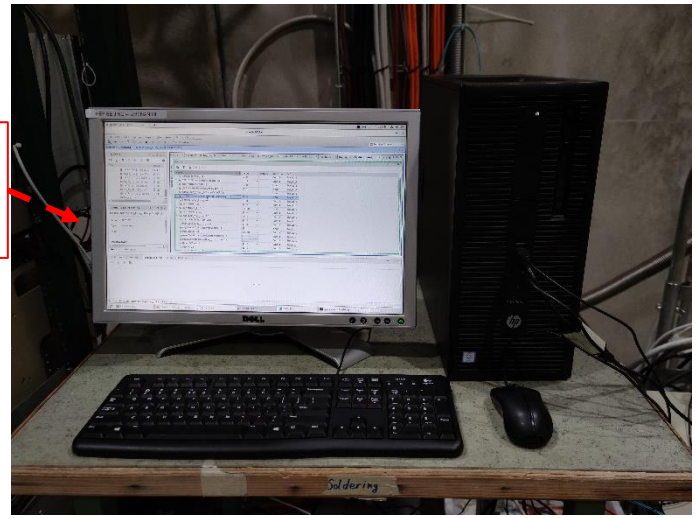
Chamber_190

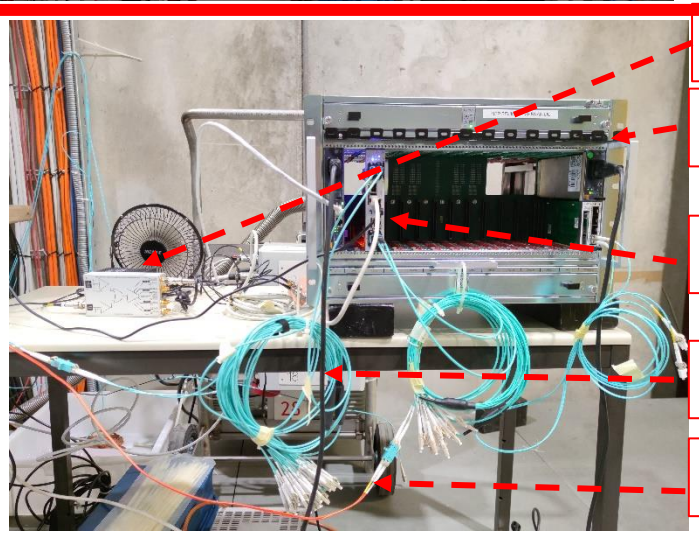
FEB v2_2c

Inside bunker

Outside bunker

DAQ and IPbus/SiTCP SC server





beam trigger

mTCA crate

BEB

GBT link

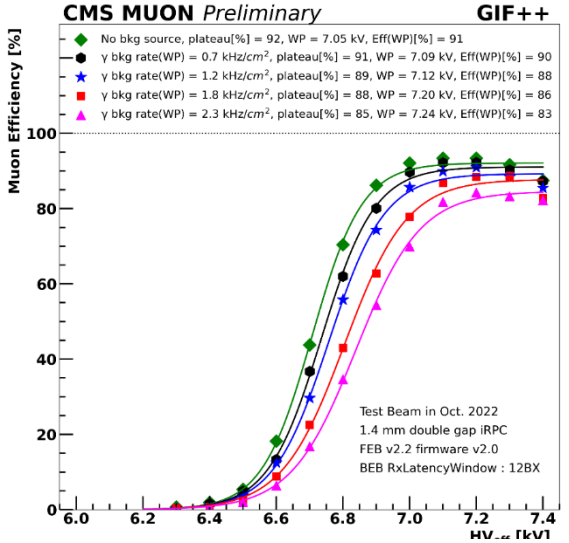
10GbE DAQ

GIF++ beam test quick result

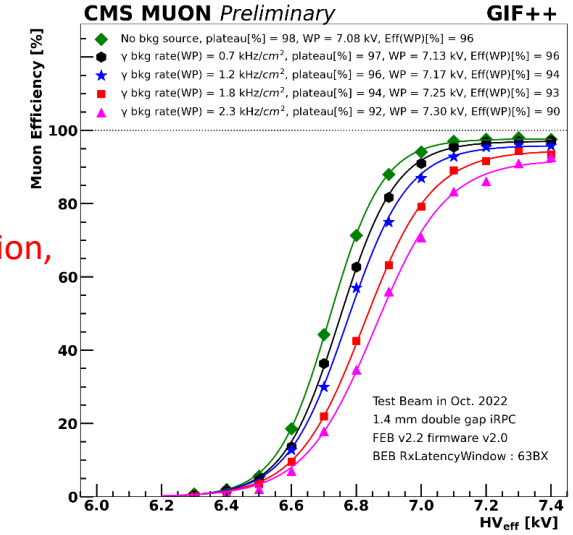
More results and details see SONG Jianing's and Weizhuo DIAO's reports.

- Beam test at GIF++ just finished yesterday (2022.10.19-11.2), showing some quick results.
- Quick result shows that the backend works normally.
  - FEB firmware V2.0
  - Petiroc configuration: DAC = 7; CCOMP = 15;
  - Top right,
    - BEB RxLW= 12 BX(normal window for DAQ),
    - The efficiency under different γ bkg rate is low because of the FEB data sending algorithm.
  - Bottom right,
    - BEB RxLW= 63 BX (Extreme test situation, at the cost of 1 link per BEB, only for joint test),
    - FEB firmware V2.0
- Should be improved by implementing Check-Sort-Push mechanism in FEB.
- More details need to be studied further.

RxLW= 12BX



Extreme test situation, RxLW= 63BX.



Next step plan

- Data analysis of GIF++ beam test for further study on DAQ readout window and clusters.
- Joint test using new FEB firmware with Check-Sort-Push mechanism.
- New version of Cluster Finder algorithm simulation and firmware development.

Summary

- iRPC Backend system has been developed based on µTCA.
- Big progress has been made on joint test with FEB and chamber in 904.
- Quick results show the preliminary success of GIF++ Beam test.

Thanks for your attention.