Status of ATLAS HGTD Peripheral Electronics Board

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2022.11.25

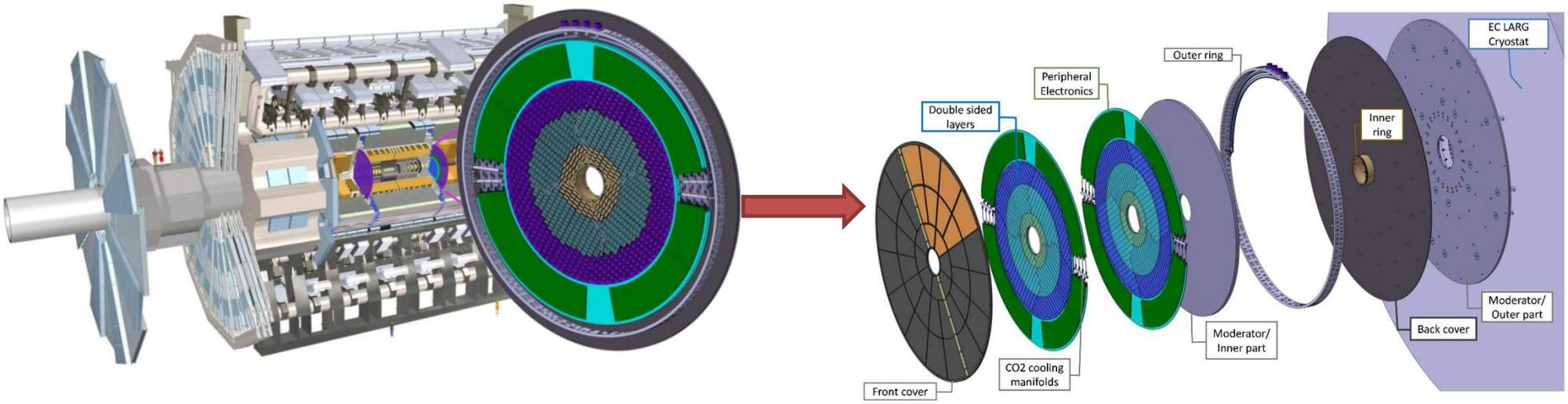
Outline

1. Introduction
2. Modular PEB
   - bPOL12V (DC/DC converter)
   - lpGBT & VTRX+
   - MUX64
   - Script template for PEB
   - Full system testing
3. PEB 1F design
4. Summary

Introduction

❑ High Granularity Timing Detector (HGTD)

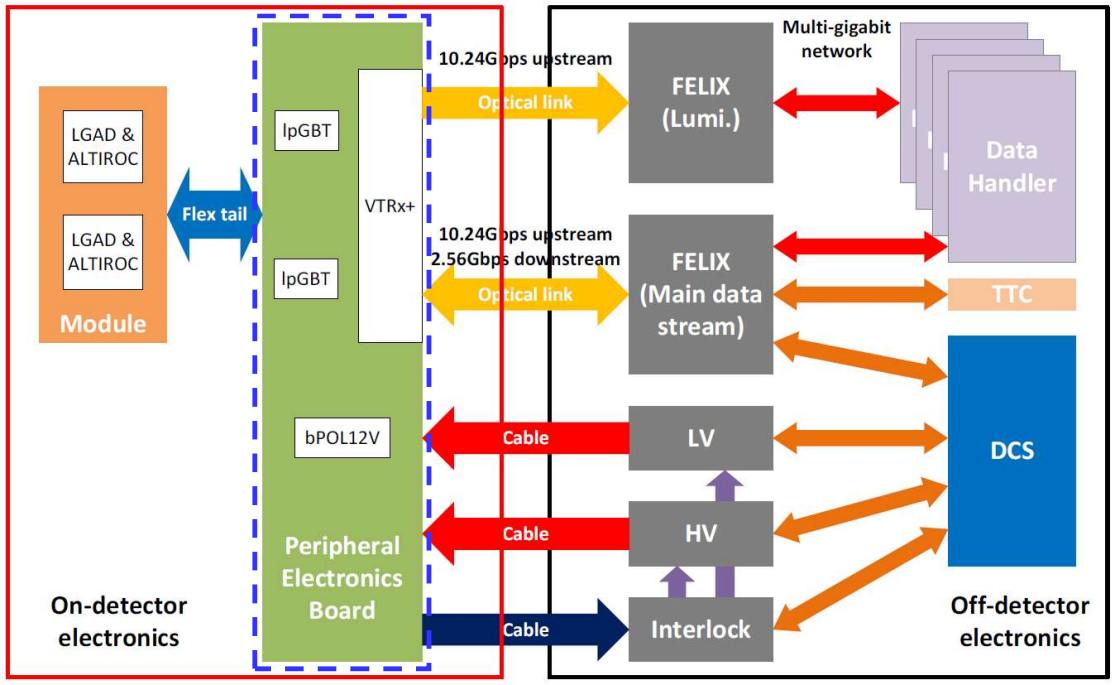
- ATLAS Phase II upgrade project
- Providing an accurate measurement of the time of tracks (< 50 ps)
- Provide an instantaneous measurement of the luminosity
- Located in the gap region between the barrel and the end-cap calorimeters



Introduction

❑ HGTD Readout Electronics

- On-detector
  - ➢ Module:
    - Module flex PCB
    - Two read-out Chips(ALTIROC)
    - Two Low Gain Avalanche Sensors (LGADs)
  - ➢ Flex tail cable
  - ➢ Peripheral Electronics Board
- Off-detector
  - ➢ Data Acquisition System (DAQ)
  - ➢ Timing, Trigger and Control (TTC)
  - ➢ Detector Control System (DCS)
  - ➢ Low Voltage/High Voltage system
  - ➢ Interlock system

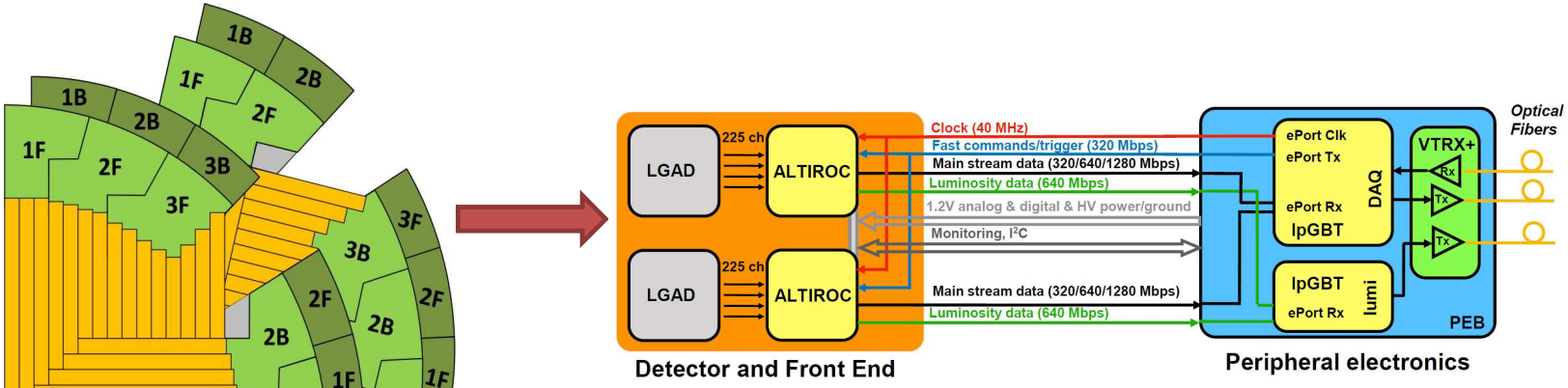


Introduction

❑ HGTD Peripheral Electronics Boards (PEB)

- Located at the outer radius of the active detector area
- Control, Monitoring & Data transmission
- Power-supply distribution: LV & HV
- Routing of temperature sensors for the interlock system
- Hosting DC/DC converter, lpGBT, optical transceiver (VTRX+), and MUX64

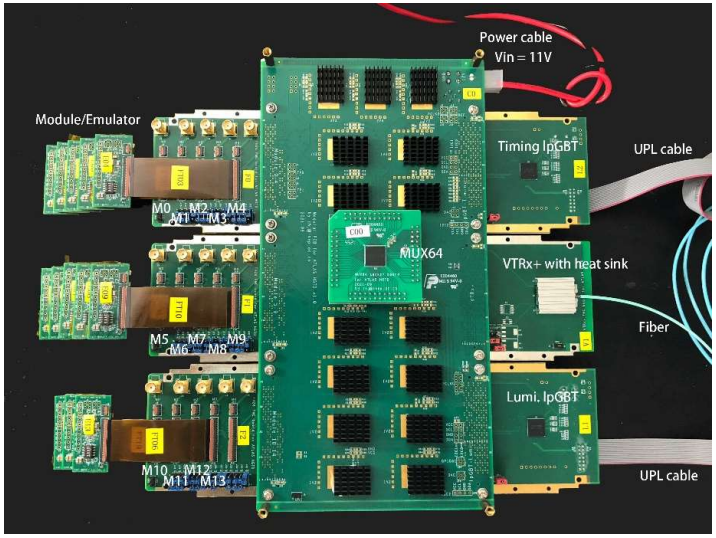
PEB	Total Qty.
1F	32
2F	32
3F	16
3B	16
2B	32
1B	32

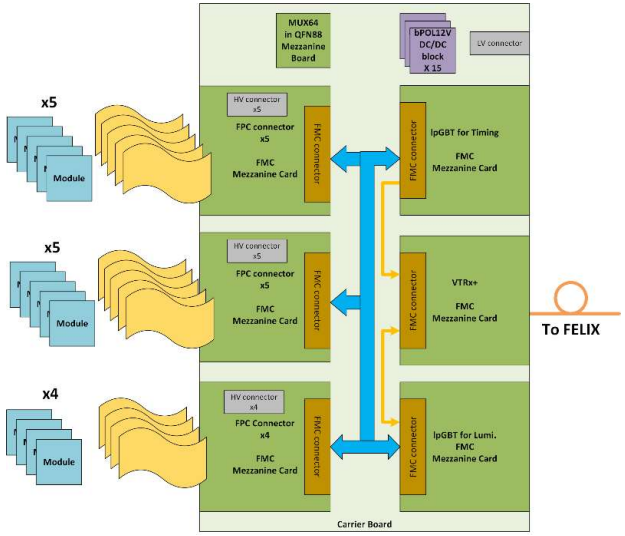


Modular PEB design

❑ Modular PEB

- A minimal system with full functions
- Disassembling PEB into sub-boards which can be connected by connectors
- Verifying the functions of each sub-boards and connectors
  - ➢ bPol12V (DC/DC converter), lpGBT, VTRX+, MUX64, FPC connector
- Connecting them together and verifying the functions in system level.





bPOL12V (DC/DC converter)

- Supplying the 1.2V and 2.5V required by ASICs
  - module, lpGBT, MUX64, and VTRX+
  - Efficiency

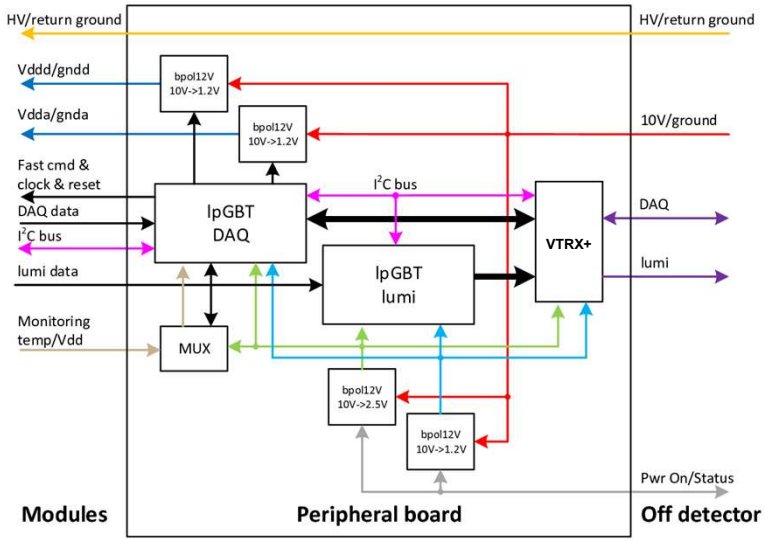
    53% ~ 63%

    The lower temperature, the higher the efficiency
  - Ripple

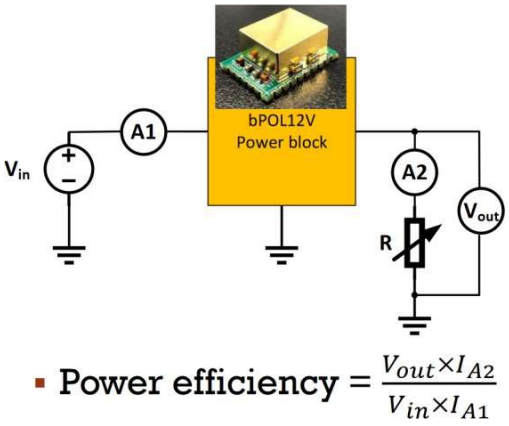
    2-10 mV

    The more output current, the larger output ripple

    Irregular point at 0.75A

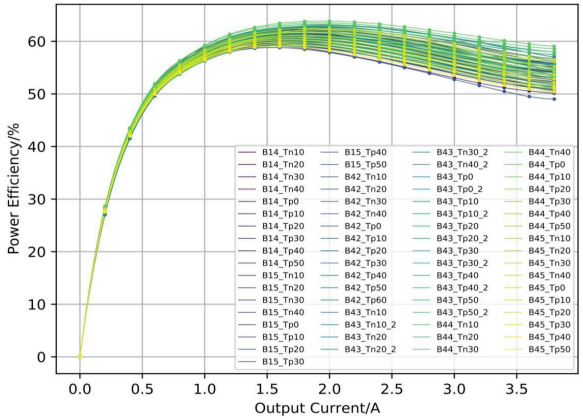


bPOL12V

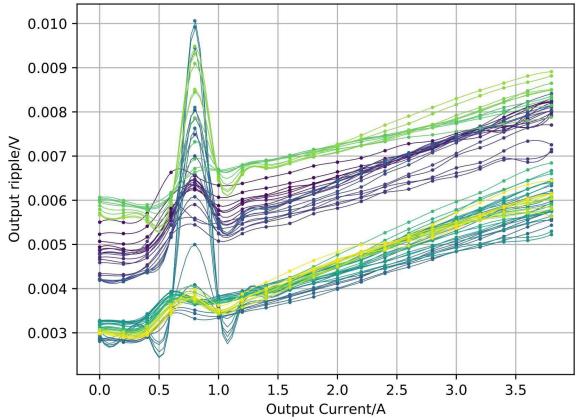


- Power efficiency = $\frac{V_{out} \times I_{A2}}{V_{in} \times I_{A1}}$

test setup



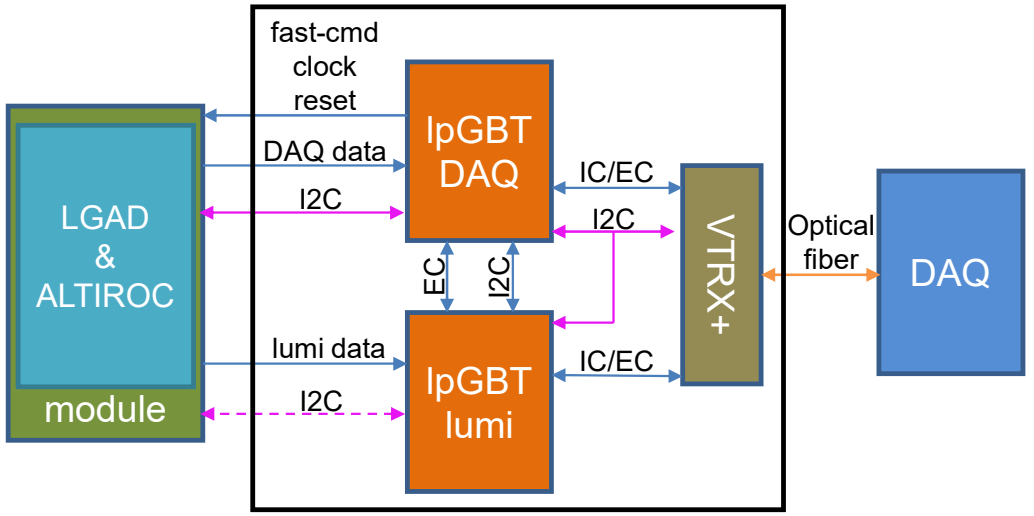
efficiency



ripple

lpGBT & VTRX+

- lpGBT
  - Data encoding and decoding
  - Transceiver
- VTRX+
  - Optoelectronic component
- Communication test
  - Clock and fast-cmd



Peripheral Electronics-Data stream

FELEX and modular PEB	Jitter (ps)			Duty			Skew between clk and fast-cmd (ns)		
ECLK	40MHz	320MHz	640MHz	40MHz	320MHz	640MHz	40MHz	320MHz	640MHz
Test points on PEB(without flex tail)	5.256	6.473	6.291	50.20%	50.95%	51.32%	1.353	1.446	0.020
Test points on bare module flex with 70 cm flex tail	7.314	7.586	7.254	50.19%	50.90%	51.28%	1.498	1.489	0.099
Test points on digital module with 70 cm flex tail	8.052	7.863	7.747	50.19%	50.88%	50.87%	1.550	1.548	0.119

lpGBT & VTRX+

- Communication test
  - I2C: write & read

Writing to module

```
(python_env) [user@localhost script]$ python3 configure.py config/altiroc/m8.yaml --dacCharge 12 --dacVth 540
Configure: module: 8, chip: 0

config/b8_startup_and_periphery.txt ========================
config/enableAllMatrix.txt ========================
config/VTHC/vthcScan_B_8_On_all_Inj_0_test.txt ========================
Injection:  0
Injection:  1
Injection:  2
            ⋮
Injection:  223
Injection:  224
```

Reading from module

```
(python_env) [user@localhost script]$ python3 altiroc2_test.py
Use default module: 6
module ID: 6, chip ID: 0:
[0, 176, 30, 236, 0, 176, 28, 128, 0, 176]
module ID: 6, chip ID: 1:
[0, 176, 30, 236, 0, 176, 28, 128, 0, 176]
```

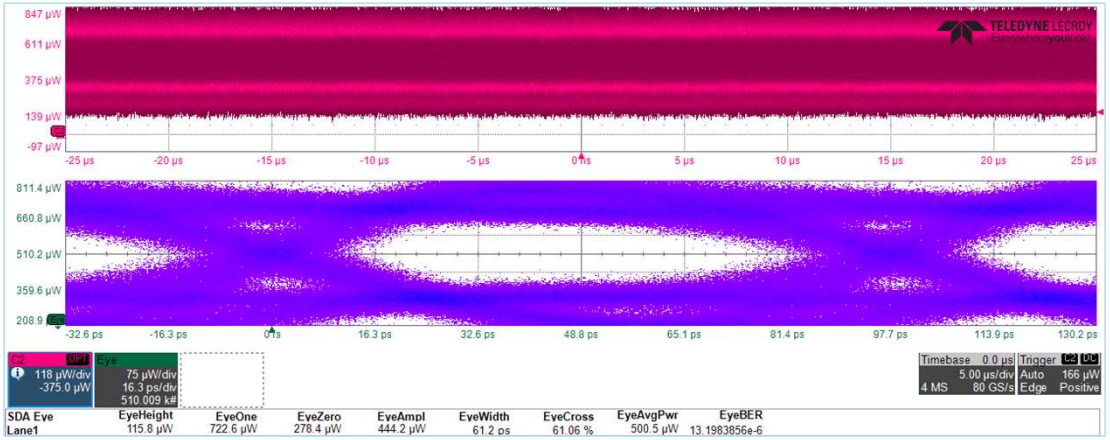
lpGBT & VTRX+

- Communication test
  - Bit Error Rate Test (BERT)

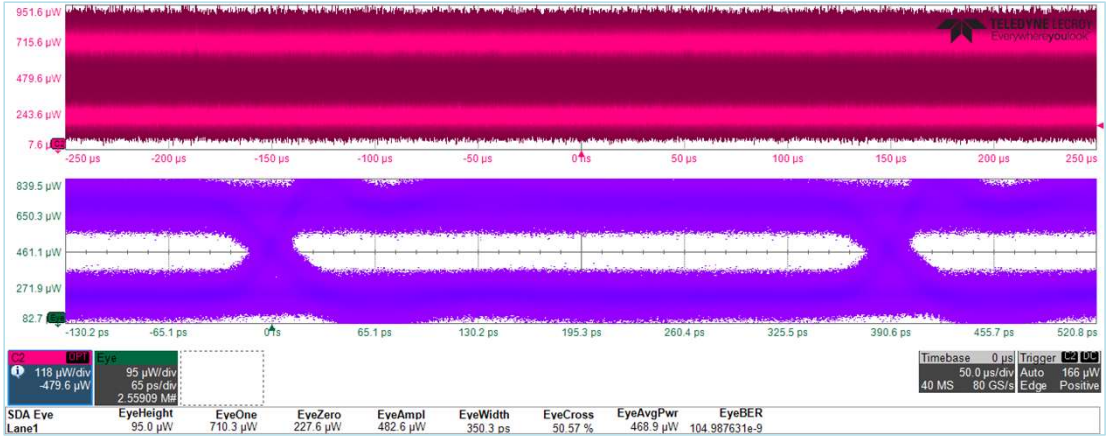
    Test by optical eye diagram

Determining configuration based on BERT result !

Uplink: 10.24Gbps



Downlink: 2.56Gbps



MUX64

- An analogue 64-to-1 multiplexer ASIC
- Transmitting 1 of 64 analogue monitoring signals.
- Details: Qiyu and Zifeng's report (The 8th China LHC Physics Workshop)

Test result

Technical Progress

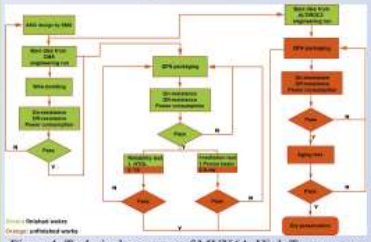


Figure4. Technical progress of MUX64. High Temperature Operating Life(HTOL). Temperature Cycling(TC)

- A total of 92 × 3 dies from CMS engineering run were wire-bonded to PCBs or being packaged chips by QFN88.

Test Setup

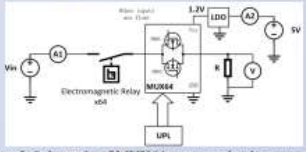


Figure5. Schematic of MUX64 mass production test setup.

Automatic test system

- A 6-bits address on the USB programmer board for lpGBT (UPL) [3] and 64 relays

Figure6. The MUX64 test-kits are shown for (a) a wire-bonded bare die, (b) a test socket for the QFN88chips, (c) a 64 electromagnetic relays, (d) the UPL used to select ON-channel for MUX64.

Quality Assurance

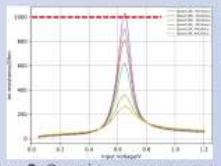


Figure7. On-resistance measurement of a wire-bonded MUX64

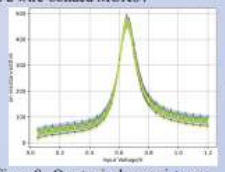


Figure8. One typical on-resistance curve of a QFN packaged MUX64 measured at 20°C

On-resistance measurement at different working temperatures

- Tested temperature ranges from -41 to +85 °C. A maximal on-resistance at 0.65 V increases as the temperature decreases.
- On-resistance of the measured MUX64 meets the design demand at -30 °C.

Batch quality assurance test

- On-resistance dependence of MUX64 is measured from 0.05 V to 1.20.

Power Consumption

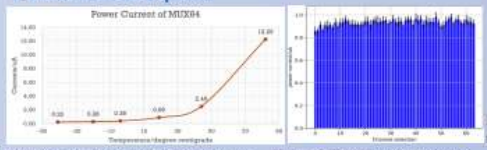


Figure9. Power consumption vs working temperature

Figure10. Power consumption vs selected channel measured at 18 °C

- Power consumption at -20 °C was 0.336 μW, much less than the design requirement 1 mW.

High Temperature Aging Test

Testing strategy

- A total of 32 MUX64s are mounted on a batch testing PCB and tested in a thermal chamber.

Figure11. Photo of MUX64 reliability test setup

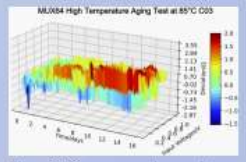


Figure12. One measured on-resistance deviation in 16 days at 85 °C.

High Temperature Operating Lifetime test result

- 32 MUX64 demonstrated negligible degradation over 16 days burn-in process of 85 °C.
- According to the Arrhenius acceleration model, lifetime for MUX64 is no less than 4 years at 60% confidence level.
- The largest on-resistance deviation during burn-in < 5 Ω.

Figure13. Dry air were injecting into the thermal chamber to reduce dewing.

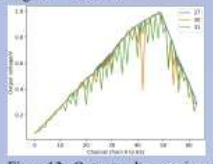


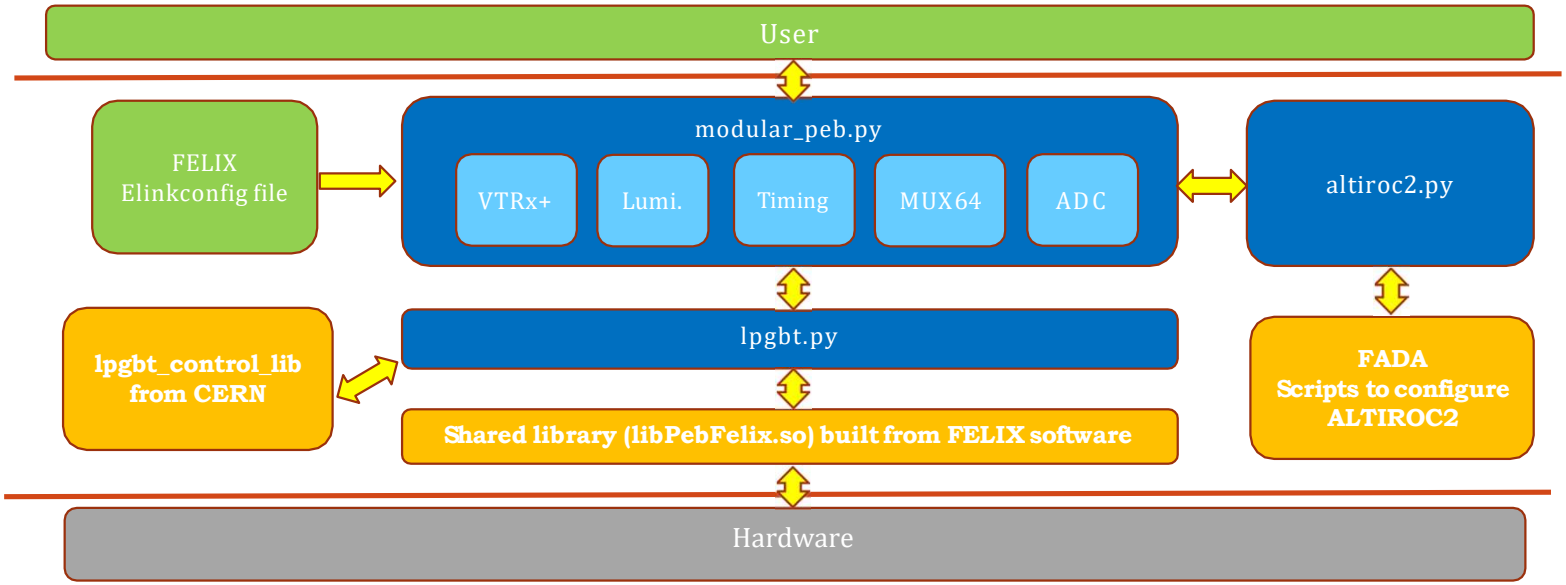
Figure13. Output voltage vs input channel in a temperature cycle. Recoverable errors are found for No. 24 and No. 25.

Temperature Cycling test result

- The temperature cycle ranges from -40 to +80 °C. Both heat up and cool down takes 30 minutes.
- A total of 32 QFN88 MUX64 sustained 300 temperature cycles. Loose contacts of the testing PCB cause recoverable errors as shown in figure 13.

Script template for PEB

- Bridge between hardware and software
- Hardware-related initialization
- Module initialization and configuration
- ADC calibration
- Module readout and threshold scan



Gitlab: [atlas-hgtd / hgtd-PEB · GitLab (cern.ch)]

Full system testing

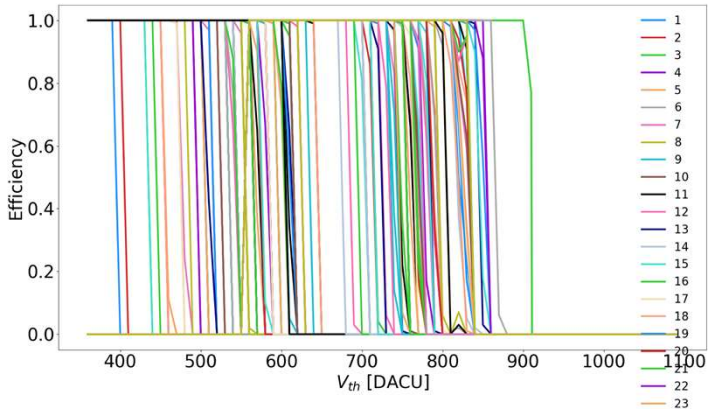
- Data taking

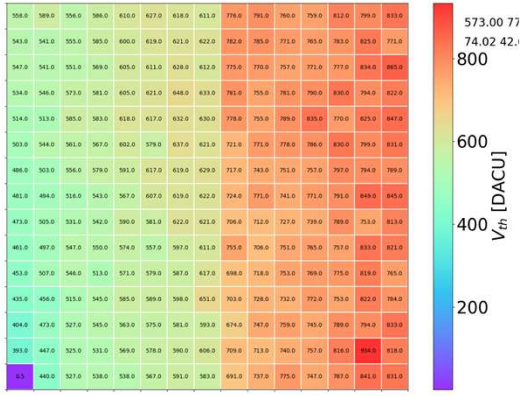
Fast-CMD

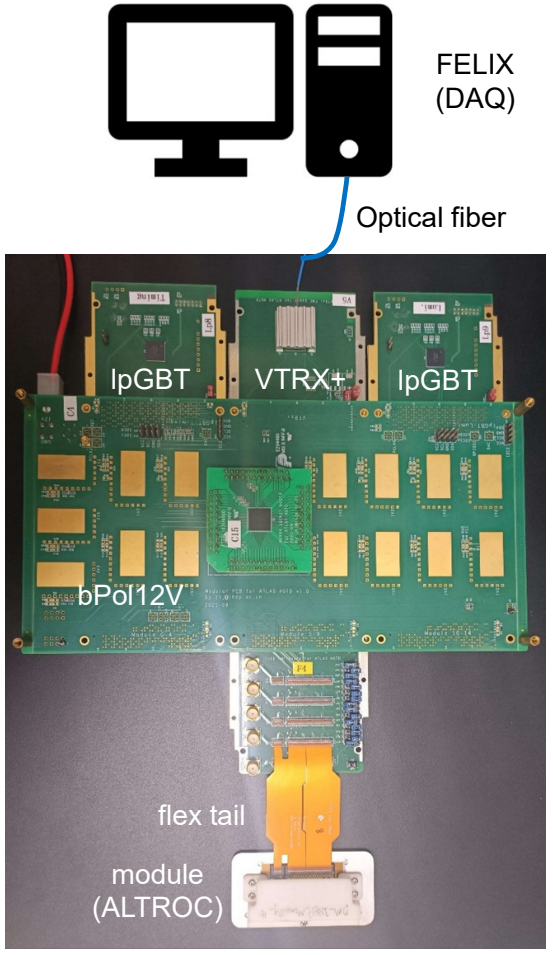
Data

```
(python_env) [user@localhost script]$ fcheck daq_10vth-1.dat -F 20
Chunk types: BOTH="<<", FIRST="++", LAST="&&", MIDDLE="==", TIMEOUT="]]", NULL="@@",
OUTOFBAND="##" and "TEC" for chunk truncation/error/CRCerr.
=> File: daq_10vth-1.dat
Blocksize: 1024
==> BLOCK 0 (E=600=24-0 seq=0): 1007 bytes payload (31 data)
 c2 92 90  0  0  0  0 e7 40  0  0 c0 d3 1a  1  0  0  0  0 e7 40  0  0  0  0  0  0  0  0 << (sz=31)
 @@
 ]] (sz=976)
==> BLOCK 1 (E=00A=0-10 seq=0): 1008 bytes payload (360 data)
 20 1e c1 7e 7f ff 7d 7f ff 7c 7f ff 7b 4f 7f 7a 20 ff 79 7f ff 78 55 7f 77 54 ff 76 58 ff 75 7f
 ff 74 36 ff 73 22 ff 72 7f ff 71 5f ff 70 7f ff 6e 7f ff 6d 7f ff 6c 4d ff 6b 50 7f 6a 7f ff 69
 7f ff 68 7f ff 67 7f ff 66 7f ff 65 7f ff 64 7f ff 63 1c a5 62 31 7f 61 7f ff 60 7f ff 5e 7f ff
 5d 7f ff 5c 4f ff 5b 7f ff 5a 44 7f 59 56 7f 58 7f ff 57 50 7f 56 7f ff 55 24 ff 54 7f ff 53 23
 ff 52 7f ff 51 7f ff 50 7f ff 4e 7f ff 4d 2a 7f 4c 2a 7f 4b 7f ff 4a 7f ff 49 7f ff 48 50 7f 47
 7f ff 46 51 ff 45 29 ff 44 54 7f 43 7f a0 42 7f ff 41 7f ff 40 7f ff 3e 51 ff 3d 7f ff 3c 24 7f
 3b 21 ff 3a 7f ff 39 7f ff 38 52 ff 37 56 ff 36 7f ff 35 7f ff 34 7f ff 33 7f ff 32 7f ff 31 7f
 ff 30 7f ff 2e 7f ff 2d 7f ff 2c 2c 7f 2b 55 7f 2a 7f ff 29 1d ff 28 2e ff 27 7f ff 26 7f ff 25
 7f ff 24 7f ff 23 4f ff 22 2d ff 21 7f ff 20 2a 7f 1e 7f ff 1d 7f ff 1c 7f ff 1b 4f ff 1a  3 7f
 19 50 7f 18 7f ff 17 5b 7f 16 62 ff 15 7f ff 14 7f ff 13 59 ff 12 7f ff 11 7f ff 10 7f ff  e 50
 ff  d 7f ff  c 4f ff  b 7f ff  9 48 7f  8 54 ff  7 5d 7f  6 5b 7f  5 7f ff  4 4f ff  3 51 ff  2
 7f ff  1 26 ff f0 6f d7 << (sz=360)
```

- Threshold Scan

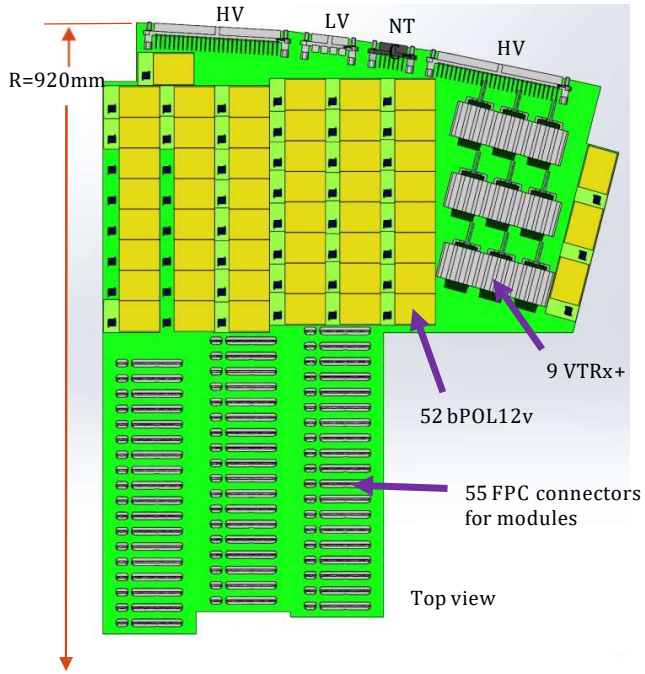






PEB 1F design

- At least nine times more complex than the modular PEB
- Details of the design
  - https://gitlab.cern.ch/atlas-hgtd/hgtd-peb/-/blob/master/design/PEB.xlsx
- Schematic and PCB design
  - Finished schematics
  - https://gitlab.cern.ch/atlas-hgtd/hgtd-peb/-/tree/master/peb/1F
- PDR
  - 15 December 2022
  - https://indico.cern.ch/event/1223224/



PEB 1F

Summary

- The verification of the sub-boards are almost completed
- The full system testing for modular PEB is ongoing
  - First full chain for HGTD

    Hardware -> 4 sites (CERN, Nikhef, KTH and IHEP) run

    Software -> script template released to help to learn the hardware

    CERN and IHEP complete the Vth scan for modules
  - Next step:

    Module and noise level evaluation and comparison

    Ground selection
- The design of PEB prototype 1F is ongoing
  - Finished the schematics
  - PDR : 15 December 2022

Thank you !