V3-LD-Partial-Half Bottom Design

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Nov 25, 2022, CLHCP

Introduction

The LHC will be upgraded to collect ten times more data than the initial design.

Phase-2 upgrade of the CMS experiment, the High Granularity Calorimeter (HGCAL) is developing.

CMS high granularity End-cap Calorimeter

	CE-E	CE-H	
	Si	Si	Scintillator
Area (m^2)	368	215	487
Channels (k)	3916	1939	389
Si modules (Tileboards)	16008	8868	(3960)
Partial modules	1008	1452	–
Weight (t)	23	205	
Si-only planes	28	8	
Mixed (Si+Scint) planes		16	

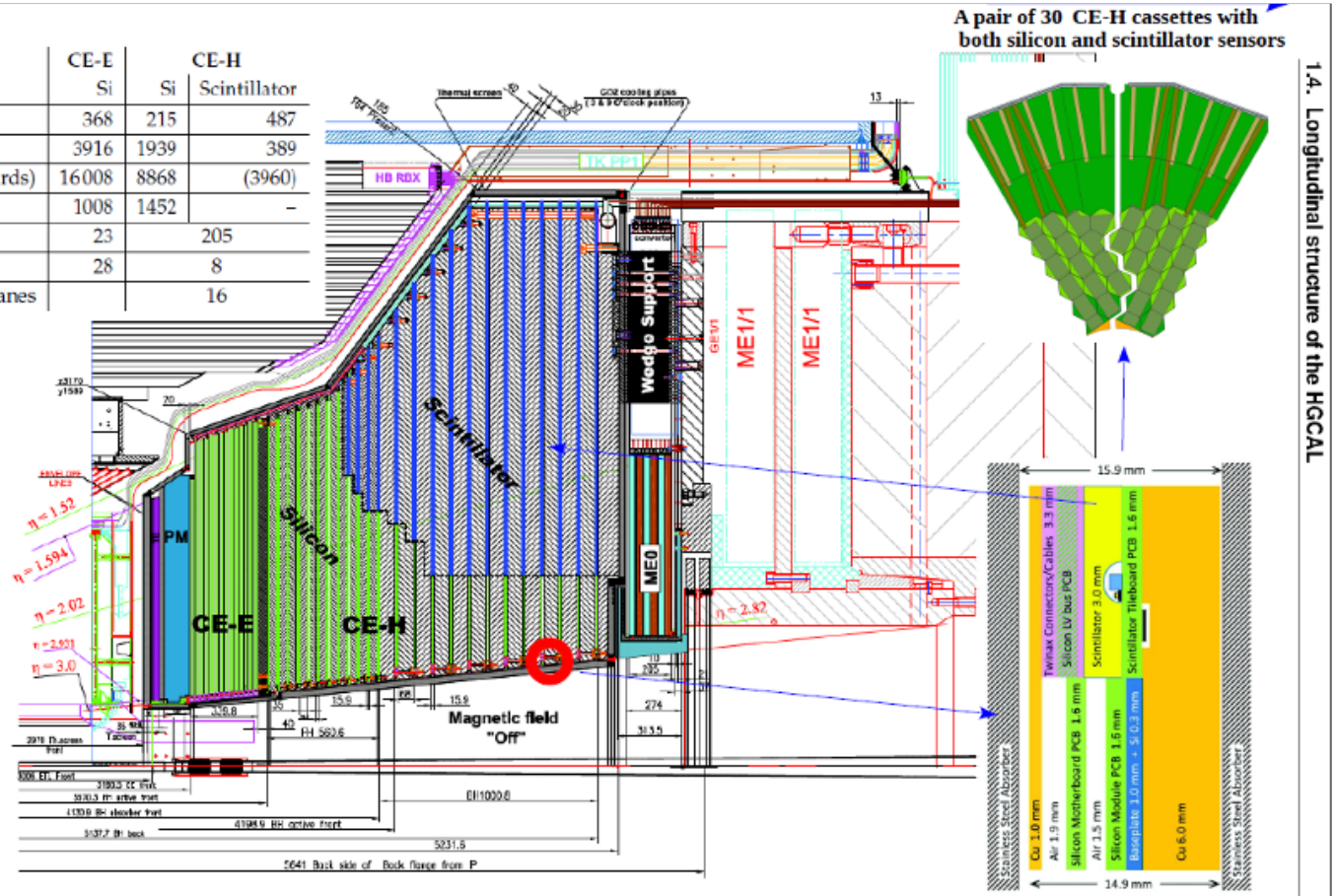
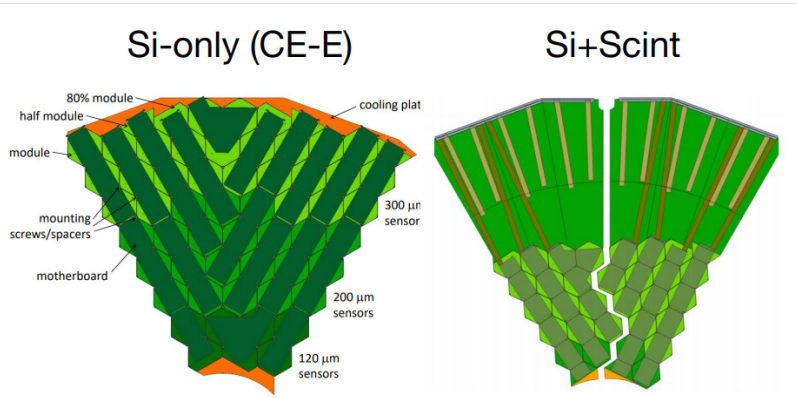
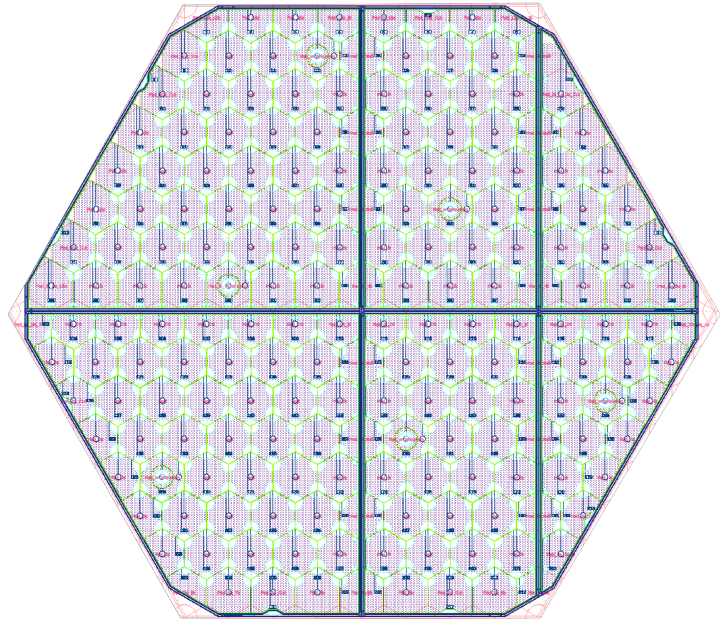


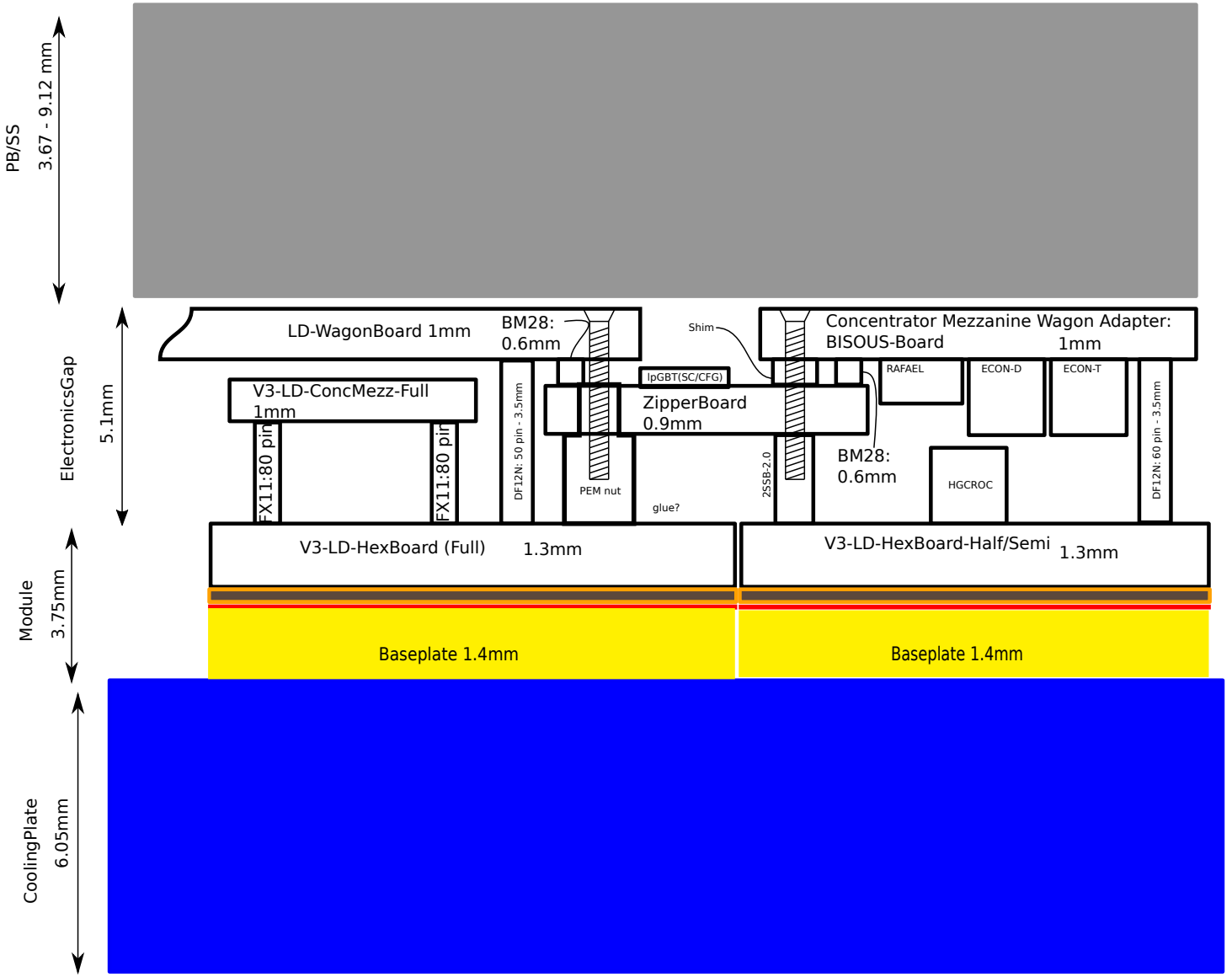
Figure 1.6: Longitudinal cross section of the upper half of one endcap calorimeter. It consists of an electromagnetic compartment (CE-E) followed by a hadronic compartment (CE-H). The green region to the lower left is instrumented with silicon detectors and the blue region to the upper right with scintillator tiles.

1.4. Longitudinal structure of the HGCAL 19





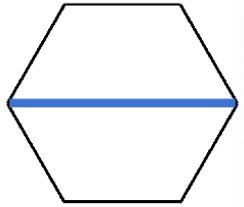
Hex module Stackup



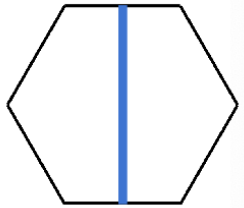
Hexaboard partial

Hexagonal LD Sensor with Dicing line (MGS) provide sensors' structures for the following partial shapes.

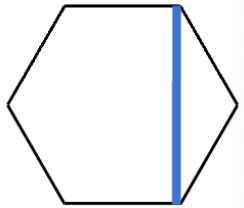
Two Halves : Top & **Bottom**

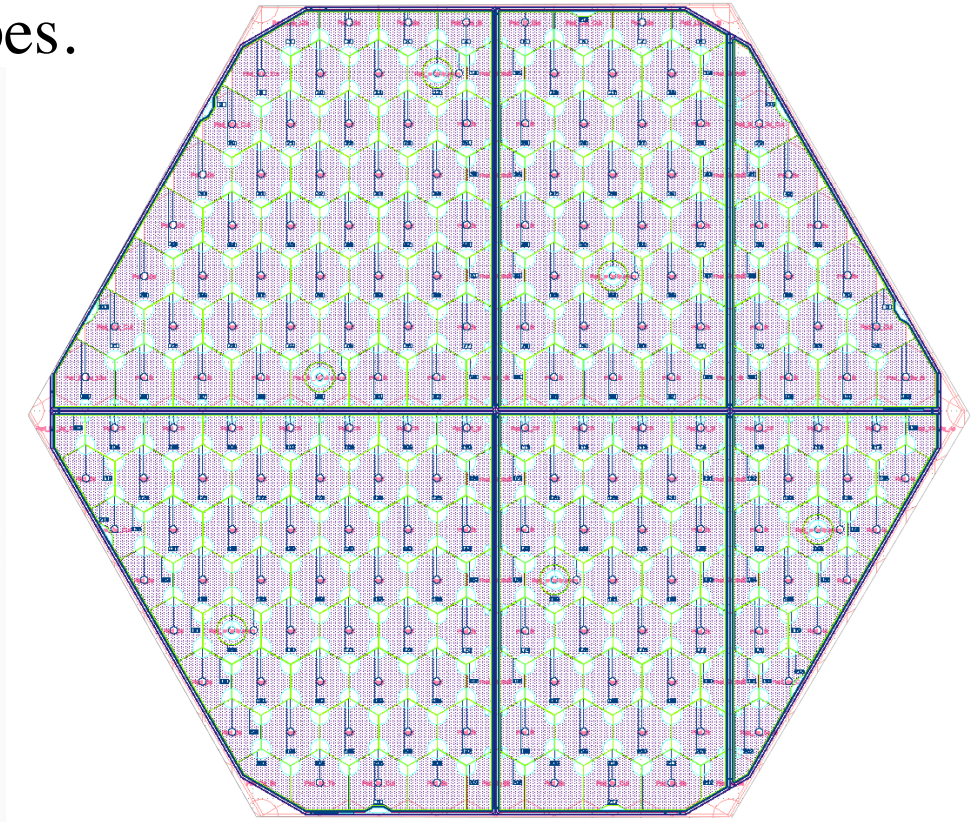


Two Semis : Left & Right



One Five and One Three



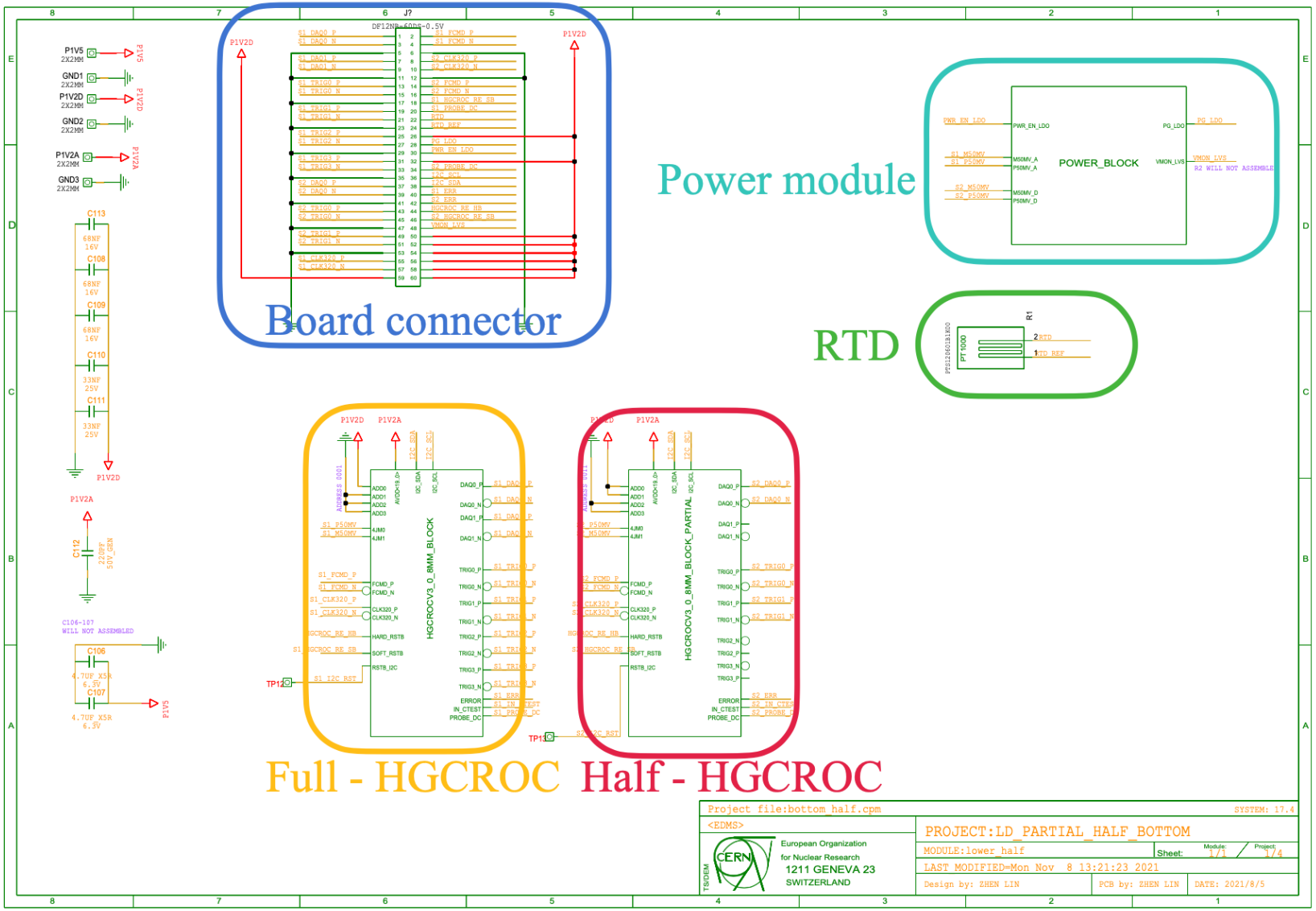


The V3-LD-Partial-HalfBottom is designed for MGS LD Sensor's Half Bottom

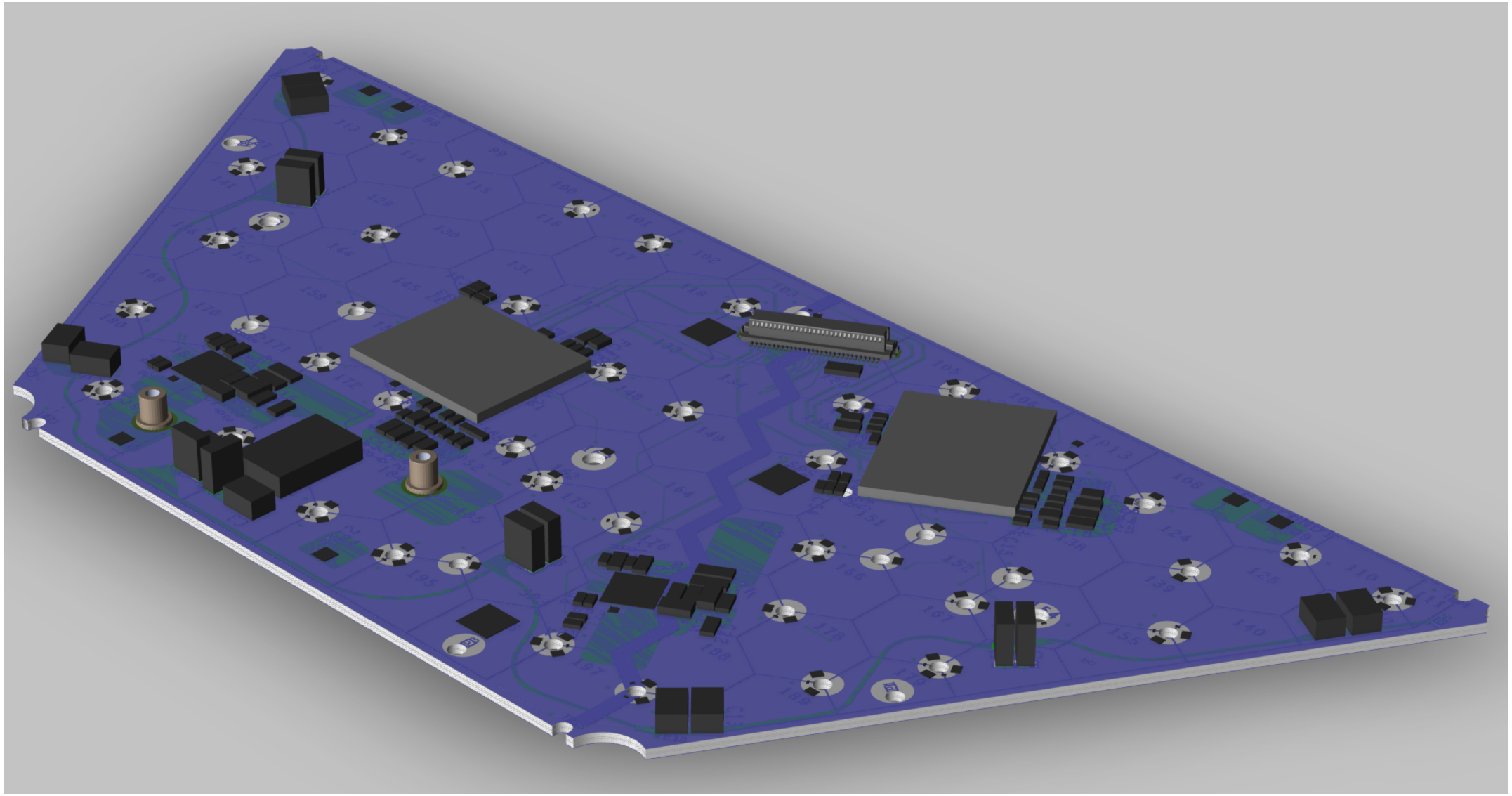
Hexaboard-Half-bottom Schematic Design

Main components:
2 × V3-HGCROCs
2 × LDOs
1 × DF12 connectors

Main Parts:
Board connector
Power module
RTD
Full - HGCROC
Half - HGCROC



Board overview



Layer Stackup

LayerID	Type	Net routing (Line width / gap micronmeters)	Finished copper Thickness	Dielectric Thickness
Top	Signal layer	FCMD CLK320 HV PLL (127/110)	35μm	
				0.150 mm/FSR(Er 4.5)
L2	Signal layer	DAQs TRIGs HGCROC_sigs (110/127)	17.5μm	
				0.200 mm /FSR(Er 4.5)
L3	GND layer	GND	17.5μm	
				0.100 mm/FSR(Er 4.5)
L4	PWR layer	P1V5 P1V2D P1V2A	35μm	
				0.100 mm/FSR(Er 4.5)
L5	GND layer	GND	35μm	
				0.100 mm/FSR(Er 4.5)/Glue
L6	Signal layer	Analog input signals	17.5μm	
				0.200 mm/FSR(Er 4.5)
L7	GND layer	GND	17.5μm	
				0.150 mm/FSR(Er 4.5)
Bottom	Empty layer	only HV pads	35μm	

Routing Constraints

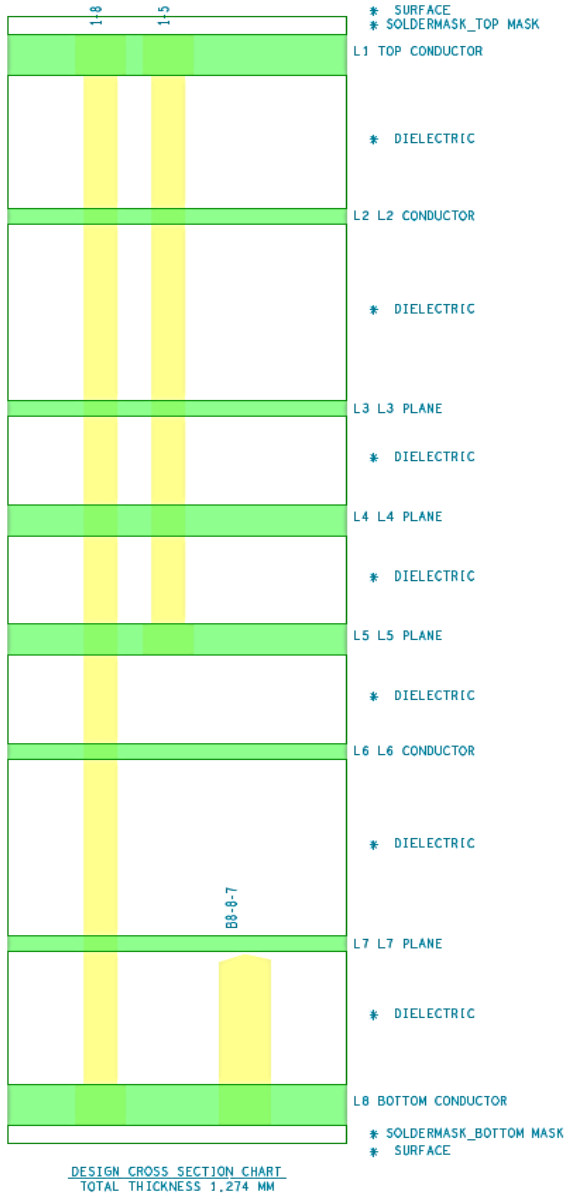
Nets	Track Width	Clearance
High Voltage	0.5 mm	2 mm
Differential Pairs 100Ω (L1)	0.127 mm	0.110 mm (gap)
Differential Pairs 100Ω (L2)	0.110 mm	0.127 mm (gap)
DP – All*	---	(~3x Track separation)
Analog Signals (BGA Region)	0.127 mm	0.127 mm
Analog Signals*	0.127 mm	0.127 mm
Power & GND	0.127 mm (almost the polygon)	0.127 mm
All Other Signals	0.127 mm	0.127 mm

Vias and Backdrills

- Two types of vias used

Via type	Drill	Pad
L1 – L5	0.150 mm	0.450 mm
L1 – L8	0.200 mm	0.500 mm

- L1 – L8 via used only for Analog channels, GND and HV nets
- For all others (including power nets) L1 – L5 via was used
- One set of back-drill [L8 to L8]

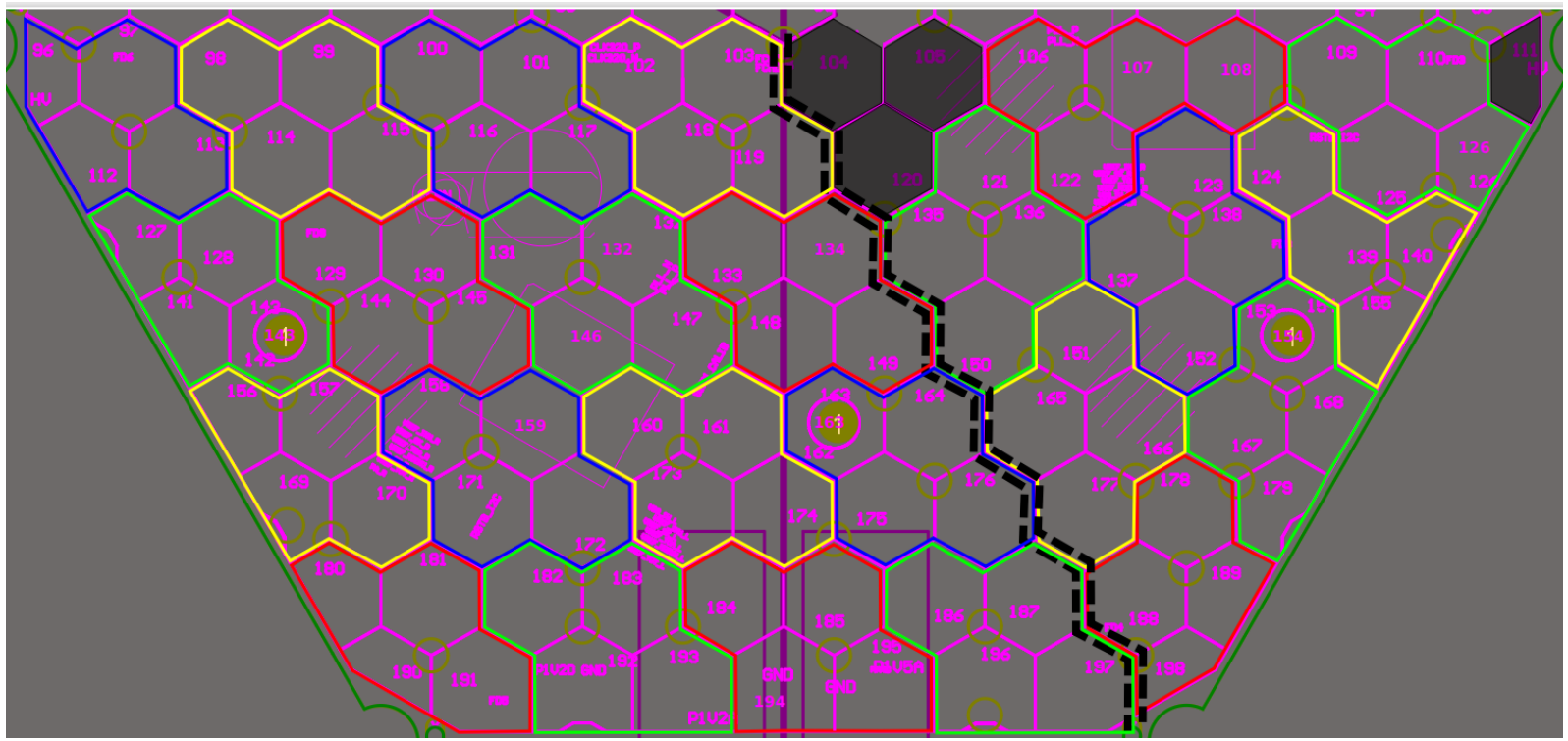


Trigger Cells

Trigger link No.	Trigger cell No.	Analog channel
0	TC0_0	7
0	TC0_0	4
0	TC0_0	6
0	TC0_0	5
0	TC0_1	0
0	TC0_1	2
0	TC0_1	3
0	TC0_1	1
0	TC0_2	13
0	TC0_2	15
0	TC0_2	14
0	TC0_2	16
0	TC0_3	11
0	TC0_3	10
0	TC0_3	9
0	TC0_3	12

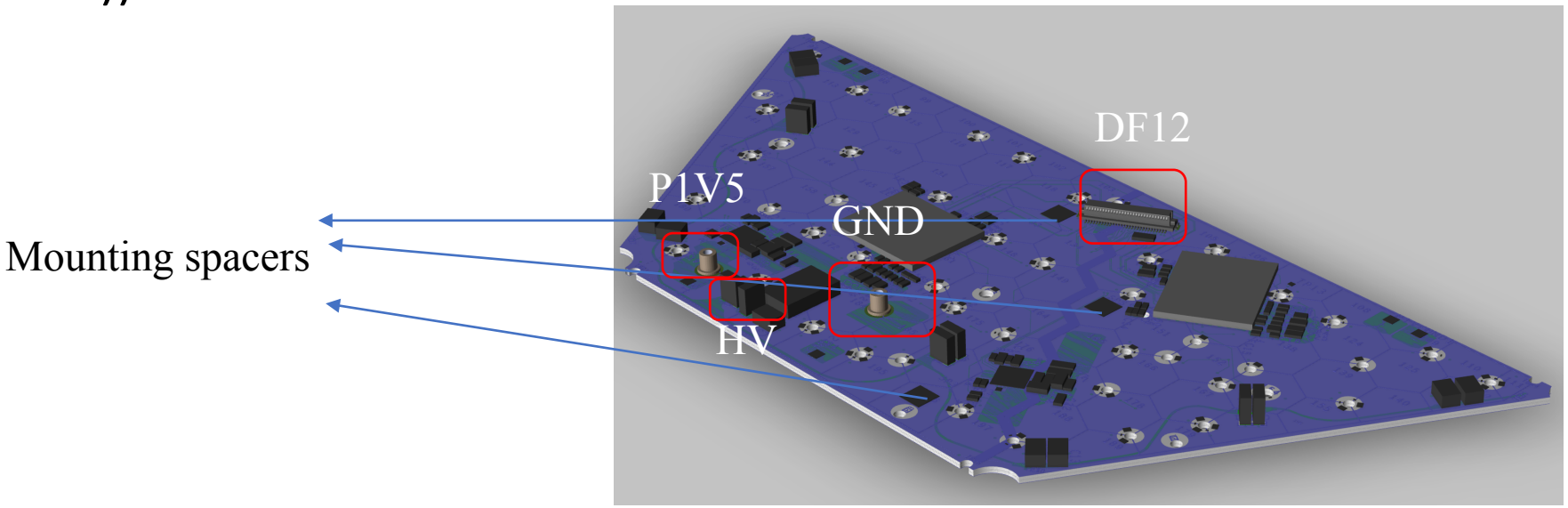
Trigger Cells Mapping

- There are 100 sensor cells that have been covered using 1 and ½ HGCROC resources.
  ------96 trigger cell and 4 non-trigger cells
- Every 4 contiguous HGCROC channels are routed to a cluster of 4 cells (trigger cell)
- The trigger cells are circled by different colour of lines and two parts are divided by a dashing line.
- 4 non-trigger cells which are filled with black



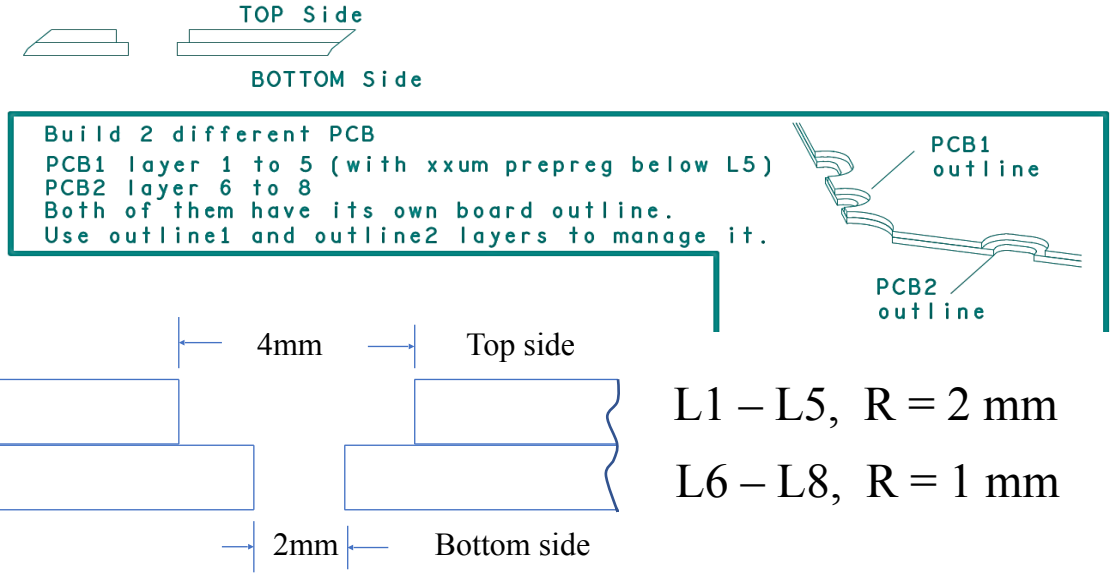
Board Interfaces

- Partial Concentrator Board(Partial CB) interface: DF12NB-60DS-0.5V (Receptacle)
  J1 at (+12,0) (in mm) with ref to full HexaBoard center
- For mounting of Partial CB MAC-8 2SSB-3.5 & 2.0 spacers
- 1.5V is supplied to Partial Semi as input of both Analog and Digital LDOs from Deported DCDC converter using MAC-8 3SSA-3 spacer
- For high voltage, 01×SM02B-BHSS-1-TB connector is used (JST BHS series 3.5 mm pitch 1.0A AC, DC (AWG# 24))



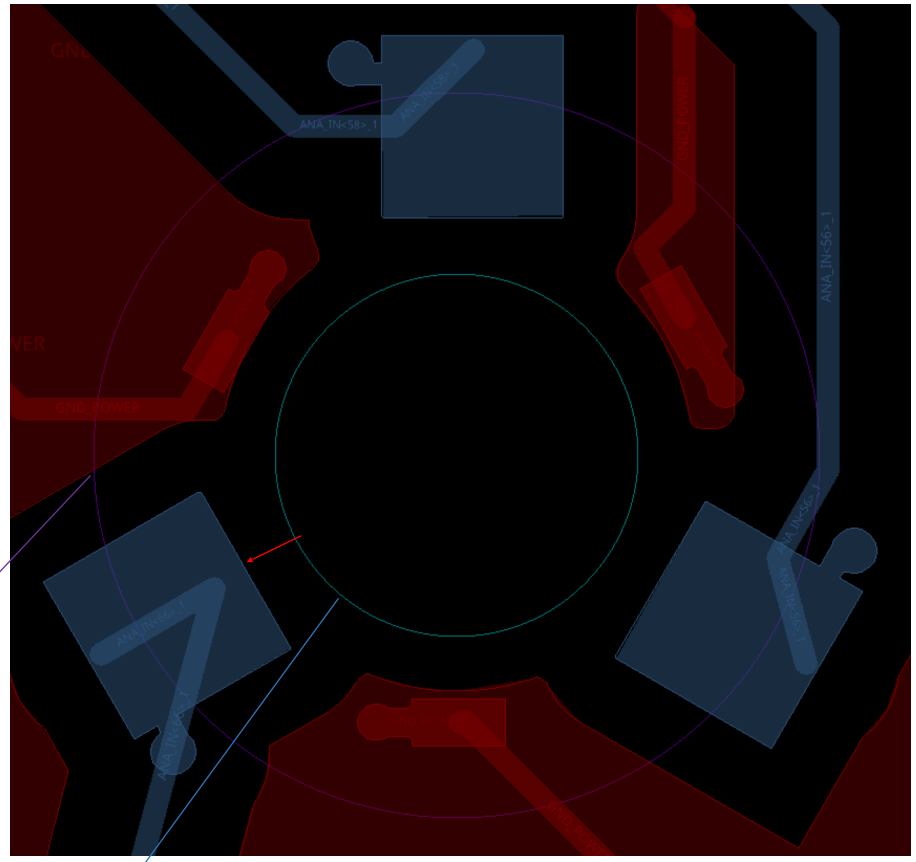
Step holes

- Every step hole contains at least one and at the most three bonding pads
- At least one GND pad is provided in each step hole



L1 – L5, R = 2 mm

L6 – L8, R = 1 mm



Outline1

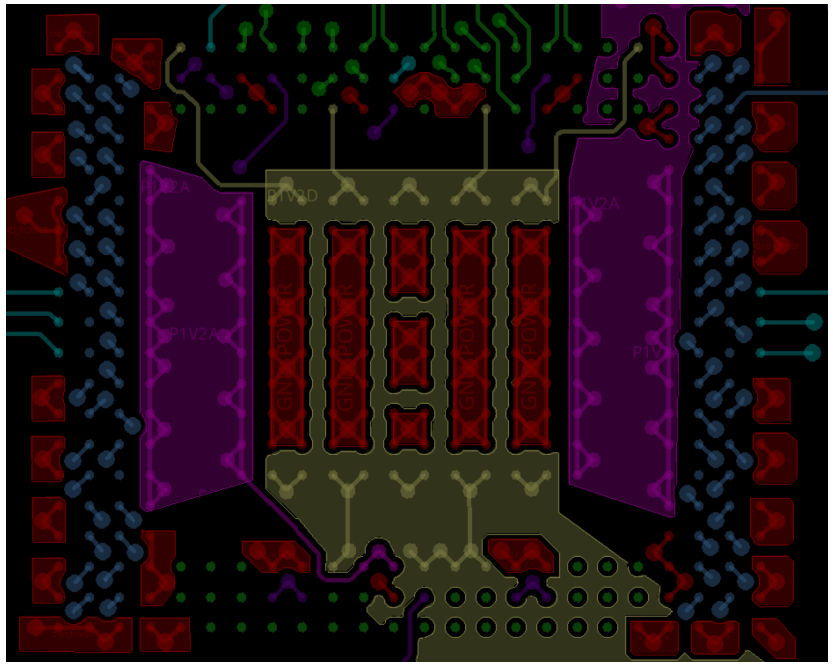
Outline2

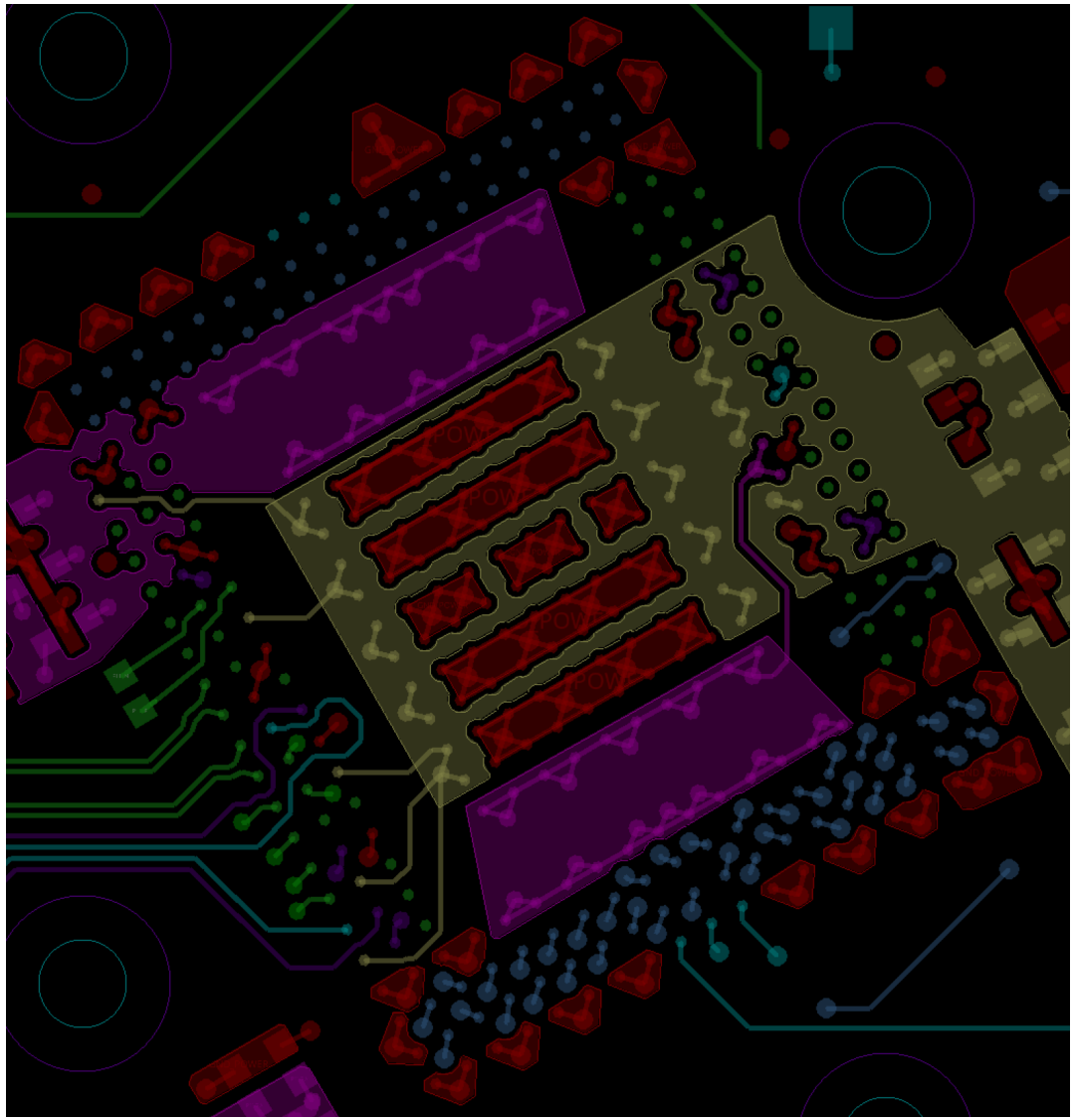
BGA Breakout

Seperate the AGND and DGND

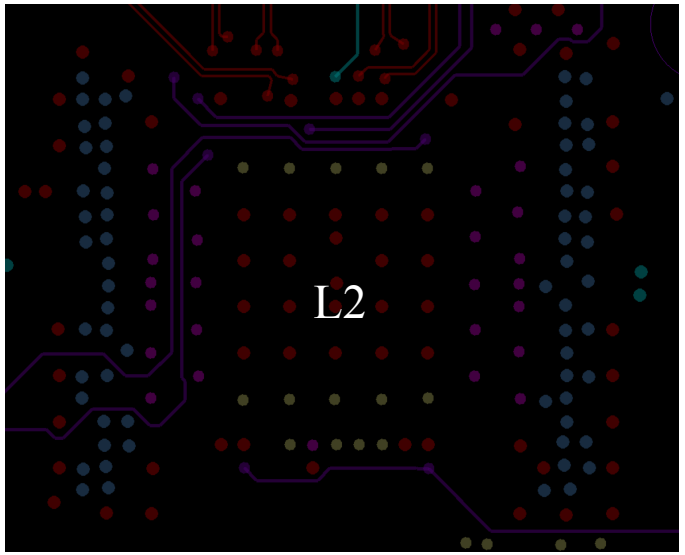
Analog channels (32+32 or 32) are connected to bonding pads on L6 with L1-L8 via (for full HGCROC)
These vias will be back drilled till L7

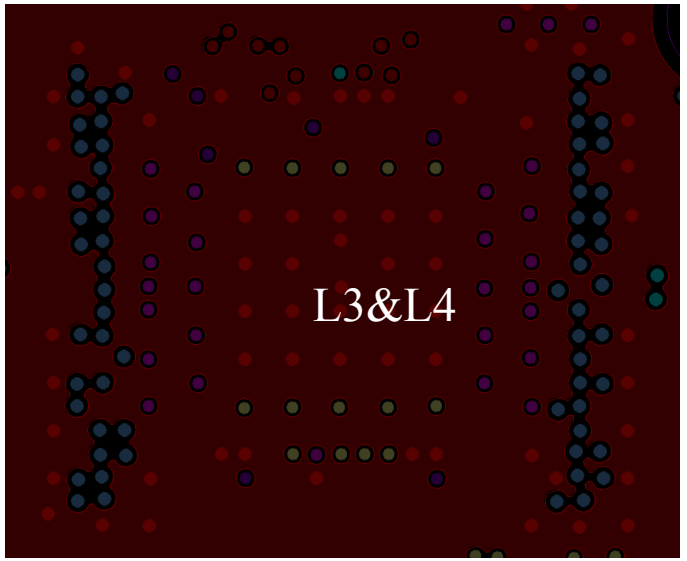
Power pins (1.2VD & 1.2VA) are connected to L4 with L1-L5 via

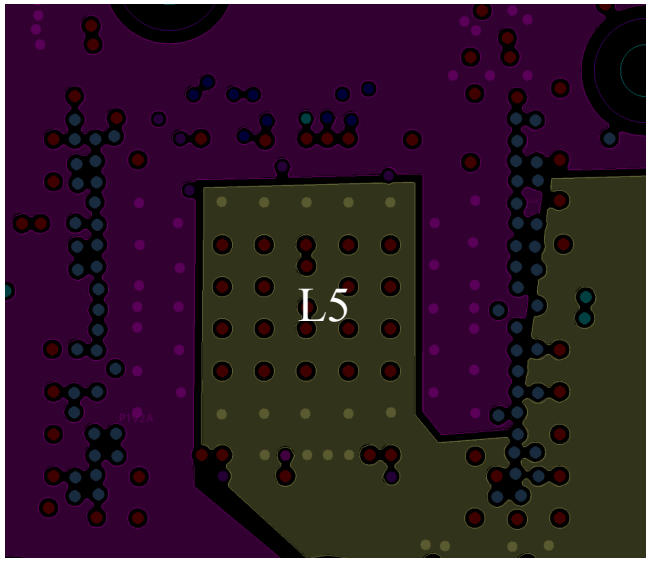


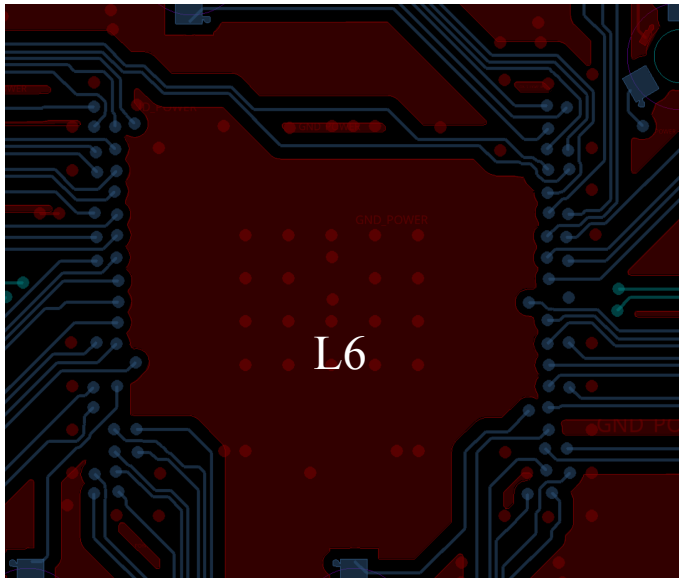


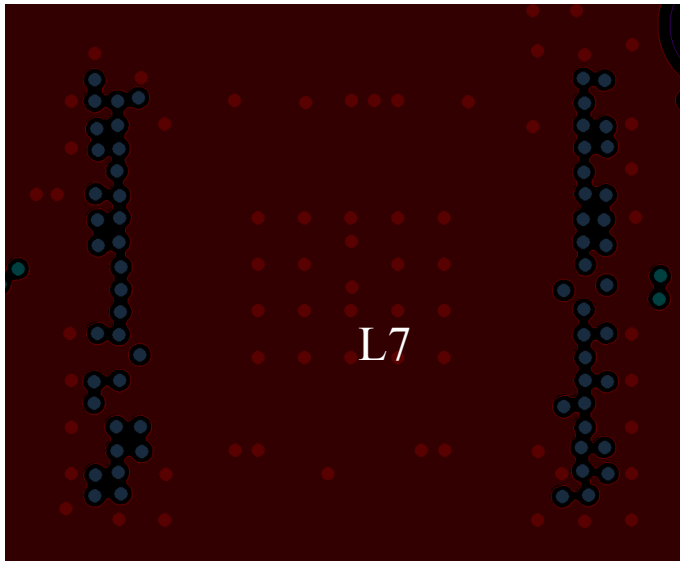
BGA Breakout – internal layer

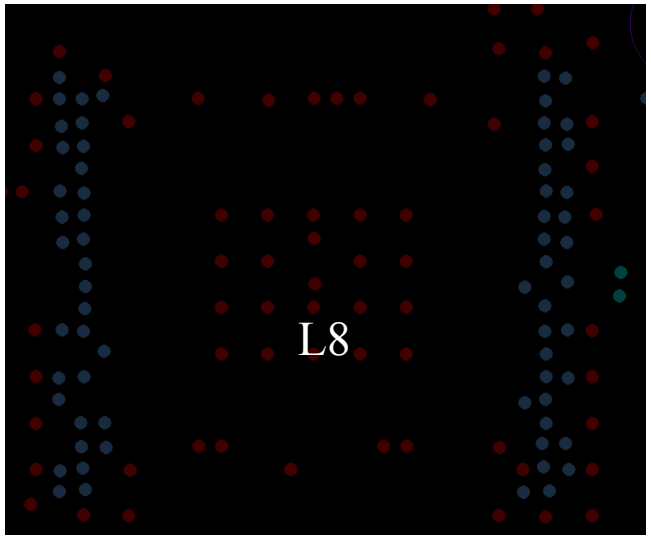






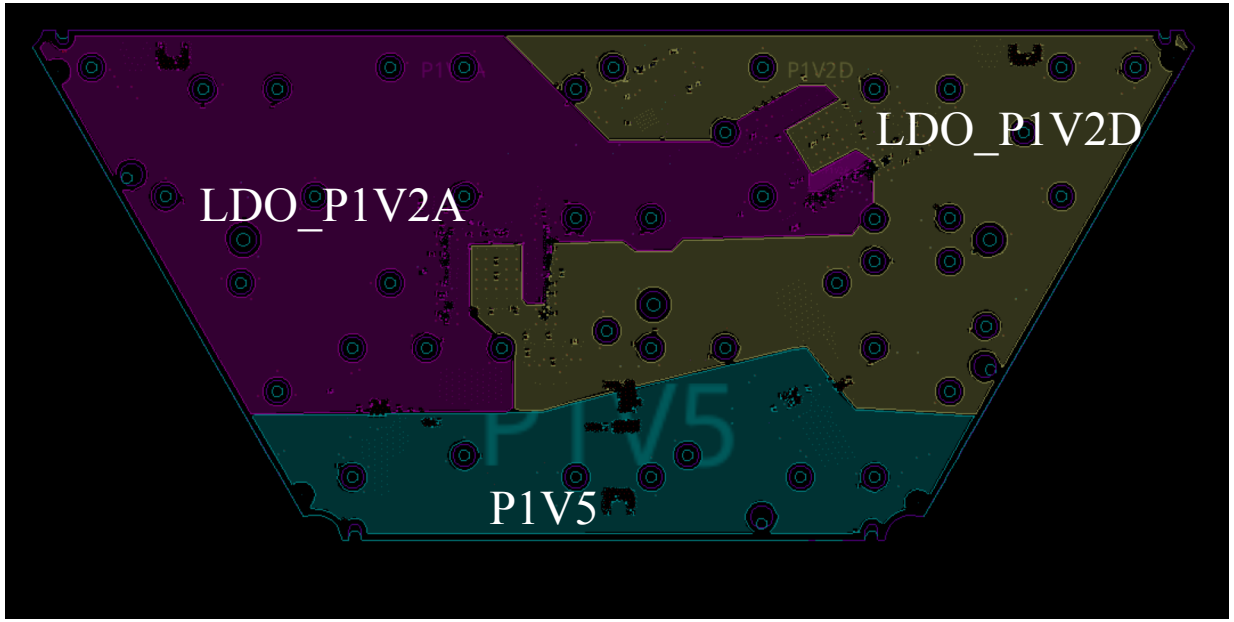


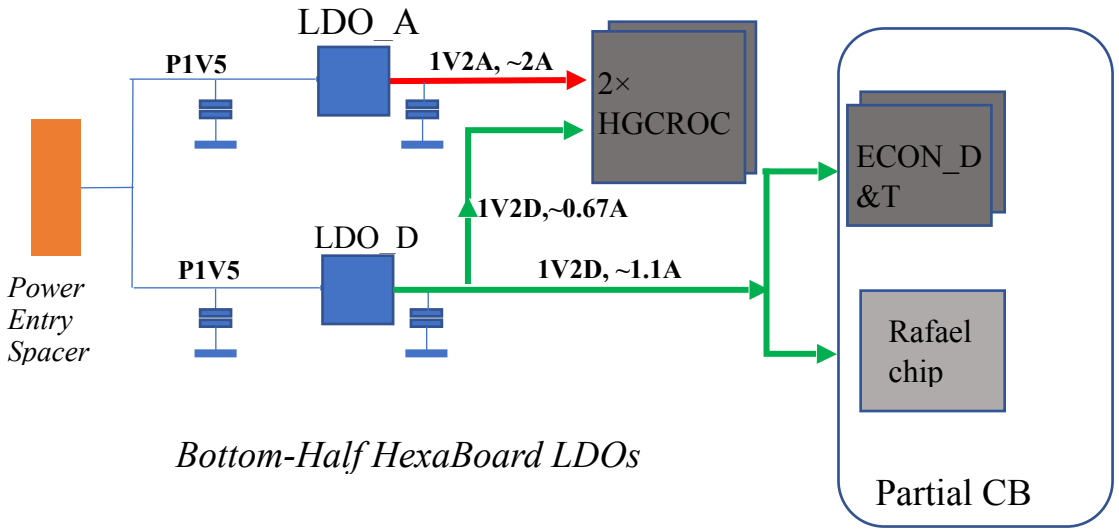




Power Scheme – Layer 4

Input 1.5V Outputs 1.2VD & 1.2VA

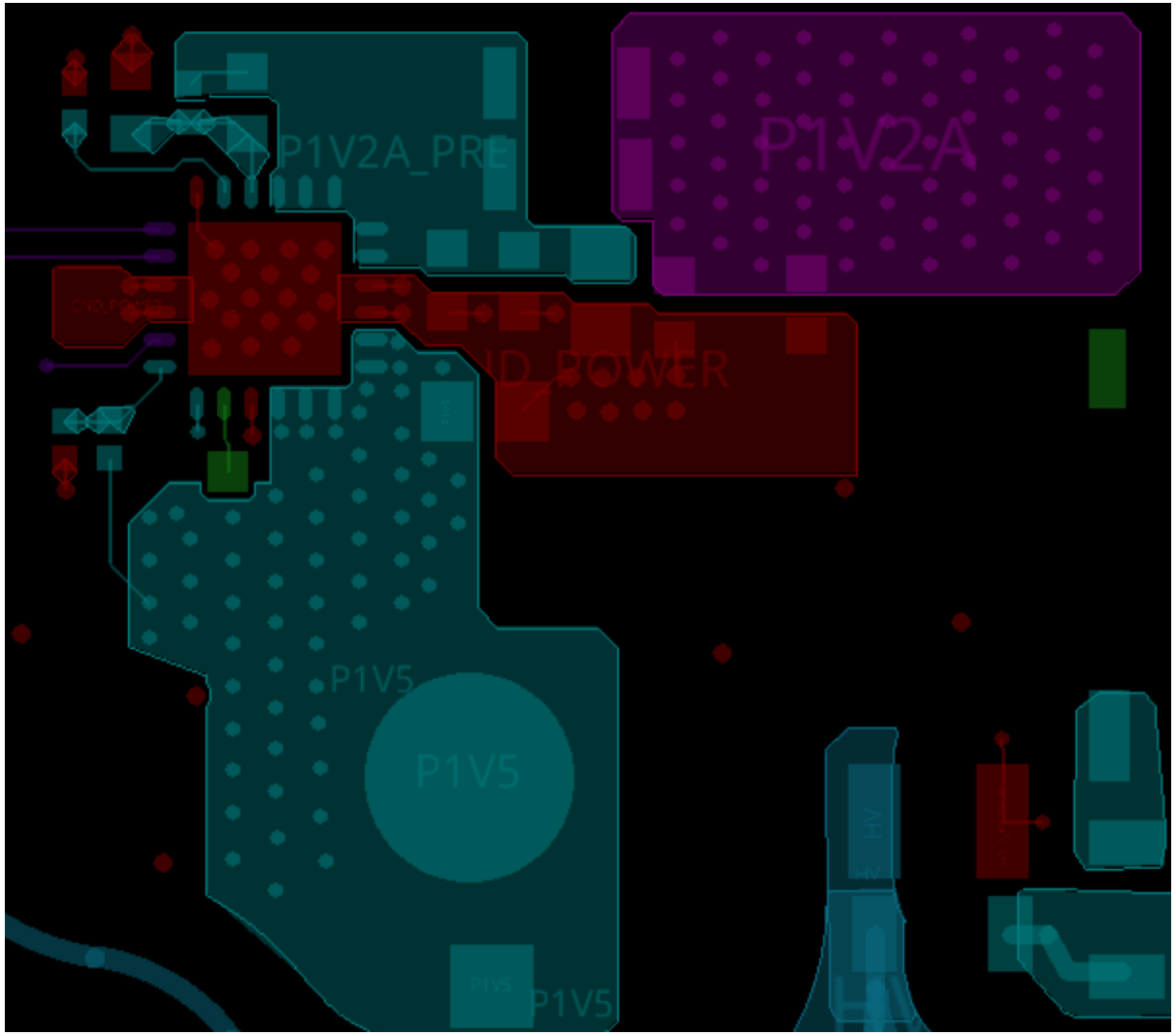




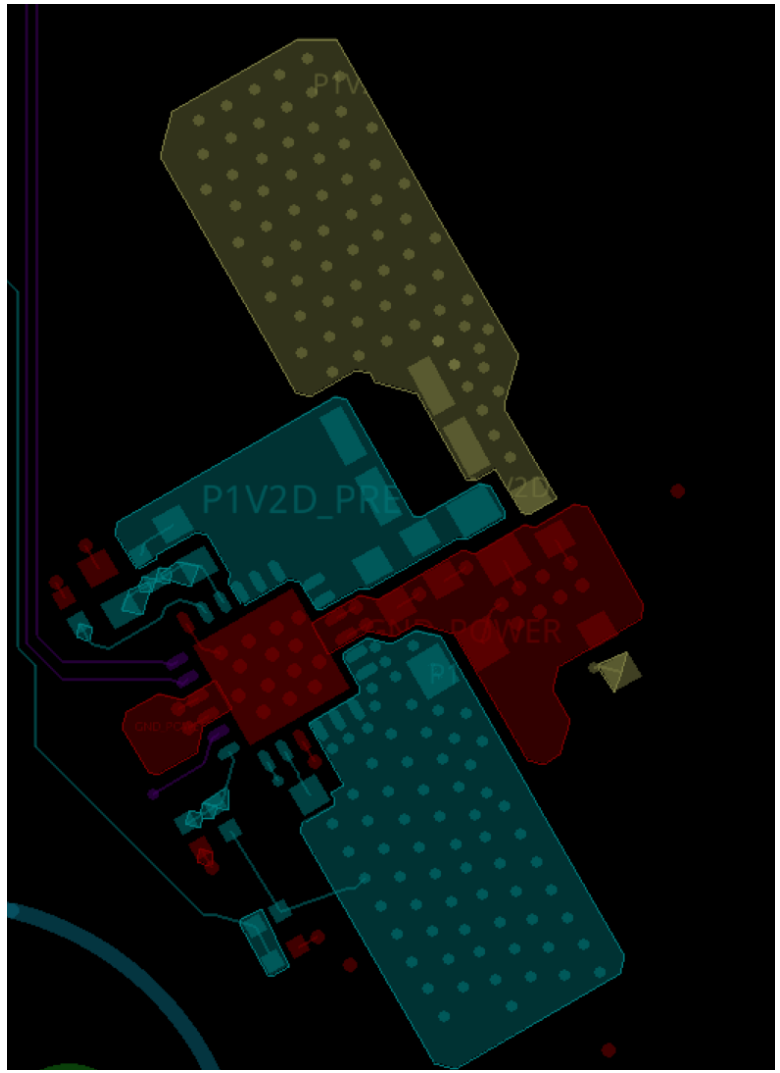
Bottom-Half HexaBoard LDOs

LDO Layout

P1V2A

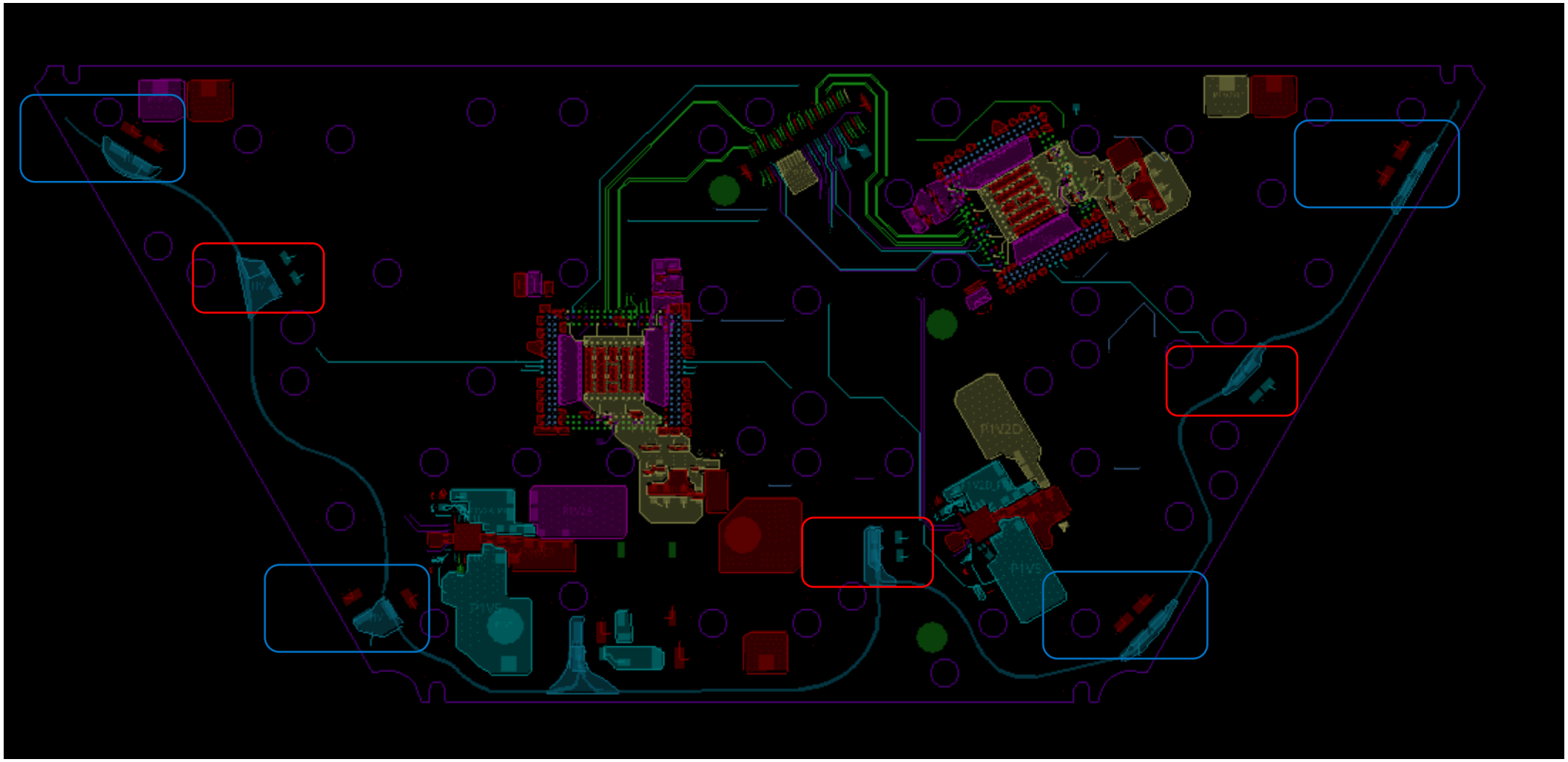


P1V2D



Layer1

HV (with 0.5mm track-width & 2mm copper-to-copper masked spacing) is routed at the corner to bond with Silicon sensor (shown in Blue box) & for common mode capacitors (shown in Red box)

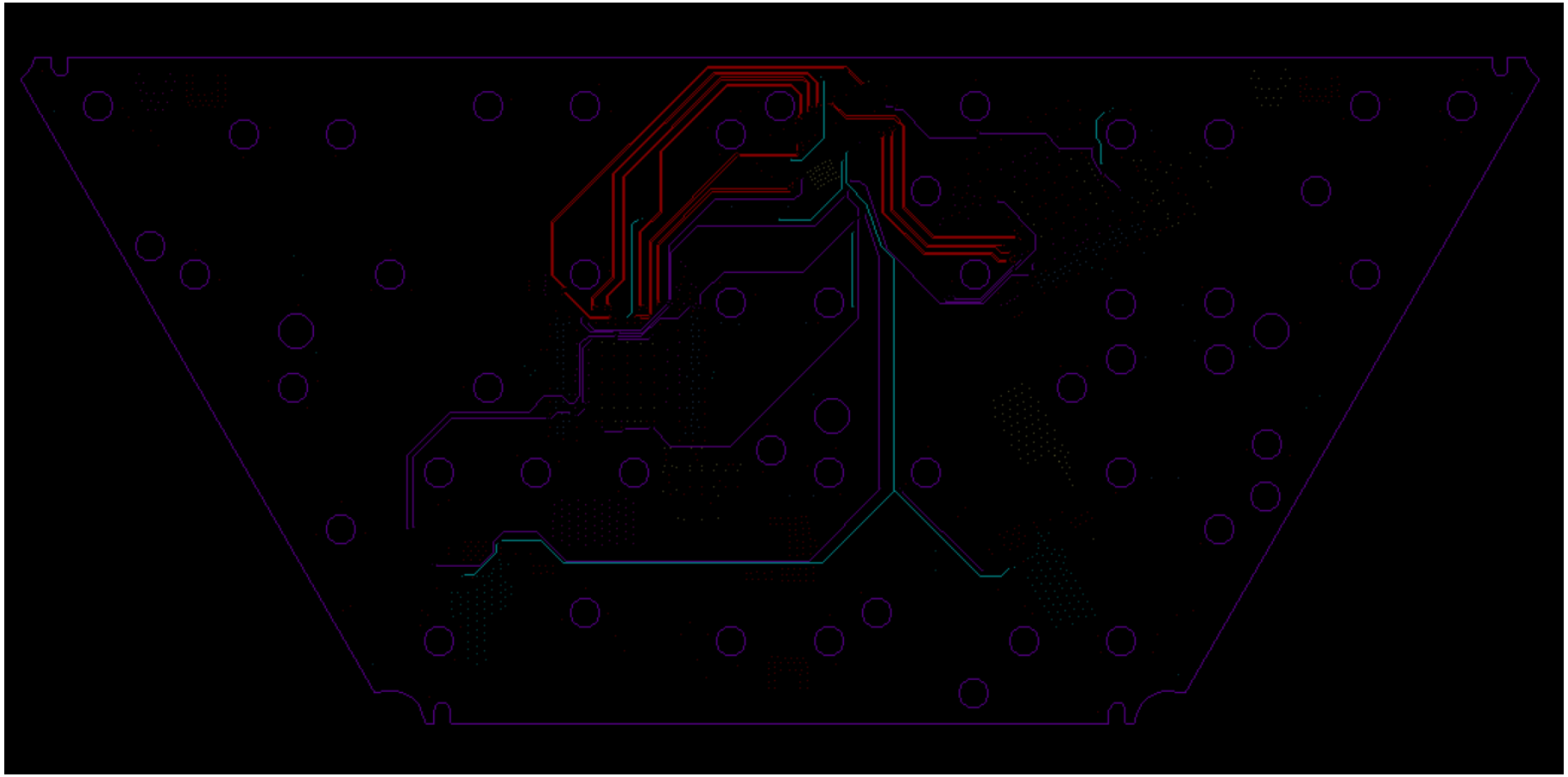


Layer2

All 06 or 03 differential signals of 1.28Gbps (DAQs & TRIGs) are routed on L2 with 100Ω impedance (for full HGCROC or half)

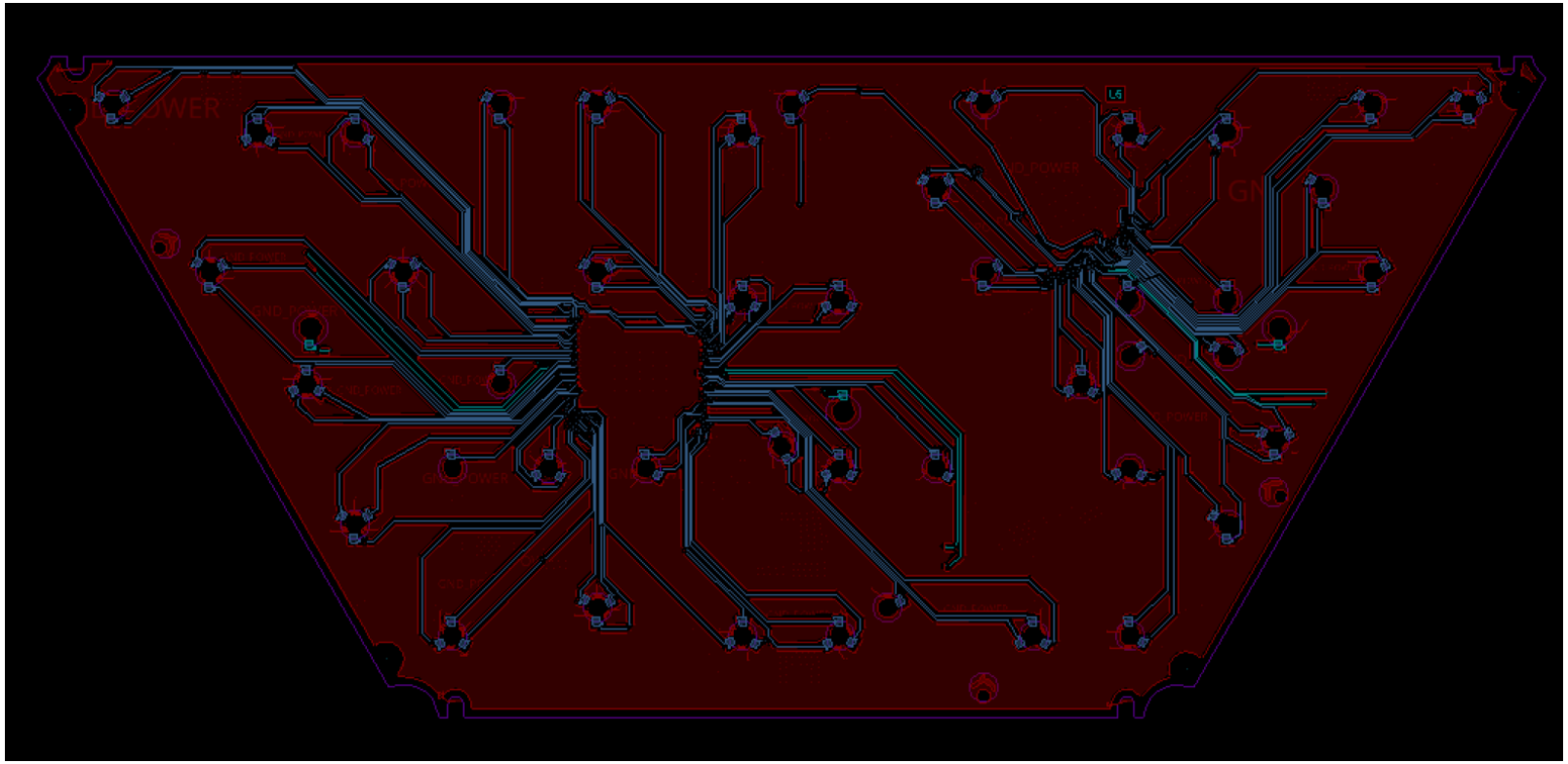
Their fanout is done with L1-L5 via to avoid PWR/GND planes blockage

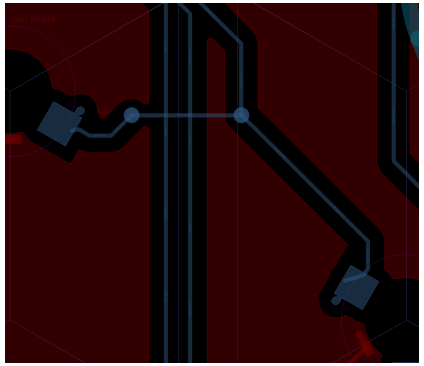
DP – DP clearance is 3 times the individual gap of a DP (outside BGA region)



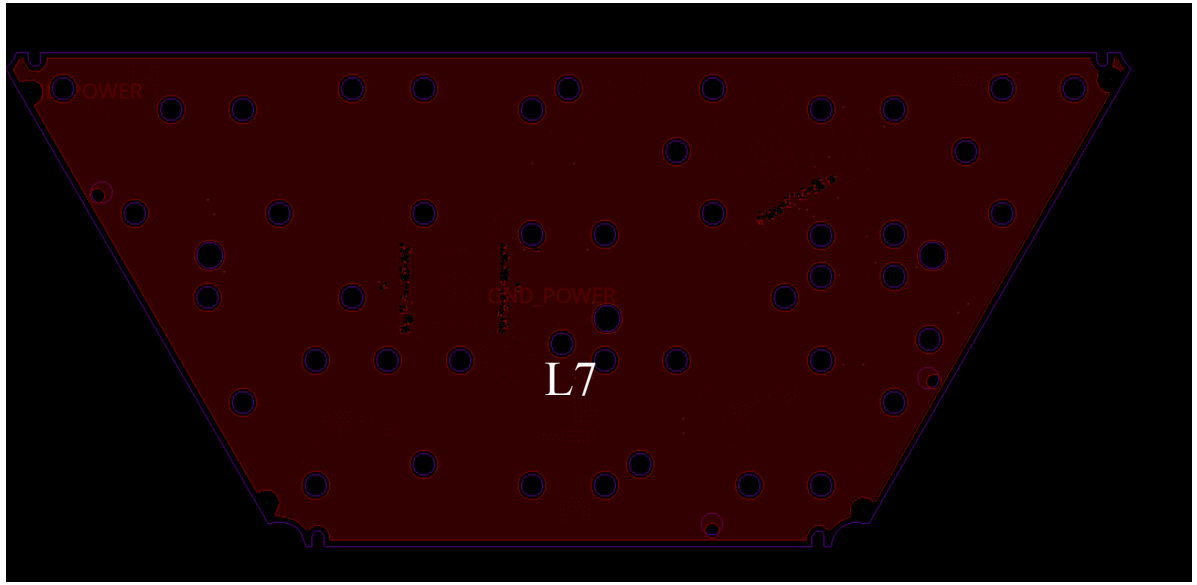
Layer6

All bonding pads and guard rings are on L6
The track width of all Analog signals is constant through out the design (0.127mm)
All Analog signals have at least 3x clearance as compared to their width Each cell is covered by one bonding pad
Cells with dicing lines have duplicate bonding pads





Layer3,5,7



Voltage drop on 1V2D and 1V2A, Layer 1

Voltage sources:
U1 => P1V2A
U2 => P1V2D

Current sinks:
M1Dig => 208 mA
M1 Ana => 604 mA

M2 Dig => 208 mA
M2 Ana => 604 mA

J2 => 400 mA

Part Designation	Current Rating	Standard Resistance (Ω)
TLRZ2B	50A	0.2m max.

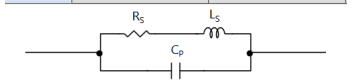
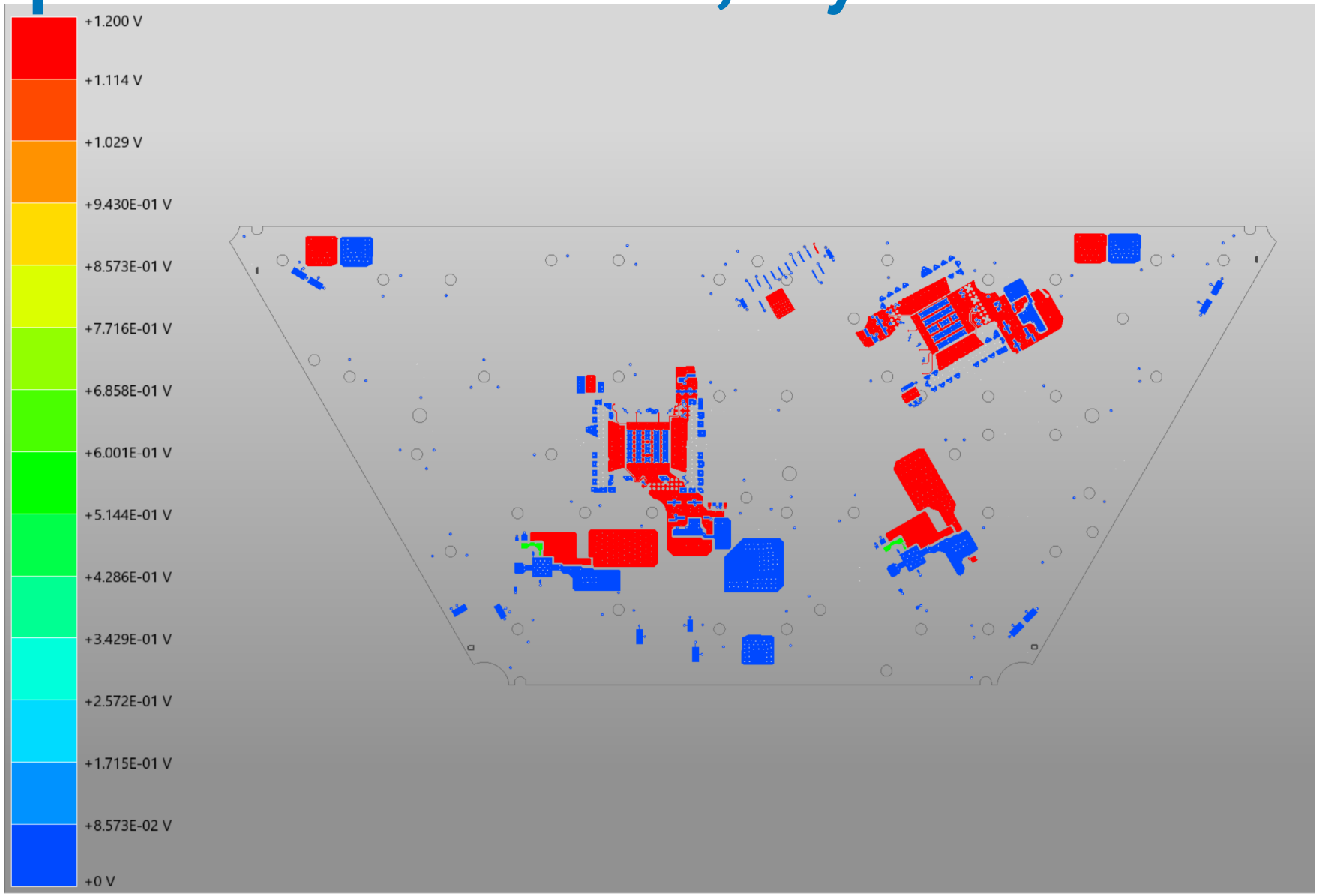


Fig. 1 Equivalent circuit of resistor

Ls = 0.1 nH
Cp = 1 pF

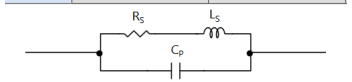


Voltage drop on 1V2D and 1V2A, Layer 4

Voltage sources:
- U1 => P1V2A
- U2 => P1V2D

Current sinks:
- M1Dig => 208 mA
- M1 Ana => 604 mA
- M2 Dig => 208 mA
- M2 Ana => 604 mA
- J2 => 400 mA

Part Designation	Current Rating	Standard Resistance (Ω)
TLRZ2B	50A	0.2m max.



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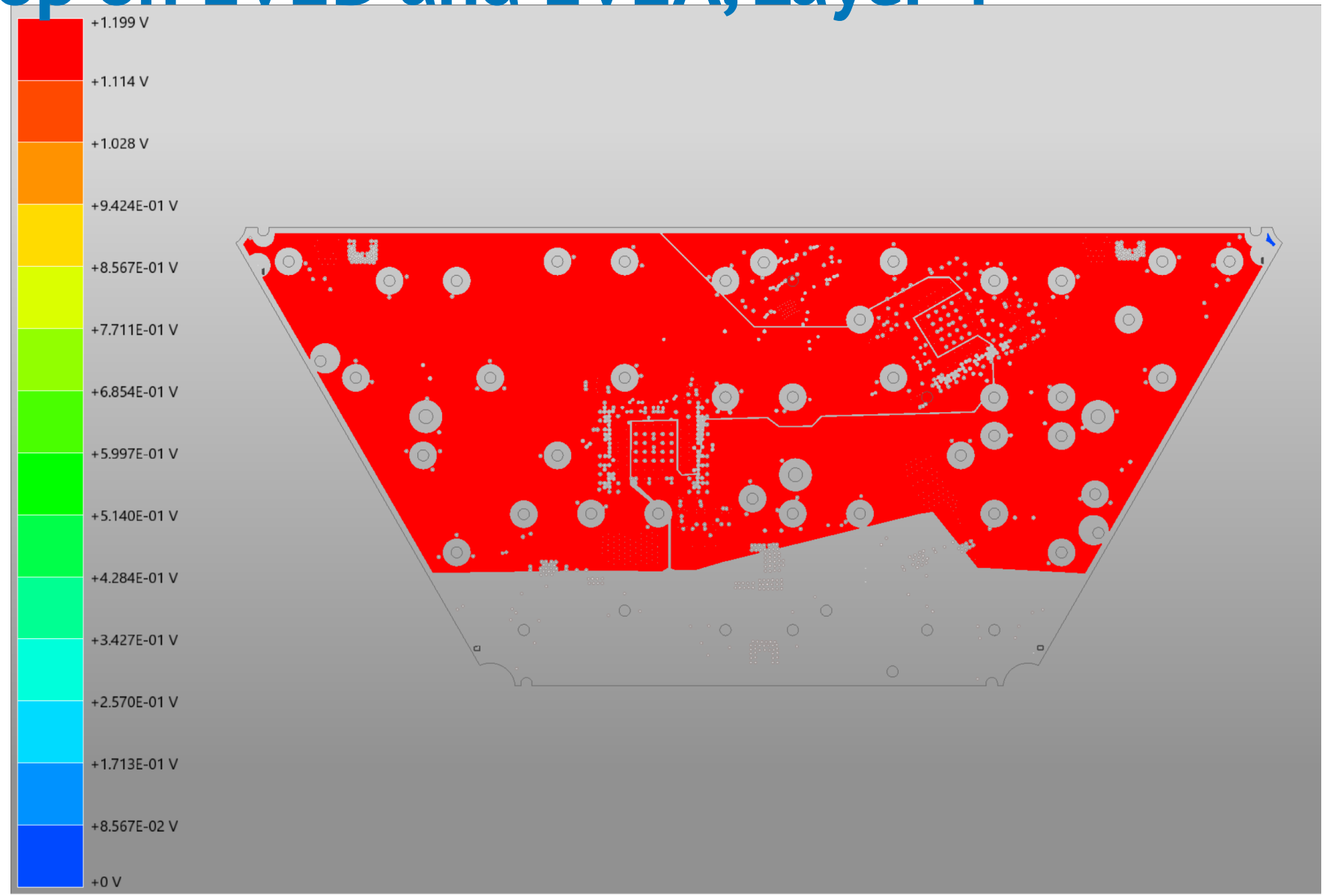

Current density, Layer 1

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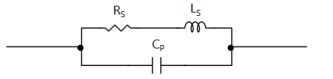

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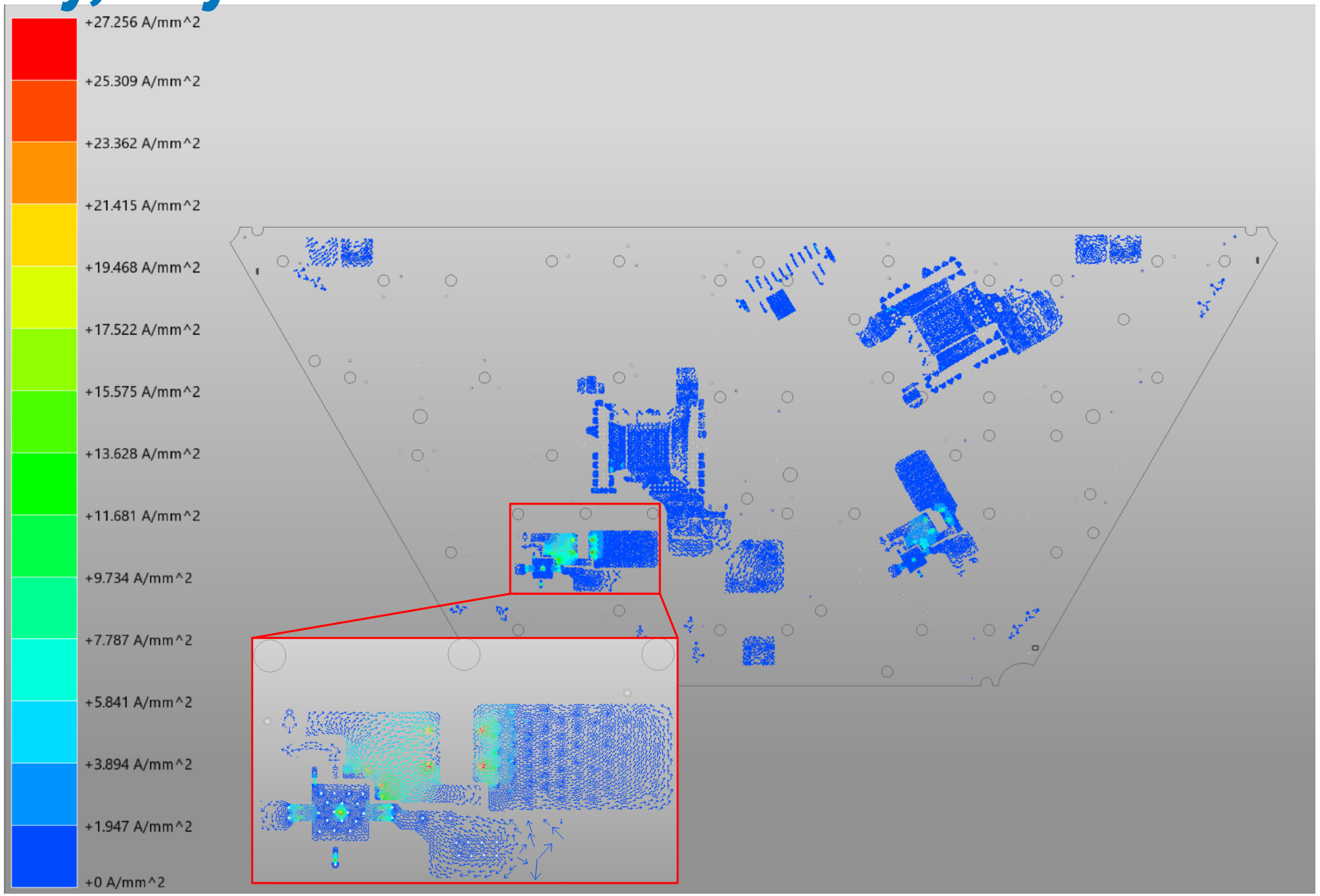
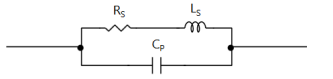


Current density, Layer 4

Voltage sources:
- U1 => P1V2A
- U2 => P1V2D

Current sinks:
- M1Dig => 208 mA
- M1 Ana => 604 mA
- M2 Dig => 208 mA
- M2 Ana => 604 mA
- J2 => 400 mA

Part Designation	Current Rating	Standard Resistance (Ω)
TLRZ2B	50A	0.2m max.



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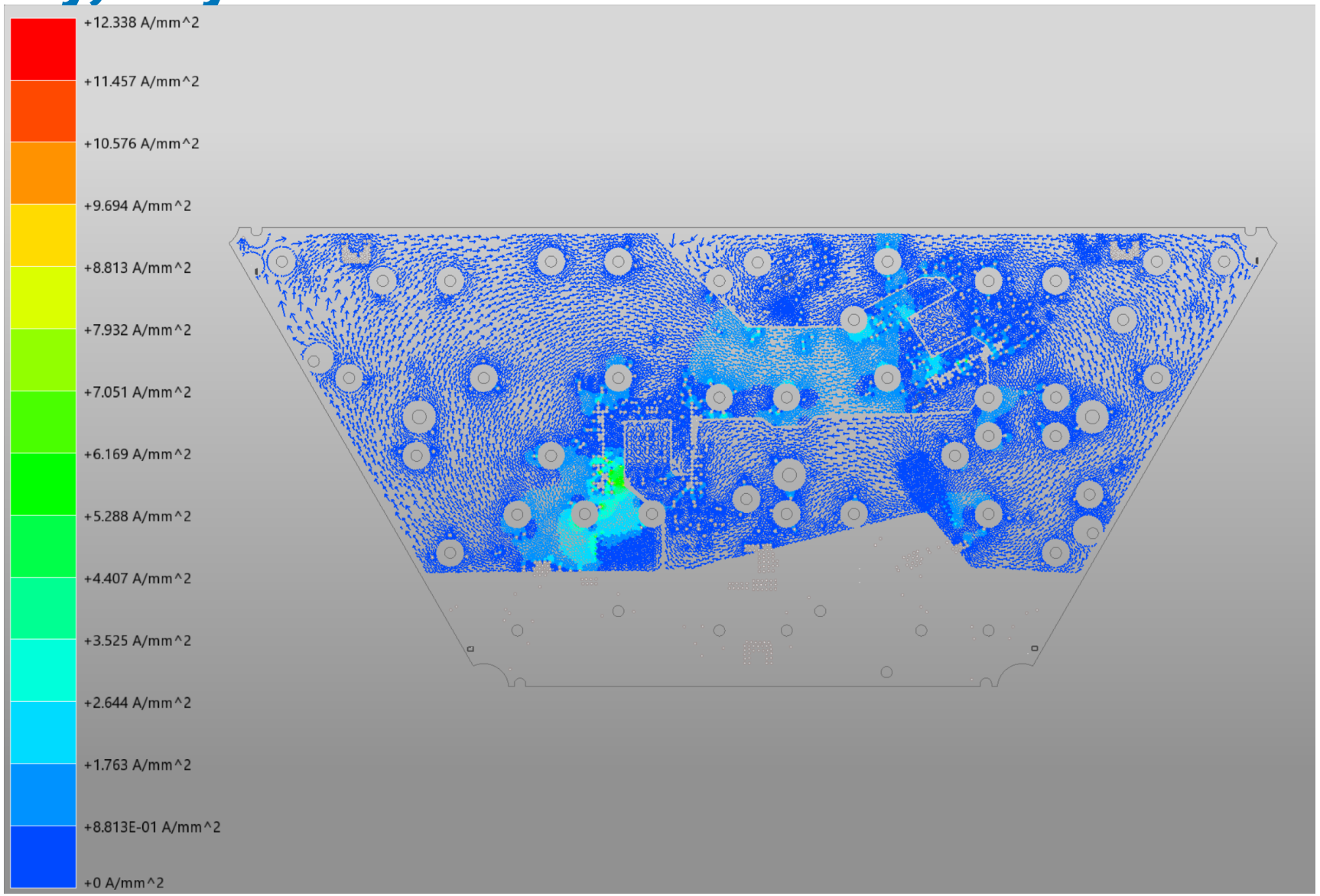

Differential S-parameter between M3 and J1

S2_CLK320
S2_DAQ0
S2_FCMD
S2_TRIG0
S2_TRIG1