# Development of a CMOS Pixel Sensor prototype for the high hit rate CEPC vertex detector

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## Abstract

The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption. It is necessary to design and construct the CEPC vertex detector with state-of-the-art silicon detector technologies. A dedicated CMOS Pixel Sensor chip, named TaichuPix, is being developed for the first 6-layer CEPC vertex detector prototype. The TaichuPix development is based on a fast in-pixel readout combined with a hit-driven architecture, which would be beneficial for the high hit rate. This work reports the requirements for the sensor and the design approach being followed to cope with it. Two small-scale prototypes (25 mm2) capable of achieving a hit rate up to 36 MHz/cm2, were designed in a 180 nm CMOS process. One of them, the TaichuPix-2 prototype was characterized with electrical and radioactive sources in laboratory. The test results on the chip functionality and the pixel performance in terms of threshold and noise as well as the timing response are reported.

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### Introduction

The Circular Electron Positron Collider (CEPC), primarily operating at the center-of-mass energy of ~ 240 GeV, has been proposed and being studied in the last few years [1, 2]. The CEPC machine is expected to deliver an unprecedented luminosity of 3×1034 cm-2s-1, with beam features much different from those planned for linear colliders [3, 4]. These operation conditions and the unprecedented precision physics program call for the dedicated CEPC vertex detector.

The Monolithic Active Pixel Sensor (MAPS) technology has become extremely attractive for future high-performance tracking detectors. With the R&D activities for the CEPC vertex detector, several CMOS pixel sensor prototypes have been developed [5-8]. The TaichuPix development is motivated by the need for a dedicated pixel chip for the implementation of the first silicon vertex detector prototype. It is desirable to design a large-scale pixel chip with full functionality, which will cope with the requirements of the assembly for the double-sided ladder. According to the latest collider design and study on the beam-induced background, the highest hit rate for the vertex detector is expected to be ~107/cm2/s. In addition, the readout system should fit the 25 ns bunching spacing for the Z-factory operation mode. As an alternative to the previously implemented prototype CMOS pixel sensors based on a rolling shutter architecture (JadePix chips) [5-7], the TaichuPix chips employ the hit-driven approach to boost the readout speed.

### TaichuPix development

### General architecture

TaichuPix, a dedicated MAPS chip, is being developed for the first 6-layer vertex detector prototype for CEPC based on the baseline design [1]. Table 1 summarizes the design specifications for the TaichuPix chip. The specification of hit rate depends on the bunch spacing, hit density and the cluster size of one hit. Supposing that the average cluster size is 3, the maximum hit rate was calculated to be 36 × 106/cm2/s for the W operation mode. A dead time less than 500 ns is required to achieve a detection efficiency higher than 99% [9].

Table1. Design specifications of the TaichuPix chip

|  |  |
| --- | --- |
| Pixel size | 25 µm × 25 µm |
| Dimension | 15 × 25 mm2 |
| Max. hit rate | 36 × 106 /cm2/s |
| Dead time | < 500 ns |
| Power density | < 200 mW/cm2 |
| TID radiation hardness | 1 Mrad |
| Bunch spacing | Higgs: 680 ns; *W*:210 ns; *Z*: 25 ns |

To meet the above requirements, we proposed the architecture of a full-scale TaichuPix chip (see Fig. 1), including a matrix of 512 × 1024 pixels. Each pixel integrated a sensing diode, a front-end and a hit storage register and logic for pixel mask and test pulse configuration. The readout of the pixel array is built based on the “column-drain” scheme, a proven architecture for high hit rate operations. Pixels are arranged in double columns, with a priority encoder within a column while timestamps are recorded at the periphery. All the 512 double columns are read out in parallel to minimize the dead time. For each double column, a fast-or busy signal is delivered to the End of Column (EOC) when any pixel generates a hit signal. An 8-bit timestamp with a resolution of 25 ns is generated at the EOC whenever a new fast-or (‘FASTOR’) busy signal is received. Fired pixels in the same cluster share a common timestamp as the Trigger ID. The pixel addresses of the fired pixels are temporarily stored in a column-level FIFO (FIFO1).



Fig.1. Functional block diagram of a full-scale TaichuPix chip.

The 512 double columns and the corresponding EOC logic are grouped into 4 blocks, and each one integrates a chip-level FIFO (FIFO2). There are four groups including 32 double columns in each block. The 32 FIFO1 inside each group are read out according to the address priority, while the 4 groups are read out sequentially to the FIFO2 in the block. The four FIFO2 are read out through a hierarchical data multiplexer. The readout of the TaichuPix chip is compatible with both trigger and trigger-less modes. In the trigger mode, only the data with matched timestamps in a maximum window of 175 ns will be sent to the chip level FIFO, which can match the speed of the chip interface. In the trigger-less mode, all the data in the 512 column level FIFOs are designed to be read out to the data interface at a frequency of 140 MHz. Each hit data includes 32 bits. A high-speed serial data transmission unit is designed to satisfy the largest data capacity up to 4.48 Gbps. An 8b10b encoder is available in the second prototype named TaichuPix2. When enable the 8b10b encoding, the data compression function [9] should be activated to fit the data transmission speed of the serializer.

### Small-scale prototypes

Two small-scale prototypes of the TaichuPix chip were developed with a 0.18 µm CMOS imaging sensor process: TaichuPix-1 (2019) and TaichuPix-2 (2020). The TaichuPix-1 prototype was designed to address the chip architecture and to perform initial R&D [10]. The TaichuPix-2 (see Fig. 2) includes 6 variants of the pixel cell and all the required features of the final TaichuPix chip. The test results obtained with TiachuPix-2 form the remainder of this paper.

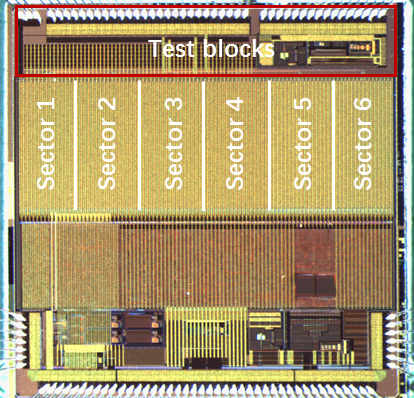


Fig. 2. Photograph of the TaichuPix-2 prototype indicating its splits on the pixel array.

The TaichuPix-2 prototype is 5 × 5 mm2 in size, and consists of a pixel matrix of 192 columns and 64 rows, with a pixel pitch of 25 μm. The collection n-well electrode has an octagonal shape fabricated on a high-resistivity (> 1 kΩ cm) epitaxial layer. The diameter of the collection n-well is 2 μm and the n-well to p-well spacing is 2 or 3 μm, refer to Table 2 [11]. The sensor is reset by a reset diode. The in-pixel front-end, derived from the ALPIDE chip [12], is optimized for a faster response. Two in-pixel digital readout designs have been implemented: a FEI3-like [13] scheme and an ALPIDE-like [14] scheme. In the FE-I3-like pixel, some modifications to the pixel address generator were made to reduce the pixel size. In the ALPIDE-like logic, the hit storage registers have been replaced by an edge-triggered flip-flop, leading to a smaller pixel size and preventing repeated hit readout before the analog front-end resets. The priority address encoder block has been modified to boost its speed to 40 MHz. The two digital readout schemes employ the same double-column drain architecture as described in the previous section. The readout time of a hit for both schemes is 50 ns. According to the hit density, the average hit number for a double column is 3. The double columns are read out in parallel, resulting in a dead time of 150 ns, which satisfies the requirement.

Six different pixel flavors, differing in front-end and pixel digital schemes, are implemented in the pixel matrix to optimize the design as listed in Table 2. The periphery of TaichuPix-2 contains DACs for the biasing of the pixel front-end. The matrix’s digital readout circuit in the periphery is implemented with the same architecture as proposed for the final TaichuPix chip, while is reduced for 192 × 64 pixels to fit the die size of TaichuPix-2. The power consumptions of the peripheral readout logics are estimated to be 25-30 mW/cm2 in the trigger mode and 35-45 mW/cm2 in the triggerless mode [9].

Table 2. The pixel sectors in the TaichuPix-2 as shown in Fig. 2.

|  |  |  |  |
| --- | --- | --- | --- |
| Sectors | Electrode spacing | Front-end design | Digital readout scheme |
| S1 | 3 μm | Reference design, inherited from TaichuPix-1 | FE-I3-like |
| S2 | 3 μm | PMOS in independent N-wells | FE-I3-like |
| S3 | 3 μm | One transistor in enclosed layout | FE-I3-like |
| S4 | 3 μm | Increased transistor size to reduce threshold dispersion | FE-I3-like |
| S5 | 2 μm | Same as in S2 | ALPIDE-like |
| S6 | 3 μm | Same as in S1 | ALPIDE-like |

For the characterization of the TaichuPix-2 in this work, periphery readout works in the triggerless mode at a data rate of 160 Mbps.

### Experimental results with TaichuPix-2

### Imaging tests

The functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was first tested with an X-ray source and a laser source. The hit map under a microfocus X-ray source machine exposure for 5 minutes is shown in Fig. 3, where the data is taken from the output of the serializer. One observes obvious distinctions among the first four pixel sectors (S1-S4, see Table 2 for the description of the different sectors). The differences in the hit counts for the S1-S4 sector result from the different pixel thresholds for each sector using a common threshold setting. The comparison of the thresholds for S1-S4 is discussed in detail in Section 3.2. The pixels in sectors 5-6, which employ the ALPIDE-like version of the in-pixel readout logic, were found to show no response to the input. This feature is probably due to the design bug in the layout of the ALPIDE-like logic by the preliminary analysis. Consequently, sectors 5-6 were masked during the following measurements.

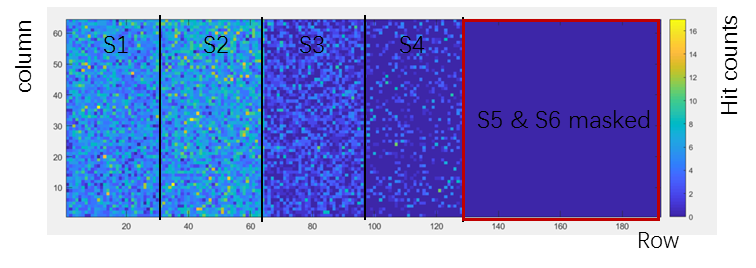


Fig. 3. Hit map of the TaichuPix-2 under X-ray for 5 min with the X-tube voltage of 8 kV. Different hit counts were observed in different pixel sectors (S5 & S6 were masked).

A 1064 nm laser source was used to perform imaging experiments. The TaichuPix2 sensor was placed in the front of the laser source, and the laser was precisely focused to make the light spot small enough. Fig. 4 shows the letter ‘E’ scanned by moving the laser source in the horizontal/vertical direction with a step of 200 µm. The imaging tests prove the functionality of the pixel array (4 of 6 pixel flavors work normally), digital periphery and serializer.



Fig. 4. Letter imaging obtained with laser spot scanning on the TaichuPix-2.

### Pixel Properties

As mentioned in section 2.2, the in-pixel front-end was optimized for a fast response. At the end of the double-column, the timestamps of hits were recorded at the positive edge of FASTOR, which is derived by an OR operation of the states of all pixels in a double column. FASTOR signal indicates that the analog signal of the pixel exceeds the threshold resulting in a hit detected in the pixel. The delay of the FASTOR response was measured with respect to the moment of the pulse injection via the timestamp at the EOC. Fig. 5 presents the delay of FASTOR as a function of the injected charge and analog power consumption. In the test, a pulse injection signal generated by the DAQ system was sent to a pixel. The DAQ system records the timestamp of the pulse injection as a timing reference with a step of 25 ns. The timestamp of hits was recorded with a resolution of 25 ns by the EOC circuit, and then was sent out to the DAQ system generating a FASTOR timestamp. For each injected signal value, the test was performed 1000 times to calculate the mean delay time. It is worth mentioning that by doing so, we assume the capacity of the charge injection system to amount precisely its layout-extracted value of 172 aF. One observes the delay time decreases with increasing injected charge. The bumps in the red and blue curves in figure 5 are likely attributed to the measurement discretization error (25 ns binning).

The time walk (variation of the delay as a function of the injected charge) varies with the bias current of the front-end (480 nA, 327 nA, 168 nA), which leads to different analog power consumption. A time walk of ~60-90 ns at a threshold of ~300 electrons was obtained for the analog power density of 50-140 mW/cm2, which basically agrees with design expectations. Note that the delay time includes the delay induced by the analog front-end, the in-pixel logic and the OR operation as well as the data transmission. The measured time walk determines the theoretical optimal time resolution of the chip. The setting of the bias current of pixels should consider the balance of low power and high time resolution. In the TaichuPix-2 chip, a trigger window of ± 3LSB (i.e. ± 75 ns) was set to cover the trigger uncertainty. Accordingly, the pixels can be set with an analog power of ~100 mW/cm2 (with the bias current of ~327 nA for the front-end) to be compatible with the default trigger window.

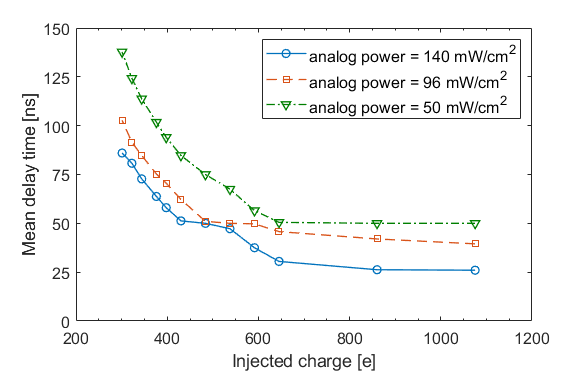


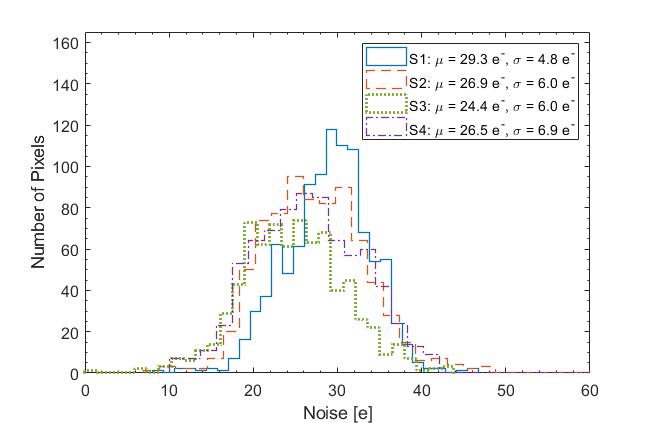
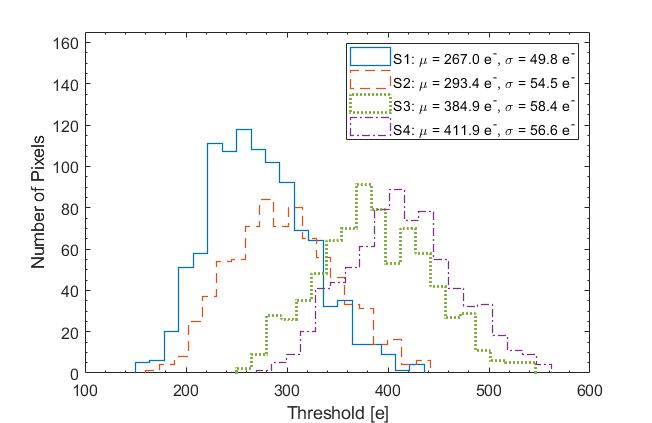
Fig. 5. Delay time of the FASTOR signal (at the EOC) of a pixel with respect to the signal injection as a function of the injected charge and the analog power consumption. The delay time was measured by the timestamp of a step of 25 ns.

To evaluate the threshold and noise performance of pixels, different charges were injected into each pixel to perform an S-curve scan. Then the threshold and noise are determined from the mean and standard deviation of the resulting S-curves. Note that all pixels share common biasing sources, due to space constraints in a pixel. Therefore, an individual tuning of the pixels is not feasible. As mentioned in Section 2.2, the biasing of the pixel was provided by the integrated DAC on the periphery. The pixel threshold increases with one of the biasing parameters ‘ITHR’. In the test, the minimum value of ‘ITHR’ was found to be much larger than the design, resulting in the desired threshold setting being unachievable. Fig.6 illustrates the measured threshold of the S1 sector as a function of ITHR, which is expressed in the DAC code. For all the threshold setting cases, the noise rates are less than 10-10/event/pixel. The simulated charge threshold with the nominal ITHR setting is about 150 e-. The design bug of the DAC is understood and will be fixed in the next design iterations but hampered us from using the nominal ITHR as design, leading to a higher threshold achieved in the measurements.



Fig. 6. Average threshold of pixel sector S1 as a function of threshold bias ‘ITHR’. ITHR was provided by an integrated 8-bit DAC.

Fig. 7 presents the threshold and the temporal noise (TN) distribution for the different pixel sectors as listed in table 2. The threshold dispersion measured in this work is the sum of both the fluctuations on the injected signal and the fluctuations on the threshold itself. The noise is found to be dominated by the Fixed Pattern Noise, which denotes the dispersion of thresholds of the pixels with the common ITHR setting. Sectors 3 and 4 show a higher threshold than sectors 1 and 2. This can be explained by the fact that the front-end designs in sectors 3 and 4 have a lower gain, which leads to a higher threshold level. The measured threshold and noise variation tendency between different sectors agree with the design. The S1 sector has the minimum mean threshold and total equivalent noise (including the temporal noise and the threshold dispersion).



1. (b)

Fig. 7. Threshold (a) and noise (b) distribution measured on the pixel sectors S1-S4.

### Response to 90Sr

The sensitivity of the TaichuPix-2 to radiation has been tested with a 90Sr source. A selected number of pixels were integrated with a dedicated readout chain, which allows observing the analog output for the pixel front-end. The analog signal of a pixel was accumulated by means of an oscilloscope, as shown in Fig. 8. One observed that the pulse length and delay times of the leading edge decrease with the signal amplitude increases. The distributions of the hits over the S1-S4 pixel sectors were also tested and remained without unexpected features.

The S1-S4 pixel sectors were exposed to the 90Sr source with different threshold settings (ITHR). The cluster size for each sector was analyzed with the hit address and timestamp information on the EOC and the acquisition system. Fig. 9 presents the average cluster size for each pixel sector as a function of the threshold setting. For all sectors, the cluster size decreases with the threshold increasing as expected. Sector 1 exhibits the largest average cluster size for the same threshold setting, which indicates S1 has the lowest threshold compared to the other sectors as verified by the test in section 3.2. The measured cluster size is larger than one and is likely attributed to charge sharing, that is beneficial for the spatial resolution.



Fig. 8. Response of a pixel of S1 sector to electrons from a 90Sr source, measured by an oscilloscope.



Fig. 9. The average cluster size for different pixel sectors exposure to a 90Sr source as a function of the threshold setting ‘ITHR’.

### Conclusion

The TaichuPix chip is a dedicated CMOS Pixel Sensor that is being developed for the first 6-layer silicon vertex detector prototype for the CEPC vertex detector R&D. The detector prototype needs to fulfill the requirement of 5 µm spatial resolution. The TaichuPix chip requires to achieve a 25 µm pixel pitch, 50 µm thickness and a hit rate of up to 36 MHz/cm2. TacihuPix-2, a small-scale prototype with the same features as the final full-scale chip, has been developed and characterized to address the chip architecture and major functionalities. Preliminary test results show the average temporal noise of pixel is 20-29 e- and the threshold dispersion is 50-58 e-, depending on the pixel variants. One of the two parallel in-pixel digital designs is properly operating at a 40 MHz clock. The measured time walk with the column-level timestamp logic indicates that a ~60 ns time resolution is conceptually reached. Preliminary tests of the TaichuPix-2 demonstrate successful integration of the in-pixel front-end and the FEI3-like digital logics, the periphery readout circuits and the slow control units. The properties of the variants of pixel cells are studied and it will guide the pixel design of the next prototype. First indications of average cluster sizes in the range of 1.6 to 2.2 could lead to benefit the position resolution. The next design iteration, a full-scale (26 × 17 mm2) TaichuPix prototype, is in fabrication. The spatial resolution and detection efficiency will be measured with the first full-scale TaichuPix with a test beam in the near future.

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