清華大學 Tsinghua University

核电子学实验室 Laboratory of Nuclear Electronics

Status of low power FEE ASIC for TPC

Wei Liu[1,2], Canwen Liu[1,2] ,Tong Wei[1,2], **Zhi Deng[1,2]**, Huirong Qi[3]

[1] Department of Engineering Physics, Tsinghua University, Beijing, China
[2]Key Laboratory of Particle & Radiation Imaging, Ministry of Education, Beijing, China
[3]Institute of High Energy Physics, Chinese Academy of Science, Beijing, China

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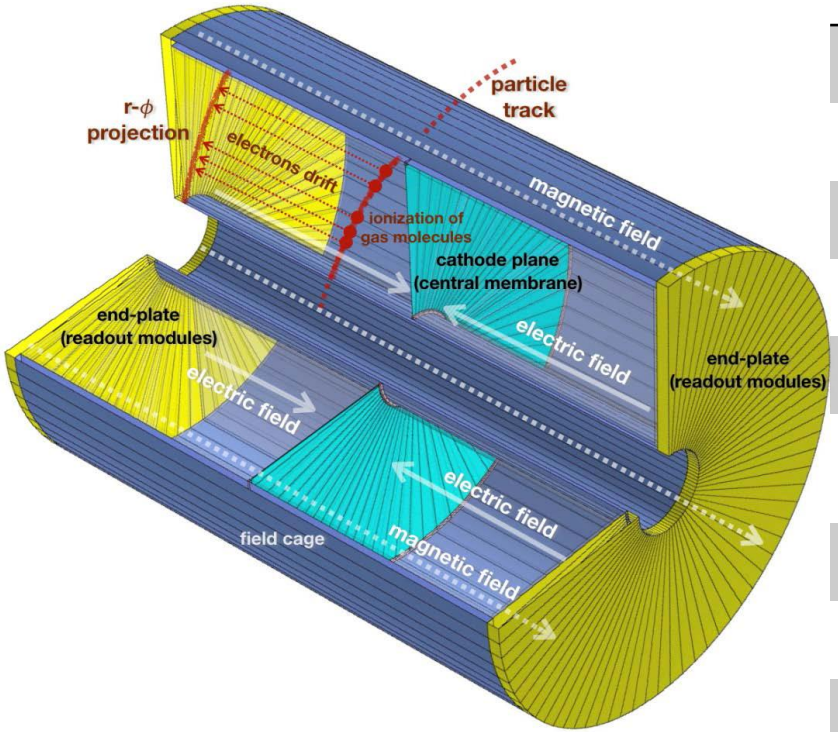
Outlines

- Introduction
- Progress of the WASA chip Development
- R&D on Macro-pixel TPC readout
- Summary

Introduction

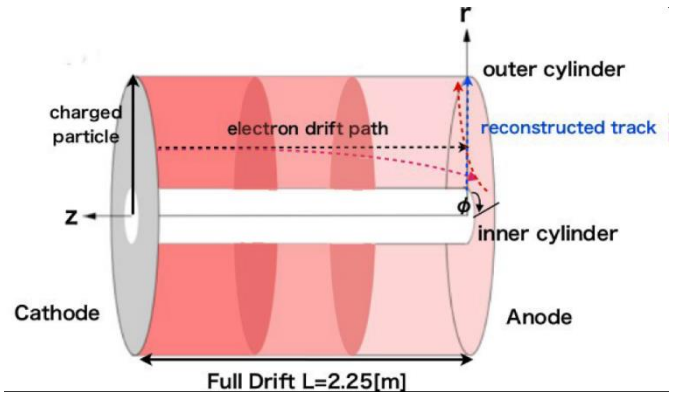


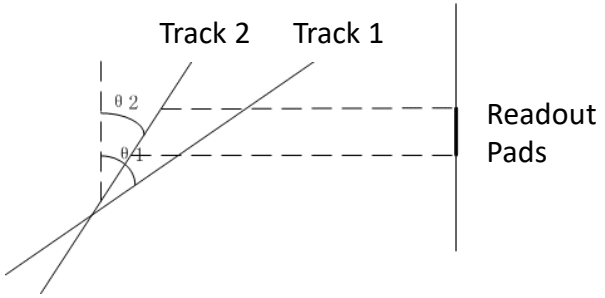
Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm × (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6mm) are needed, resulting in ~1 million channel of readout electronics
- Need low power consumption readout electronics working at continuous mode

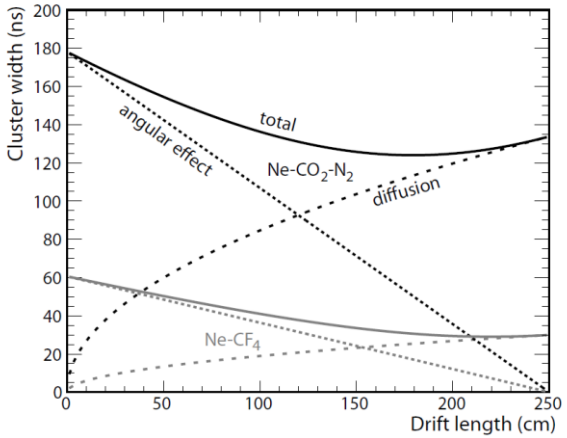
Requirements for TPC Pad Readout

- Pad readout needs waveform sampling

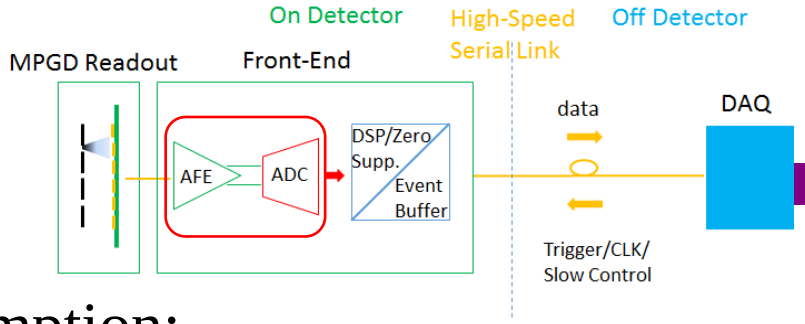




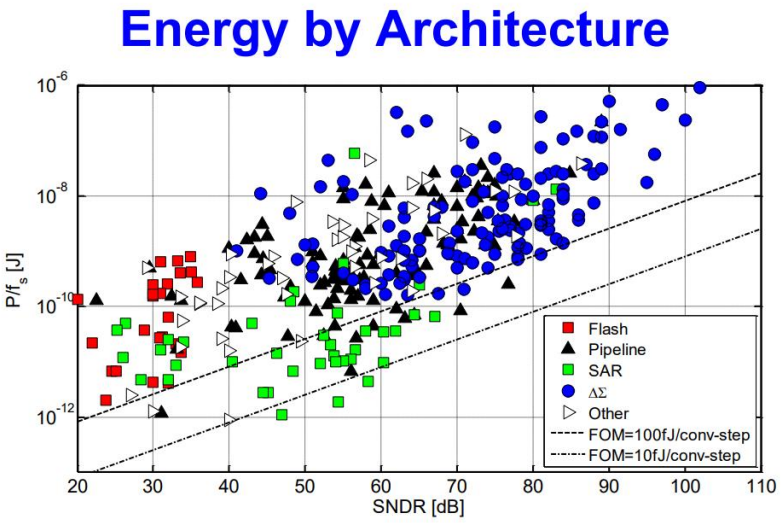
Parameters	**SPECs**
No. of channels	2×10^6
Power Consumption	<10 mW/ch
SNR	~20 @10 pF
Dynamic Range	120 fC
Noise	900 e@10 pF
Peaking time	~160 ns
Sampling Rate	20-40 MS/s
Sampling resolution	8-10 bit

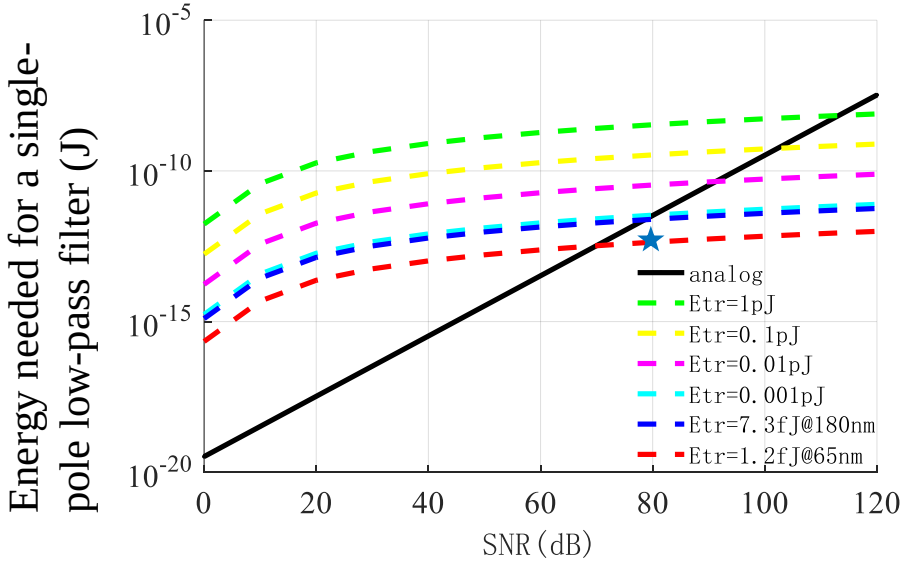


How to save power…



- In order to reduce the power consumption:
  - Using more advanced 65 nm CMOS process favoring digital logics
  - Less analog circuits:
    - ADC structure : pipeline → SAR (Successive Approximation Register)
    - CR-(RC)^n →CR-RC, moving high order shaping to digital domain

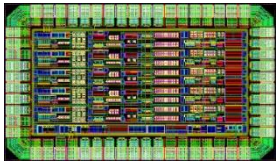




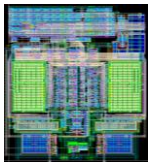
Progress on the WASA chip Development

2017

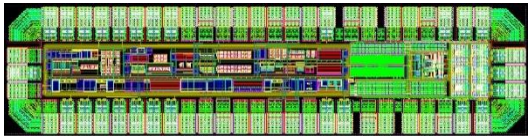
5ch Analog FEE



SAR ADC

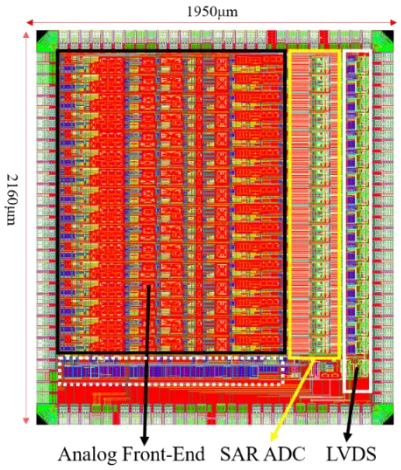


AFE+SAR ADC



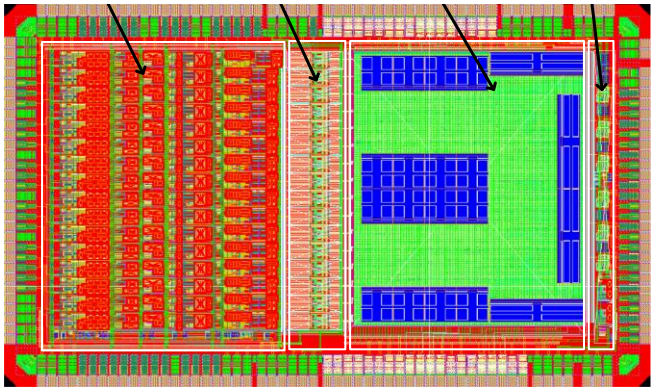
2019

WASA_v0: 16ch AFE+SARADC



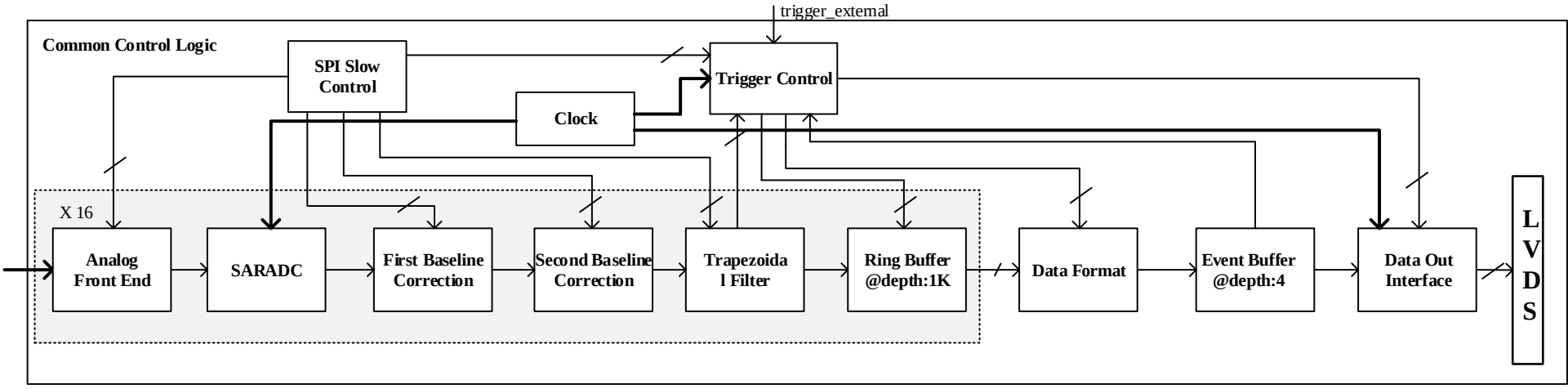
2021

WASA_v1: 16ch AFE+SARADC+DSP



WASA: WAveform SAmpling ASIC for TPC

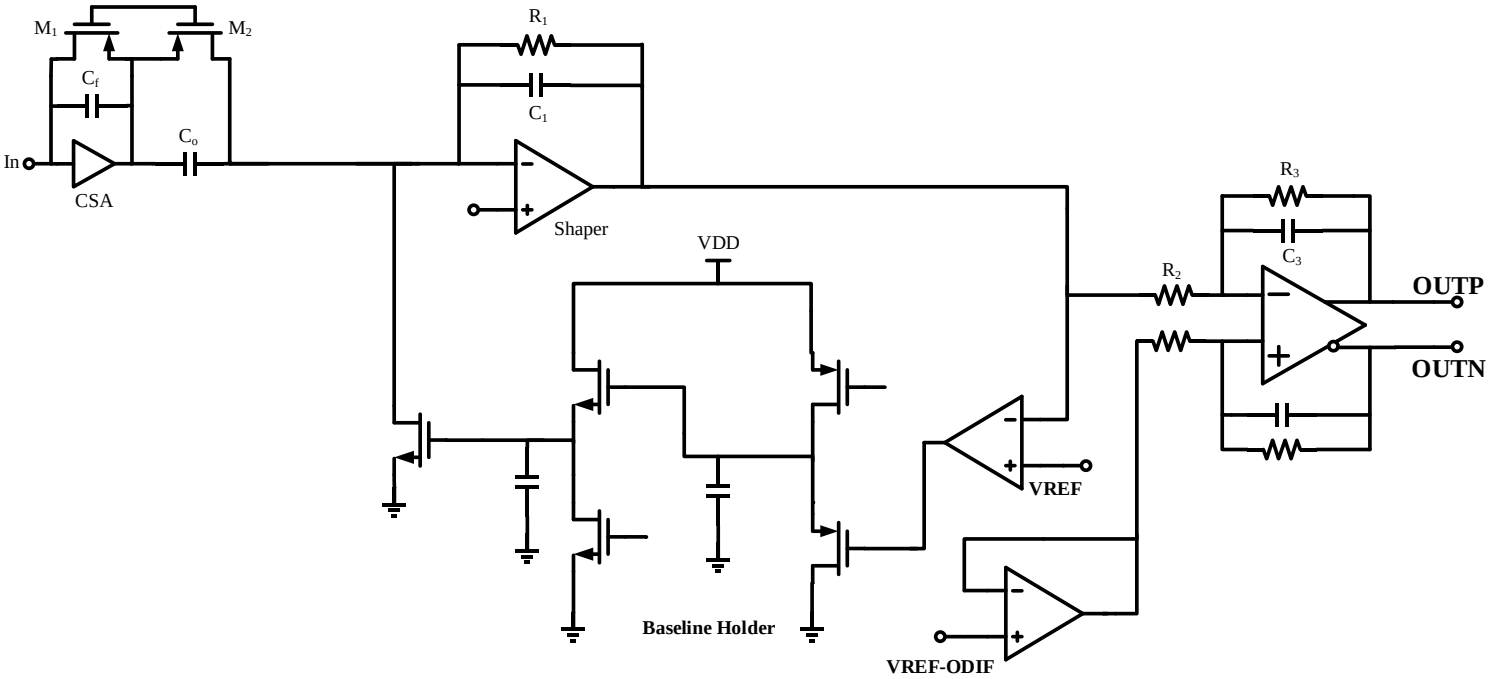
- Analog Front-End: Preamplifier + CR-RC shaper + Fully differential output
- SAR ADC: contributed by Fule Li's group @ Tsinghua
- Digital signal processing:
  - Two stage baseline corrections (learnt from SAMPA)
  - Digital trapezoidal filter, to make pulse shape symmetric and shorter
- Control logics: Trigger + data buffer (ring buffer and event buffer)



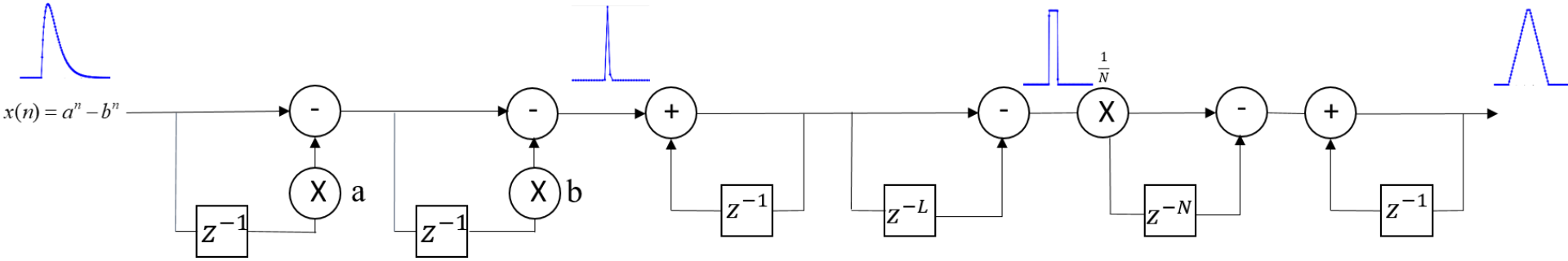
WASA: analog front-end

- Low power supply design: 1.2 V
  - Fully differential output
- Power optimization orientated, instead of noise optimization orientated

Parameters	SPECs	Simulation
Shaper	CR-RC	CR-RC
Shaping time	160 ns	160 ns
Gain	10 mV/fC	10 mV/fC
Dynamic Range	120 fC	120 fC
INL	<1 %	<1 %
ENC	500 e @ 10 pF	306 e @10 pF
Crosstalk	<1 %	0.12 %
Power	<2.5 mW/ch	1.4 mW/ch

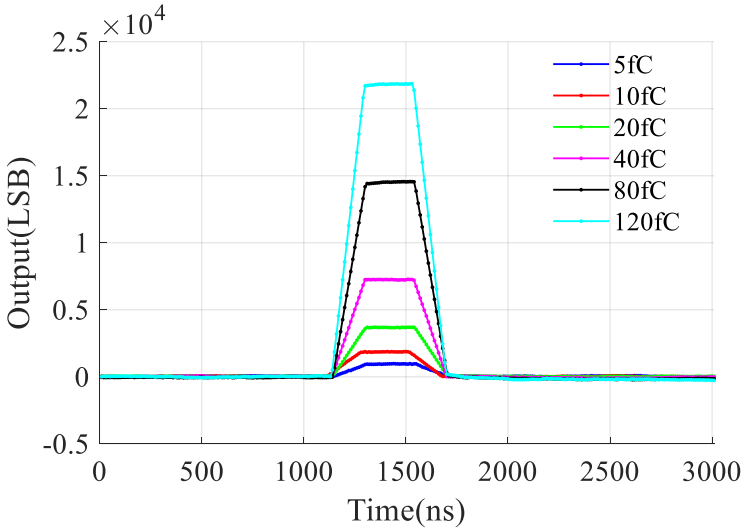


WASA: digital trapezoid filter

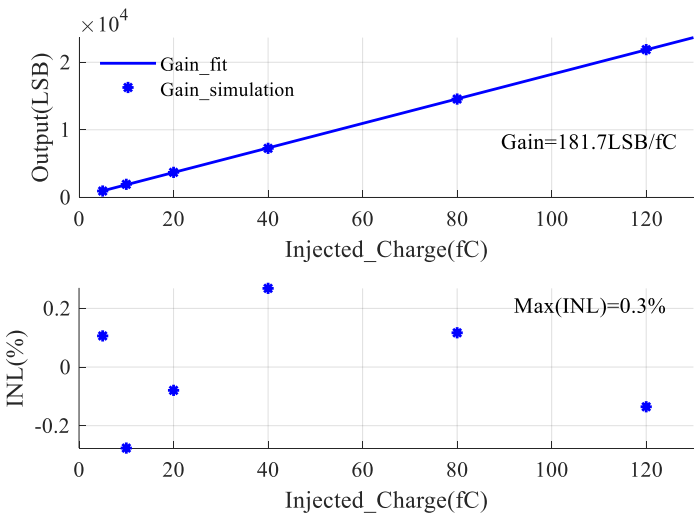


Valentin T. Jordanov, Unfolding-synthesis technique for digital pulse processing. Part 1: Unfolding, NIMA Vol 805, 2016， 63-71

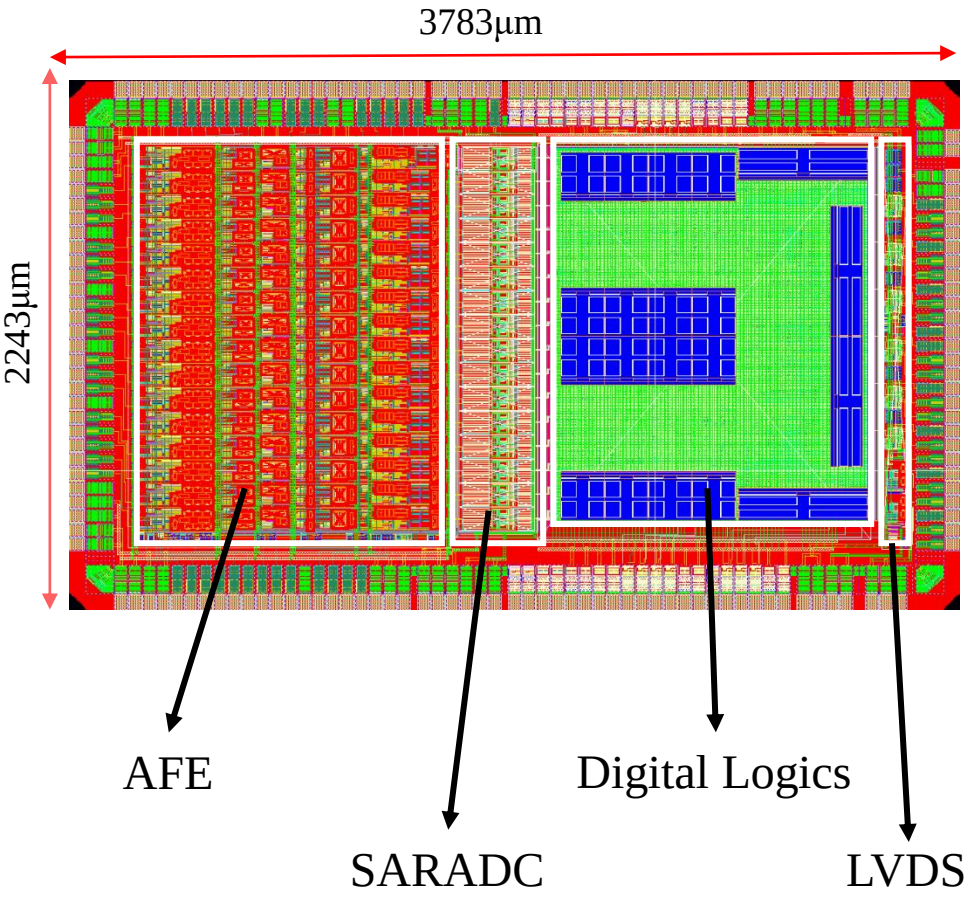
- Transient Outputs



- Linearity



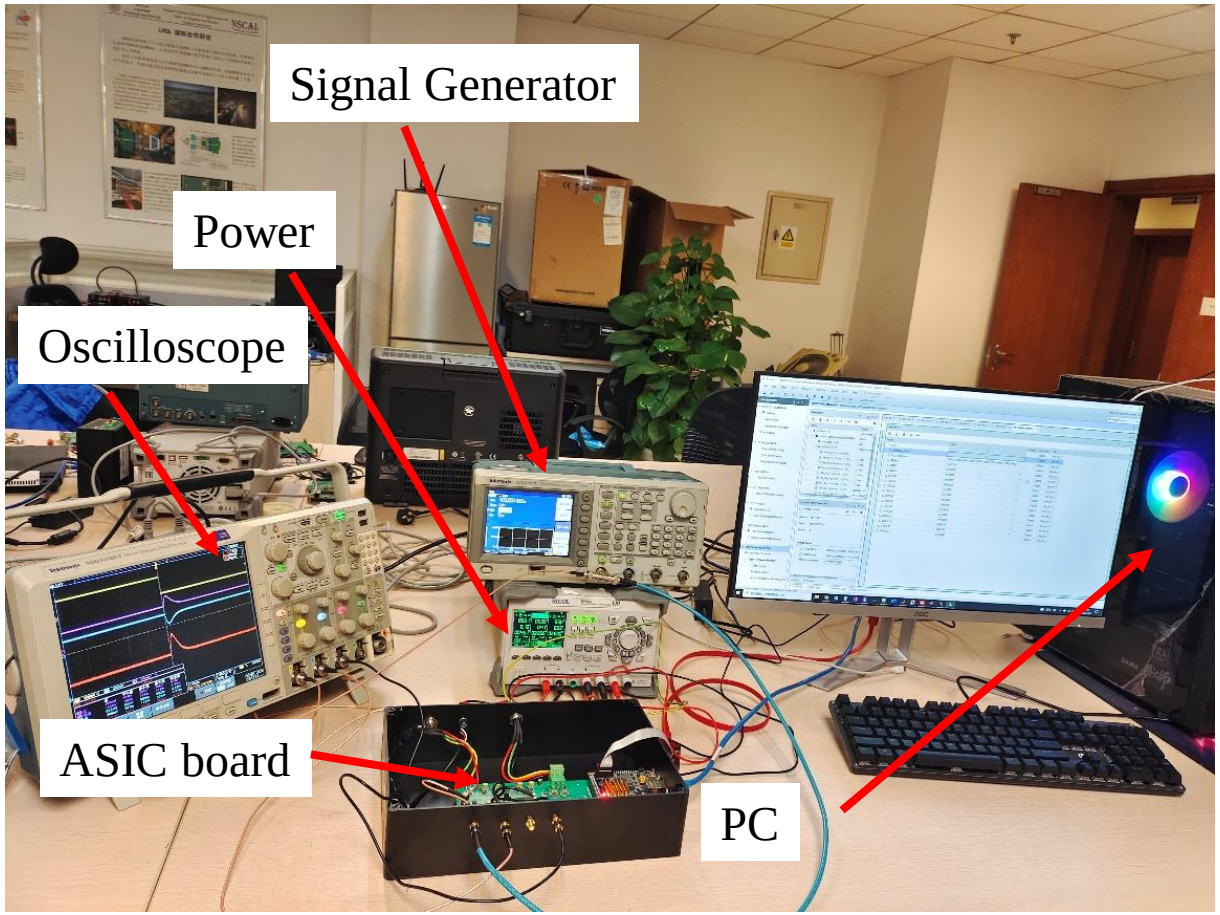
WASA: chip layout



- Layout floor plan:
  - The die size: 3783 µm x 2243 µm
  - Separated power supply:
    - Analog Front-End
    - SAR ADC
    - Digital Logics
    - LVDS driver
  - Guarding ring insert between
- ASIC submitted in Jan, 2022 and received in March, 2022

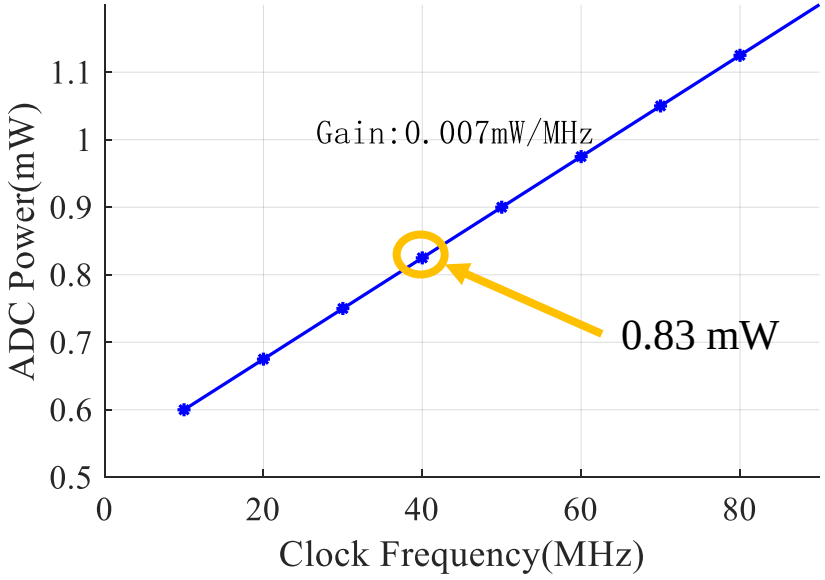
Test results

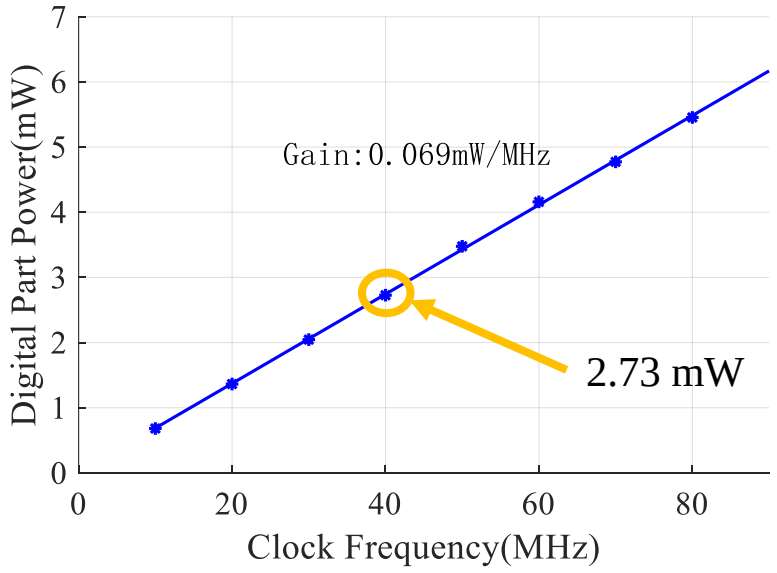
- Test Setup



Test results

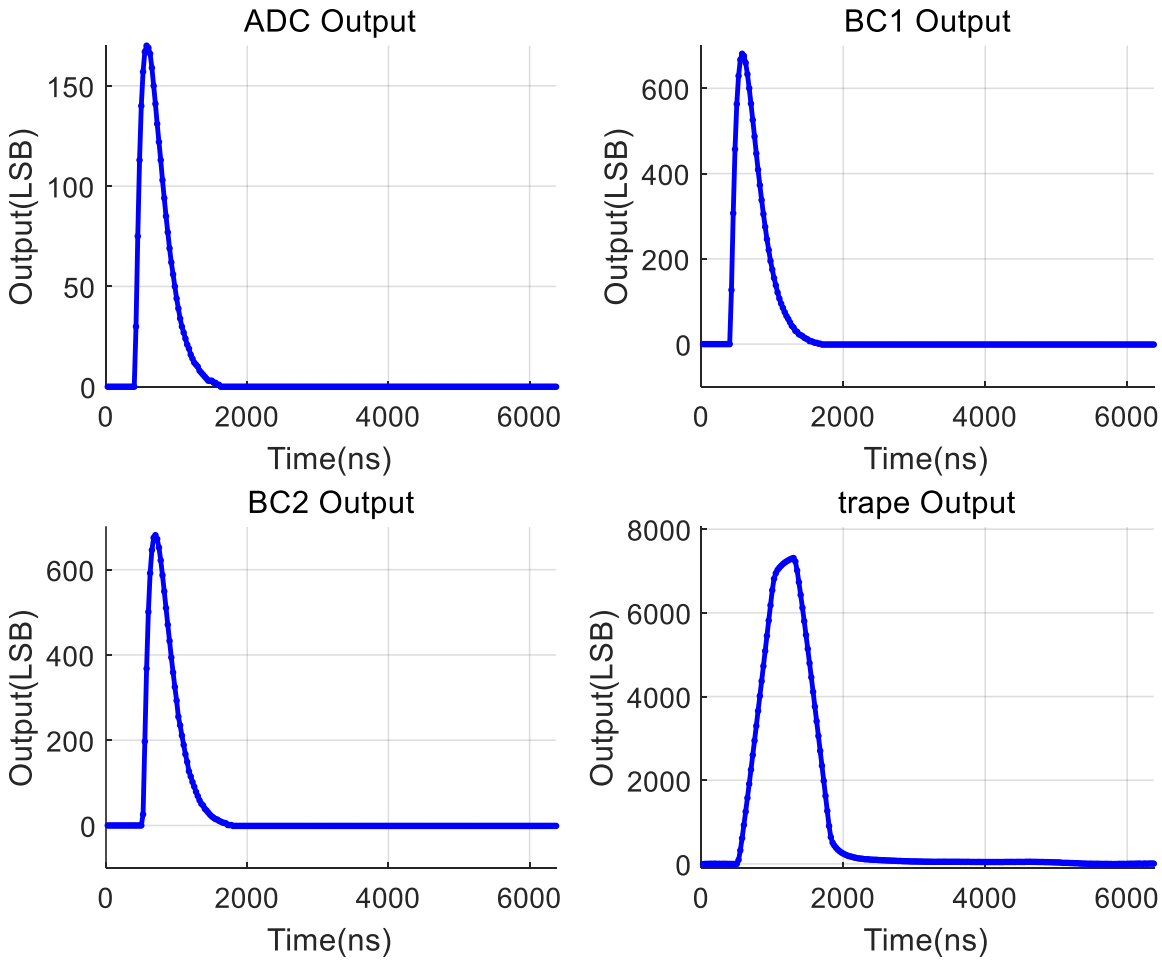
- Power consumption = 4.94 mW/ch @ 40 MHz
  - AFE: 1.38 mW/ch
  - ADC: 0.83 mW/ch
  - Digital logics: 2.73 mW/ch
- Power consumption = 3.42 mW/ch @ 20 MHz





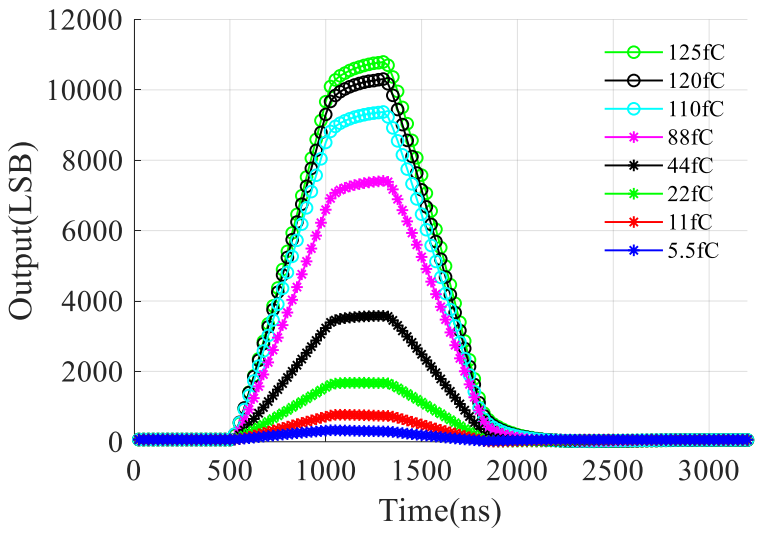
Test results

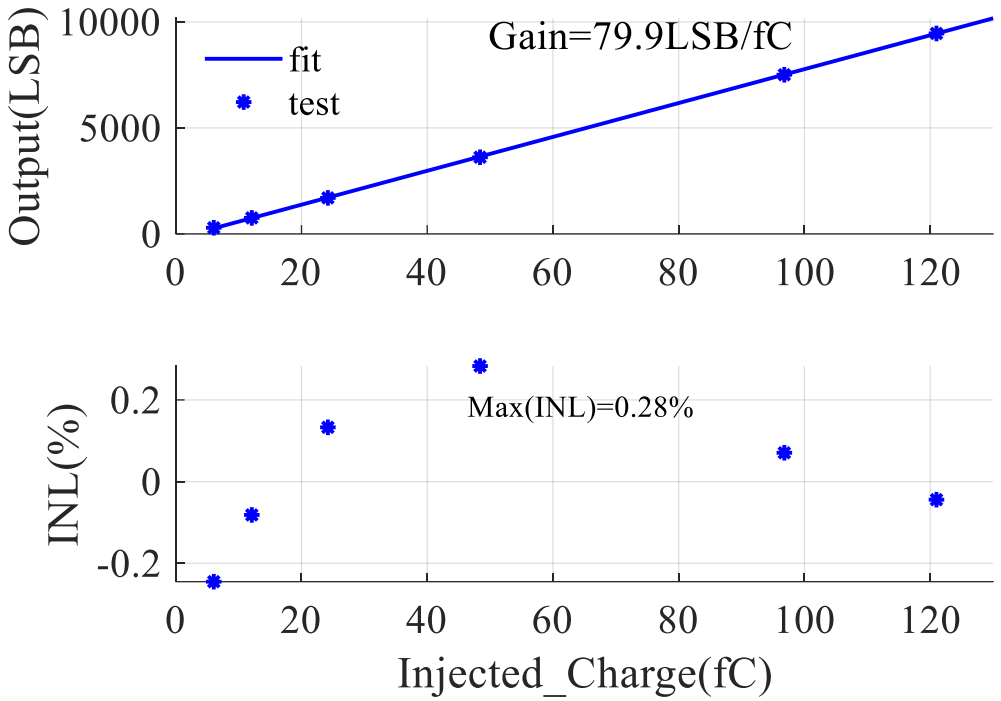
- Transient Waveforms of internal signal processing nodes



Test results

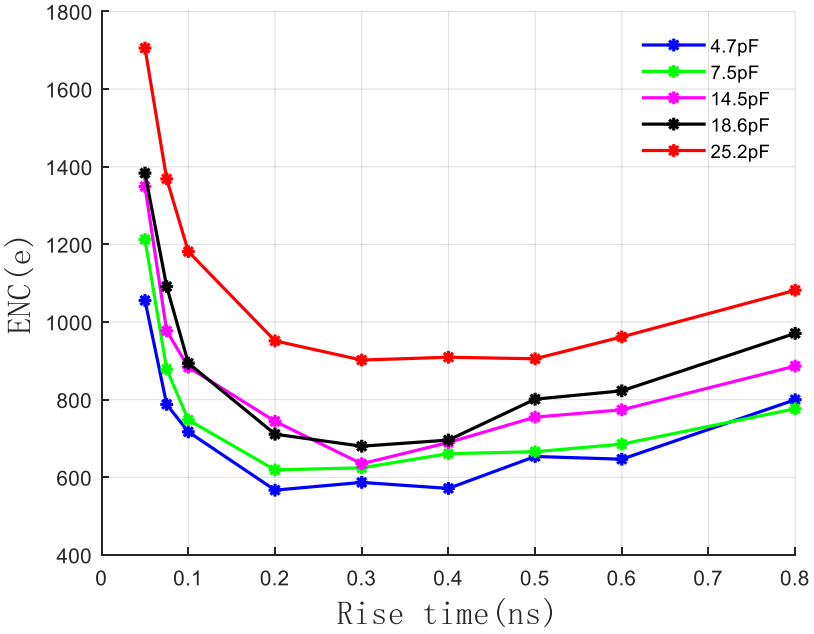
- Non-Linearity: INL< 0.28%

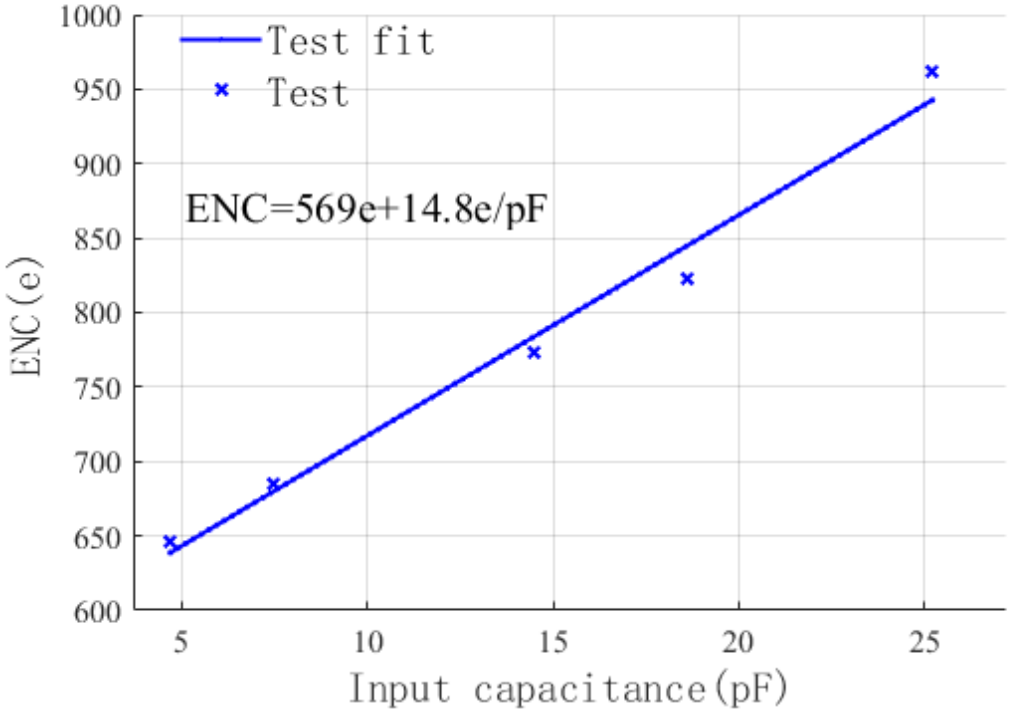




Test results

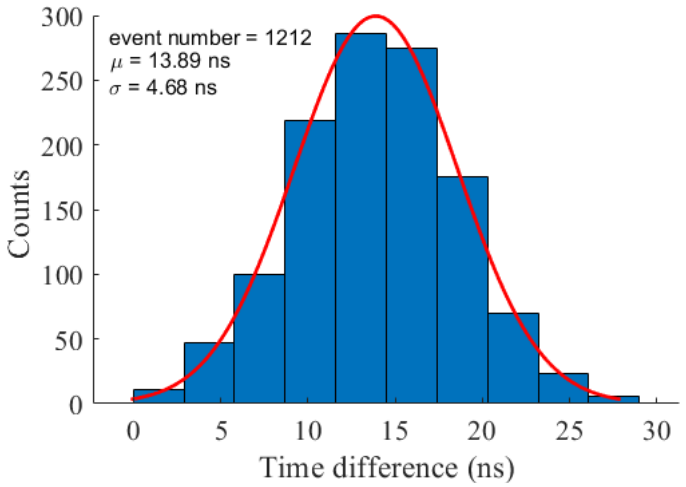
- Noise @ 10mV/fC:
  - ENC = 569 e+14.8 e/pF @ rising time = 0.6 μs and flat top time = 0.2 μs

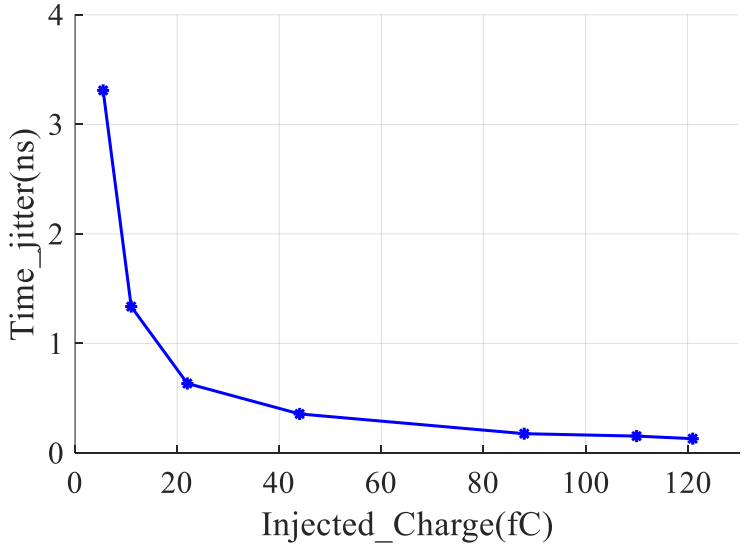


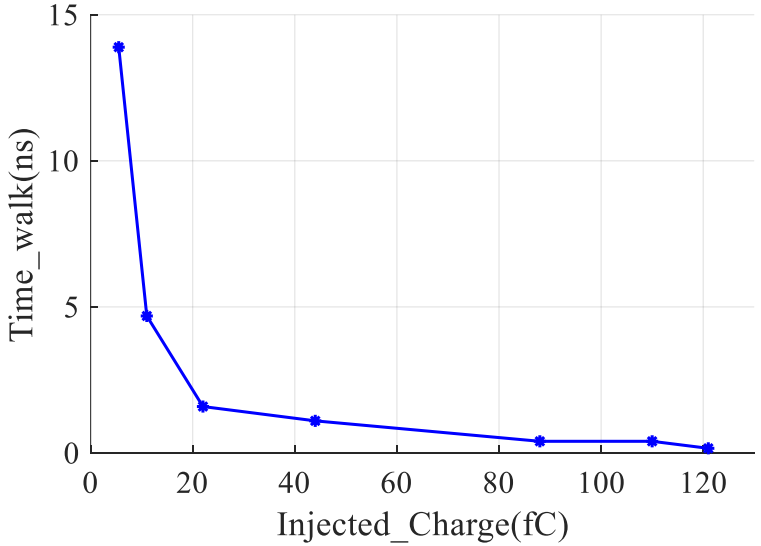


Test results

- CFD Timing @ Vth = 0.4 Vp
  - CR-RC shaping time = 160 ns
  - T_r = 600 ns, T_{flat} = 200 ns
  - Time jitter < 3 ns
  - Time walk < 15 ns







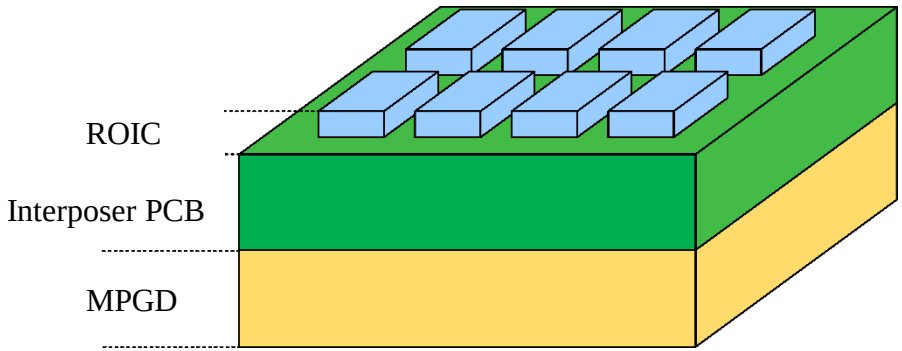
Test results

- Compare to current TPC FEE ASICs

	PASA+ALTRO	Super-ALTRO	SAMPA	WASA_v1
TPC	ALICE	ILC	ALICE upgrade	CEPC
Pad Size	4x7.5 mm^2	1x6 mm^2	4x7.5 mm^2	1x6 mm^2
No. of Channels	5.7× 10^5	1-2 × 10^6	5.7 × 10^5	2 x×10^6
Readout Detector	MWPC	GEM/MicroMegas	GEM	GEM/MicroMegas
Gain	12 mV/fC	12-27 mV/fC	20/30 mV/fC	10-40 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^4$	CR-$(RC)^4$	CR-RC
Peaking time	200 ns	30-120 ns	80/160 ns	160-400 ns
ENC	370+14.6 e/pF	520 e	246+36 e/pF	569+14.8 e/pF
Waveform Sampler	Pipeline ADC	Pipeline ADC	SAR ADC	SAR ADC
Sampling Rate	10 MHz	40 MHz	10 MHz	10-100 MHz
Sampling Resolution	10 bit	10 bit	10 bit	10 bit
Power: AFE	11.7 mW/ch	10.3 mW/ch	9 mW/ch	1.4 mW/ch
Power: ADC	12.5 mW/ch	33 mW/ch	1.5 mW/ch	0.8 mW/ch@40 MHz
Power: Digital Logics	7.5 mW/ch	4.0 mW/ch	6.5 mW/ch	2.7 mW/ch@40 MHz
Total Power	31.7 mW/ch@10MHz	47.3 mW/ch@40 MHz	17 mW/ch@10 MHz	4.9 mW/ch@40 MHz
CMOS Process	250 nm	130 nm	130 nm	65 nm

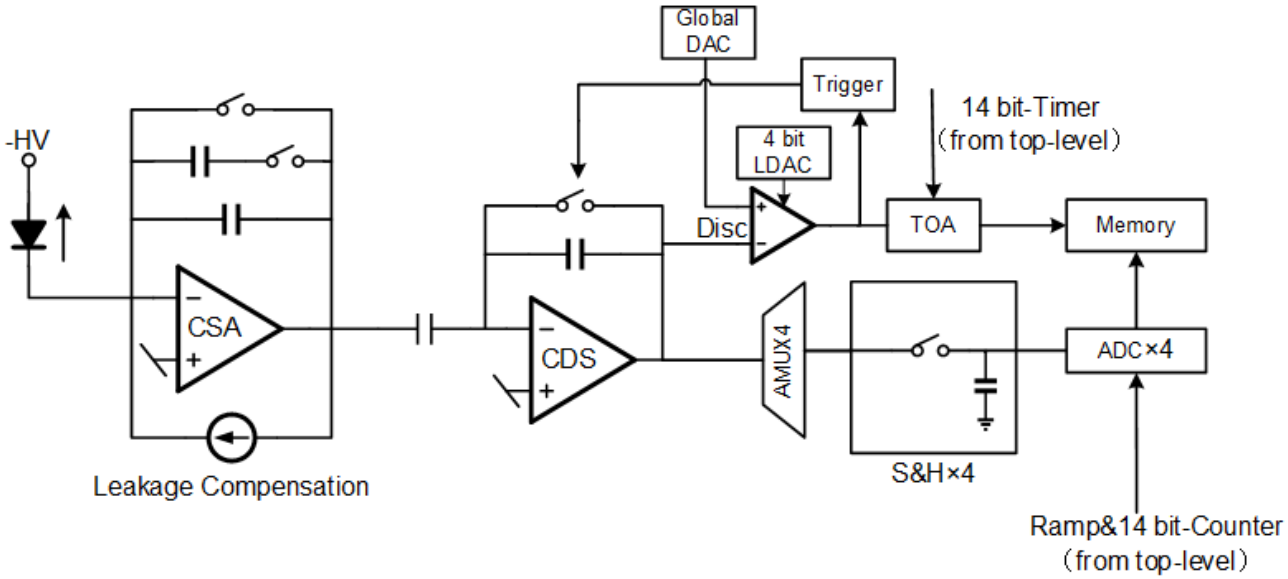
R&D on Macro-Pixel TPC Readout

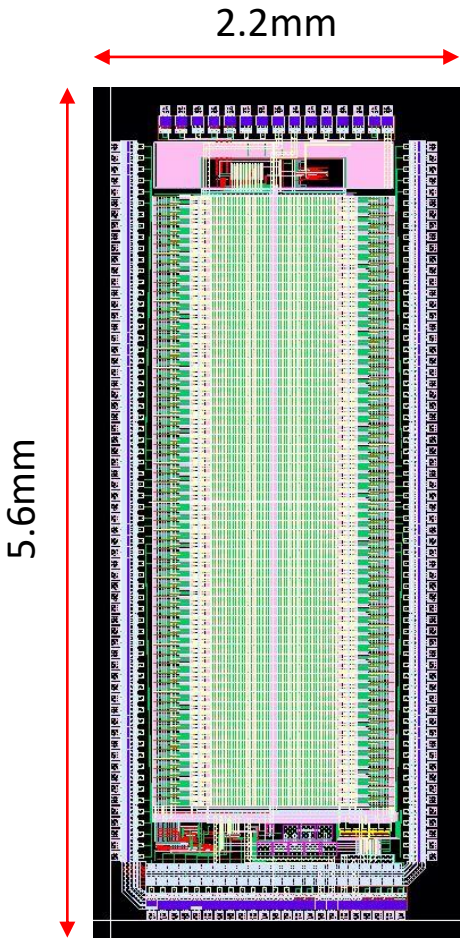
- Large Pixel Readout
  - 1 mm x 6 mm → 0.5 mm pixel
  - Higher precision, higher rate
  - Potential for dN/dx
- Concept Design
  - ROIC +Interposer PCB as RDL
  - High metal coverage, 4-side buttable
  - Low power Energy/Timing measurement ASIC
    - ~100 e noise
    - 5 ns drift time resolution
    - <100 mW/cm^2 (GOAL, not first version)



Readout ASIC Design

- Charge Sensitive Preamplifier(CSA)
- CDS amplifier provides additional gain and noise shaping
- 14-bit Wilkinson type ADC each pixel
- Timing discriminator with14-bit TOA (Time of Arrival) information

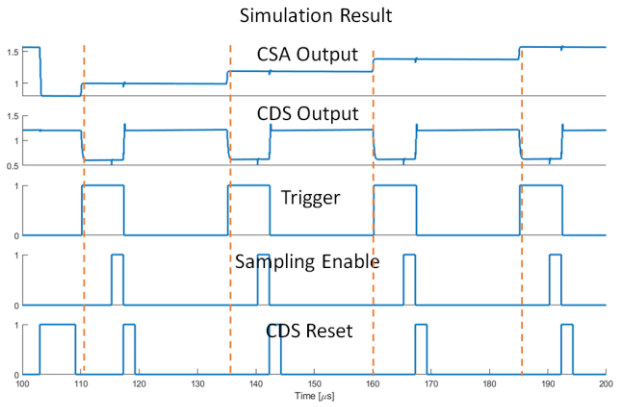


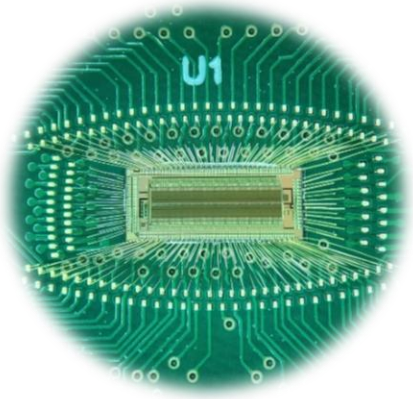


Readout ASIC Design

- Specifications

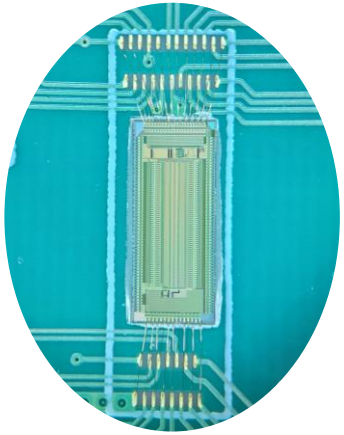
Channel No.	128	Integration Time	≥90% Frame Cycle
Frame Rate	10 kfps	Noise(simulated)	~100 e(ENC@0.5 pF Input)
Gain	40 mV/fC 6 mV/fC	Resolution	Energy:14 bit Time:14 bit(5ns bin)
Memory Depth	4 events/pixel/frame	Power Consumption	1.36 mW/pixel 531mW/cm2
Input Range	18.75 fC 125 fC	Trigger Mode	1. Local Self Trigger 2. Global Self Trigger 3. Global External Trigger
Count Rate	40 kcps/pixel	Technology	180 nm CMOS

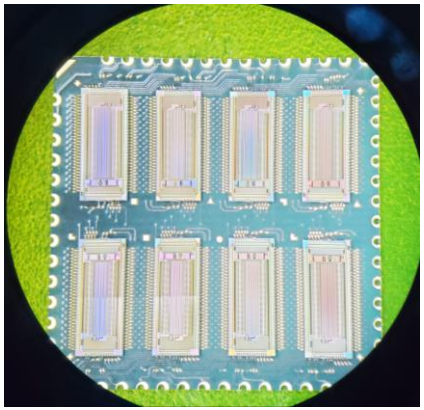


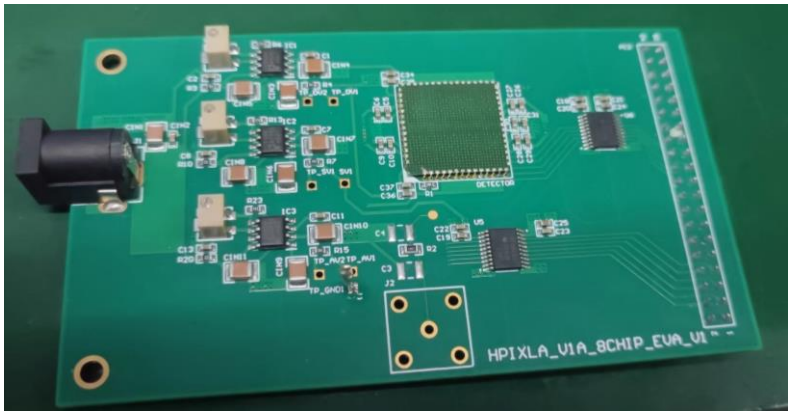


Readout Module

- PCB interposer as RDL:
  - Pixel size: 0.5 mm x 0.5 mm
  - Pixel array per module: 32 x 32 (1024 channels)
  - Chips per module: 8

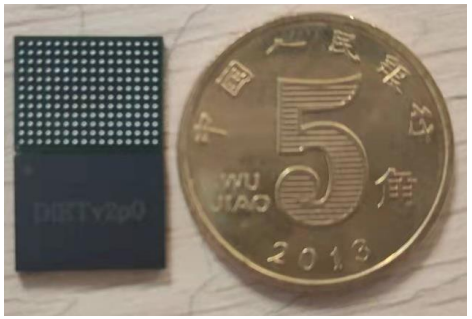






Summary

- A 16 channel low power readout ASIC WASA has been successfully developed and evaluated
  - The power consumption is 4.94 mW/ch @ 40 MHz
    - P_{AFE}=1. 38 mW/ch
    - P_{ADC} = 0.83 mW/ch
    - $P_{Digital}$ = 2.73 mW/ch



  - ENC = 569 e+14.8 e/pF @ gain=10 mV/fC with on-chip digital trapezoidal filter
  - Next step: BGA package 16 x 11 (11.05 mm x 7.8 mm)
- R&D on macro-pixel TPC has been started
  - The first version ROIC has been received and under test
  - RDL PCB substrate has been designed and module assembly tested
  - Next step: ROIC and module test

Thank You