FE and DAQ electronics for a cluster counting drift chamber

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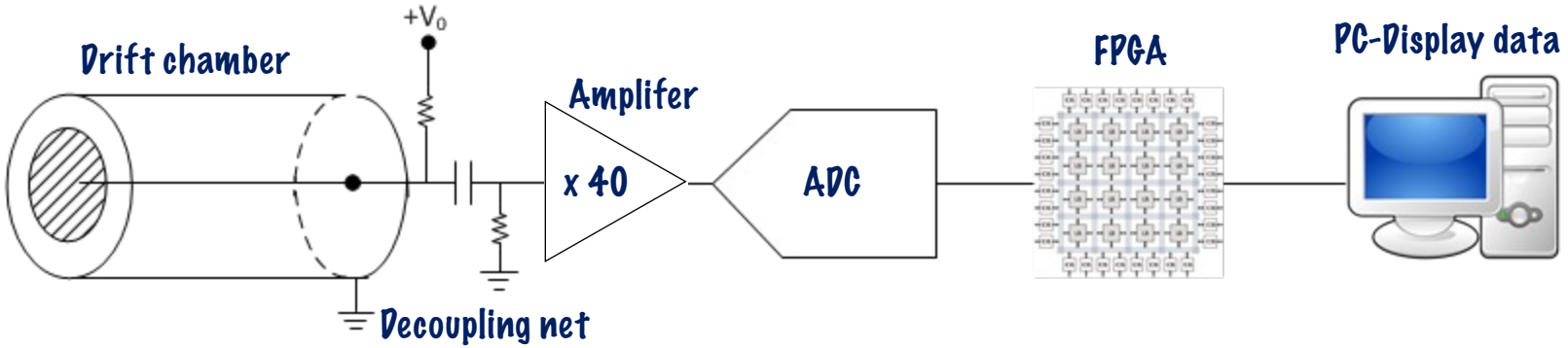
Outline

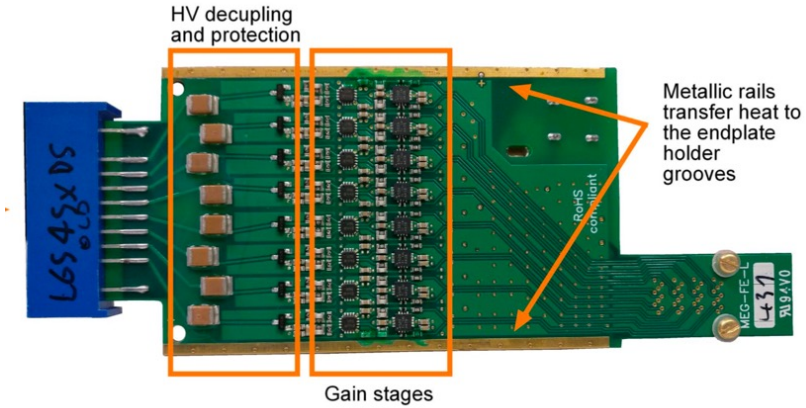
- Data acquistion
- The front end
  - MEG CDCH FE
  - VGA amplifier
  - DVGA multichannel amplifier
- CCT algorithm
- Digitizier and ADC

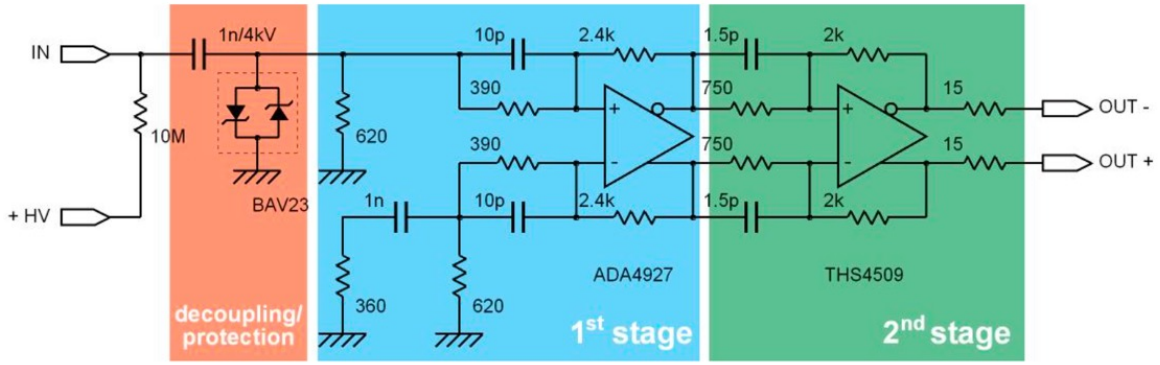
Data acquisition chain

- To read the signals produced by a drift chamber you need some essential elements, each of which must be designed according to the specifications (gas, wire size, electric field …) of the detector. In particular for drift chambers with helium-based gas mixtures, where the low amplitude signals from the sense wires are of a ~few mV.
- The signals have to be managed from the following chain:
  - **Decoupling net**
  - **Amplifier:** it has to be designed for a gain which must produce a suitable read-out signal for further processing, low power consumption, a bandwidth adequate to the expected signal spectral density and a fast pulse rise time response, to exploit the cluster timing technique.
  - **ADC+FPGA:** The resolution and the bandwidth of the ADC are chosen according to the signal produced by the amplifier. In particular, resolution is important to be able to find even the smallest signal peaks. The FPGA must be chosen based on the number of ADC channels it has to acquire and process.



The Amplifier for DC (1/3)



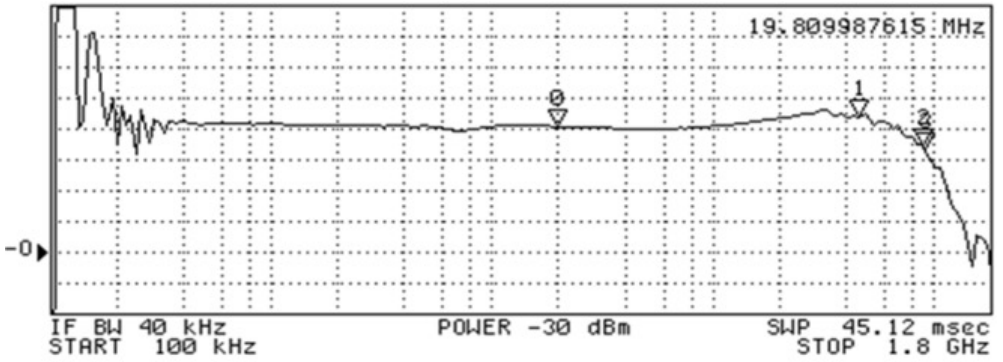


Amplifier used in MEG-II Cylindrical DCH

- **Two stage amplifiers** based on commercial devices:
  - **ADA4927 (AD)** **Ultralow distortion** current feedback
  - **THS4509 (TI)** Wideband **low noise** fully differential amplifier (driver for the ADC)

- **Pre-emphasis implemented** on both stages to balance the attenuation of output cable
- High overall bandwidth (F.E. input to DRS WD input): **~1 GHz**
- Low power: **50 mW @ ±2V**

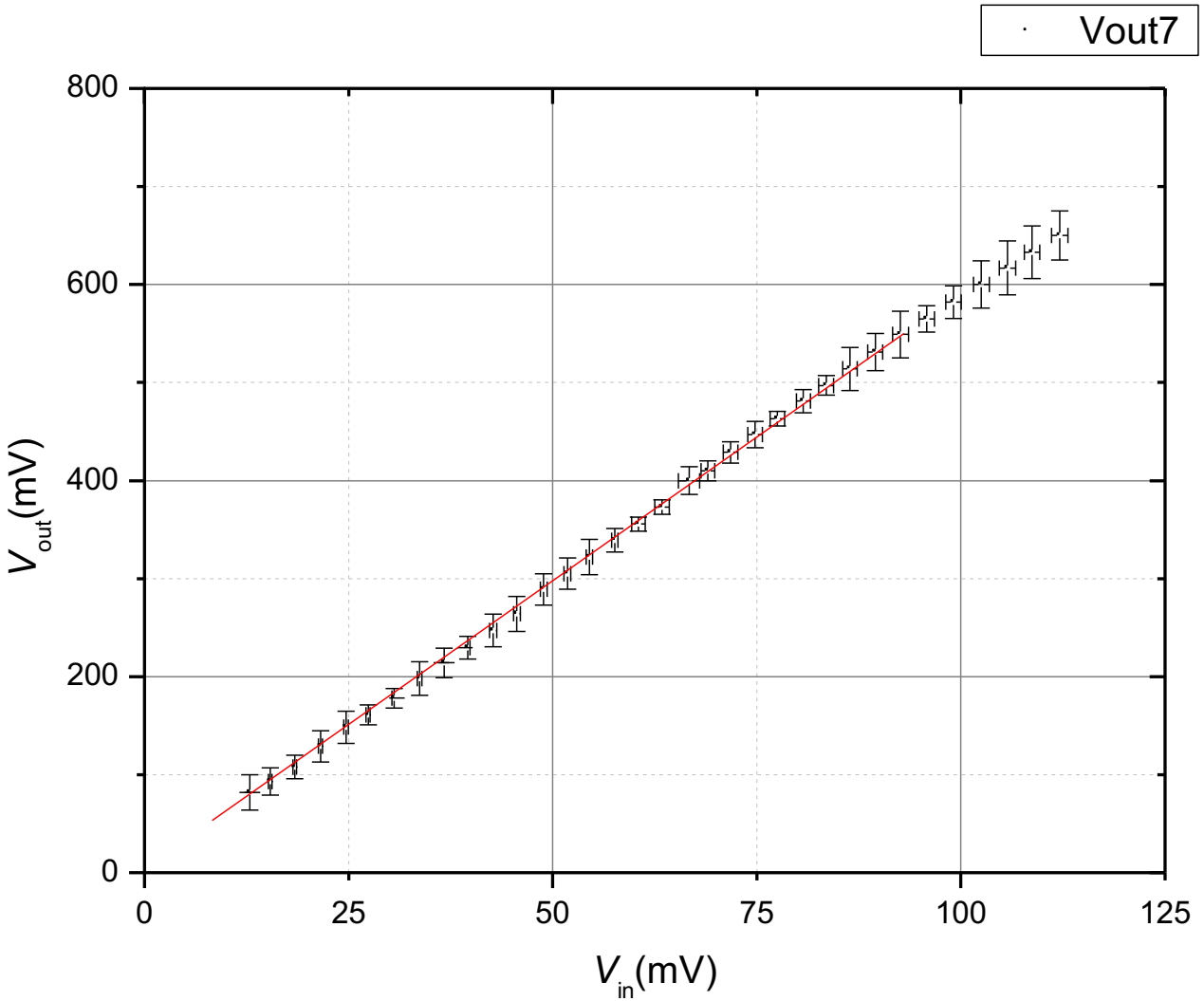
Gain and Bandwidth after cable



N	SWP PARAM	VAL
0	19.809987615 MHz	20.279 dB
1	456.600249532 MHz	21.773 dB
2	884.527480154 MHz	17.094 dB
3	899.750691731 MHz	16.686 dB

The Amplifier for DC (1/3):Some performance

- Linearity for each channel of the FE board has been measured
  - Gain (V_{out}/V_{in}) is 19 dB (middle bandwidth) on 120Ω load
  - Mean non-linearity is less then 0.10% (V_{in}: 15mV ÷ 75mV)
- Cross talk between adjacent channels (Ch+1) is 1.3%, cross talk to next channel (Ch+2) is negligible (<0.5%)
- Noise level measured (in area) is less then 2mV, after 5m long cable on a 120Ω resistive load



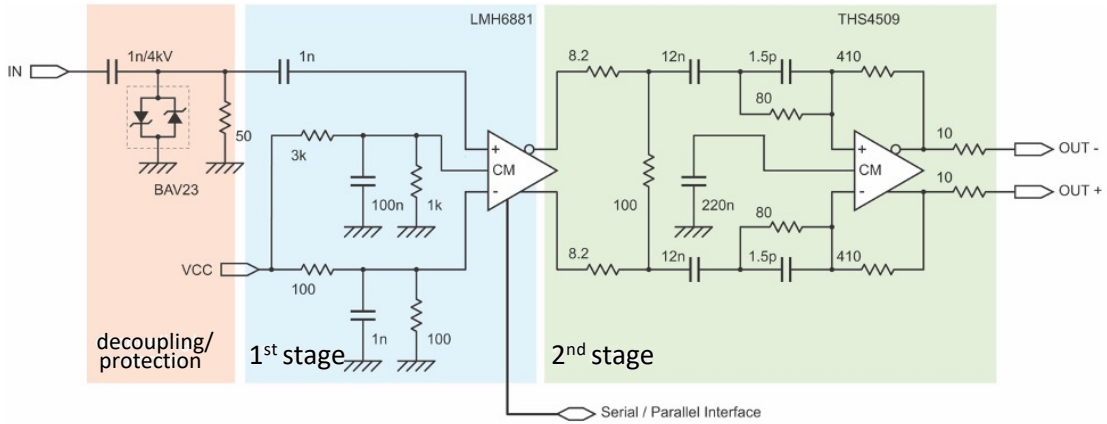
The Amplifier for DC (2/3)

Possible Amplifier

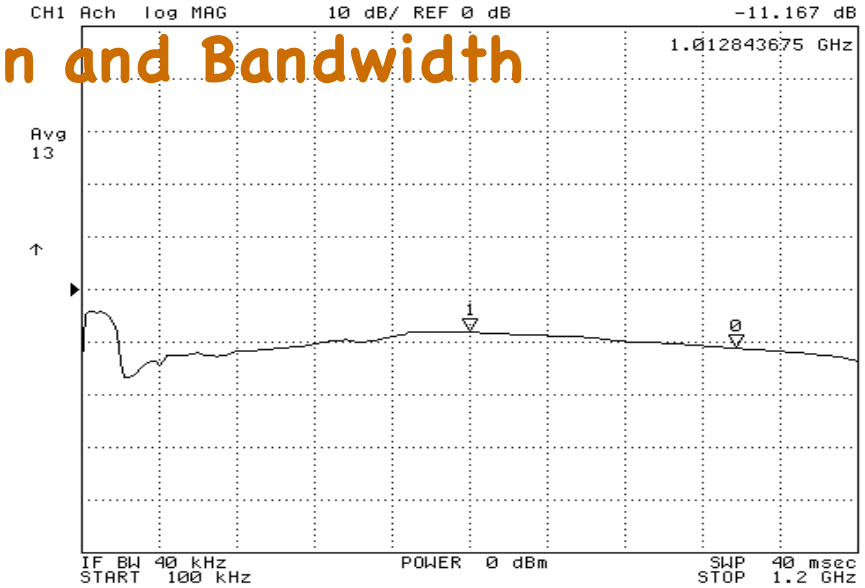
- Two stage amplifiers based on commercial devices:
  - **Variable gain LMH6881** is a high-speed, high-performance fully differential programmable amplifier (remote control via SPI)
  - **THS4509 (TI)** Wideband low noise fully differential amplifier

- The gain stage supports **gain settings** up to about **50 dB** with small accurate **0.25 dB gain steps**. The VGA can be also parallel programmed.

- The Bandwidth is about 1GHZ

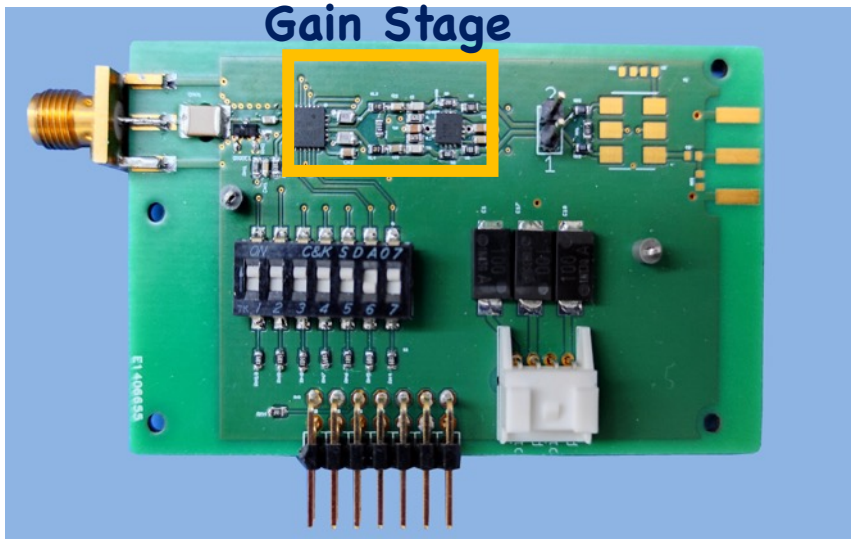


Gain and Bandwidth



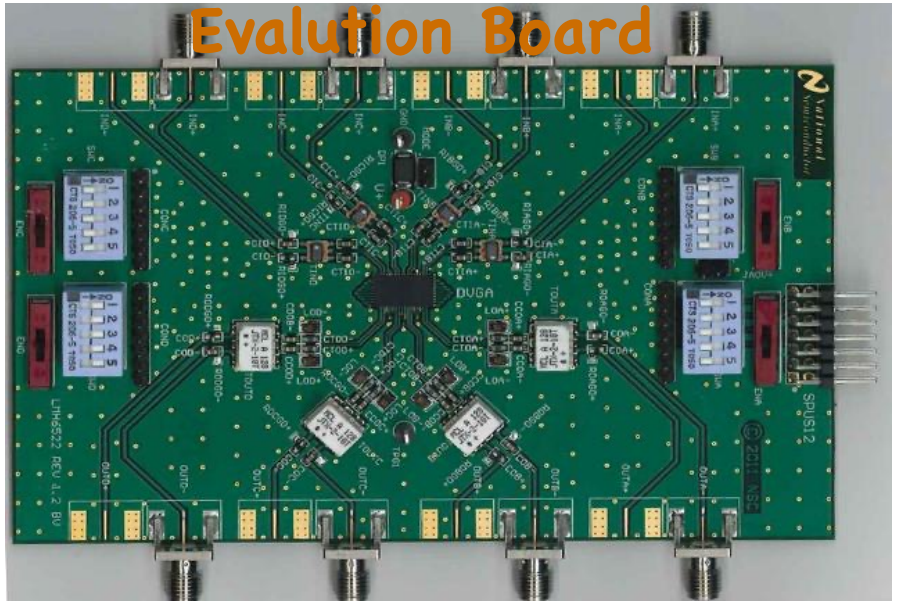
Mode/Gain programming. Through these dip switches it is possible to select the way to **control the gain of the first stage**, serial or parallel, in the **20 dB ÷ 49 dB** range.

Prototype PCB



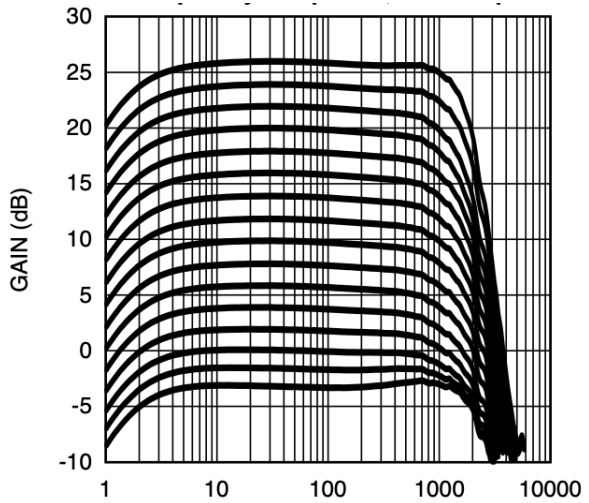
The Amplifier for DC (3/3)

- The problem with the amplifiers seen above is that they are single-channel. Therefore, for a DC with several tens of thousand channels, the amplifier PCBs need considerable space close to the detector and one has also to consider the distribution of the power and of cooling.
- The basic idea is to use a single chip to drive one or more multi-channel digitizers



Possible Multi-channel Amplifier

- The **LMH6522** contains four, high performance, digitally controlled variable gain amplifiers (DVGA).
- The gain is digitally controlled over a 31 dB range.
- Gain Step Accuracy: 0.2 dB
- Disable Function for Each Channel
- The Bandwidth is about 1,5 GHz
- Cross talk between adjacent channels is -65 dBc
- Low Power Mode for Power Management Flexibility (about 400mA)



Data reduction and pre-processing of DCH signals

High speed digitization (2 GSa/s) for CC ⟹ Transfer rates in excess of TB/s at the Z–pole running

- **Data reduction strategy:** transfer, for each hit drift cell, only the minimal information relevant to apply the **Cluster Counting/Timing (CTT) techniques**, i.e. the **amplitude** and the **arrival time of each peak** associated with **each individual ionization electron** ⟹ **CTT algorithms!**

  ► Use of a **FPGA** for the **real-time data analysis** of drift chamber signals **digitized by an ADC.**
  Acquire the signals converted ⟹ process with cluster counting algorithms (aimed also at **reducing the data throughput**) ⟹ send the processed information to a back-end computer via an Ethernet interface.

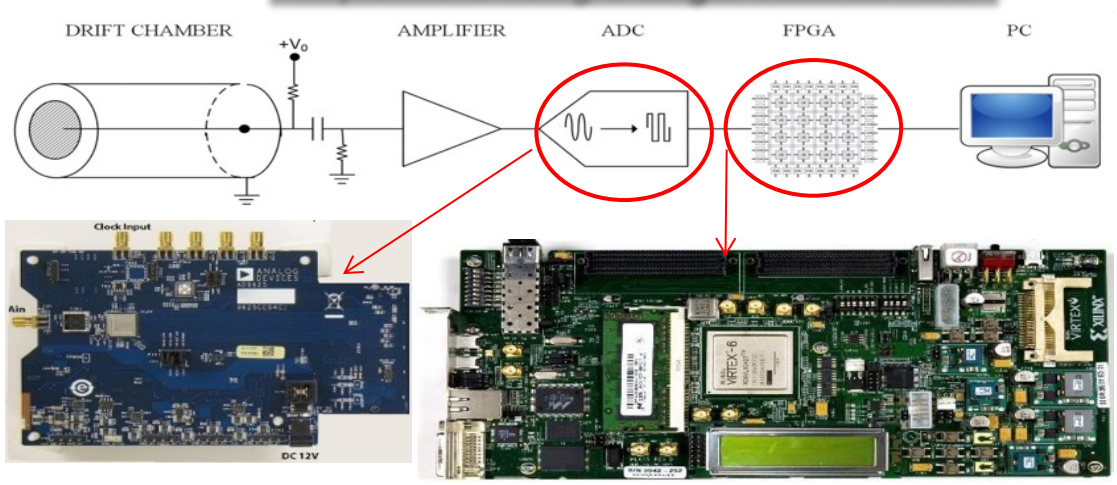
- A fast read-out CTT algorithm has been developed as **VHDL/Verilog** code implemented on a **Virtex 6 FPGA (maximum input/output clock switching frequency of 710 MHz)**. The hardware setup includes also a **12-bit monolithic pipeline sampling ADC** at conversion rates up to **2.0 GSPS.**

Goal

Implement on FPGA more sophisticated peak finding algorithms for the **parallel pre-processing** of **many ADC channels**:

- **reduce costs** and **system complexity**
- **gain on flexibility in determining proximity correlations** among hit cells for track segment finding and triggering purposes.

Implemtend using a **single channel ADC**

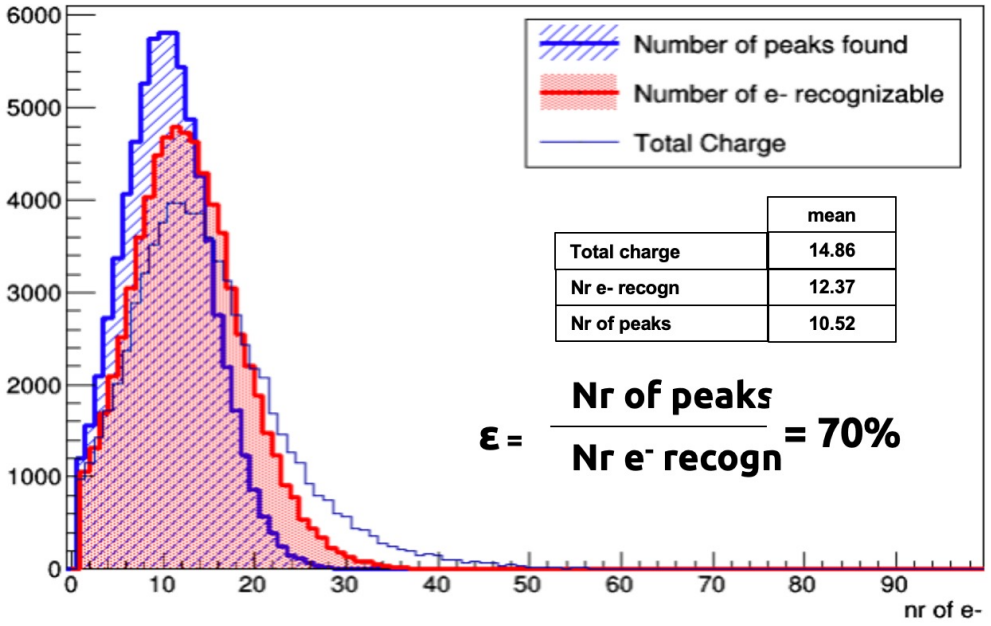


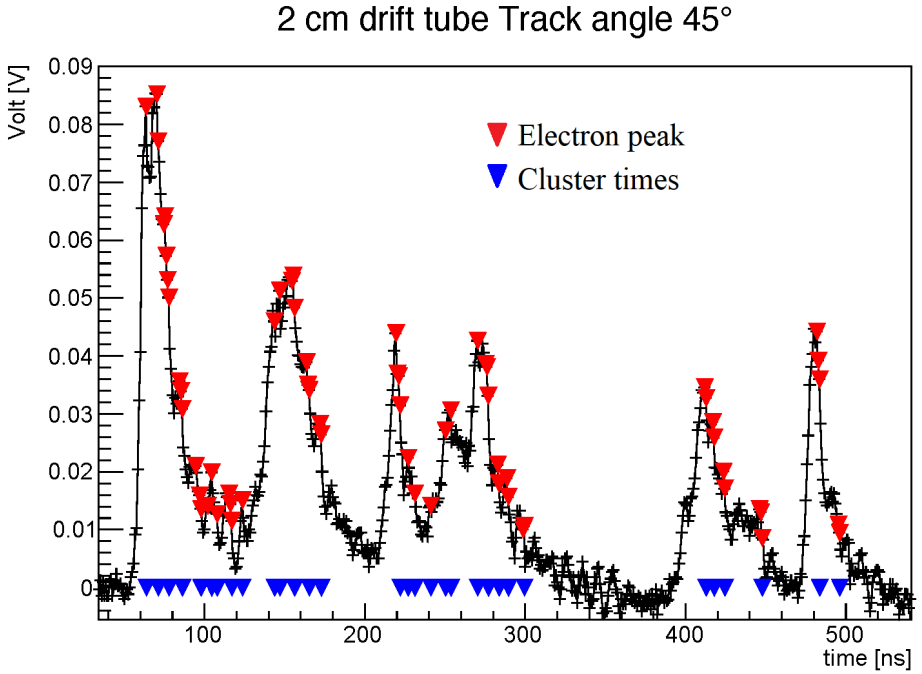
Derivate algorithm

- A first simple tested algorithm of peak finder is based on the first and second derivative of the digitized signal function f, is defined for each time bin i, Δb being the number of bins over which the average value of f is calculated:

$$f'(i) = \frac{f(i) - \bar{f}(i - \Delta b)}{\Delta b} \qquad f''(i) = f'(i) - f'(i-1)$$

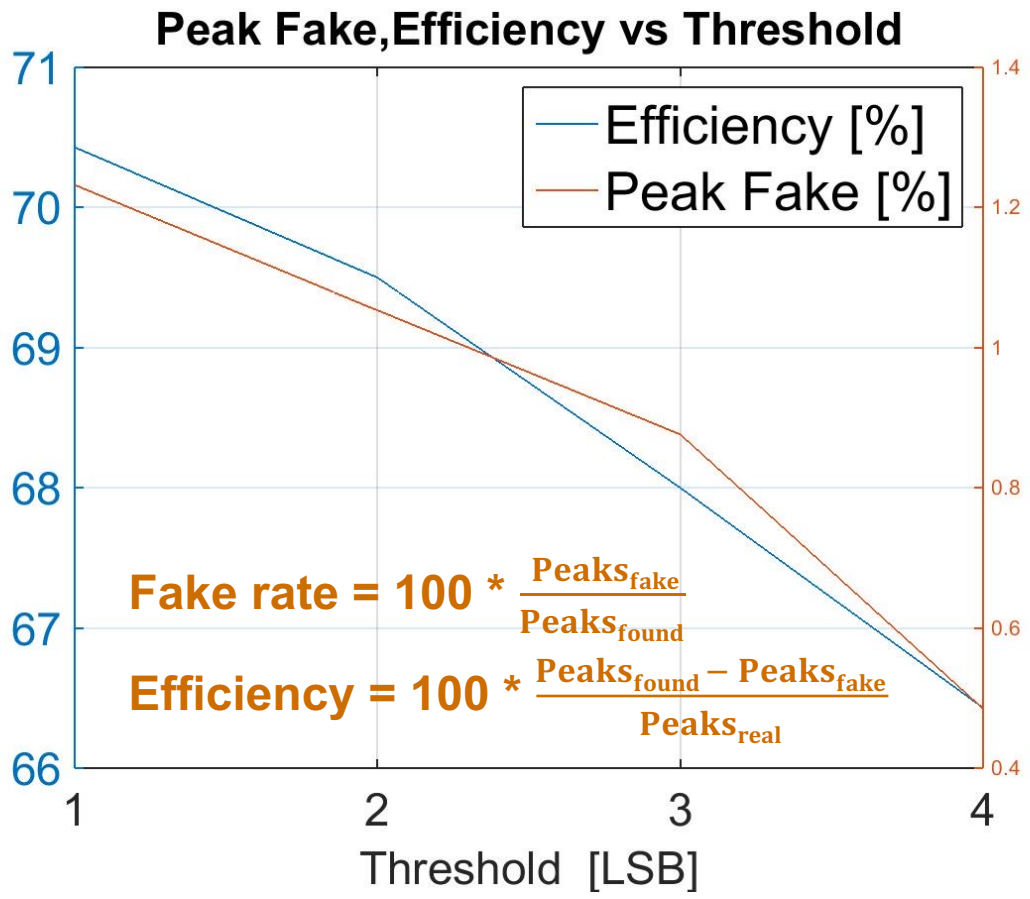
- A peak is found when Δf, f' and f'' are above a pre-defined threshold level.





Derivate algorithm

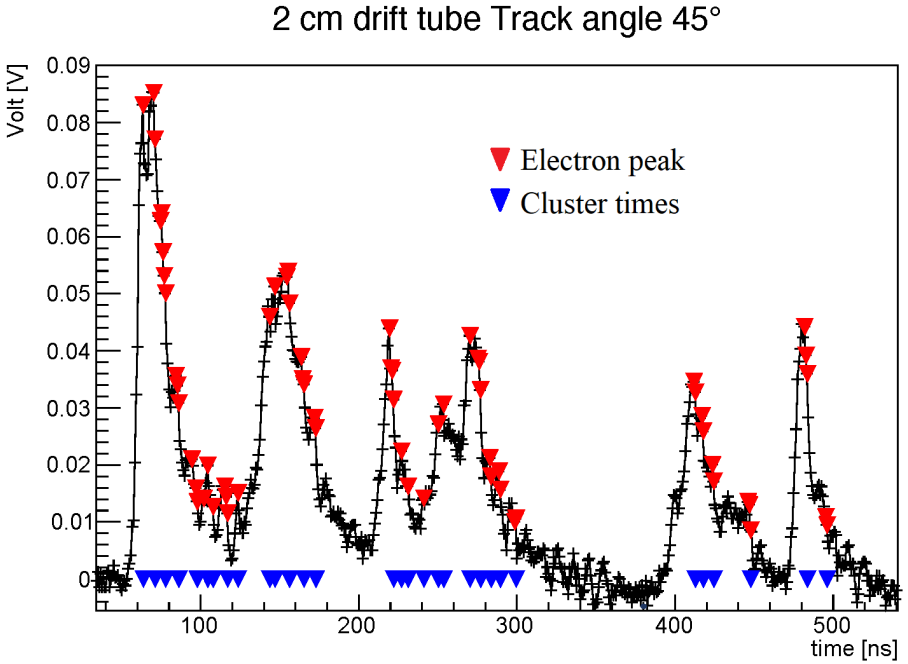
The CCT algorithm (DERIV) performances on FPGA



- Efficiency can be improved by using a **higher resolution ADC**
  - ▶ To recognize **smaller peaks.**
  - ▶ To increase the signal to noise ratio by filtering and amplifying the analog input signal.
- Using an **FPGA** with **better** performances (**timing and power**) allows us to reduce the **processing time** and to manage **multichannel ADCs**.

RTA algorithm

- A further algorithm that is being implemented on FPGAs is the Running Template Algorithm (RTA). It is based on a bin-by-bin difference of the waveform with a normalized search template.

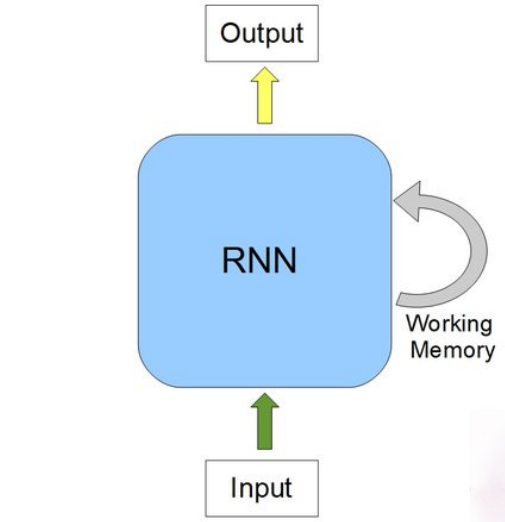


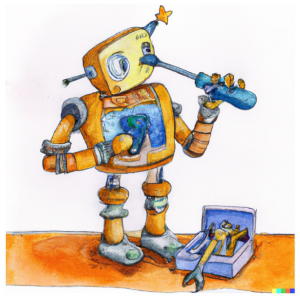
The RTA algorithm is based on the definition of a digitised electron peak model, composed by a raising and a falling exponential over a fixed number of bins, adapted to experimental data and sampling rate. If inside the waveform there is a peak that corresponds, to the properly scaled electron peak template, the algorithm will save its amplitude and subtract it from the waveform. The procedure is repeated until no further peaks are found

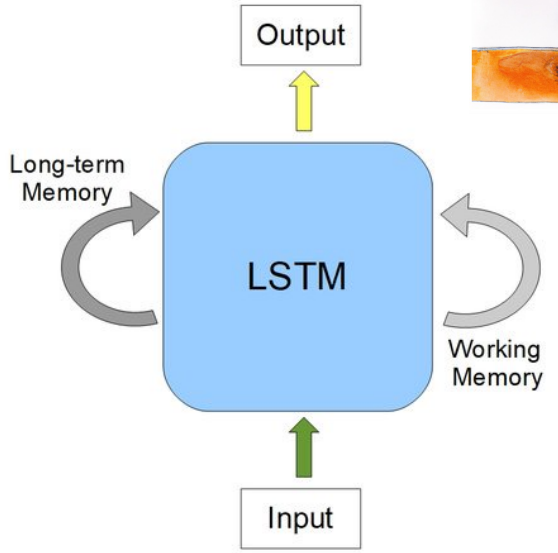
- The derivate algorithm has been implemented and tested on FPGAs, while the RTA algorithm is in the testing phase with PC simulations and testbench. From these tests, it results that there is a peak detection efficiency of 72%, with 1.2% fake peak rate, for the derivative algorithm, while 70% for the RTA algorithm, with 1% of fake peak rate

Future algorithm: Improving Performance

- In the cluster counting working group it was noted that Deep Learning algorithms with RNN are very promising
- We are trying to understand if it is possible to use similar algorithms directly on FPGA in a real time in order to speed up the acquisition process particularly with noisy signals
- This process is still in a very early stage but from other works using DL on FPGA it is worth to try.
- Checking that the hardware we use is sufficient to run the DL algorithms







Actual e future strategy

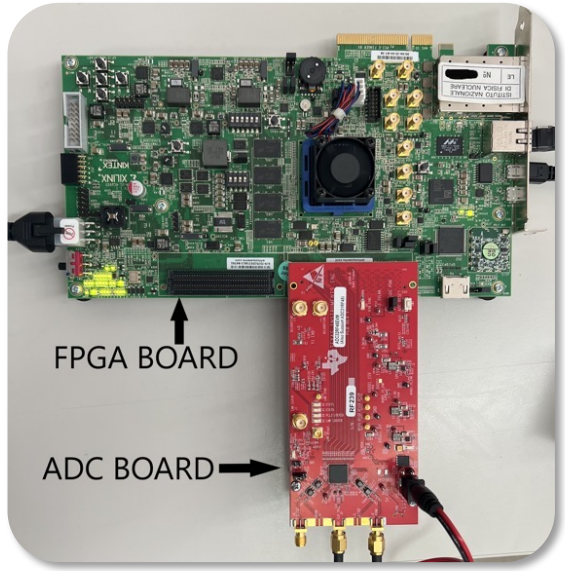
- We implemented successfully the CTT technique on **a single-channel ADC**
- To implement a **multi-channel DCH signals** reading, different digitizers are under test:
  1) ADC TEXAS INSTRUMENT **ADC32RF45**
  2) CAEN **digitizer**
  3) NALU SCIENTIFIC **ASoCv3**

- Understand how to best implement the data transfer to the DAQ, using **optical fiber with SFP + connectors** or **SFP + to RJ45 adapters** to use the new **10Gbit/s standard** (particularly for (1) and (2)).

- Investigate the best way **to save information before the transfer** (in case of possible bottlenecks during the transfer procedure).

ADC TEXAS INSTRUMENT ADC32RF45

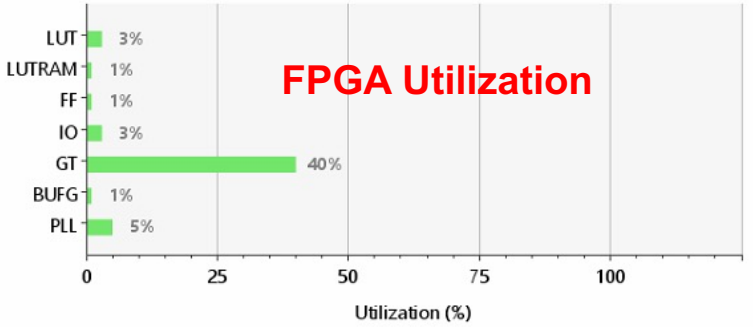
- The new hardware to test the algorithm is:
  - Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit
  - ADC dual channel ADC32RF45EVM



- The choice of the FPGA and ADC was made by choosing the ADC that ensured good resolution and transfer capacity.

- The new FPGA allows to have better time constraints.

- The ADC has a higher resolution than the previous one and also it allows the reading of two channels simultaneously.



CAEN digitizers

- Test with the **new high performance CAEN digitizers**:
  - start testing **CAEN low performance digitizer VX2740** (waiting for themore performing **board VX2751**)
  - Use the **CAEN "OPEN FPGA" system**

- Using the CAEN HW we do not have access to the **whole firmware infrastructure** but only in the **green areas** in the figure, where we will implement the cluster counting algorithm.

VX2740: the first of a kind

64 channel, 125 MS/s, 16 - bit waveform digitizer

- High channel density spectroscopy
- Good fit for Neutrino and Dark Matter experiment
- **Open FPGA**: SCI-Compiler tool for beginners (**COMING SOON**) or advanced firmware template
- Four 40-pin, 2 mm header connectors with DIFF or SE inputs
- **1 GbE, 10 GbE, USB 3.0** and CONET 2.0 (optional) connectivity
- Common Trigger (waveforms) or Individual Self-trigger modes
- **DPP options**: PHA, QDC, PSD, CFD
- Advanced Waveform Readout modes: ZLE, DAW
- DT2740, 64 channels in Desktop form factor (**COMING SOON**)

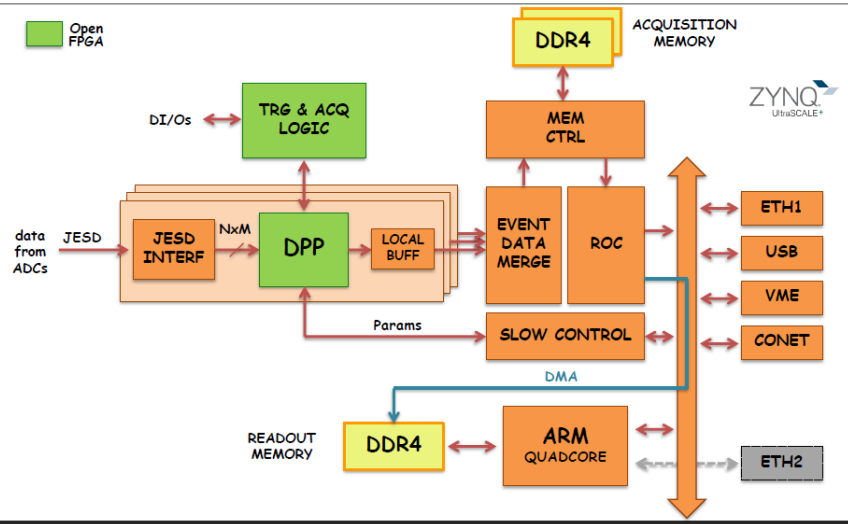
Model	# channels	MS/s	# bit	Applications
x2740	64	125	16	64 MCAs for high channel density spectroscopy Good fit for Neutrino and Dark Matter exp.
x2745 Advanced version of x2740	64	125	16	Variable gain input stage Designed for Si detectors readout
x2725/x2730	32	250/500	14	Medium-fast detectors Sub-ns timing combined with high energy resolution Optimal trade off between cost and performances
x2751	16	1000	14	Ultra-fast detectors (diamond, MPCs, SiPMs) with ps timing applications Potential upgrade to higher sampling rate
x2724	32	125	16	Spectroscopy & MCA Advanced Front-End (gain, shaping, AC/DC coupling ...) Semiconductor detector (HPGe, Clover, SDD ,...) Typically connected to charge Sensitive Preamplifier

Currently available

COMING SOON

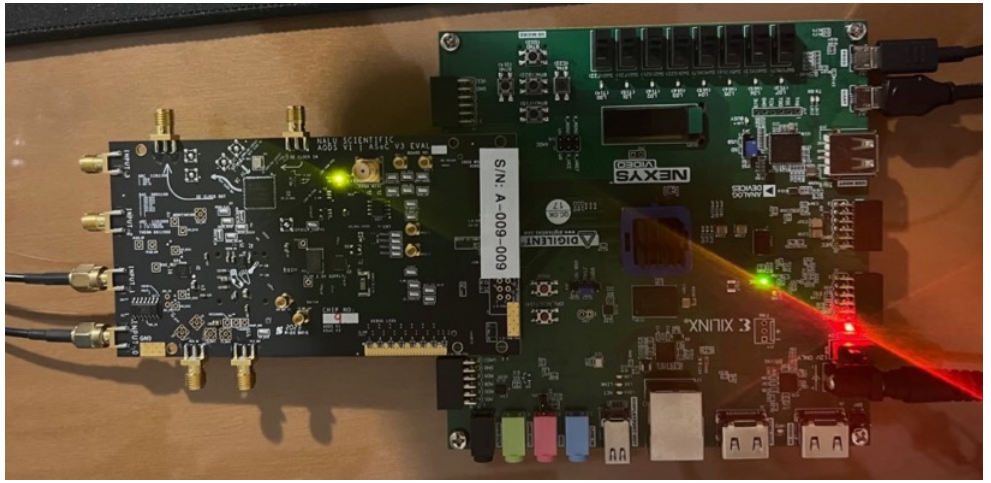
Birdseye view – what's coming

Digitizers 2.0 - FPGA Block Diagram



Naluscienfic ASoCV3

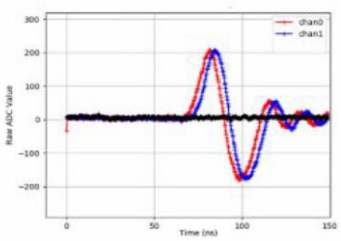
- Naluscientific has provided us with an evaluation card with the **ASoCV3 chip**:
  - **4 channel**
  - **Analog Bandwidth 850 MHz**



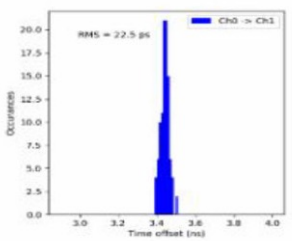
Some **performances of the tests** made by Naluscientific on the **old-version chip V2**

*V3 under test

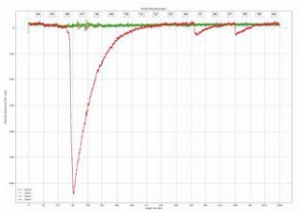
Live demo at IEEE NSS-MIC 2019



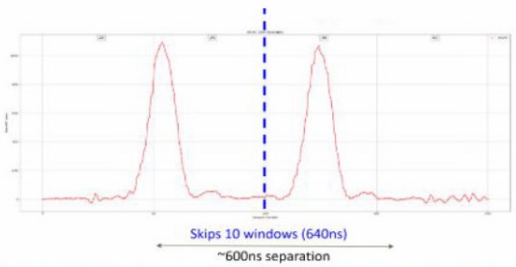
Timing resolution: 22ps

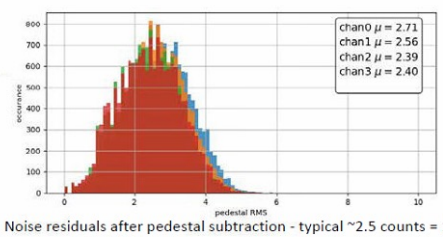


SiPM waveform readout



ROI Readout





Noise residuals after pedestal subtraction - typical ~2.5 counts = 1.0mV

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NALU SCIENTIFIC ENABLING INNOVATION

ASoC V3 DESIGN DETAILS

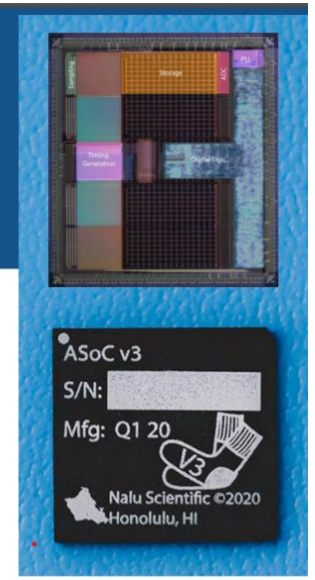
Compact, high performance waveform digitizer

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

Parameter	Spec
Sample rate	2.4-3.6GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps (see below for details)
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- Self triggering
- Completed DOE Phase II SBIR
  - Eval cards avail
  - Custom boards under dev

IEEE NSS 2021



Conclusion

- We have described a generic acquisition chain for DC with the CTT
- Possible amplifiers that can be used on a DC
- CTT, possible and future algorithms described
- Future strategies for real-time implementation of CTT algorithms

Data reduction and pre-processing of DCH signals

- The Cluster Timing Technique (CTT), which consists in measuring the arrival times on the sense wires of each individual ionization electron, overcomes a substantial bias in the impact parameter estimate and offers the possibility of greatly improving the particle identification.
- This technique uses statistical tools to reduce the biased estimate, by exploiting the information of all clusters detected with a peak finding algorithm. Measuring both the amplitude and the arrival time of each peak in the signal associated to each ionisation electron is the minimum requirement on the data transfer for storage to prevent any data loss.
- The developed general CTT algorithm is able to process the data in real-time and in particular it:
  - identifies, in the digitized signal, the peaks corresponding to the different ionization clusters;
  - stores each peak amplitude and timing in an internal memory;
  - sends the data stored to an external device when a specific trigger signals occur.