INVOLVEMENT OF HONG KONG ALTAS TEAM ON STGC TEST AND COMMISSIONING

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Hong Kong ATLAS Cluster
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NEW SMALL WHEELS UPGRADE

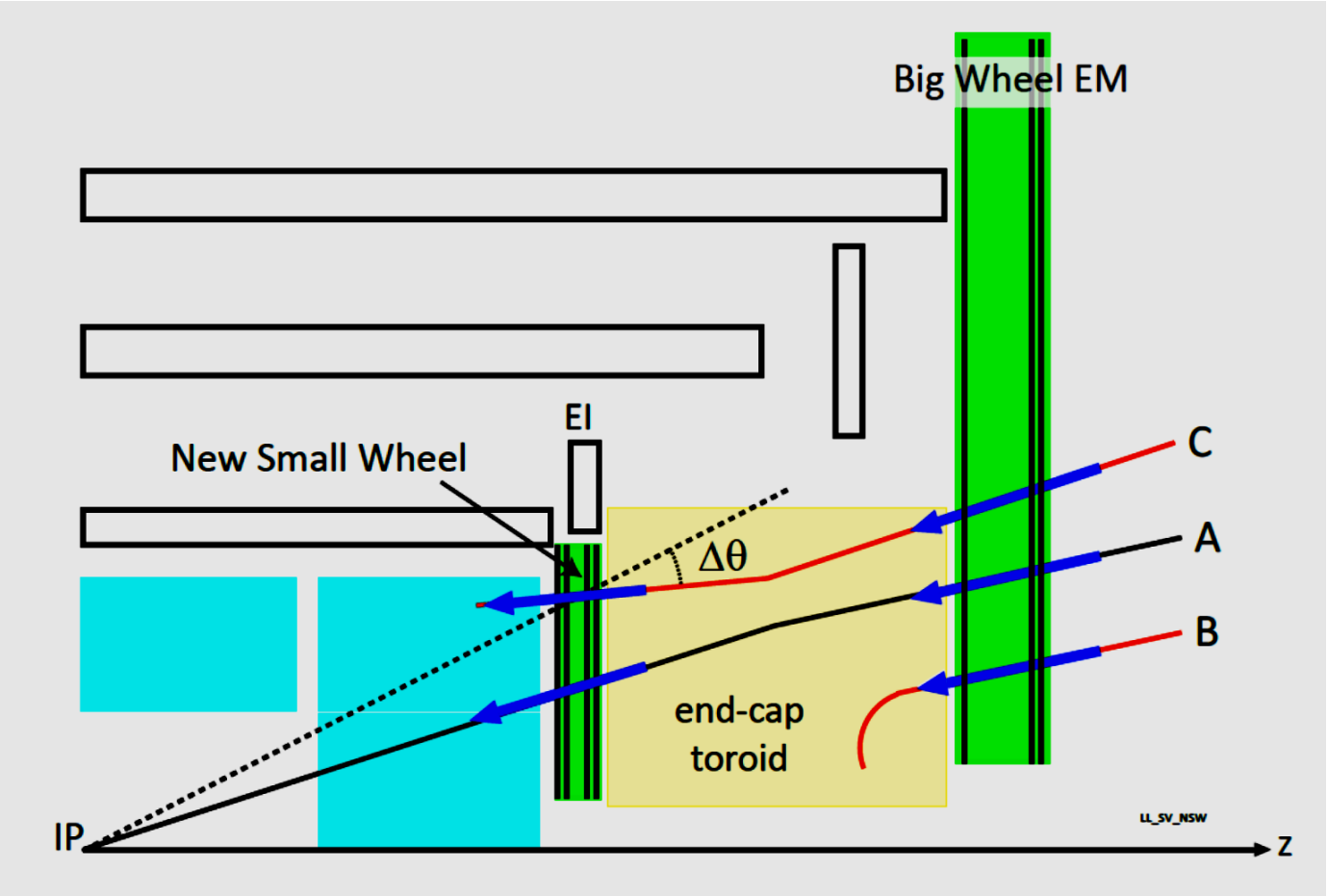
Upgrade of the muon spectrometer:
New Small Wheels (NSW)

Mission of Phase I Upgrade:

- Online trigger < 25ns
- High background radiation ~ 10kHz/cm2
- Position resolution ~ 100um

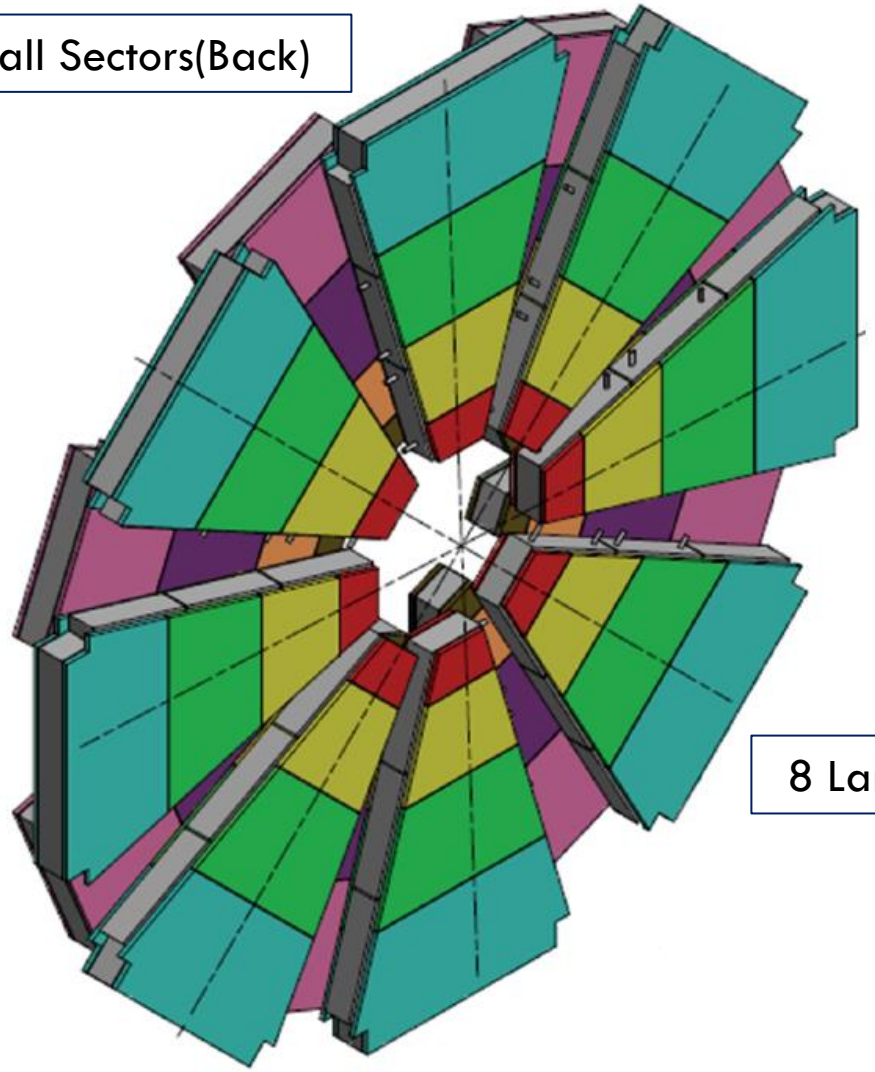
2012 : ~90% of the Muon L1 Triggers are fake i.e., not coming from the interaction point.

NSW enhances high momentum muon selection efficiency by adding extra precision measurement in high-rate environment.

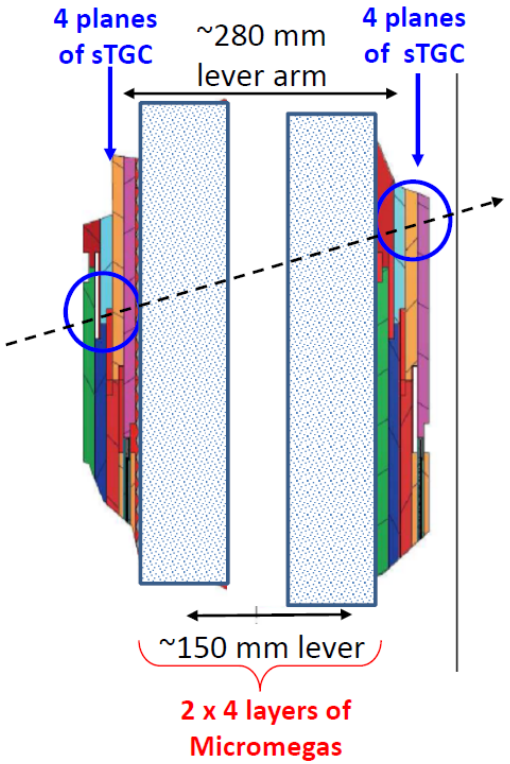


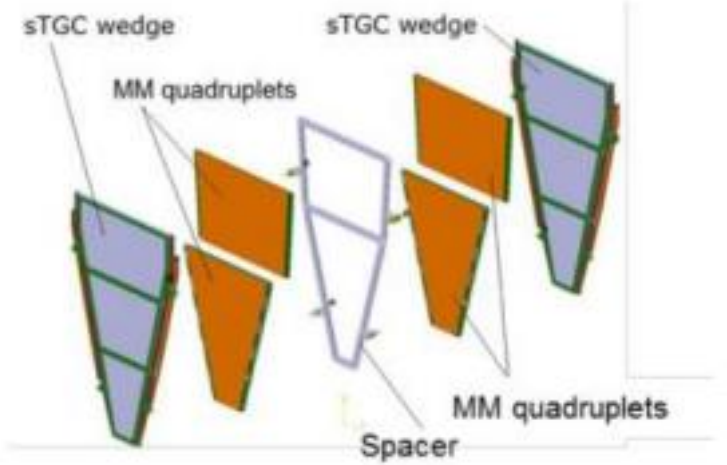
NSW WHEEL

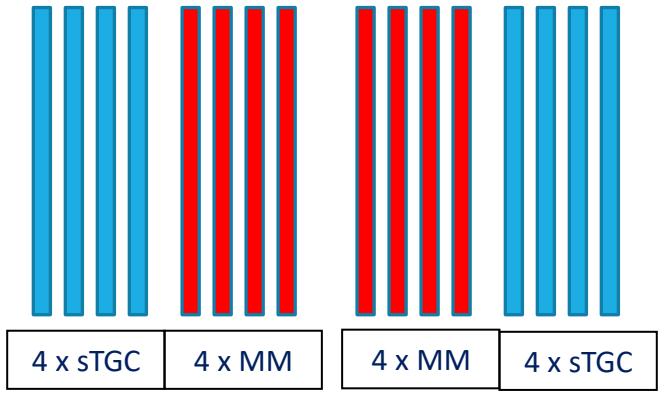
8 Small Sectors(Back)



8 Large Sectors(Front)

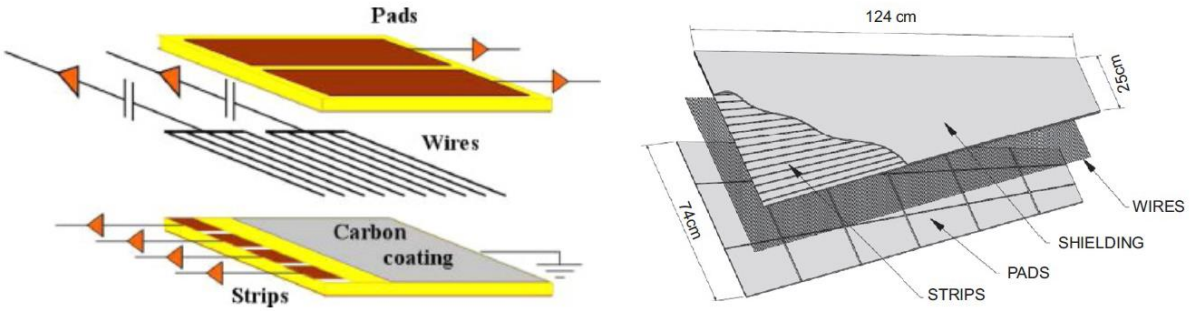






Cross Section of a sector

STGC AND MICROMEGAS



(a) a (b) b

Figure 4.1: The sTGC internal structure.

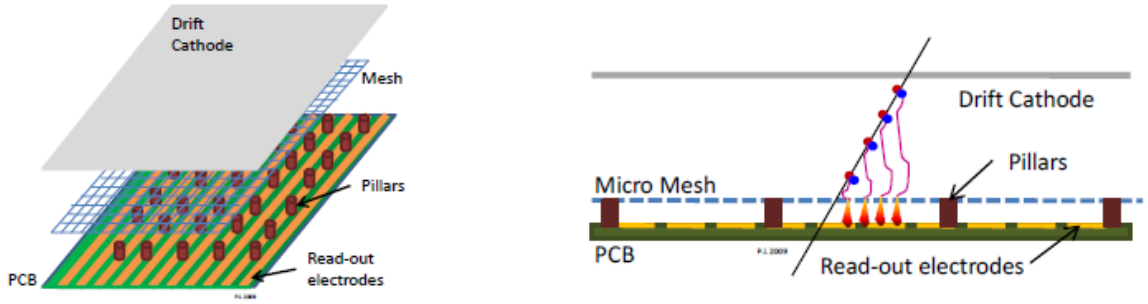


Figure 5.1: Sketch of the layout and operating principle of a MM detector.

Small-strip Thin Gap Chambers

Each Wheel includes 16 Sectors

(3 Segments x 8 Layers per Sector)

Each Chamber consists of three parts:

1) Pad (φ, L0 trigger)

2) Strip(R, L1 trigger)

3) Wire (offline track reconstruction)

~400k readout channels

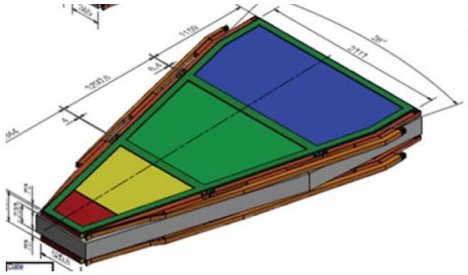
Micromegas: "micro mesh gaseous structure"

Electrons drift towards micro mesh

The electron avalanche takes place in the thin amplification region. Read-out electrodes read out the signals to the front-end.

STGC WEDGE ASSEMBLY

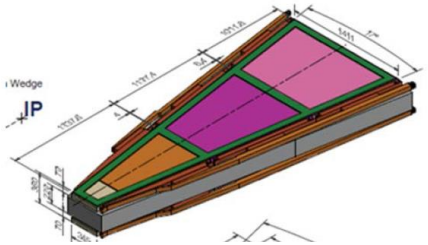
QL3 QL2 QL1



Large sectors:

- QL1: Israel (WIS, Tel Aviv)
- QL2: Canada (TRIUMF, Carleton, Montreal)
- QL3: Russia (PNPI St. Petersburg)

QS3 QS2 QS1

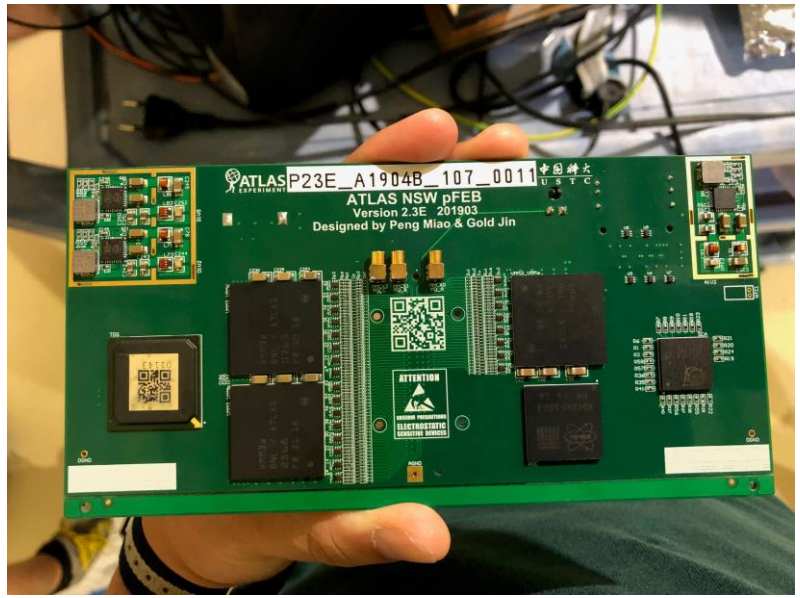


Small sectors (for each NSW, needed first for installation)

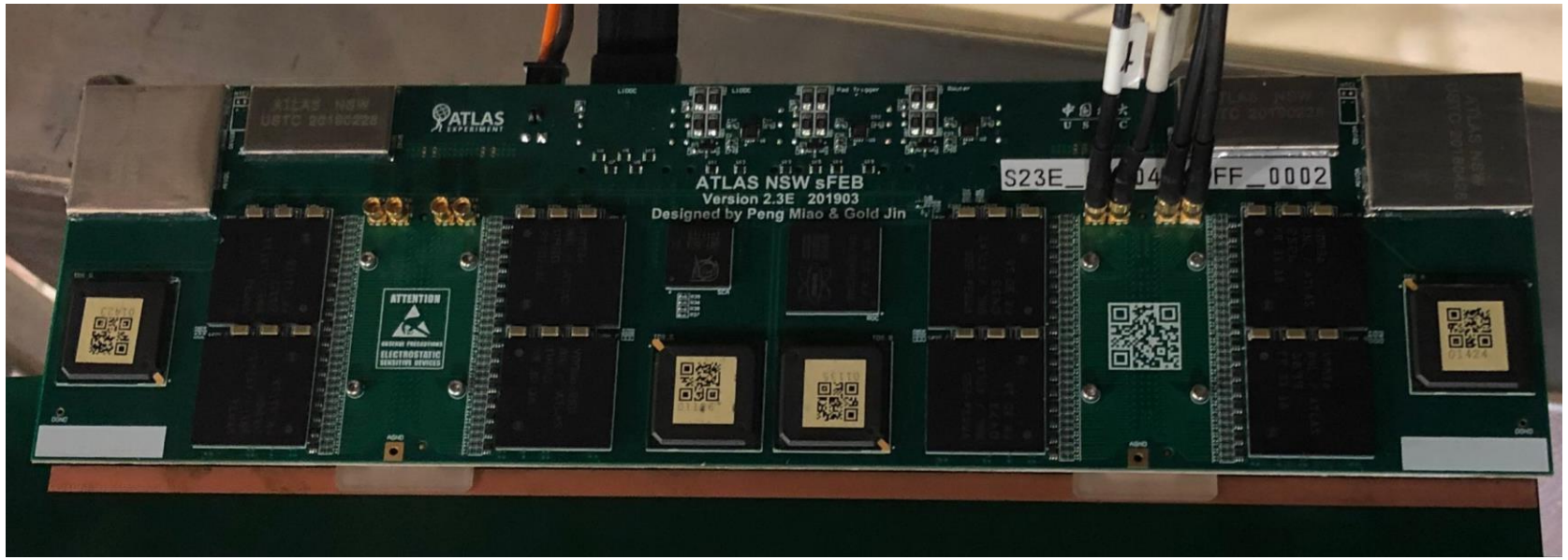
- QS1: Chile (UTFSM Valparaiso + PUC Santiago)
- QS2: China (Shandong)
- QS3: Canada (TRIUMF, Carleton, Montreal) + Israel (WIS, Tel Aviv)

FEB ON STGC WEDGES

PAD/STRIP FRONT END BOARD (V2.3E)



pFEB



sFEB

On Front End Board there are different ASICS:

VMM – ASD(Amplifier-Shaper-Discriminator) ASIC handling max. 64 channels per chip

TDS(Trigger Data Serializer) – Serialize data from VMM to backend (Router -> FELIX/SWROD)

ROC (Readout Controller) – Receive LHC clock and trigger and distribute to VMM and TDS

SCA – ASIC configuration with embedded ADC (Analog to Digital Converter)

sTGC Integration Flow-Chart

Preparatory Task

- FEB Reception Test
- Assemble L1DDC Array
- Install LVDB and LV Cables
- Cooling pipe manufacturing
- Mounting FEB Cooling plate
- Twinax Cable Bundling

Extra Step

- Analog- connectivity measurement with the final boards

Electronics Mechanical Integration

- L1DDC, FEB Installation
- Twinax Cable Installation
- Cooling Pipe Mounting

Validation of Electronics Power, Temperature and Board mapping validation

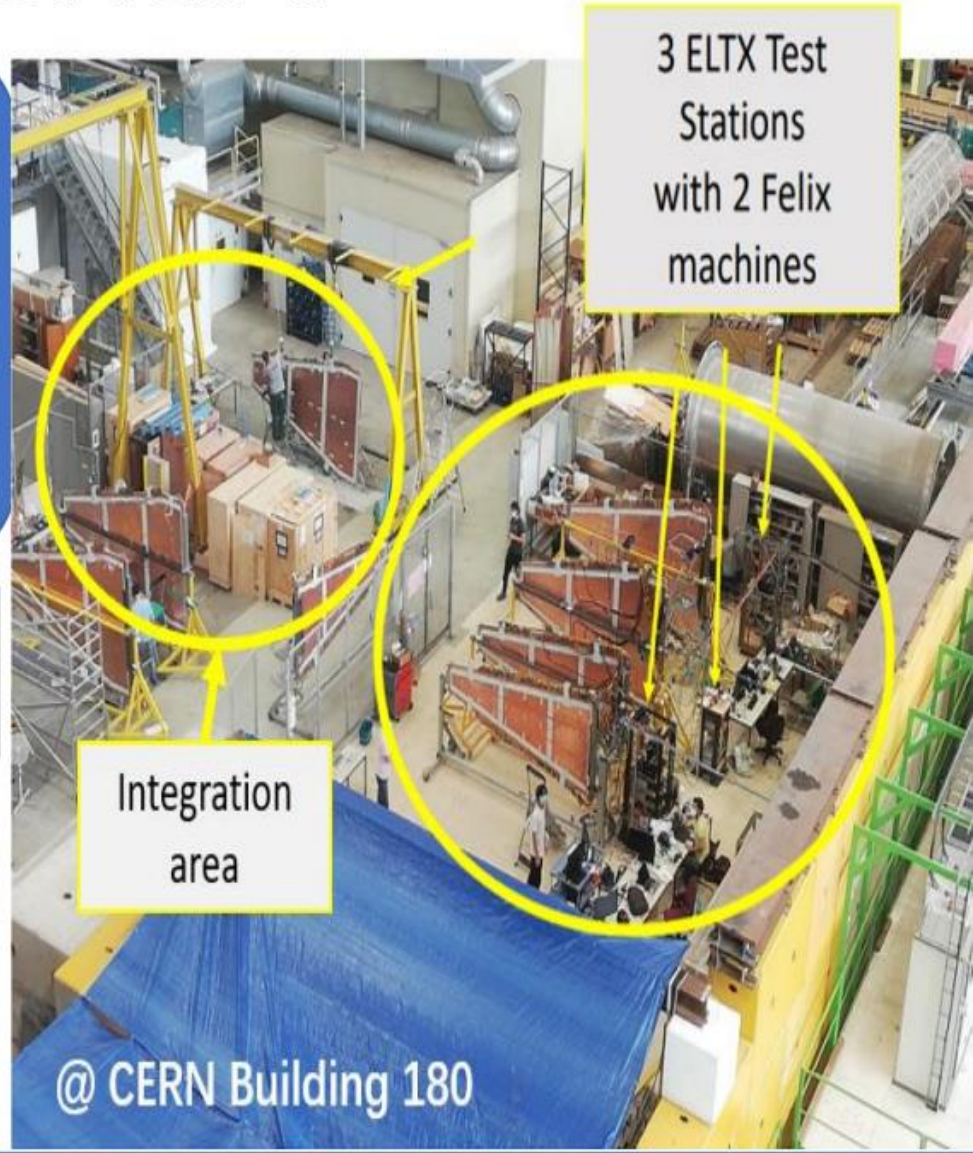
Electronics Testing And Validation

- Trigger Interface Connectivity
- Test Pulse Readout
- VMM Calibration for trimming and noise scan with SCA-ADC

Organizing the test results. Adding the mapping, results, etc to the database.

Final services mounting, envelope conformity check and sign off

From Prachi Atmasiddha



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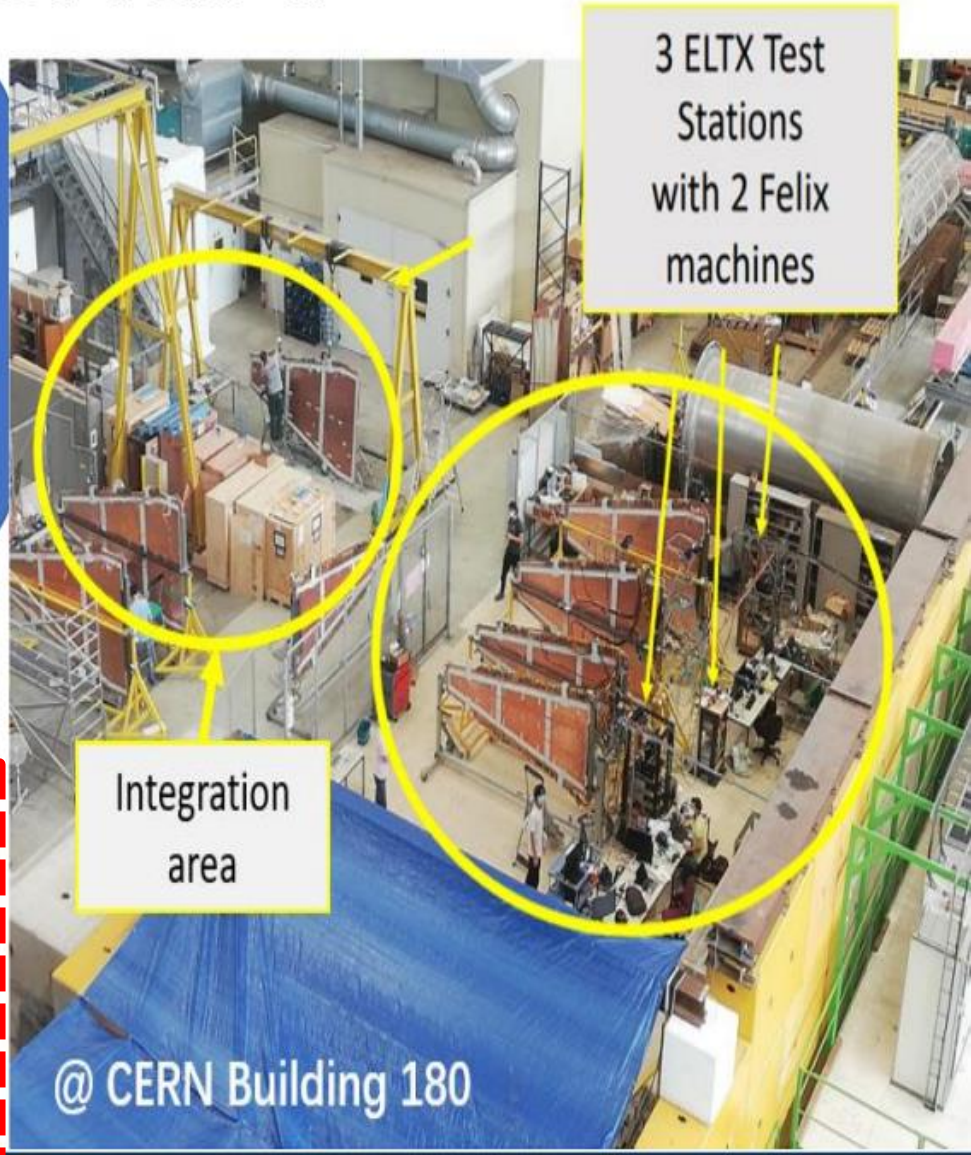


WEDGE NOISE MEASUREMENT

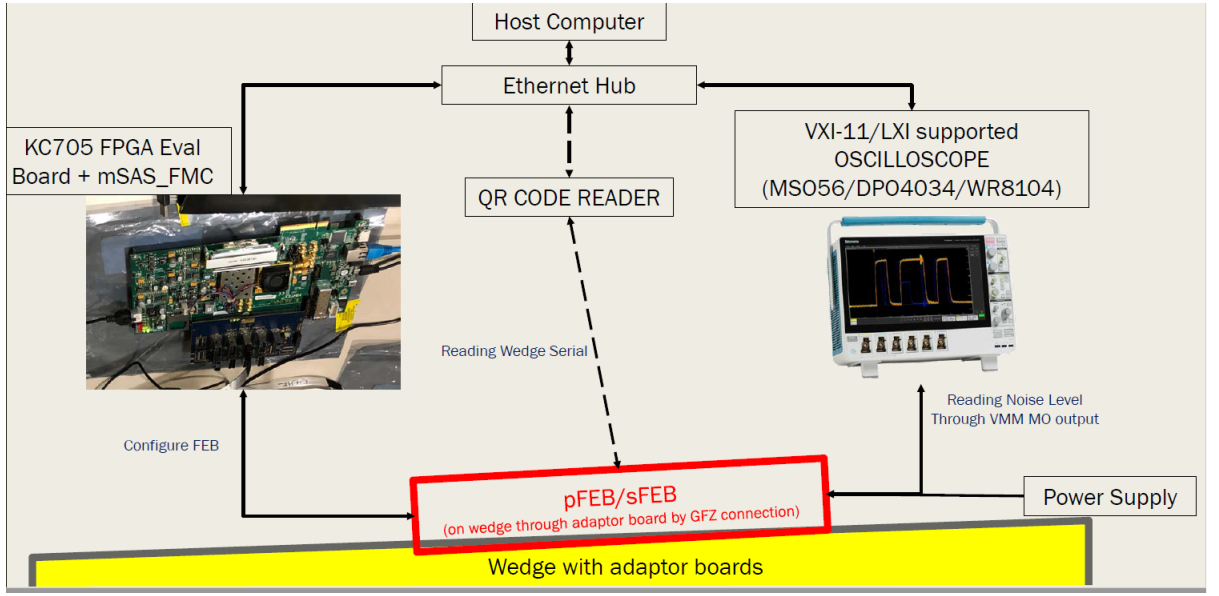
Objective:

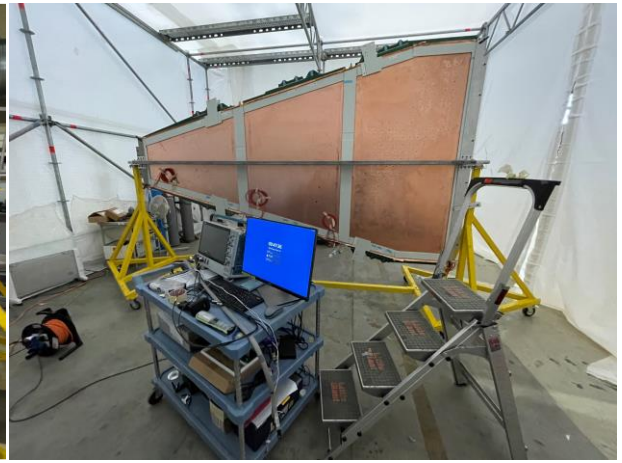
1) To verify the **connectivity of pad and strip** for wedges

2) To provide a **relative comparison between wedges**

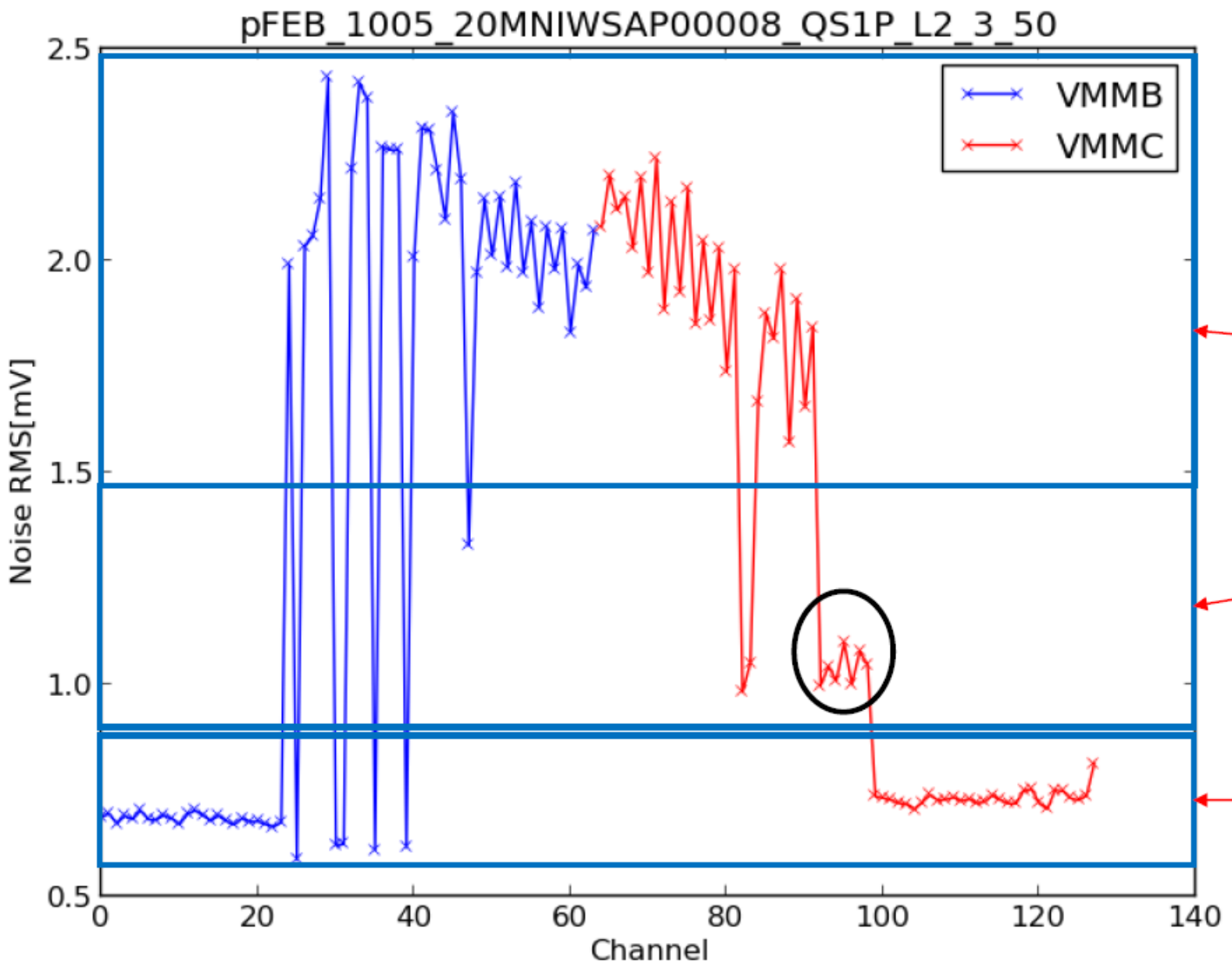
3) To record the **noise history** on wedges for further references

4) Feedback to Wedge Assemble Team to **check and fix the problematic channels**





WEDGE NOISE MEASUREMENT RESULTS FOR REVIEW (1)

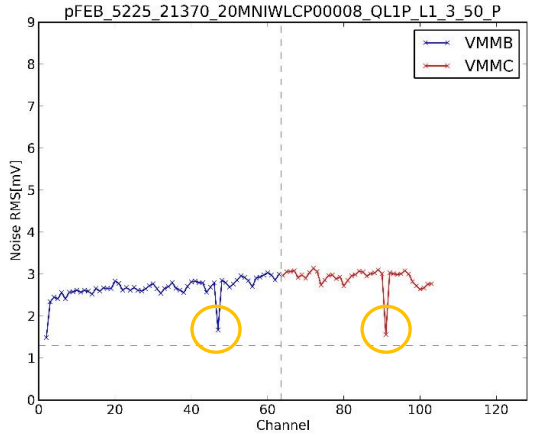


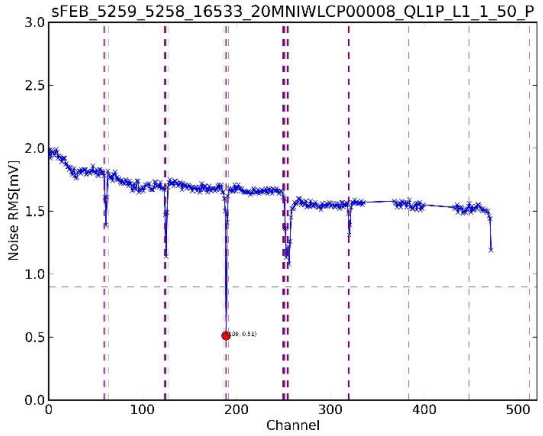
Nominal noise level: VMM connected to pad or strip

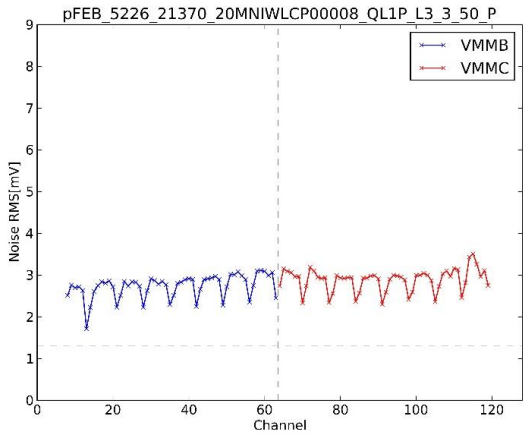
Noise level steps in-between : VMM connected to pad or strip e.g. total 75 traces in QS1P2 adaptor board with only 68 channels connected -> 7 channels

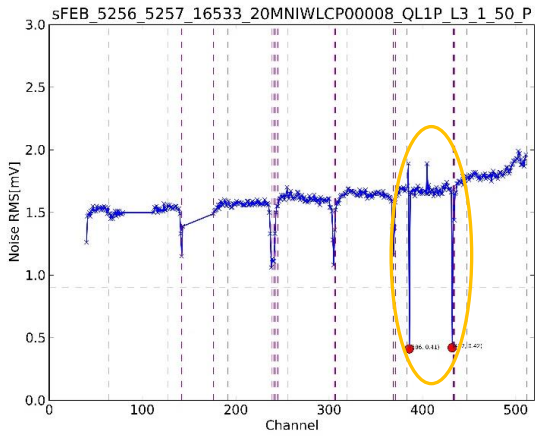
Minimum noise level: VMM channel not connected to anything

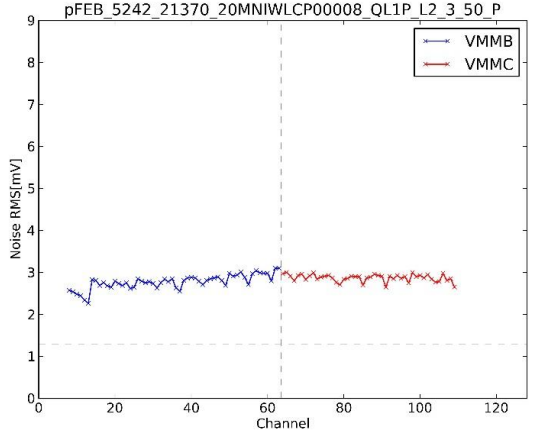
WEDGE NOISE MEASUREMENT RESULTS FOR REVIEW (2)

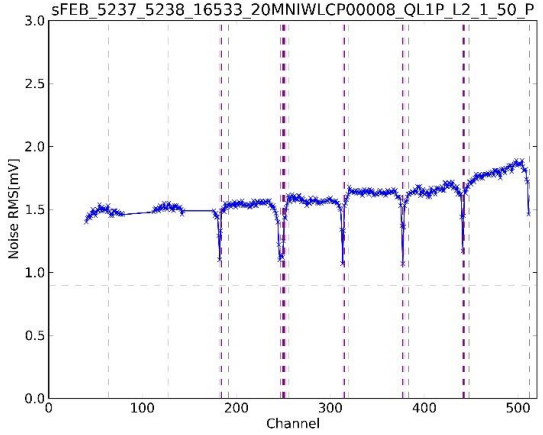


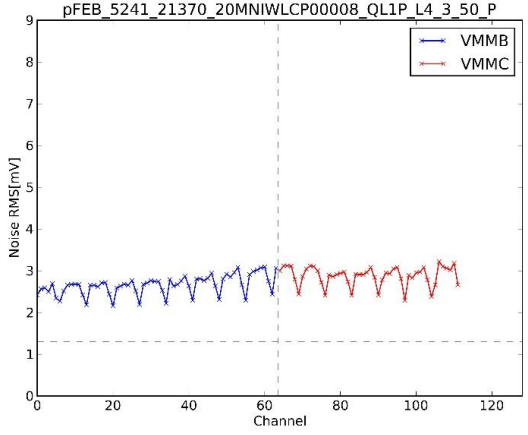


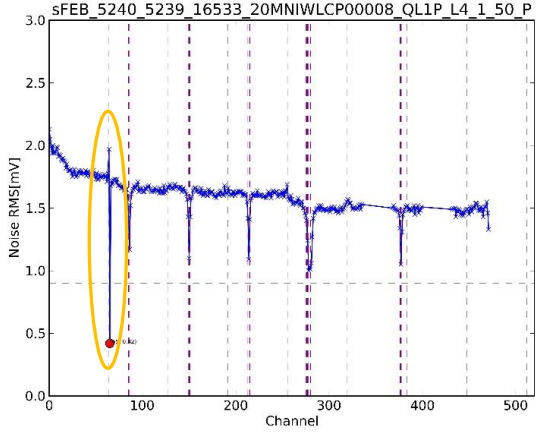












- Summery is generated per wedge (3 quadruplets)
- Channels having problem (Circled) would be returned to fix

READOUT COMMISSIONING TESTS

Baseline Scans

- Validates FEB mounting and connection between adaptor board and physical channels.

Trimmer Scans

- Equalizes difference between threshold and baseline for every VMM channel

Pulser Tests

- Configure internal test-pulse to validate readout chain. Mainly for testing VMM

Noise Scans

- Scan the noise readout on electronics together with sTGC

Phase-2 Tests

- Used for HL-LHC, opens a second set of sROC's for faster VMM data readout

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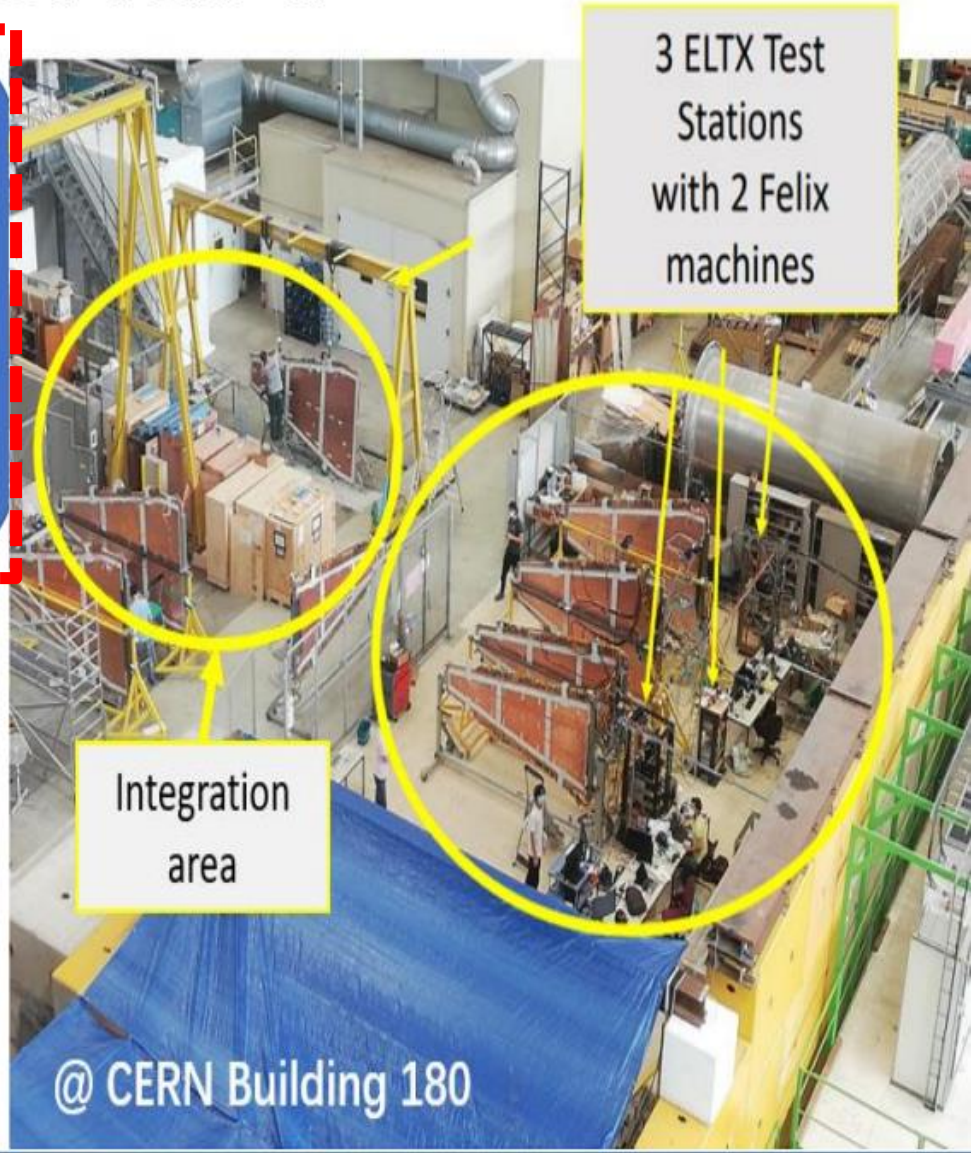


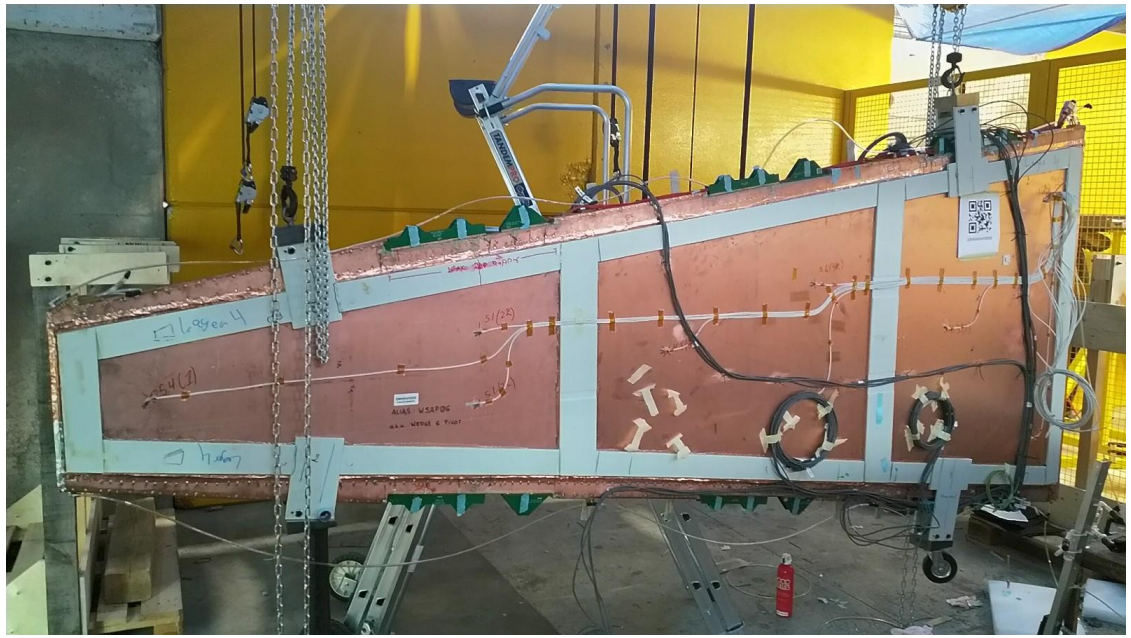
STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (1)

Work flow at Building 180:

1) Chambers roll out from the clean room of B.180 after gluing
2) Gas leakage test
3) Putting the chamber on rotating stand
4) Installation of electronics (FEBs, L1DDC, etc)
5) Installation of cooling system
6) Installation of cables
7) Installation of gas pipes
8) System testing (electronics, cooling and gas systems)
9) Completely equipped chamber is transported to B.191 for putting onto the NSW

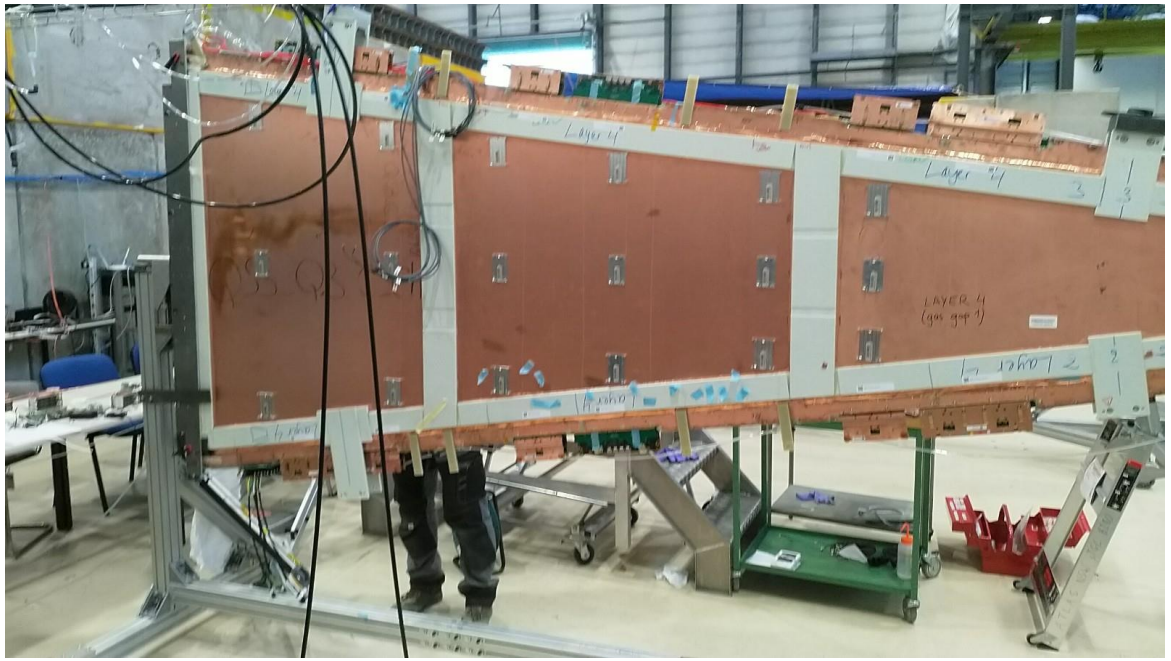
STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (2)

1) Chambers freshly finished out of the clear room



2) A chamber undergoing gas leakage test

STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (3)

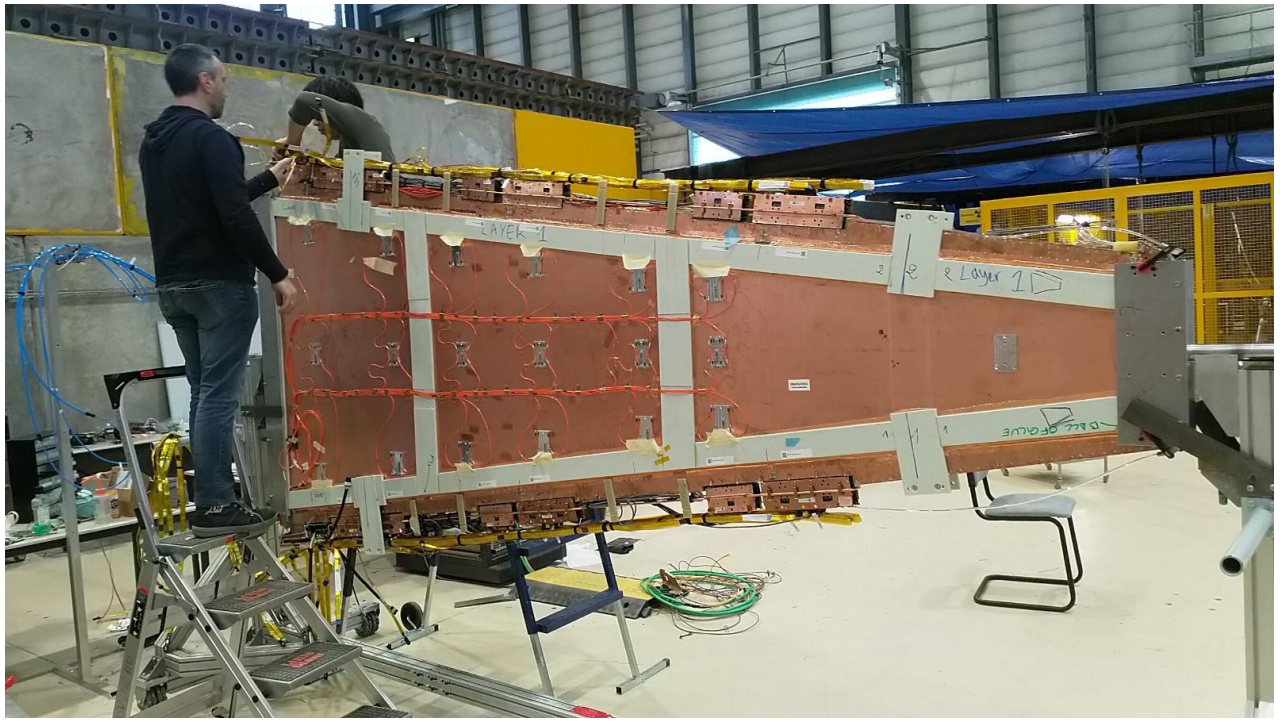


3) A chamber being moved from “temporary standing wheels” to a “rotating stand” using a gantry crane. The chamber can now be flipped safely for installations.

STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (4)

4) &5) All electronics are installed. The technician is installing the cooling system.

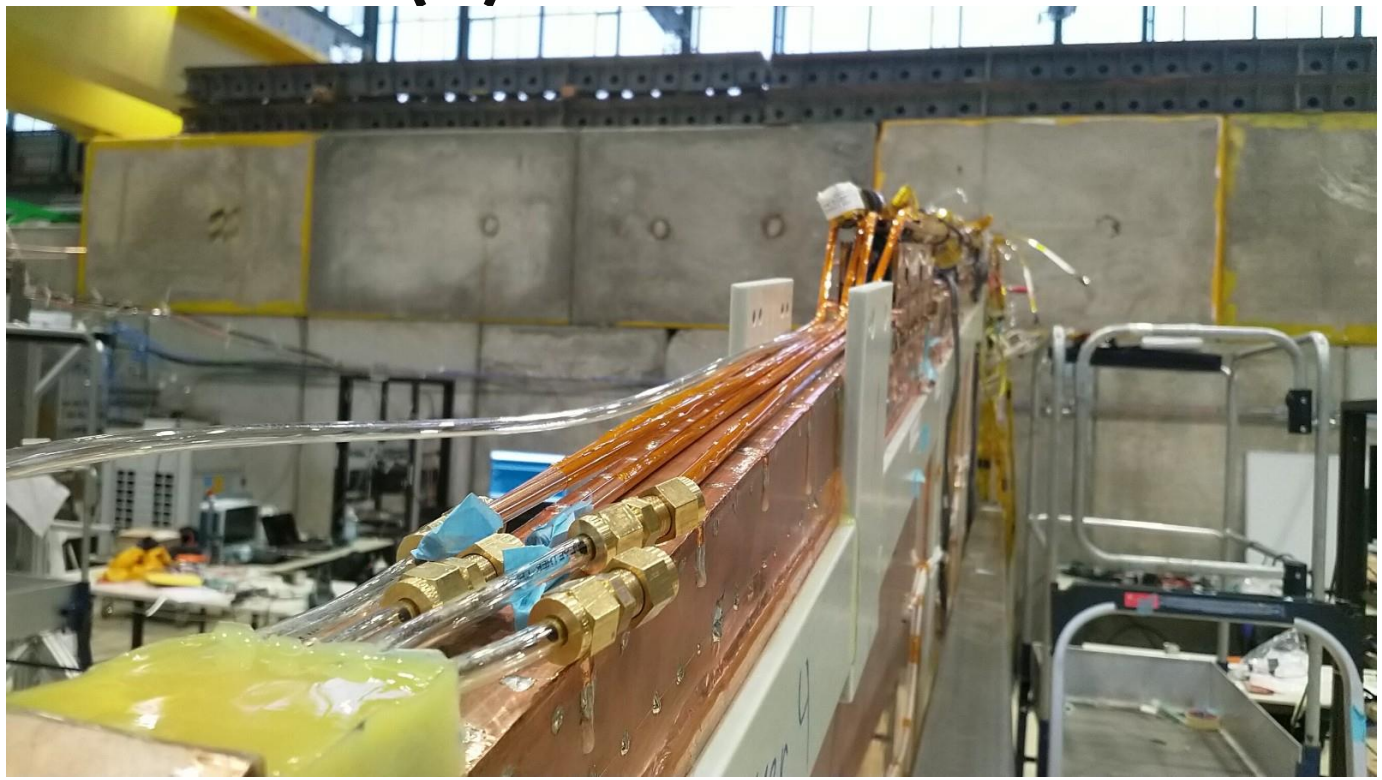
STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (5)



6) Installation of cables. The process can take a few hours due the very limited space designated for the cables.

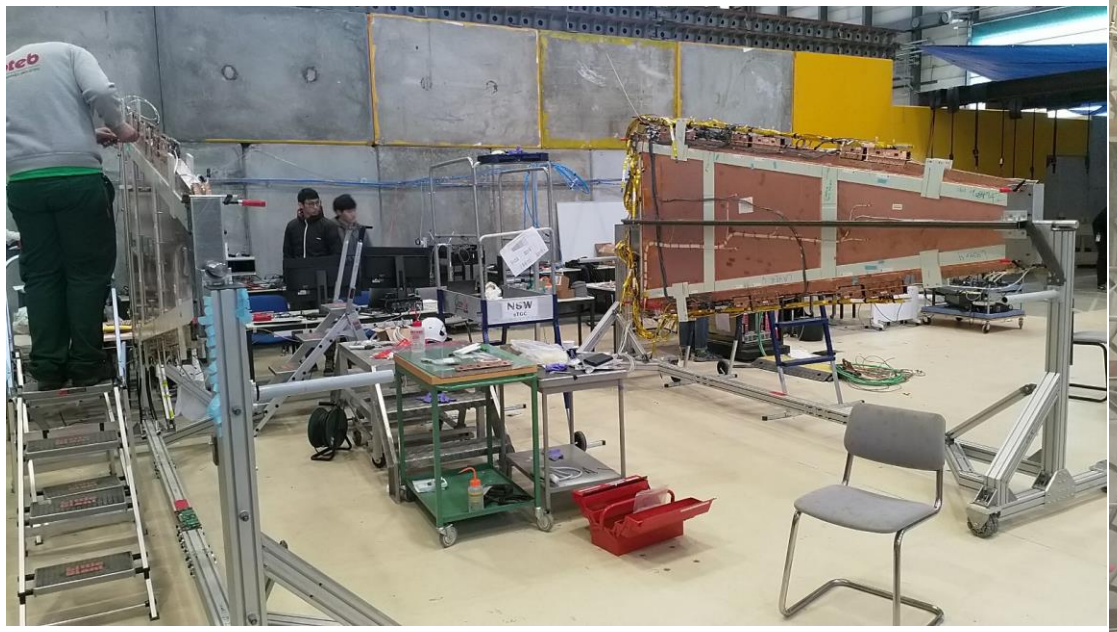
Showing the density of cables. The cable has to be bundled and folded carefully or they will not fit for the space allowed. Mishandling can break connectors on the FEBs. Colour labels help to ensure correct connections.

STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (6)



6) Installation of gas pipes. The gas pipe circuits are completely in the middle of cable installation process as some part of the pipes have to be buried into the cable bundles.

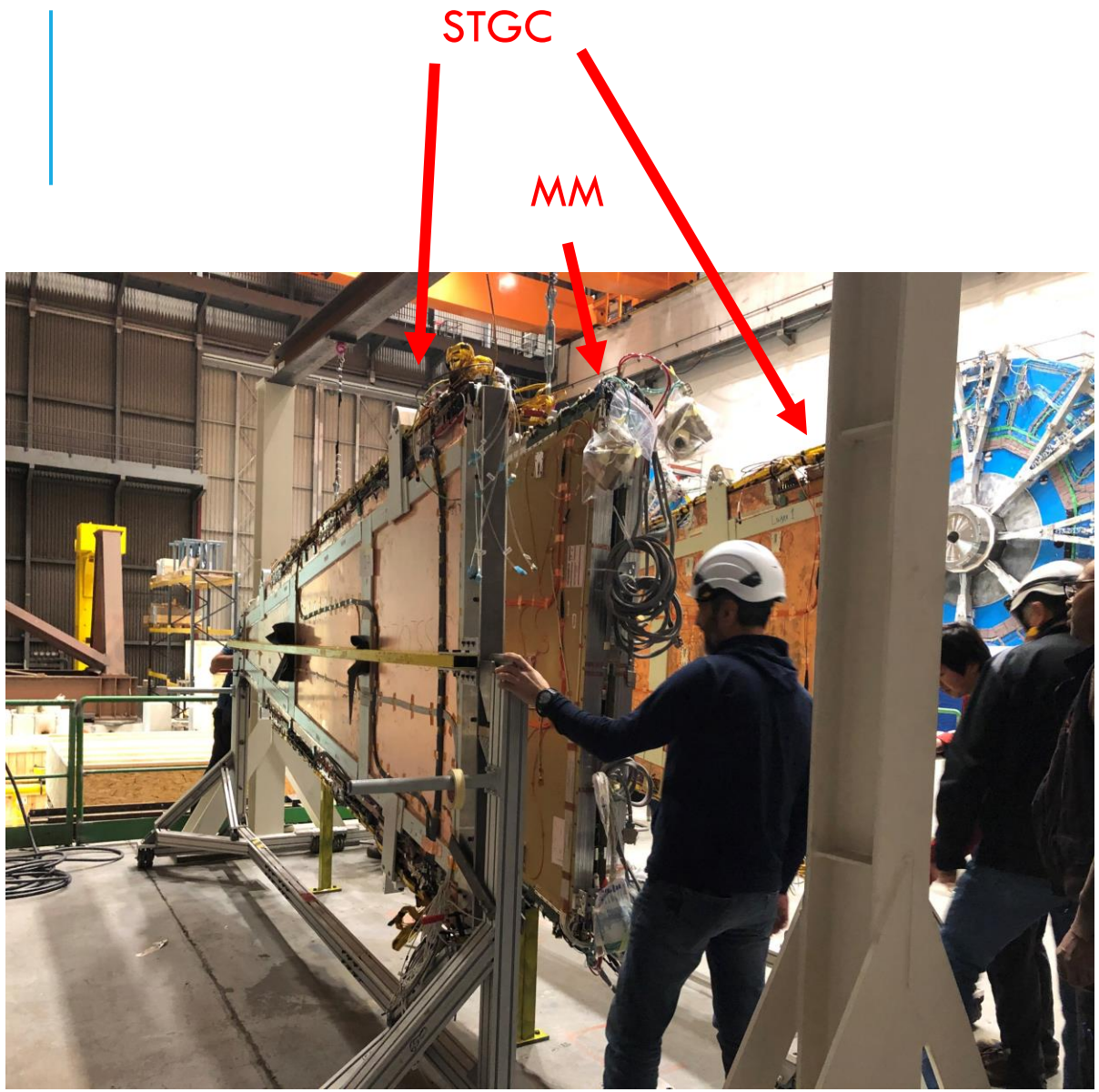
STGC CHAMBER EQUIPMENT INSTALLATION AT B.180 (7)

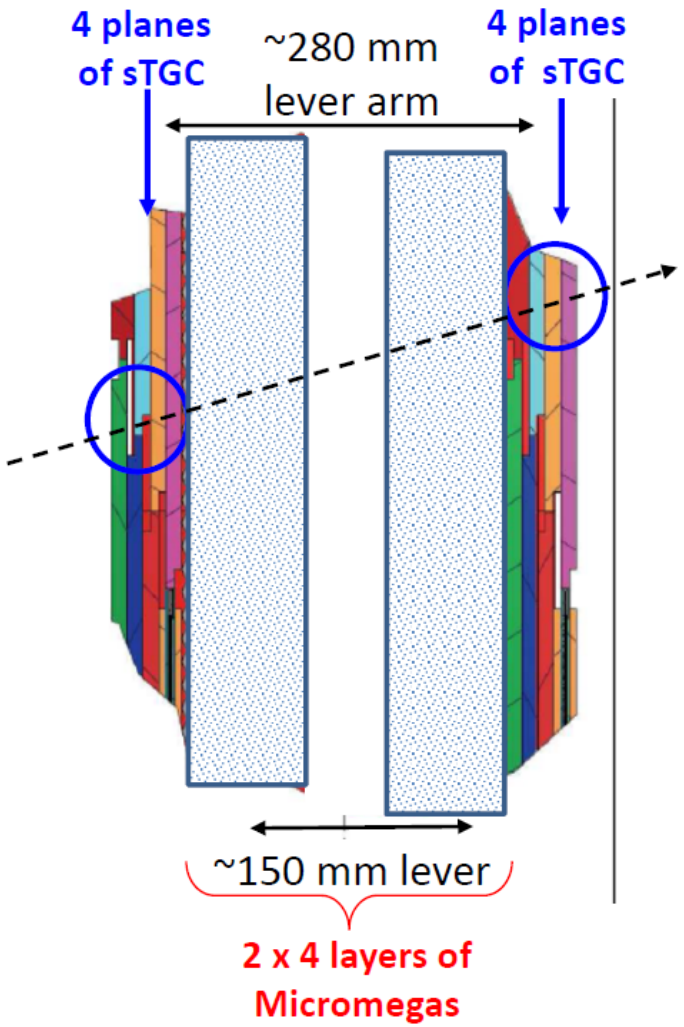


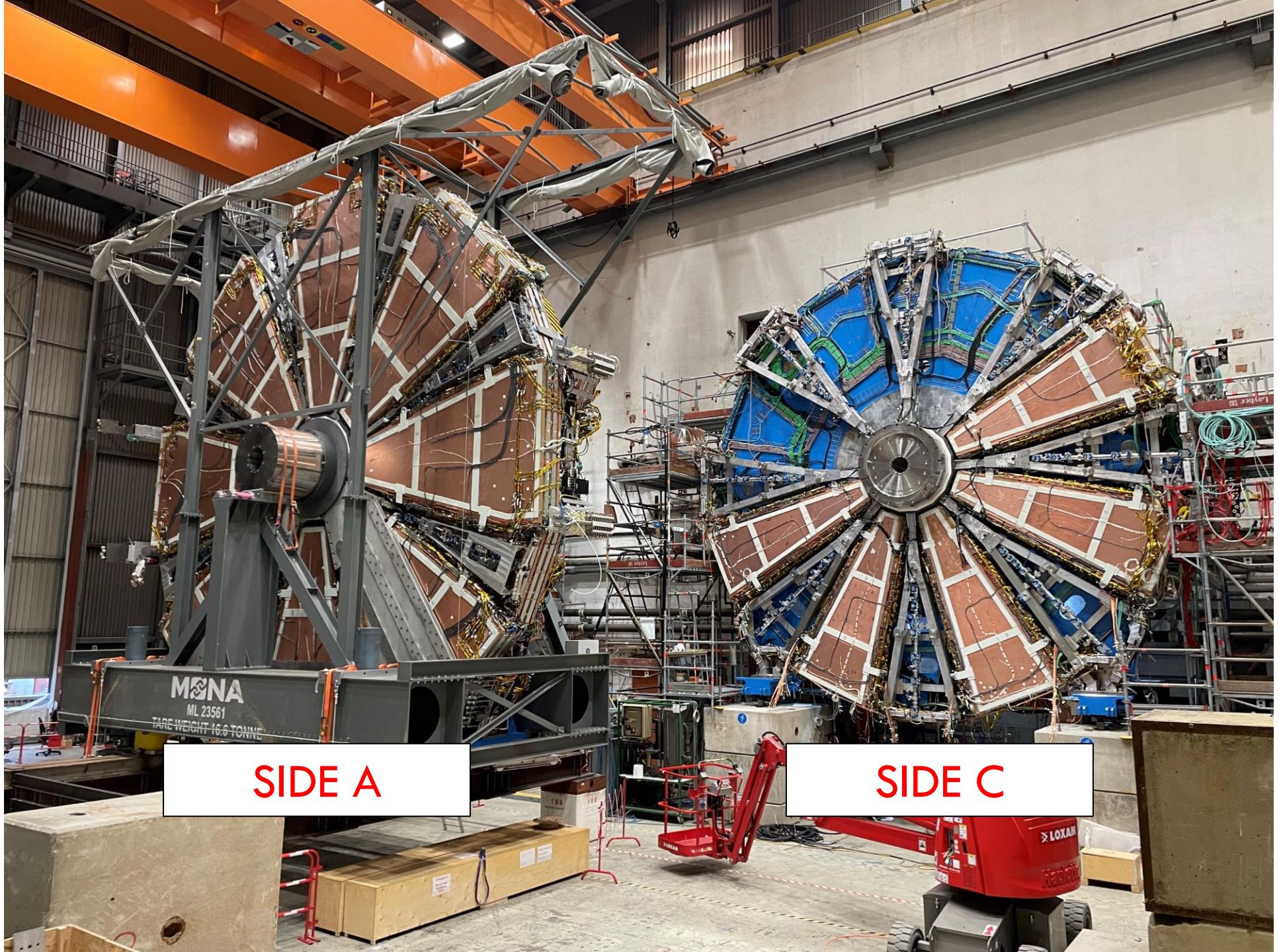
8) An installed chamber undergoing system tests: electronics, cooling and gas.

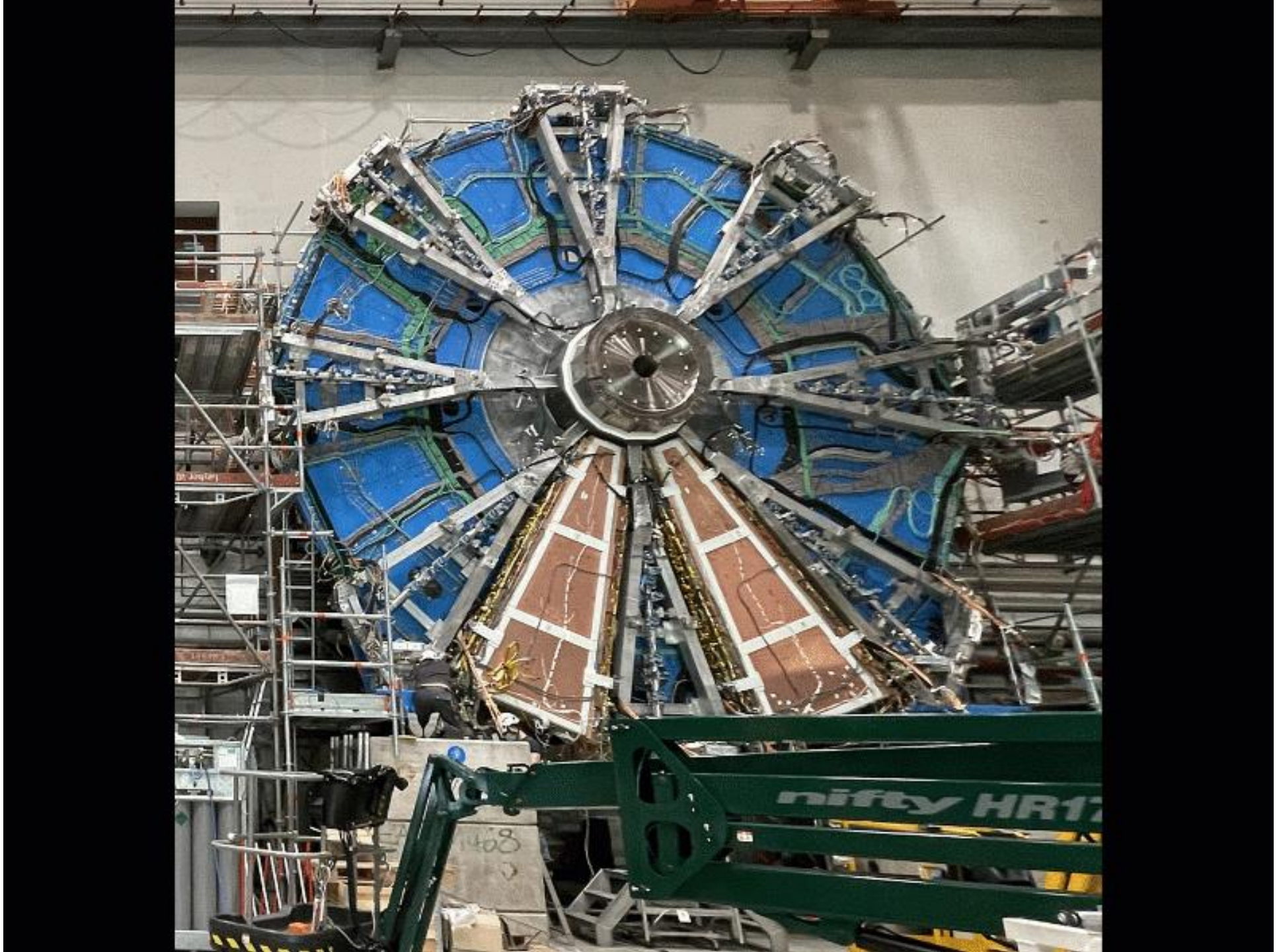
9) An installed chamber will be moved carefully from B.180 to the next door B.191 and then put onto the NSW structure.

COMMISSIONING AND SECTOR INSTALLATION TOWARDS THE TUNNEL


STGC
MM


4 planes of sTGC
~280 mm lever arm
4 planes of sTGC
~150 mm lever
2 x 4 layers of Micromegas


MONA
ML 23561
SIDE A
SIDE C


nifty HR17

CONCLUSION

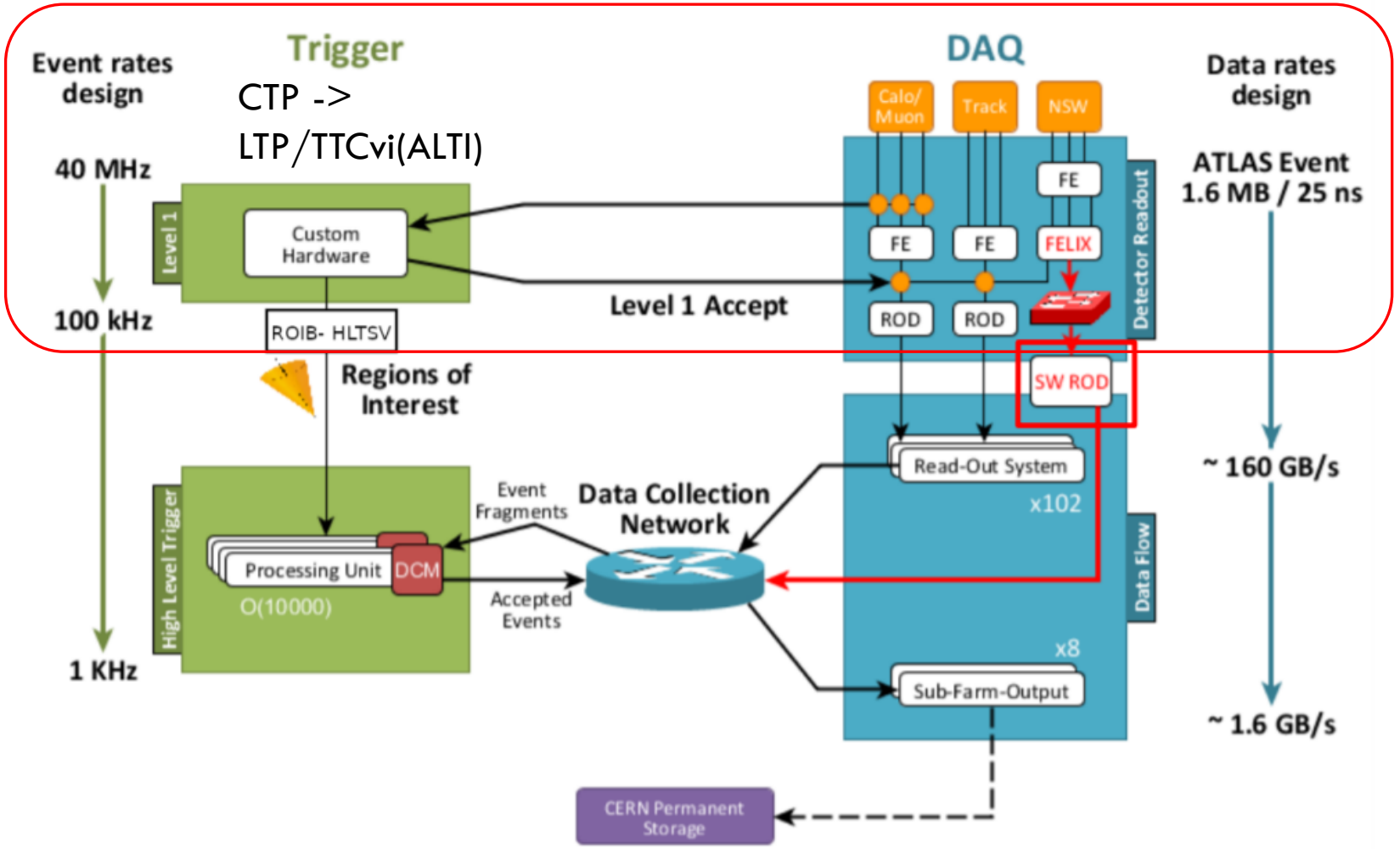
- Electronics and services installation for sTGC has been completed in AUG2021
- Both sides of NSW has been installed into the ALTAS detector before OCT2021
- Both sides of NSW are participating on the Run-3 of LHC

THANK YOU!

BACKUP

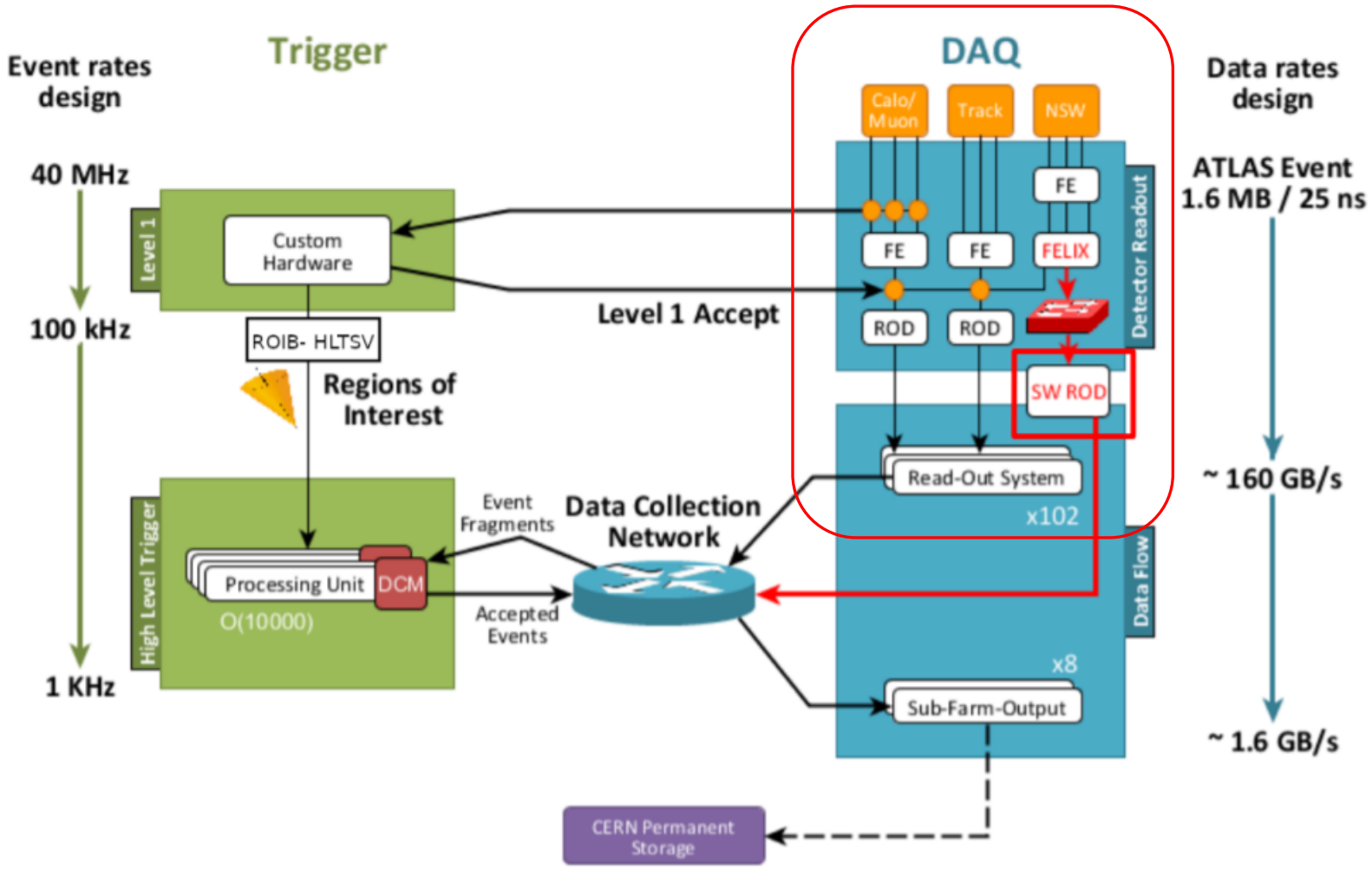
L1 TRIGGER

- Reduces the event rate down to 100 kHz(peak)
- Data is passed between CTP(Central Trigger Processor) and FE via local TTC crates
  (LTP ->`TTCvi -> TTCvx/ex)
- TTC in NSW will go through FELIX



LEVEL 1 DATA

- FE receive L1A and send out data to ROD (Readout Driver)
- In NSW case, ROD is SWROD which via FELIX
- SWROD can be configured to subscribe to multiple e-links, and combine them into a ROB(Readout Buffer) fragment

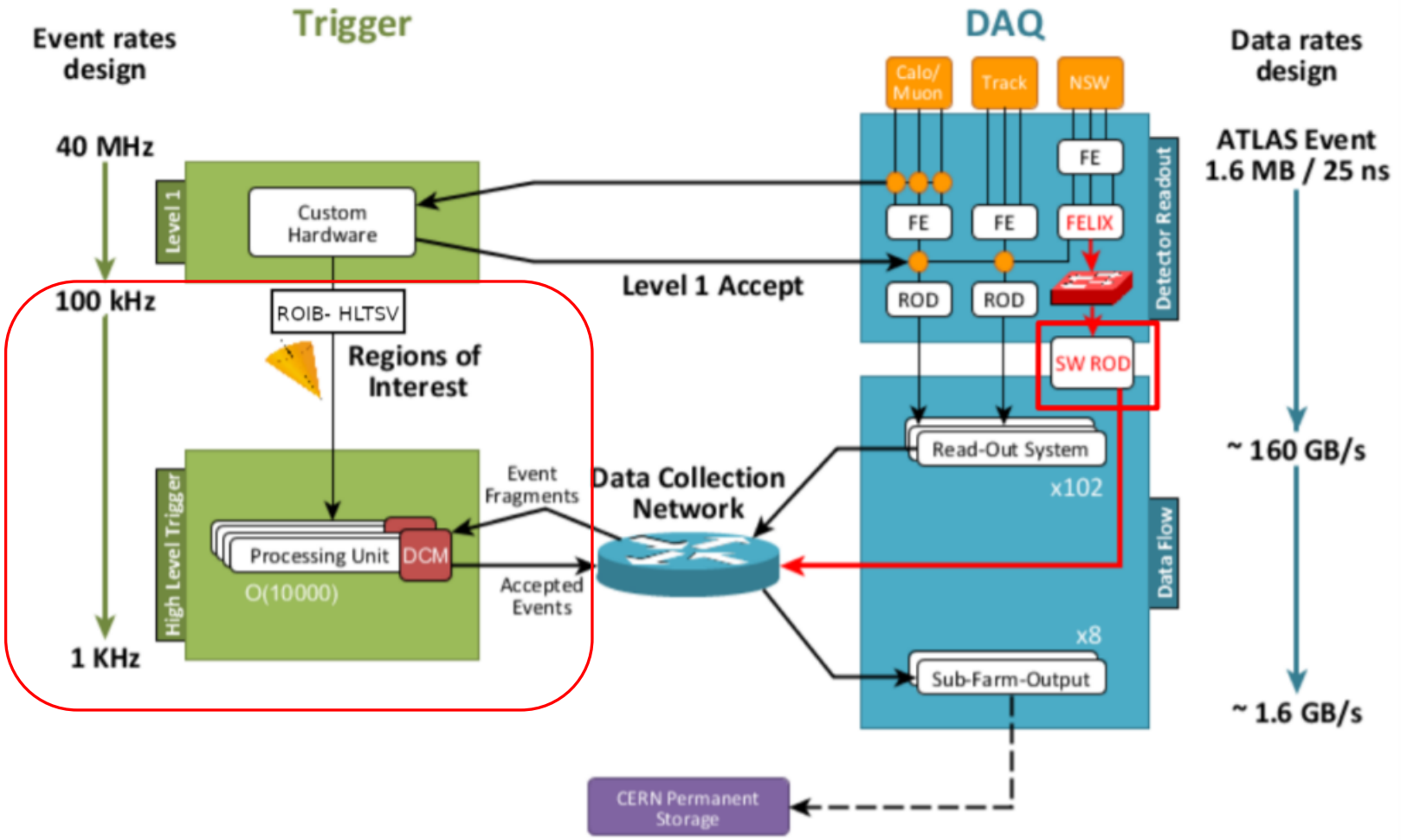


HIGH LEVEL TRIGGER

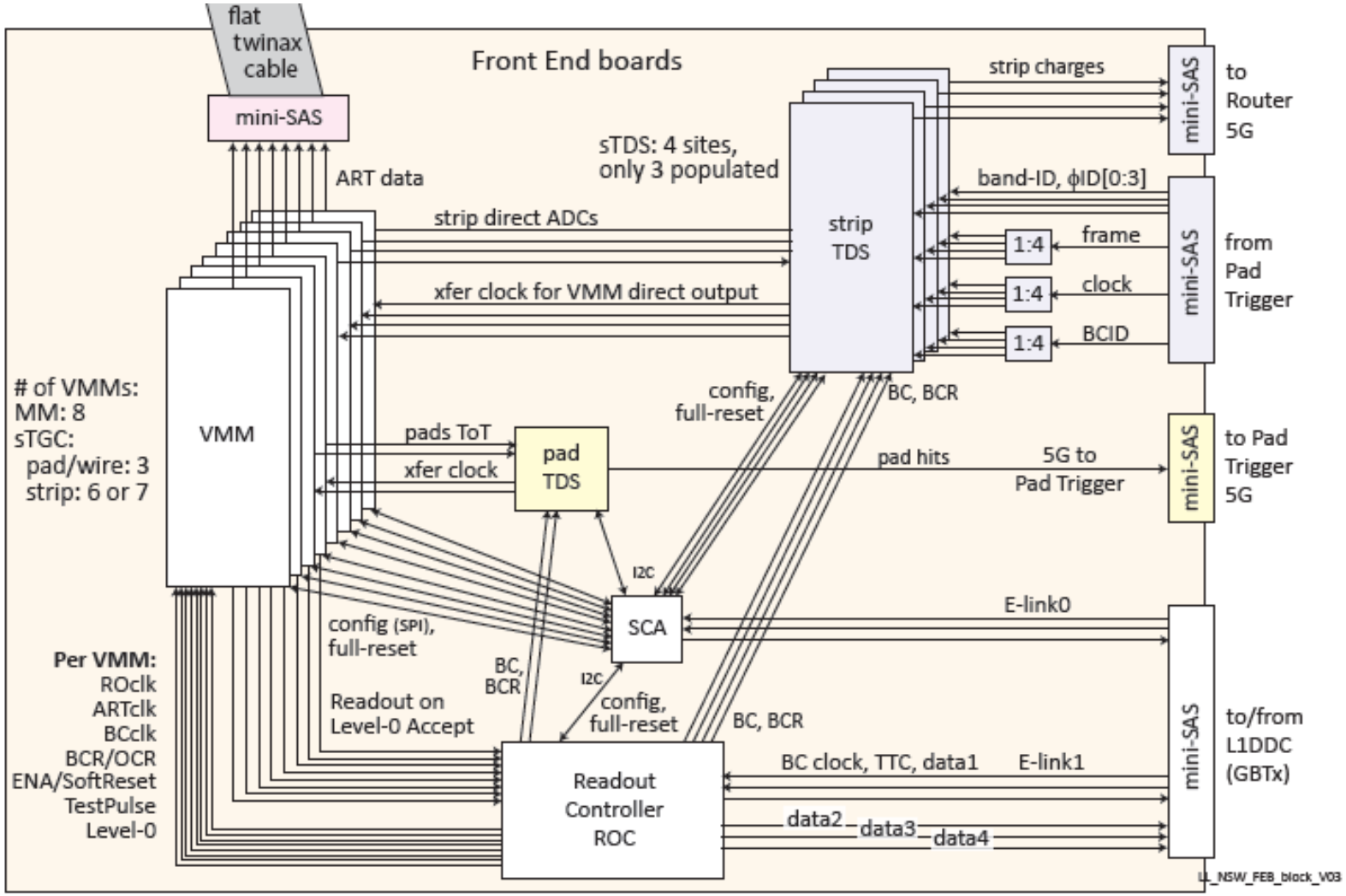
- Reduces the event rate from 100 kHz(peak) to few kHz

- Combines information from all L1 sources (Calo, Muon, Topo) and CTP into RoI(Region of Interest) Record and sends it to the HLT Supervisor (HLTSV)

- HLTSV distribute RoI Records to HLV farm (~2k nodes, ~50k cores), also send signals to SWROD on which ROB can be cleared



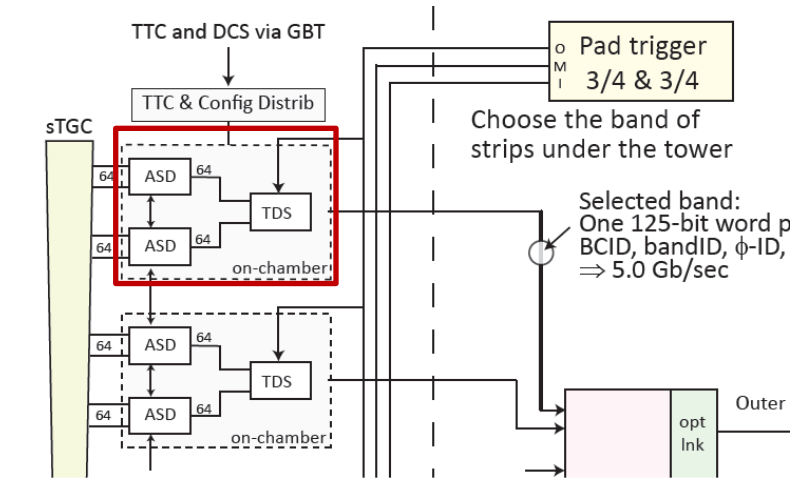
FRONT END BOARD (FOR STGC CHAMBER)

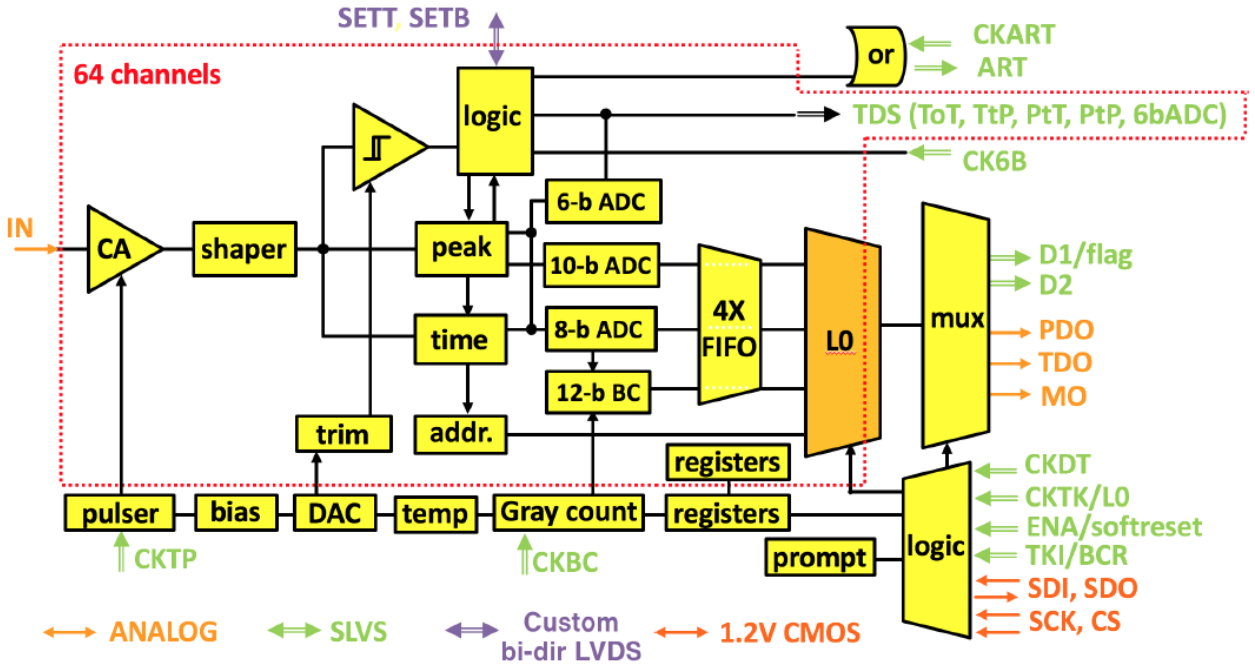


VMM

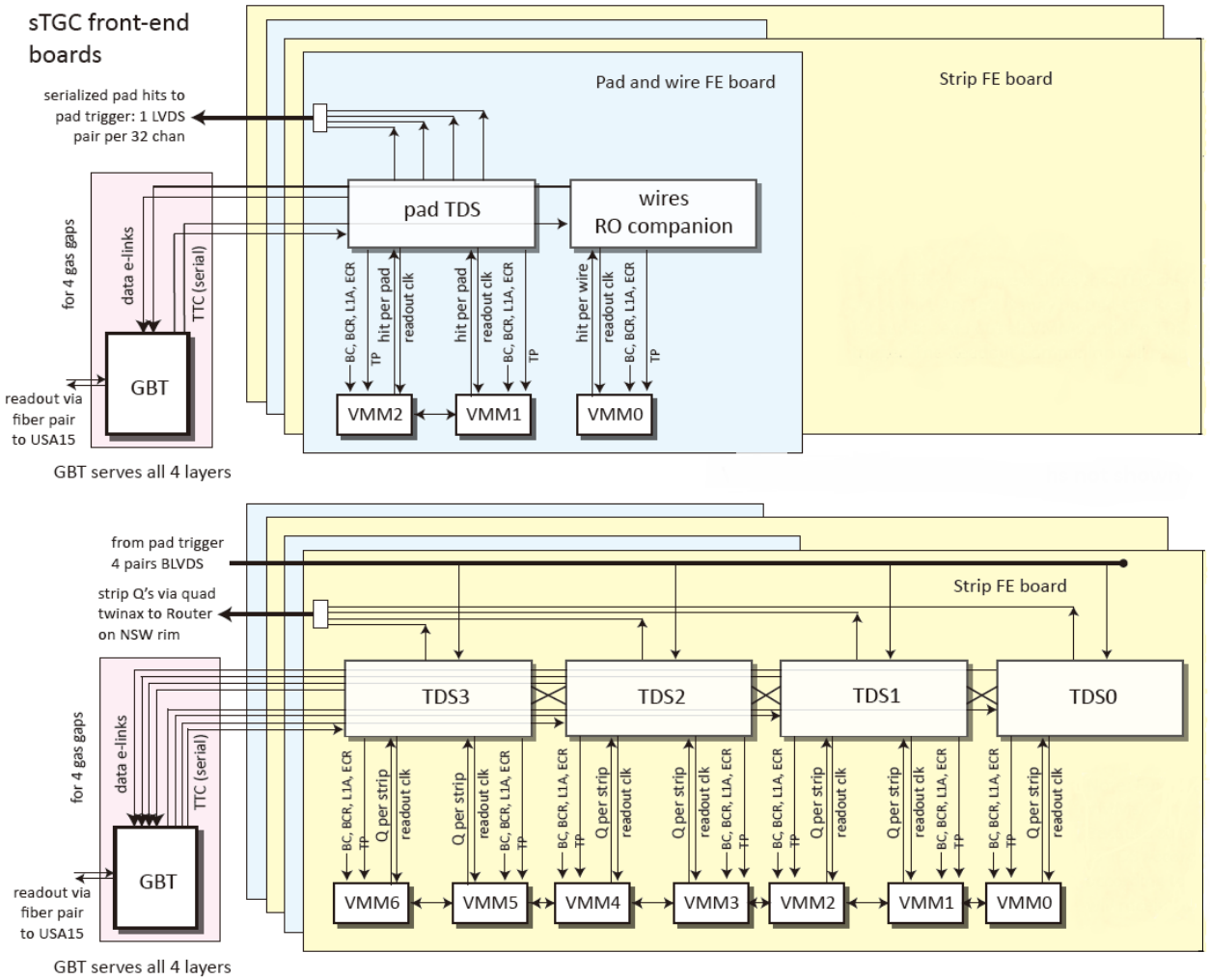
- Designed by BNL, it is a ASD(Amplifier-Shaper-Discriminator) ASIC that is planned to used for general detector (including MicroMegas and sTGC) readout.

- It can handle maximum 64 channels detector channels

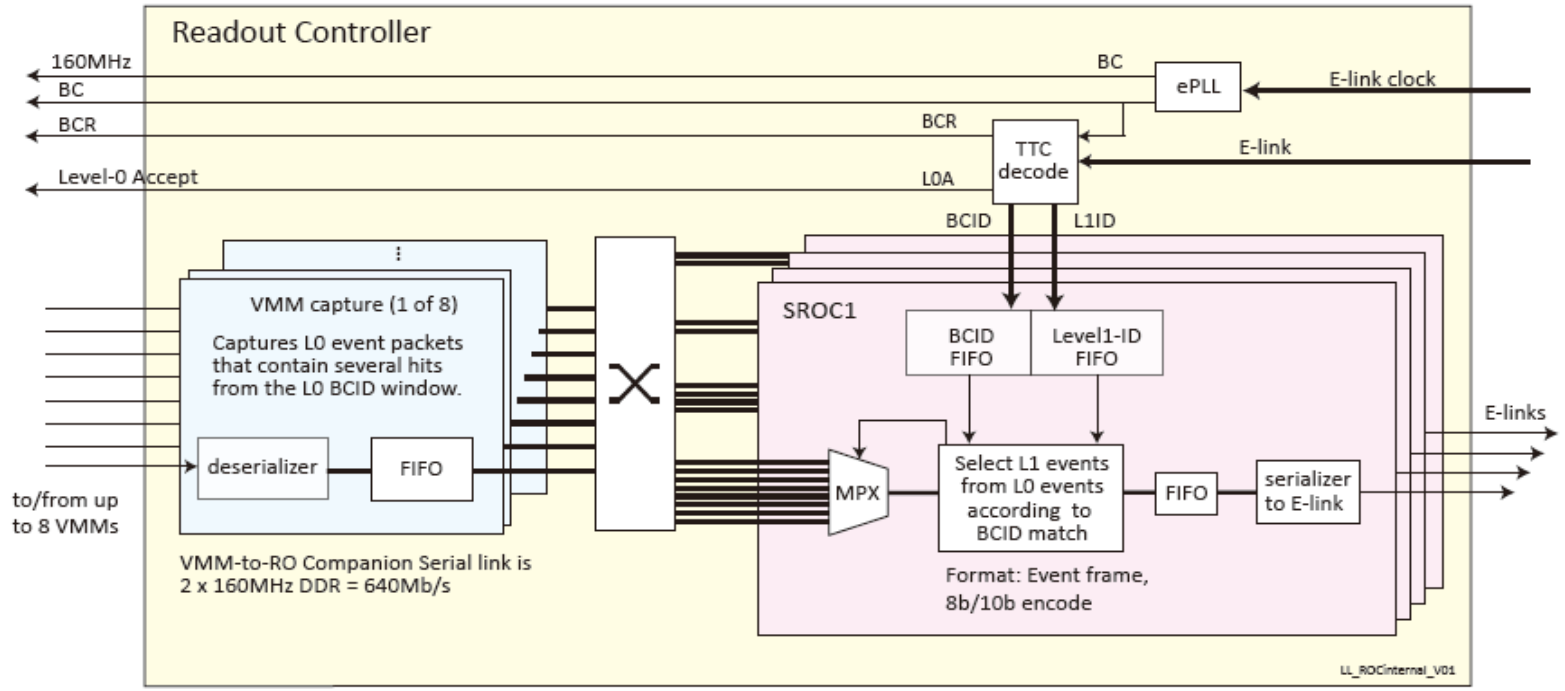




TDS (TRIGGER DATA SERIALIZER)

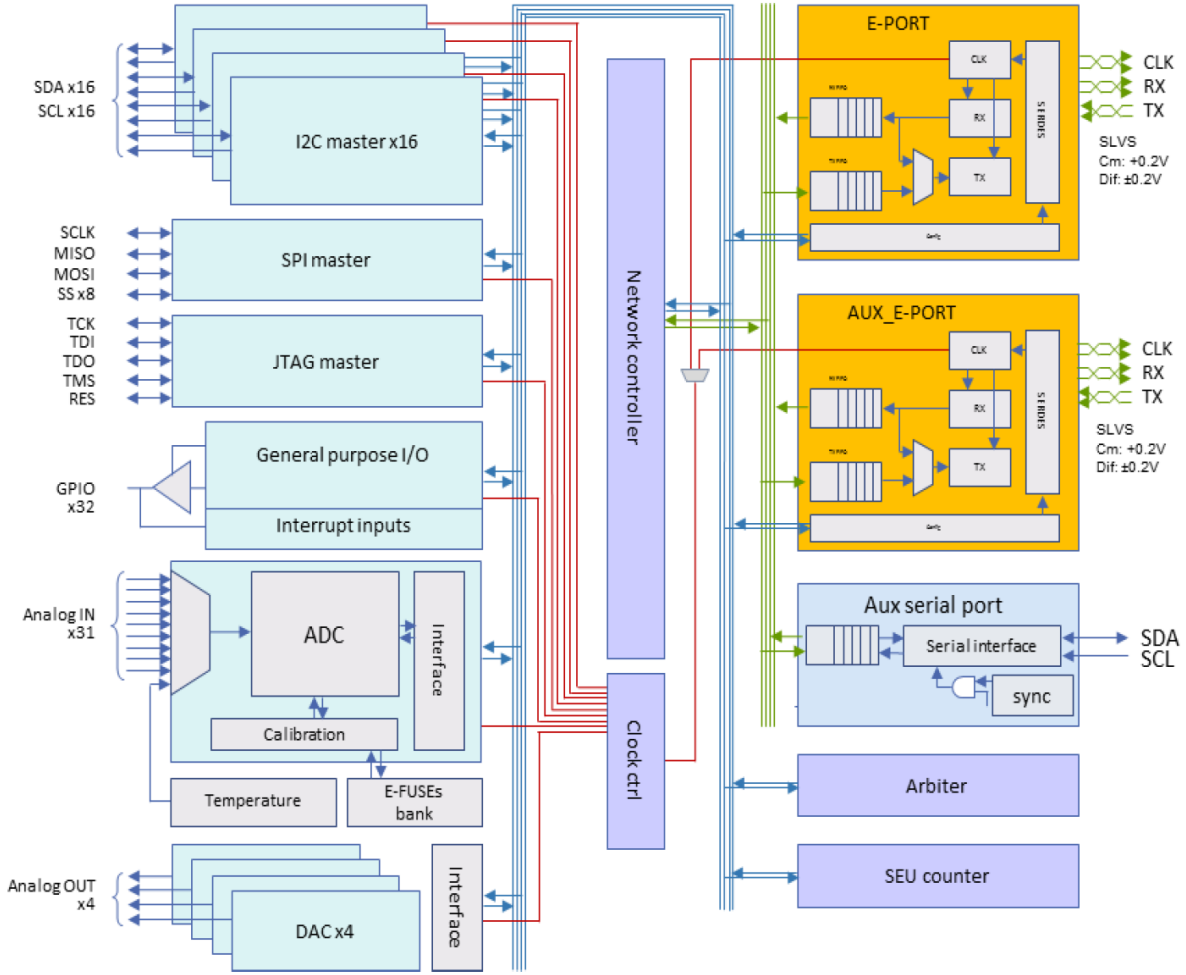


ROC (READOUT CONTROLLER)



- ROC used for receiving TTC signals(BCR,L1A) from FELIX which is used for readout of VMM

GBT-SCA



- General communication(I2C, SPI, JTAG, GPIO) ASIC