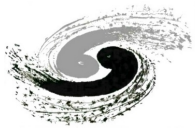

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Status of the CEPC vertex and tracking detector R&D

Yunpeng LU, Ying ZHANG, Yiming LI and Wei WEI
On behalf of the CEPC detector design teams

2022-10-24

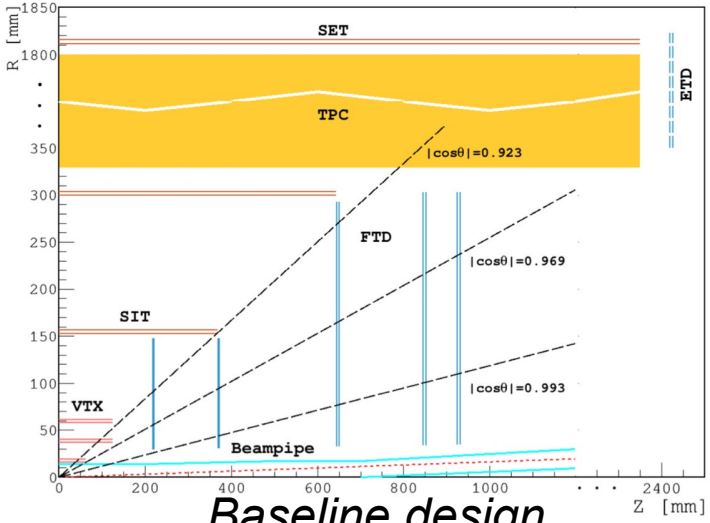
The 2022 international workshop on the high energy Circular Electron-Positron Collider (CEPC)

Outline

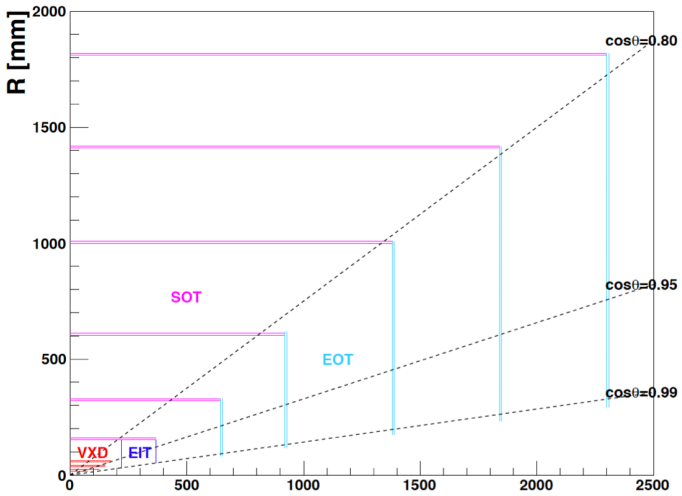
- Overview of the CEPC Vertex and Tracking detectors
- Progress of the JadePix chips
- Progress of the TaichuPix chips
- Other related talk in the workshop
- Summary and outlook

CEPC Vertex & Tracking Detector

- **CEPC requires a high-resolution and low material vertex and tracking system**
- **Vertex**
  - Challenge of high spatial resolution + 0.15% X0/layer material budget
  - MAPS/CMOS Sensor technology is favorable for low detector capacitance and noise
- **Tracker**
  - Baseline Design: Mixed Tracker (TPC + ~70m^2 Silicon）
  - Full Silicon Tracker: ~140m^2 Silicon
  - HVCMOS is more a promising technology for cost effectiveness and performance, while less constraint on detector noise



Baseline design



Full Silicon Tracker

CEPC Vertex detector requirements

Circular Electron Positron Collider (CEPC) proposed as a Higgs factory.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

  ➔ Impact parameter resolution,

$$\sigma_{r\emptyset} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$

Physics driven requirements		**Running constraints**	**Sensor specifications**	
$\sigma_{s.p.}$	2.8 μm		Small pixel	***~16 μm***
Material budget	0.15% X_0/layer		Thinning to	***50 μm***
		Air cooling	low power	***50 mW/cm²***
r of Inner most layer	16 mm	beam-related background	fast readout	***~1 μs***
		radiation damage	radiation tolerance	***≤3.4 Mrad/ year***
				≤6.2×10¹²n_{eq}/ (cm² year)

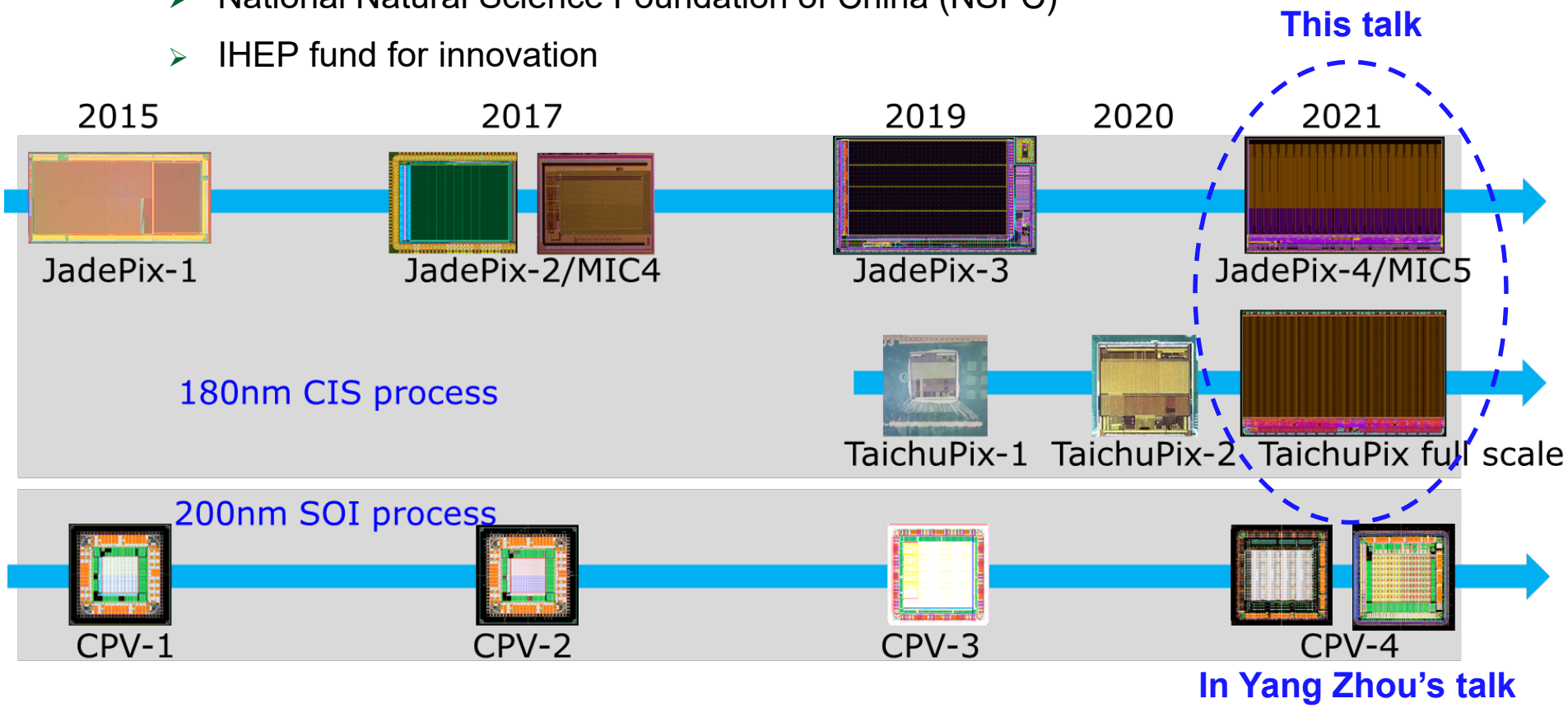
Baseline design parameters for CEPC vertex detector

	R (mm)	$\lvert z \rvert$ (mm)	$\lvert \cos\theta \rvert$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Overview of pixel sensors in China for CEPC VTX

- **Development of pixel sensors for CEPC VTX supported by**
  - Ministry of Science and Technology of China (MOST)
  - National Natural Science Foundation of China (NSFC)
  - IHEP fund for innovation

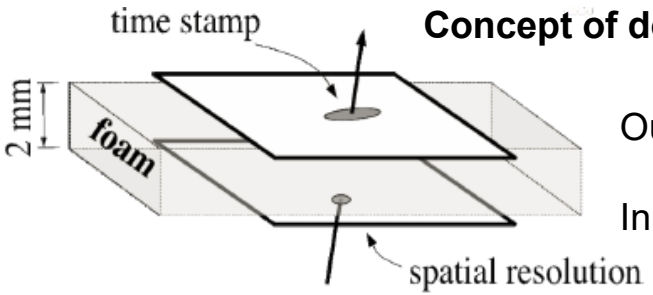


Ref: "Status report on MAPS in China", 2021 CEPC workshop, Yunpeng Lu

JadePix chips strategy

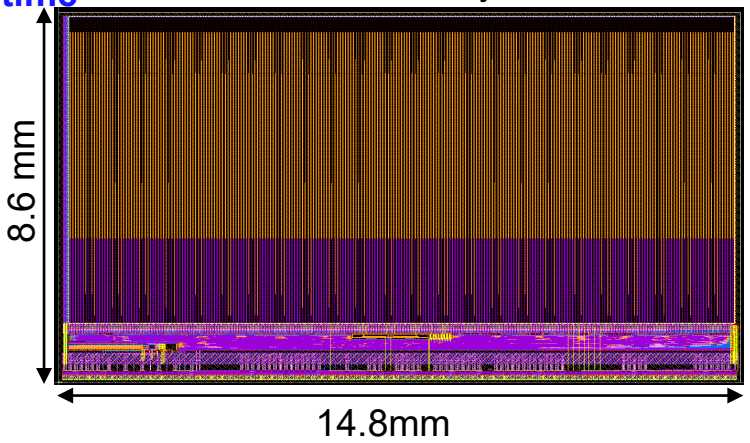
- **JadePix concerns the concept of double-sided layer**
  - Fine pitch & low power sensor for spatial resolution
    - Laser test on JadePix-3 indicates **s.p. < 3 μm achievable**
  - A faster sensor to provide time-stamp
    - **JadePix-4/MIC5 s.p. < 5 μm, 1 μs integration time**

Concept of double-sided layer

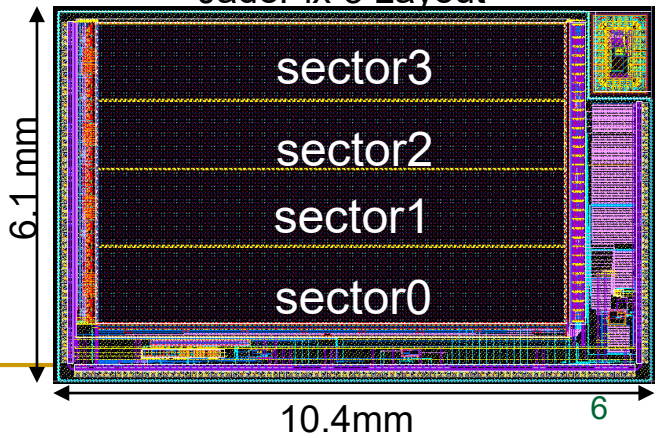


	JadePix-3	JadePix-4/MIC5
Pixel size	16 μm × 23.1 μm	20 μm × 29 μm
Integration time	98.3 μs	~ 1 μs
Average power	< 100 mW/cm^2	< 100 mW/cm^2
Pixel array	512 row × 192 col.	356 row × 498 col.
Die size	10.4 mm × 6.1 mm	14.8 mm × 8.6 mm
Readout mode	Rolling shutter	Data-driven

JadePix-4 Layout

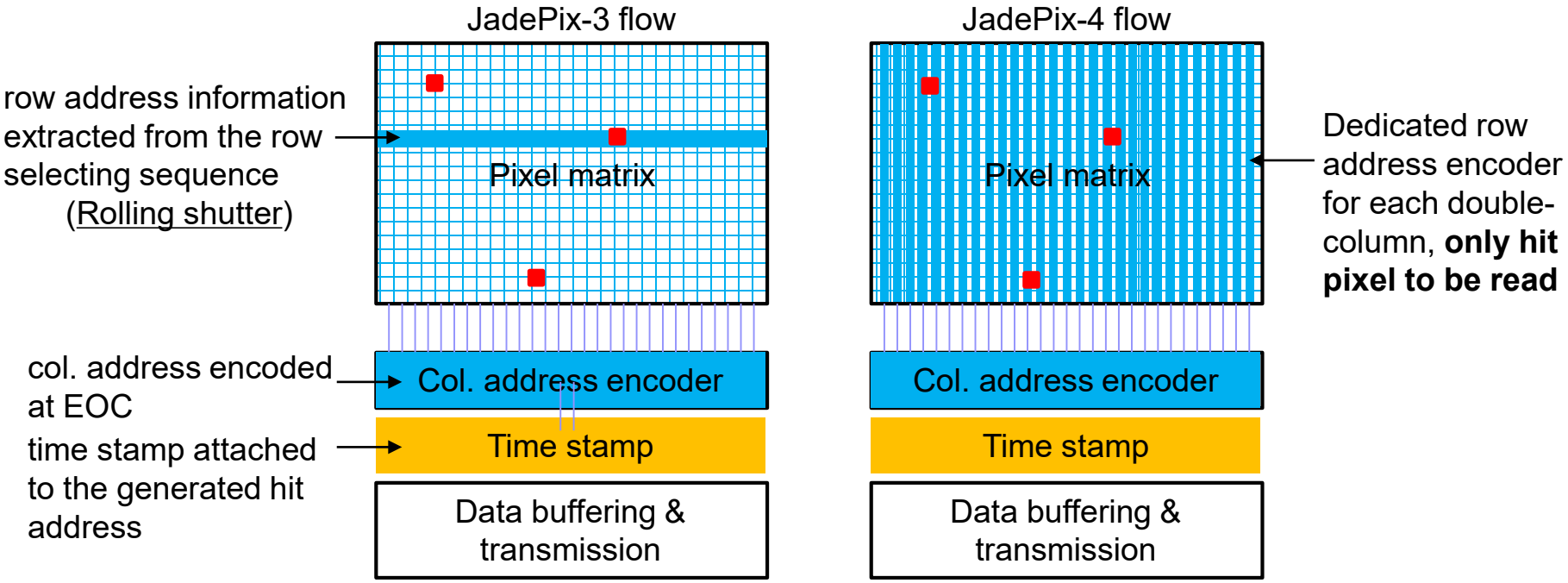


JadePix-3 Layout



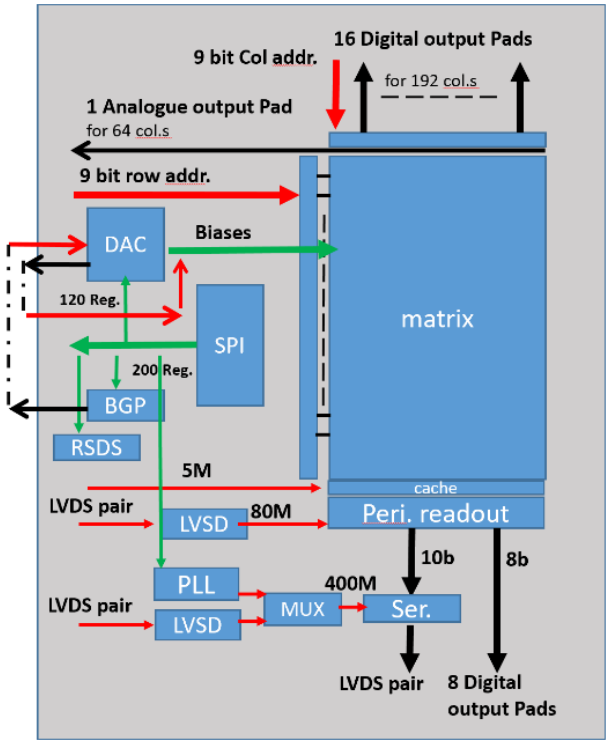
Hit processing flow of JadePix-3/4

- **Hit registered in each pixel needs fast processing**
  - Hit position (col. and row address) to be encoded
  - Time stamp to be attached
  - Register to be reset for the next hit
- **A major difference on the row address encoding**
  - JadePix-3, **rolling shutter** → minimized pixel pitches
  - JadePix-4/MIC5, **row address encoder** embedded in the matrix → much faster



An overview of the JadePix-3 design

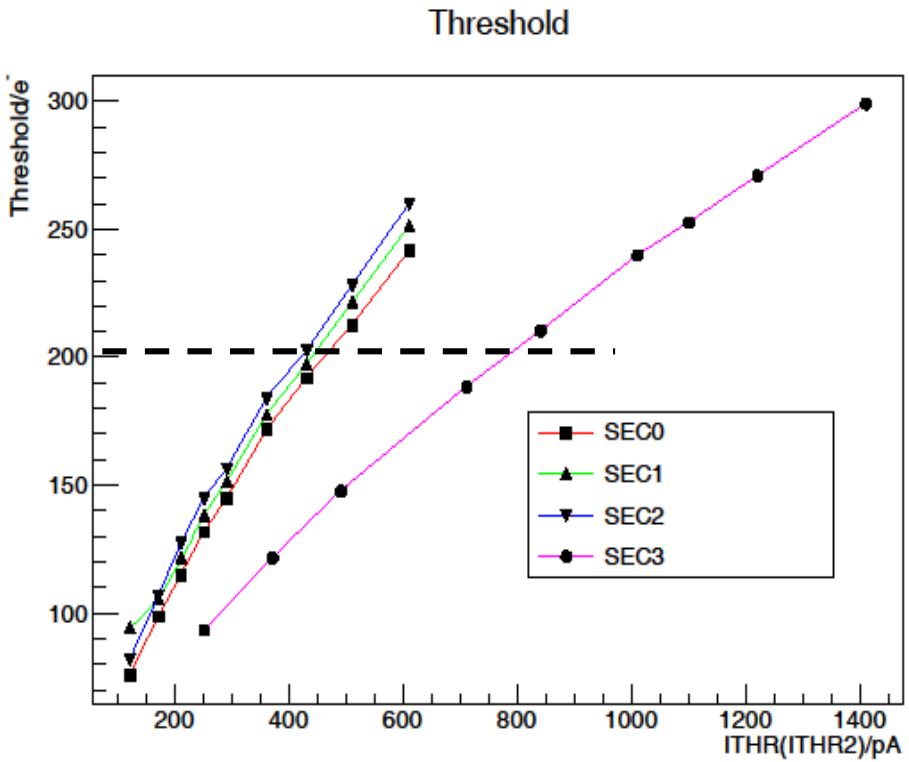
- **Full-sized in the rφ direction of detector layout**
  - Matrix coverage: 16 μm × 512 rows = 8.2 mm
- **4 parallel sectors, scalable in the z direction**
  - 48 × 4 = 192 columns
- **Rolling shutter to avoid heavy logic and routing in pixel matrix**
  - Minimum pixel size: **16 μm × 23.11 μm**
  - Matrix readout time: **98.3 μs/frame**
- **Full functional blocks in the chip peripheral**
  - Zero suppression, data buffering, Serializer, PLL, DACs, SPI
  - 8-bit parallel output or serial differential output @ 833 Mbit/s

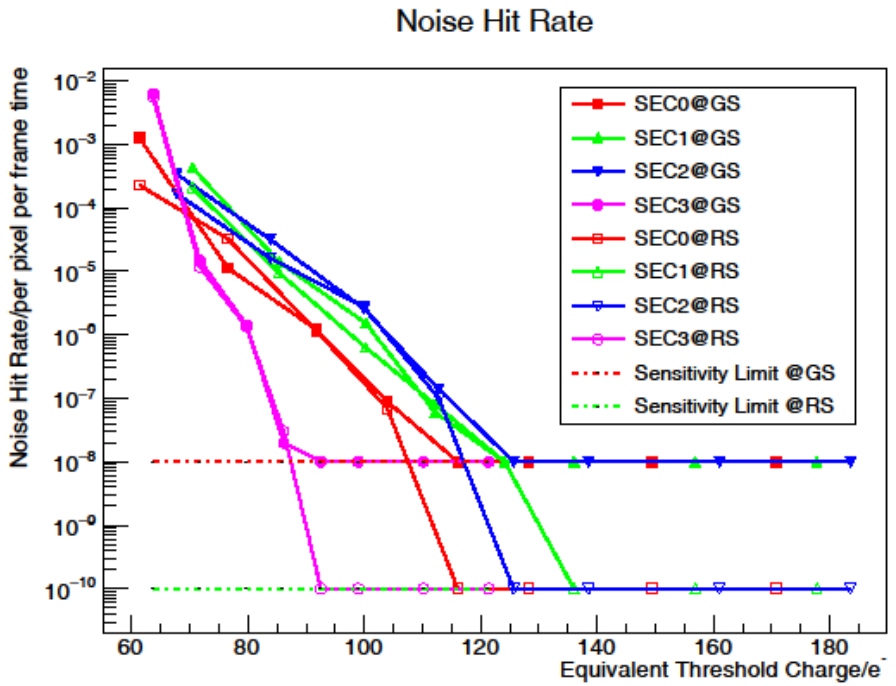


Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm^2
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm^2
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm^2**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm^2

Threshold and noise

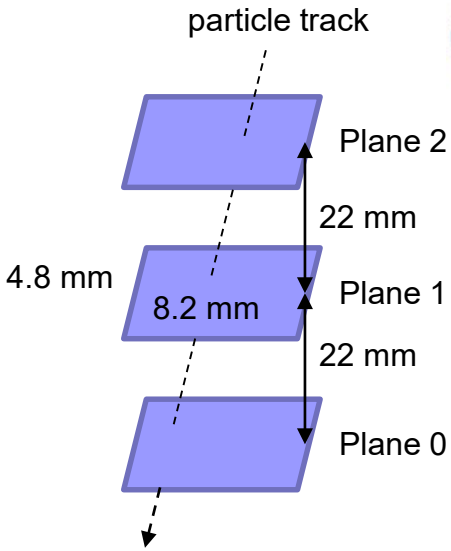
- **Threshold calibrated with electrical test pulse**
  - 200 e- applied to the full matrix
- Noise hit rate below 10^{-10} /frame/pixel
  - Sensitivity limit due to the statistics
  - Compared between Rolling shutter and Global shutter

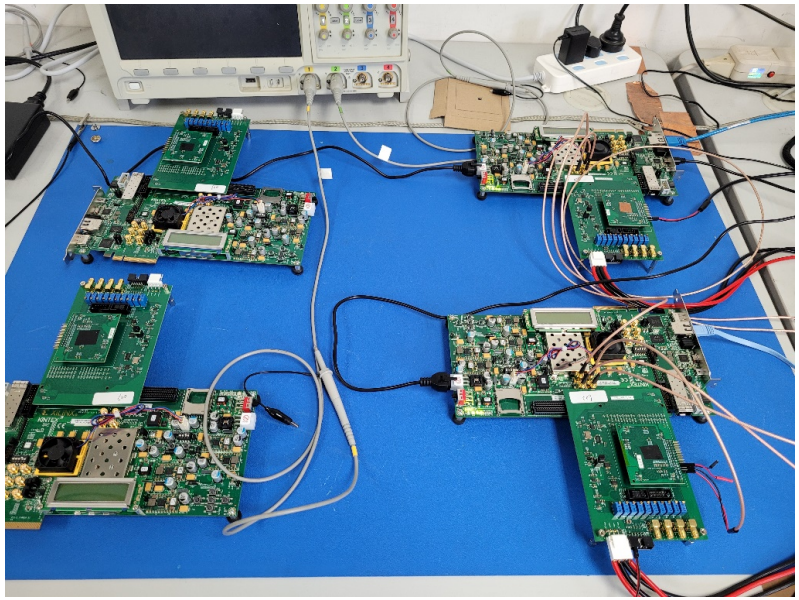


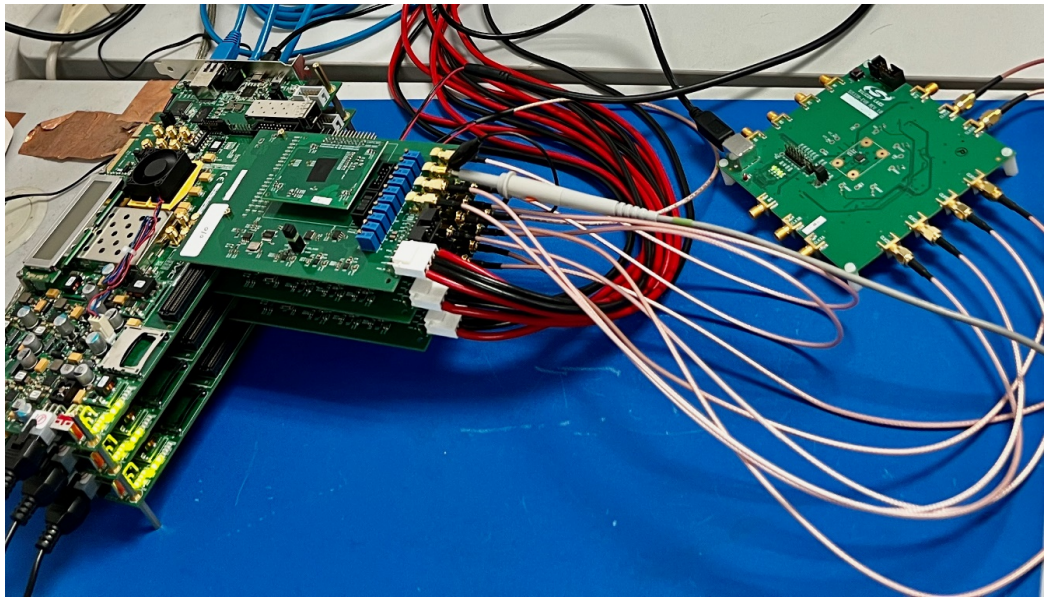


JadePix-3 Telescope

- **5 detector planes prepared.**
- **3 detector planes assembled for debugging**
  - Sensitive area 8.2 mm * 4.8 mm
  - Detector plane distance 22 mm

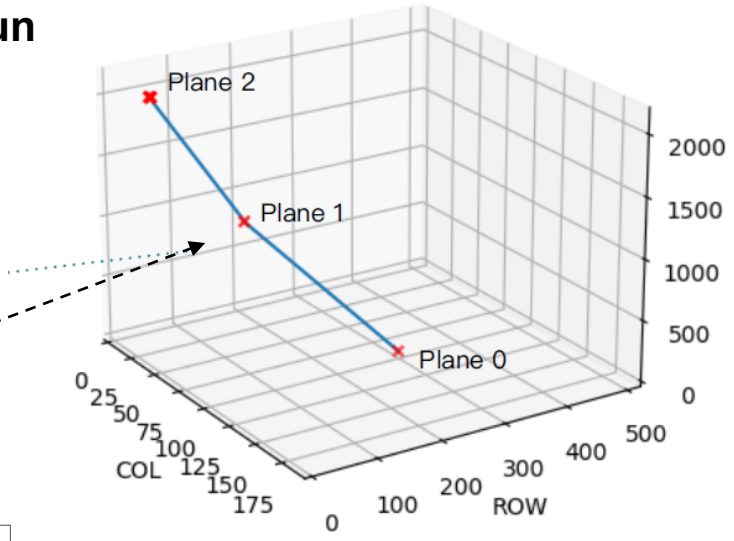


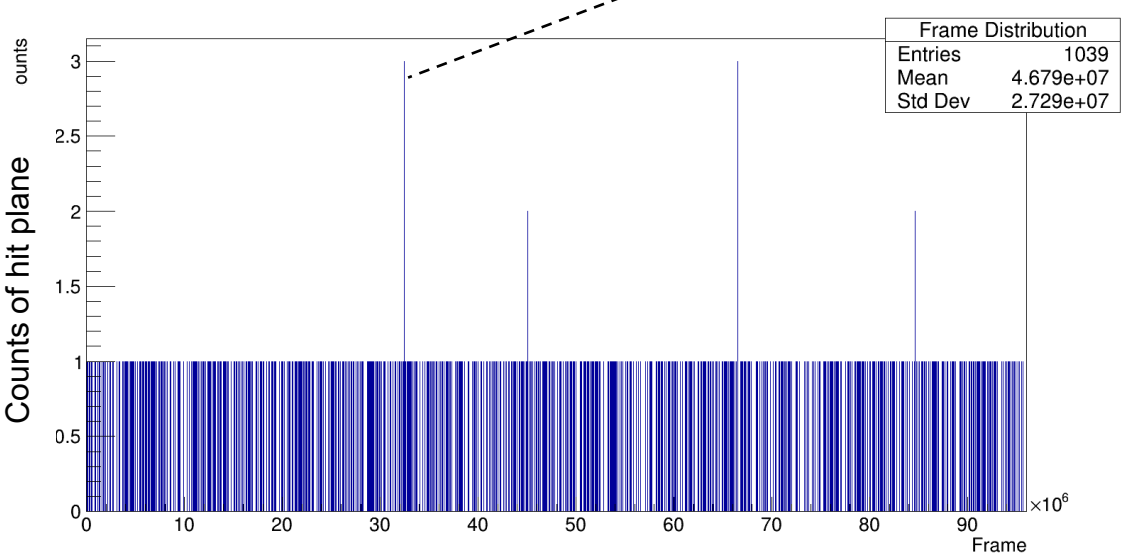


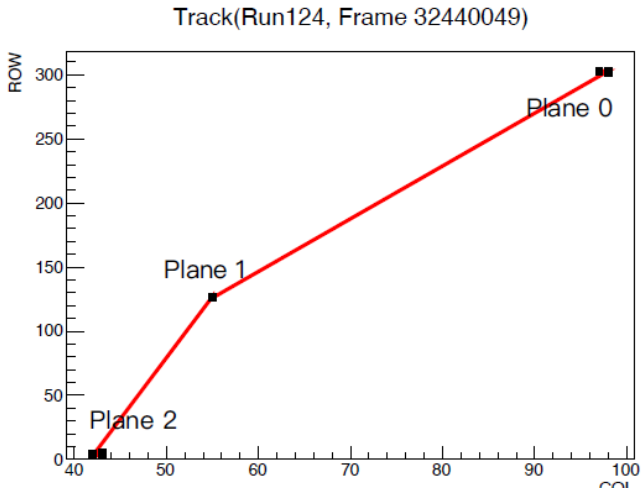


Initial test with cosmic ray

- **96 M frames scan in 160 minutes for a typical run**
  - 1035 frames have hits on single plane
  - 2 frames have hits on 2 planes
  - 2 frames have hits on 3 planes
- **Event rate 5.7/cm^2/min (assume one frame hits belong to one event)**
  - Possible contribution from noise hits, but at very low rate



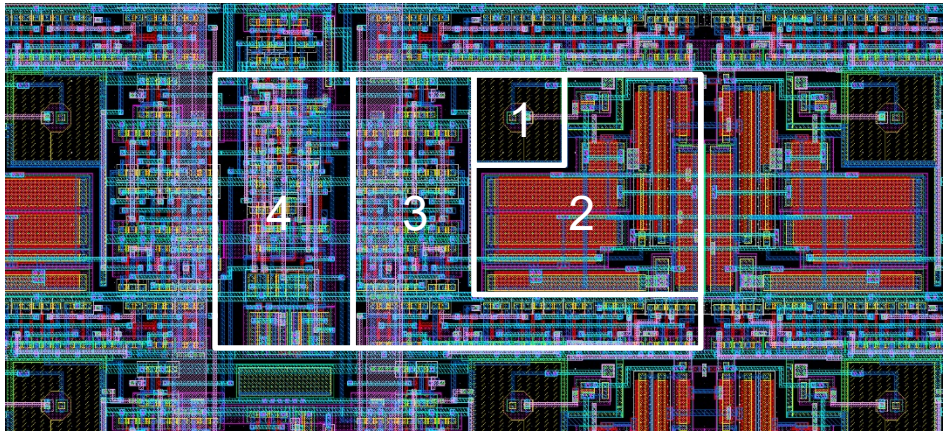




Implementation of JadePix-4/MIC5 pixel

- **Key component verified and reused from JadePix-3**
  - Diode
  - Analog frontend
  - Hit register
- **Asynchronized Encoder and Reset Decoder (AERD) ***
  - Generating col. and row address from hit pixel
  - Tracing back to reset hit pixel
- **Final layout of pixel matrix**
  - pixel array: 356 row × 498 col.
  - Pixel size: 20 μm × 29 μm

*P. Yang, etc., NIMA 785 (2015) 61-69

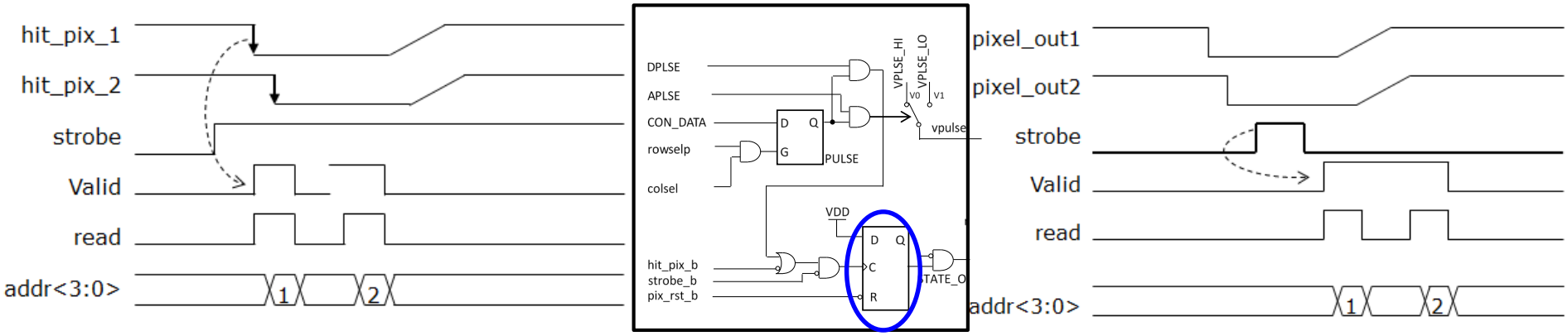


JadePix-4 pixel layout
(MET4 and above not shown)
1. Diode
2. Analog frontend
3. Digital logic
4. AERD shared by 2 col.

- Submitted to a shared engineering run in Oct. 2021
  - Chips received in July 2022, ready for test

Readout modes

- **Triggerless mode**
  - Global gate signal, **strobe==1**
  - All hits registered at their leading edge
  - 0.2 hits/μs per double col. with the estimated hit density of inner most layer
  - Occupancy 0.02% @ integration time = 1 μs
- Trigger mode
  - Global gate **controlled by trigger signal**
  - Hits registered only when overlapped with a trigger (analog buffer)
  - Capable to handle very high hit density with a dead time for readout, 50 ns/hit



Outline

- Overview of the CEPC Vertex and Tracking detectors
- Progress of the JadePix chips
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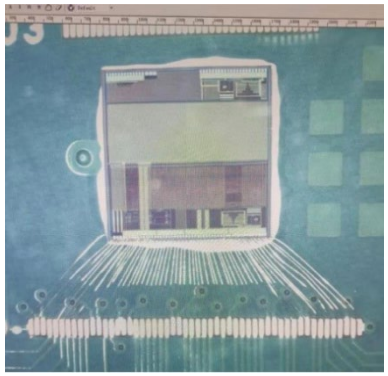
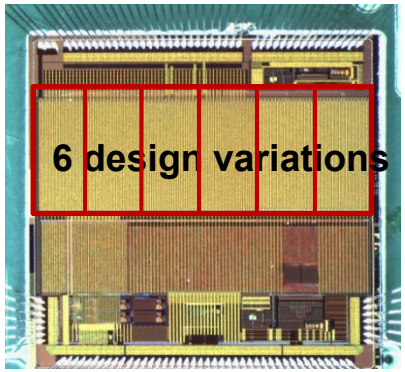
TaichuPix sensor prototyping

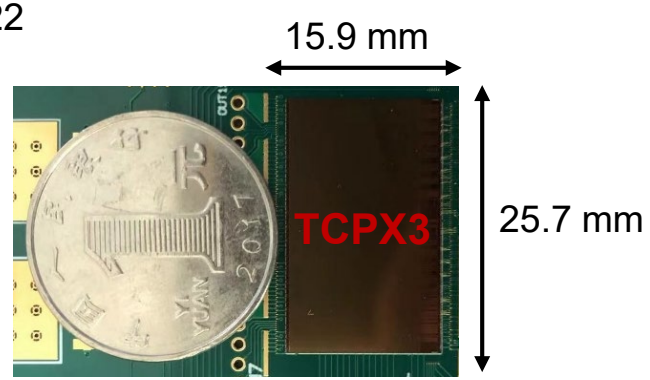
- **Major challenges for the CMOS sensor**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 round of sensor prototyping in TJ-CIS 180 nm process**
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019.06 – 2019.11
    - TaichuPix-2: 2020.02 – 2020.06
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022



TaichuPix-1

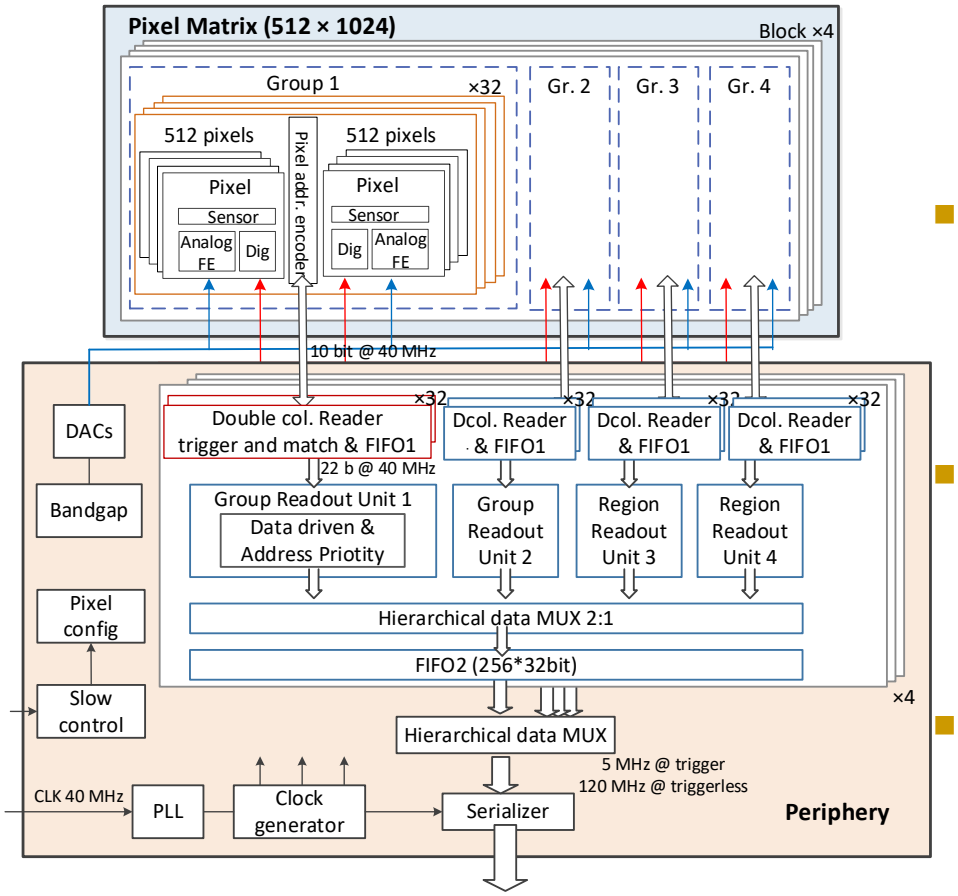


TaichuPix-2



TaichuPix-3
Pixel size：25 μm × 25 μm

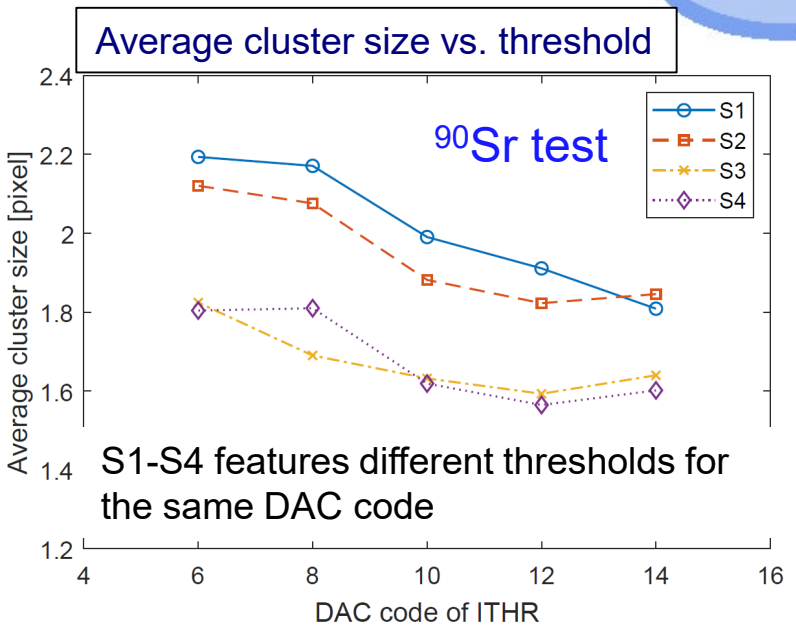
TaichuPix architecture



- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - **Time stamp added at EOC**
  - **Readout time**: **50 ns** for each pixel
- **2-level FIFO architecture**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 4.48 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

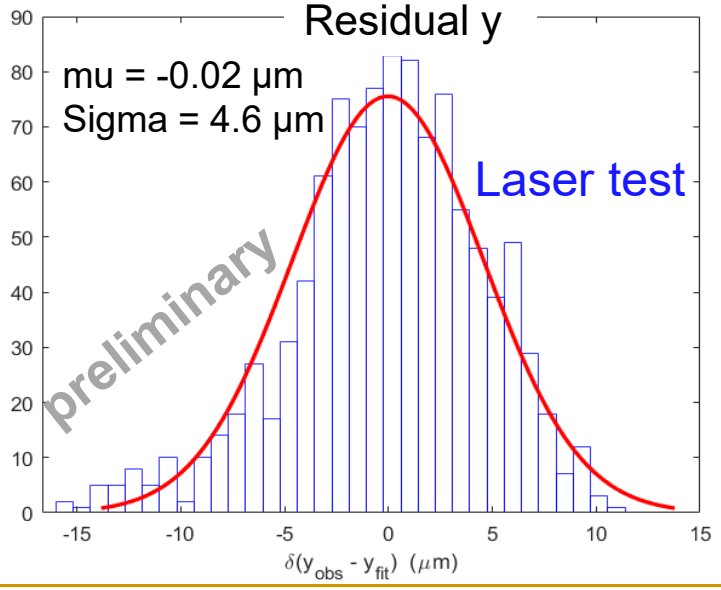
Update on TaichuPix chips

- **TaichuPix2 test with ^{90}Sr**
  - Average cluster size decreases with threshold as expected
  - **Cluster size < 3** indicates the estimated maximum hit rate (36 MHz/cm^2) reasonable
  - **Cluster size > 1** could benefit the spatial resolution (better than $\boldsymbol{pitch}/\sqrt{\mathbf{12}}$ = 7.2 μm)



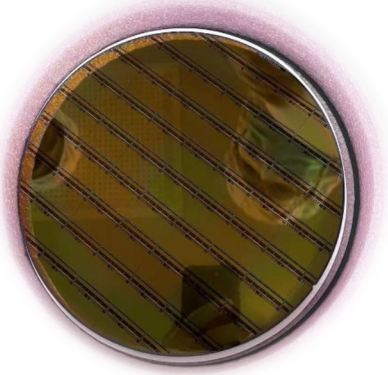
S1-S4 features different thresholds for the same DAC code

- **Laser test**
  - Laser diode with 658 nm wavelength
  - One dimension laser scan on the test chip with fixed step of 1 μm
  - Preliminary result indicates a resolution **less than 5 μm**
  - Further investigation ongoing
    - Laser 1064 nm
    - With different laser power and/or diff. pixel threshold

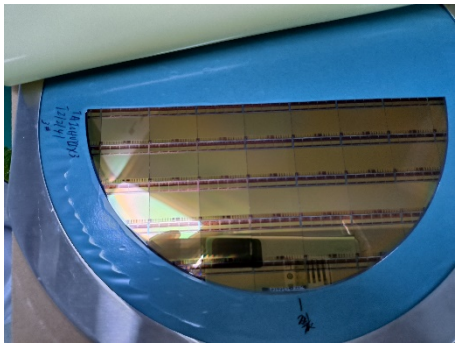


Large-scale sensor TaichuPix-3

- **6 TaichuPix-3 wafers arrived at IHEP in July**
  - **One wafer thinned down to 150 μm and diced**



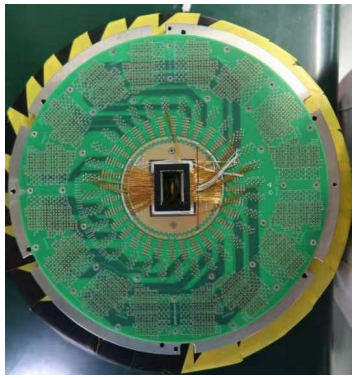
8-inch wafer



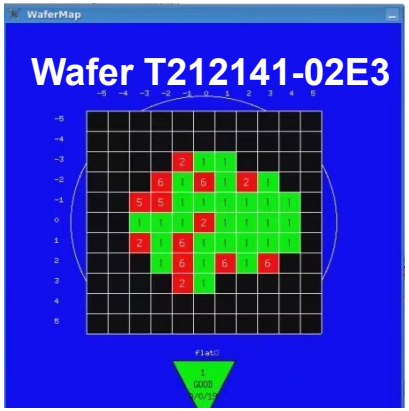
Wafer after thinning and dicing

Thickness after thinning

  - **Complete wafer testing on probe-station** → chip selecting & yield evaluation



Probe card for wafer test



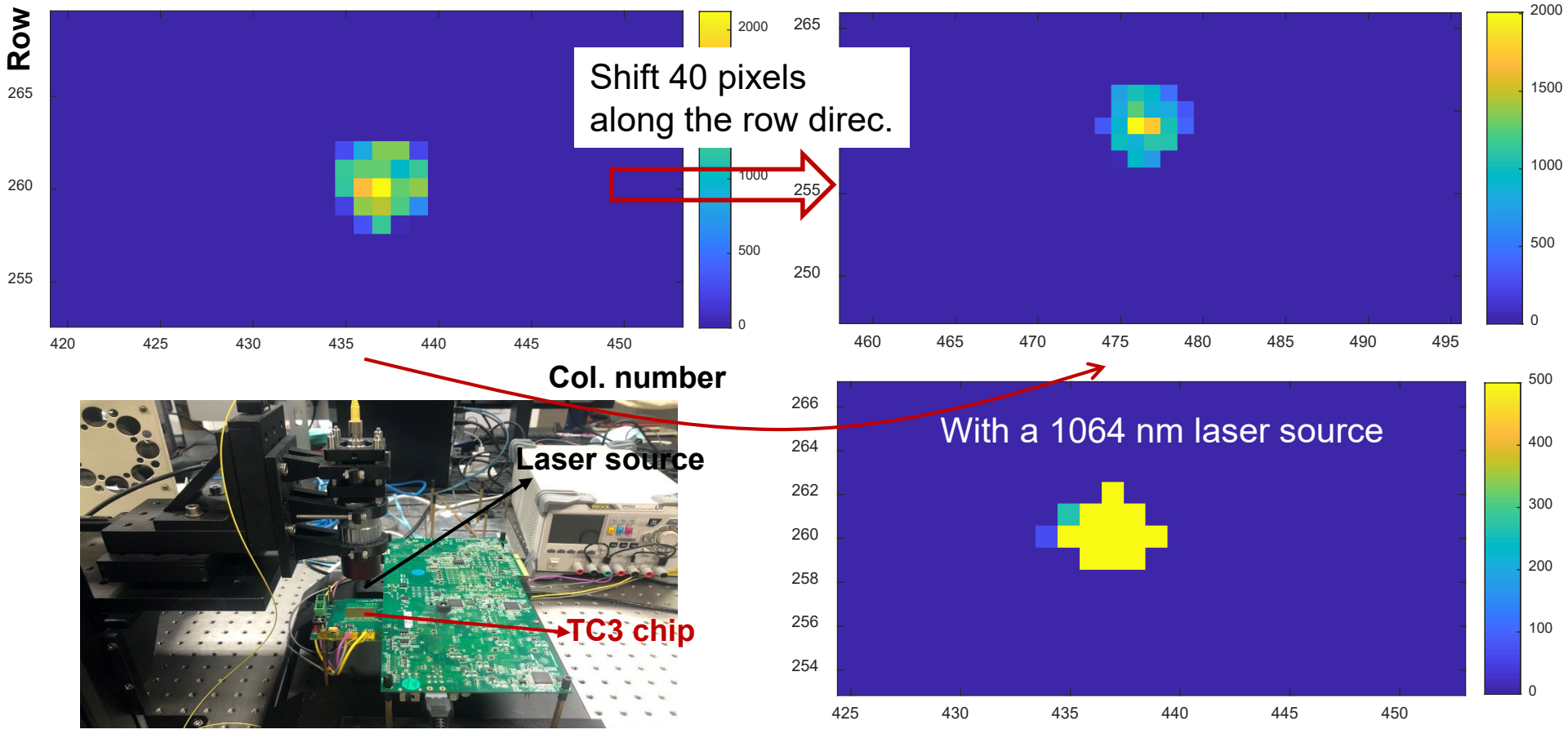
Typical yield of wafer test: 60~70%

5 wafers tested

- 2 wafer based on standard process
  - Reasonable yield achieved
- 3 wafer based on modified process
  - Preliminary result indicates lower yield than the std. process

First laser tests on TaichuPix3

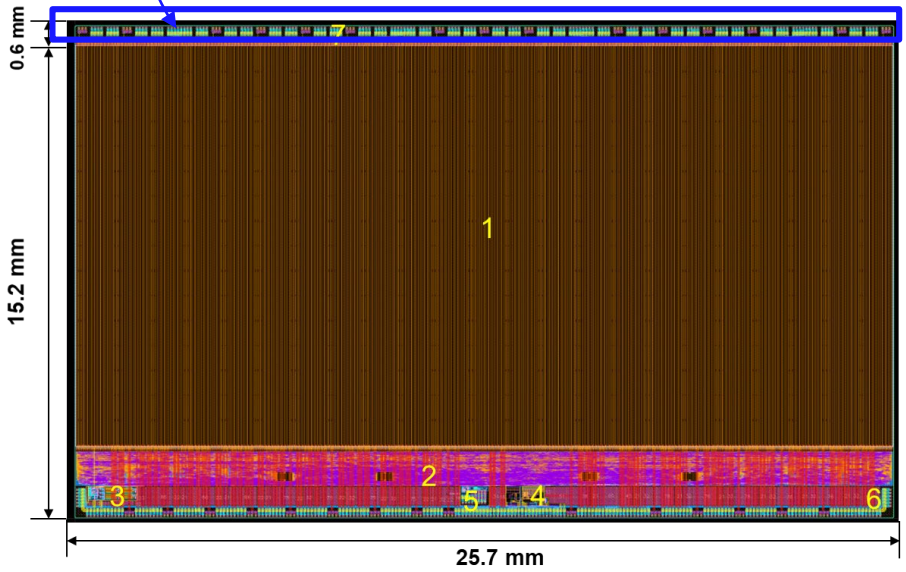
- **Using laser sources to verify the functionality**
  - With a 653 nm laser source & all pixels unmask



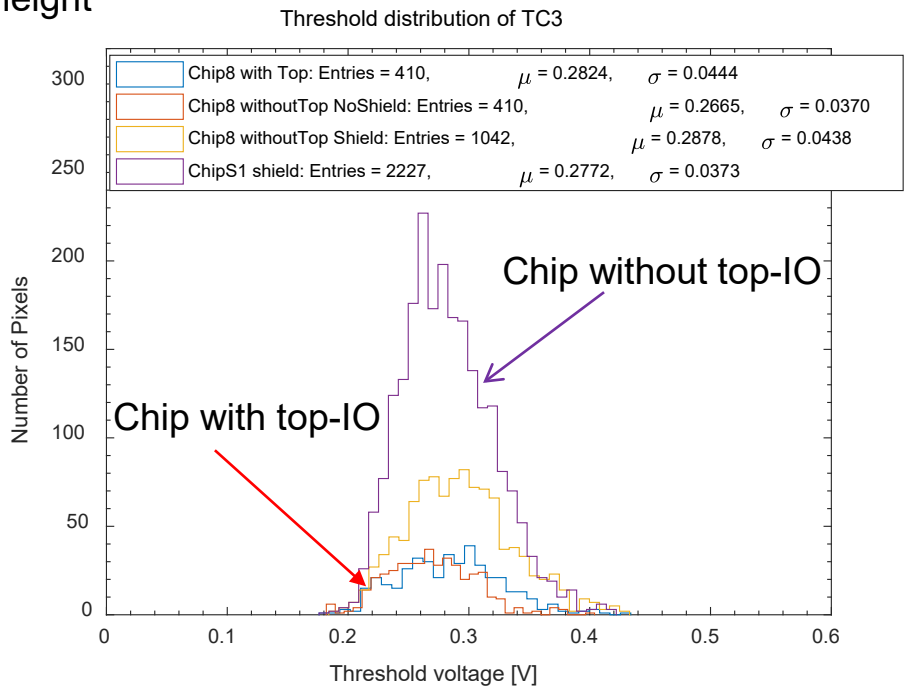
- **Functionality of the full signal chain proved**
  - Sensor+ pixel analog + pixel digital + periphery readout + data interface

Power IR-drop study of large-scale sensor

- **Power pads and power/bias rails at the top to help ease the IR Drop**
  - 2 levels dice-able for complete power study
    - Top IO (400 μm) + power rails (200 μm) : full testability at the test board
    - Only with power rails:
      - Extra power path; extra bias connection make the resistance half
    - Can be fully diced, 600 μm smaller in height



TaichuPix-3



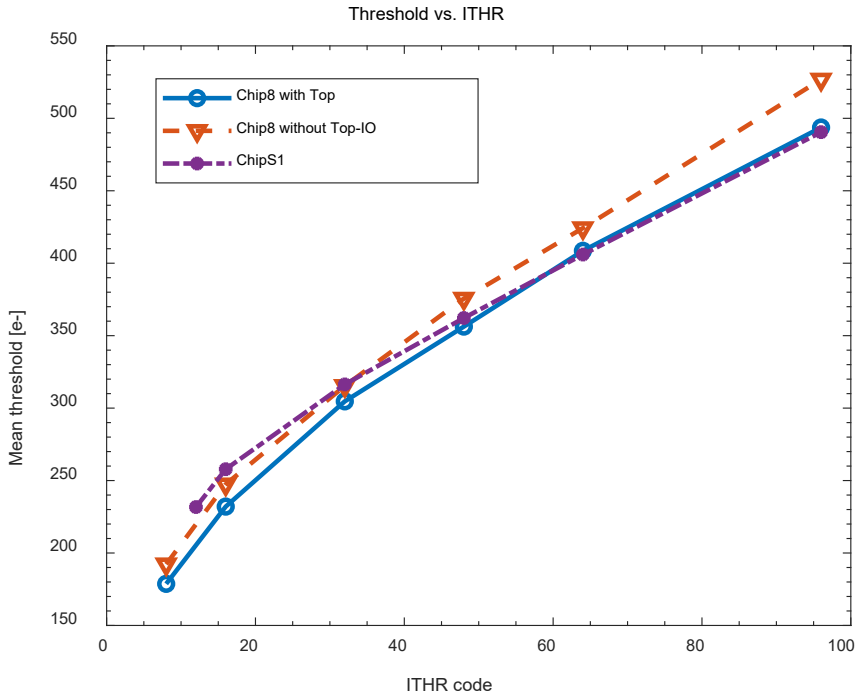
- **Chips without top-IO work normally thanks to good power net arrangement**

Threshold and noise of TaichuPix-3

- **S-curves measured for different chips**

	Mean threshold	Threshold rms	Mean noise	Noise rms
Chip8 with top IO bonding	310.4 e	48.8 e	21.1 e	4.8 e
Chip8 without top bonding	316.2 e	48.1 e	21.4 e	4.8 e
ChipS1 (no top-IO)	304.6 e	41.0 e	19.3 e	4.4 e

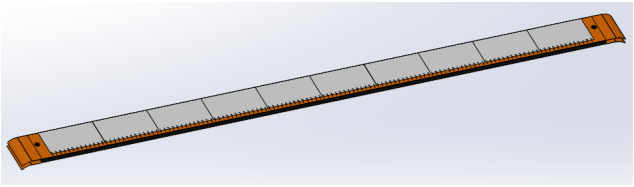
- **Top-IO has minor effect on threshold and noise**
  - Minimum mean threshold need to be further verified with more chips
  - Cluster size test with a ^{90}Sr on-doing



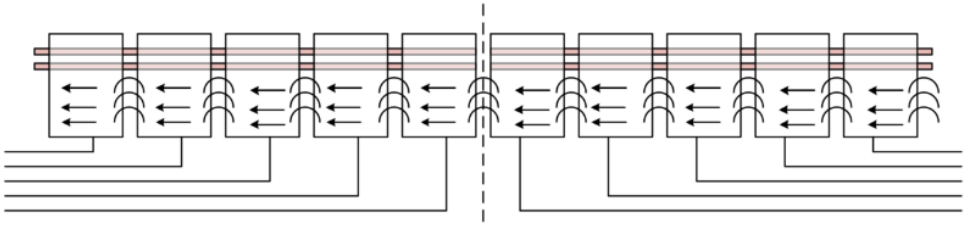
Detector module (ladder) R&D

- **Completed preliminary version of detector module (ladder) design**
  - Detector module (ladder) = 10 sensors + flexible PCB + support structure + control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB

3D module of the ladder

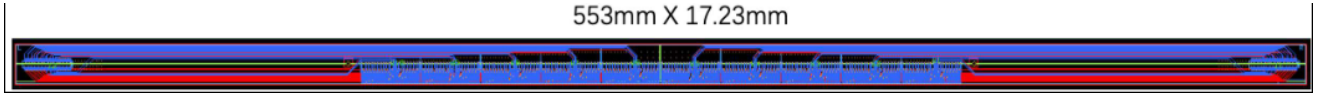


Schematic of ladder readout



Double sided ladder
10 sensors/ladder side, read out from both ends

Flexible PCB design



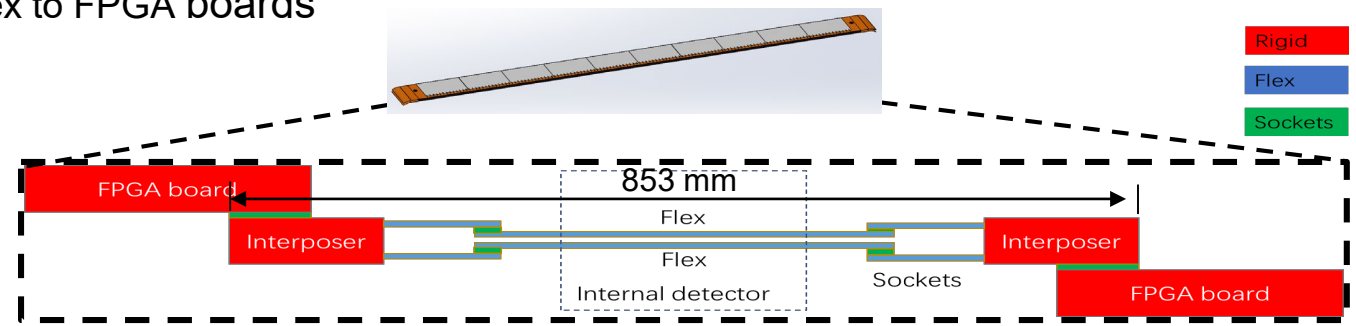
Profile of flexible PCB

	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

Ladder readout design

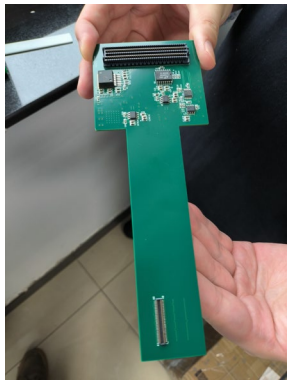
- **Flex board**
  - 1st version produced, glue and wire bonding performed at IHEP with dummy chips
  - 2nd version submitted (2-layer version and 4-layer version)
- **Interposer board**
  - First version ready (rigid PCB)
  - Connecting flex to FPGA boards

Detector module (ladder) prototype

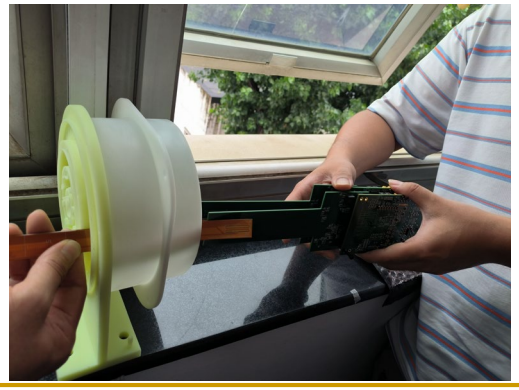


Dummy TaichuPix-3 bonded to the flex board

Interface board



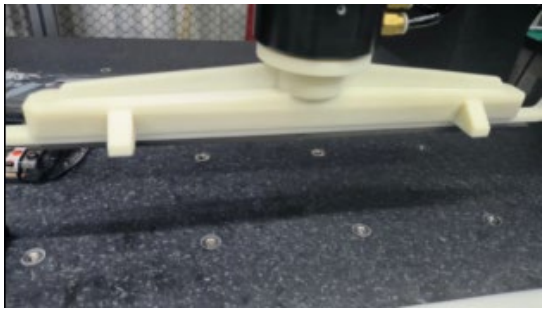
Ladder readout in vertex detector mockup



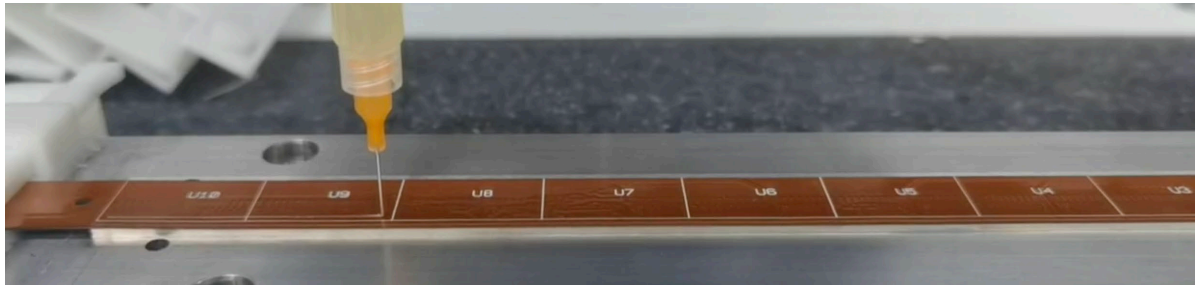
Detector module (ladder) assembly

- **Ladder (double side)= 20 ASIC chips + two flexible PCB + carbon fiber support**
- **Ladder assembly procedure verified with dummy ASIC (glass) using gantry**

New pickup tools



Dummy ladder glue automatic dispensing using gantry



Ladder on wire bonding machine

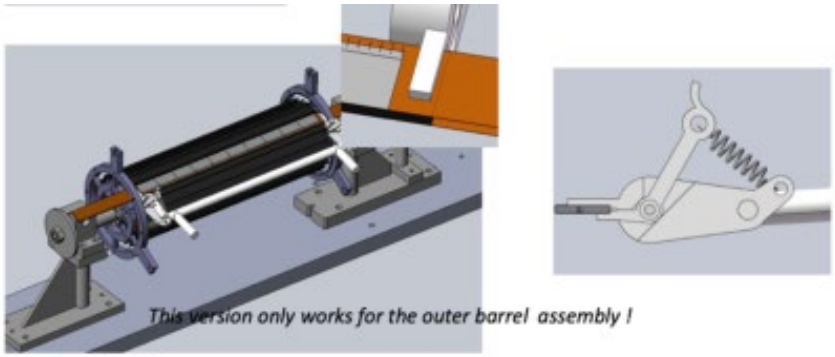
Dummy Ladder on holder

Tooling design for barrels assembling

- Ladder installation procedure designed
- 3 sets of tooling for 3 layer of barrel assembling
- Tooling and special tool for inner and middle barrels assembling

Installation procedure

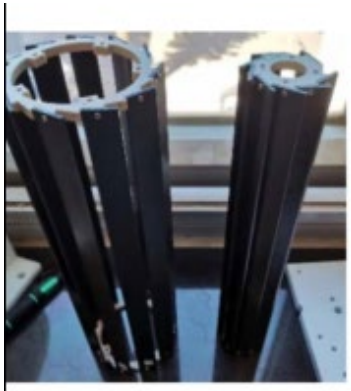
Tooling for installation

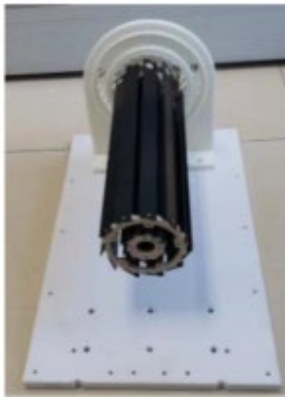


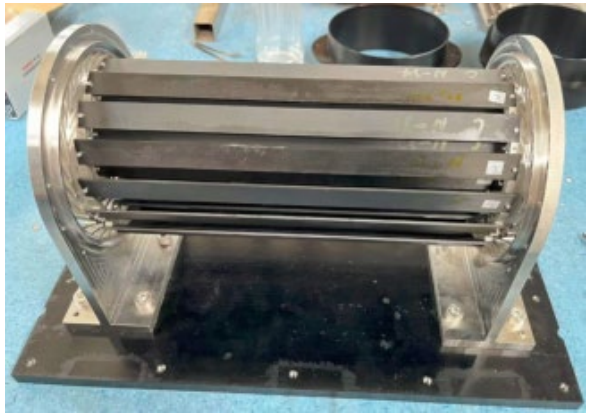
Vertex detector prototype assembly procedure

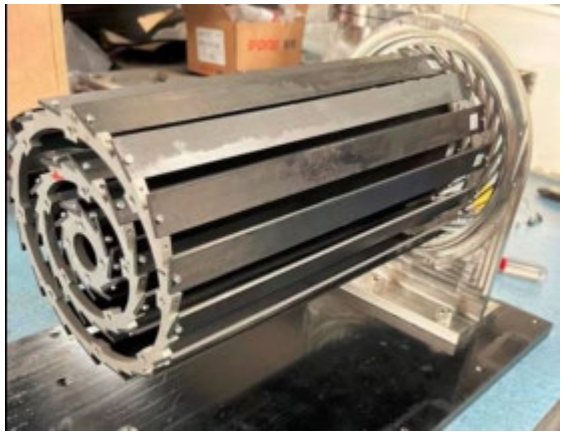
- **Mockup with 3D printing production done**
  - Assembly with 3D mockup model verified the installation procedure
- **Production with aluminum machining done**
  - Assembly will be performed at IHEP early Oct

Prototype support with aluminum machining



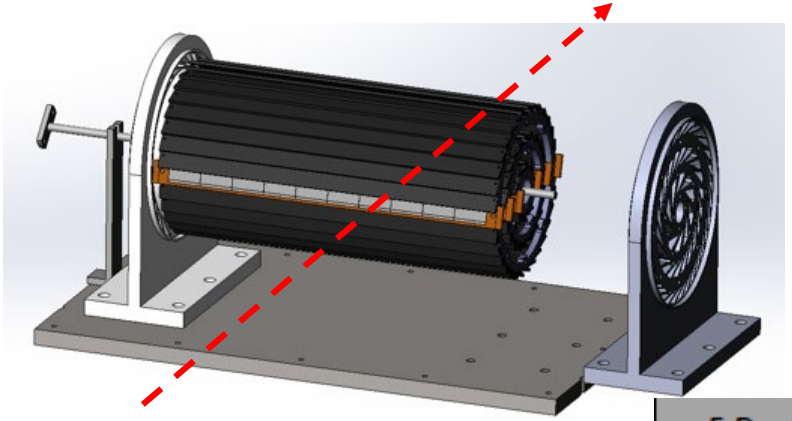






Plan for test beam

- **Plan to perform beam test at DESY in December this year**
  - 3-7 GeV electron beam
- **Rehearsal testbeam at Beijing Synchrotron Radiation Facility (BSRF)**
  - 1~2 GeV electron beam
- **Plan to install 6 real ladders on prototype**
- **Plan to install all the carbon fiber support structure for full vertex detector**
- **Beam is shooting at one section of vertex detectors**



Electron beam

	DESY	IHEP E3 beam	BSRF
Momentum	1-6 GeV	<1 GeV secondary beam	1~2.5 GeV
Particles	electrons	Protons/ Pions/ /Electrons	electrons
Trigger rate	4000 Hz/cm²	0.6 Hz/cm²	~50 Hz/cm²

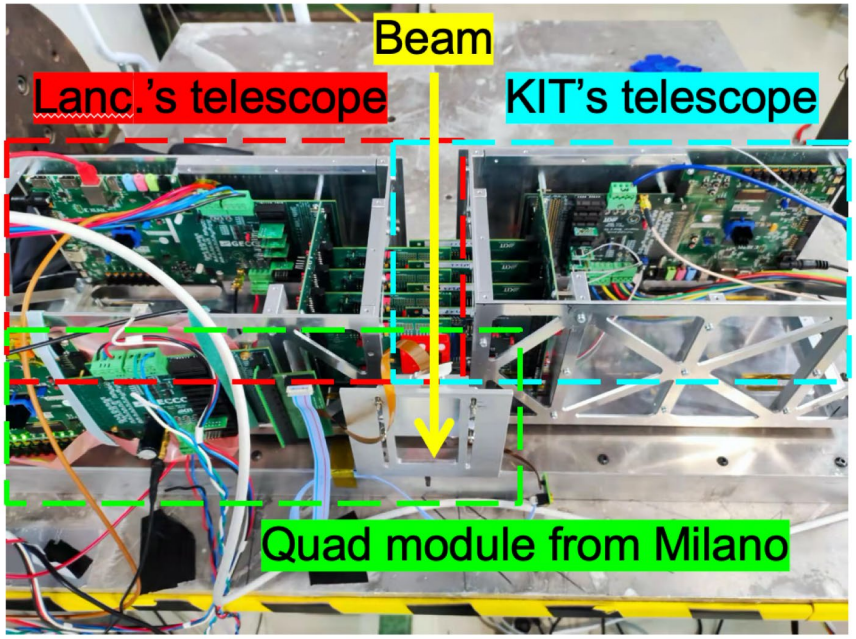
5-Dec-22	49		CMS-InnerTracker	X
12-Dec-22	50		CEPC Vertex	X
19-Dec-22	51	Beam till 22/12 0800	CEPC Vertex	X
26-Dec-22	52			

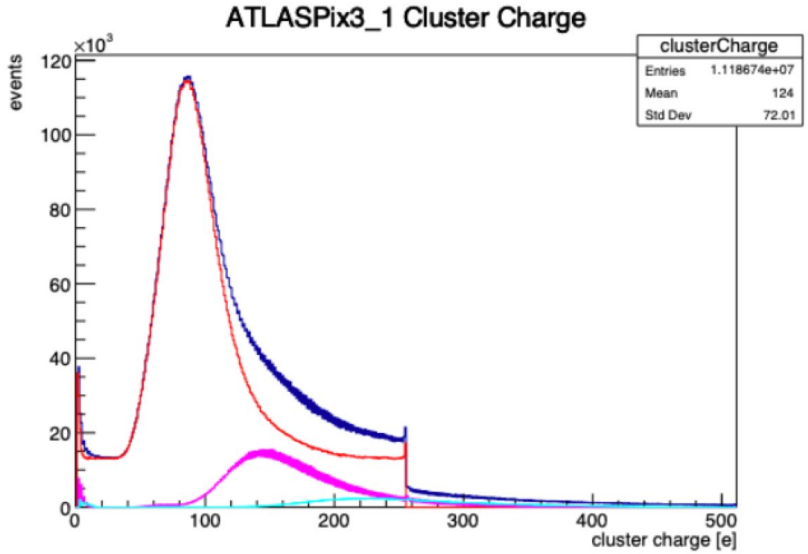
Summary and outlooks

- **Development of JadePix series towards the baseline requirements of CEPC vertex detector**
  - JadePix3: excellent noise performance; spatial resolution reach the requirement in one direction
  - Jadepix4/MIC5：a complementary design to the JadePix-3, to complete the R&D for the double-sided concept
- **Large-scale sensor chip (TaichuPix-3) from engineering run ready**
  - Detector module (ladder) assembly in progress
  - Full vertex detector prototype assembly in process
  - Next major milestone
    - Test beam at DESY in December 2022
    - MOST2 project review meeting at Q2 2023
- In future, more advanced technology node (65/55nm CMOS) or new process techniques (3D-integrated devices or stitching) may significantly improve the performances of the design

Other activities not covered in this talk

- **SOI**
  - In the next talk
- **CEPC Tracker R&D on ATLASPix3**
  - Closely related to the talk on Mightytracker this afternoon
- **Open for wide international collaboration**





Provided by Yiming Li

Pixel sensor teams

- **JadePix-3/4**
  - IHEP: Ying Zhang, Yang Zhou, Zhigang Wu (graduated), Jing, Dong, Wenhao Dong/ USTC, Chunhao Tian/ USTC, Yunpeng Lu, Qun Ouyang
  - CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng (graduated), Anyang Xu (graduated), Sheng Dong, Hulin Wang, Xiangming Sun
  - SDU: Liang Zhang
  - Dalian Minzu Unv: Zhan Shi
- **TaichuPix**
  - IHEP: Wei Wei, Ying Zhang, Xiaoting Li, Jun Hu, Hongyu Zhang, Ziyue Yan, Jia Zhou, Jinyu Fu, Zhijun Liang, Joao Guimaraes da Costa
  - CCNU/ IFAE: Tianya Wu, Raimon Casanova, Sebastian Grinstein
  - NWPU: Xiaomin Wei, Jia Wang
  - SDU: Liang Zhang, Jianing Dong, Long Li

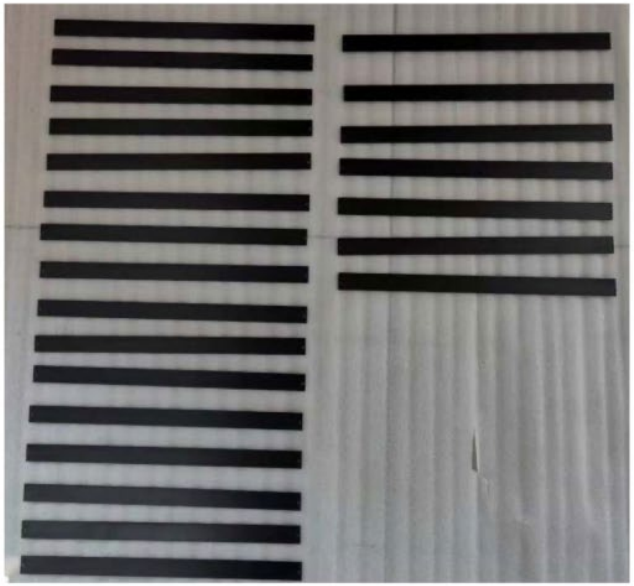
Thank you very much for your attention!

Backup slides

Support structure of the ladder

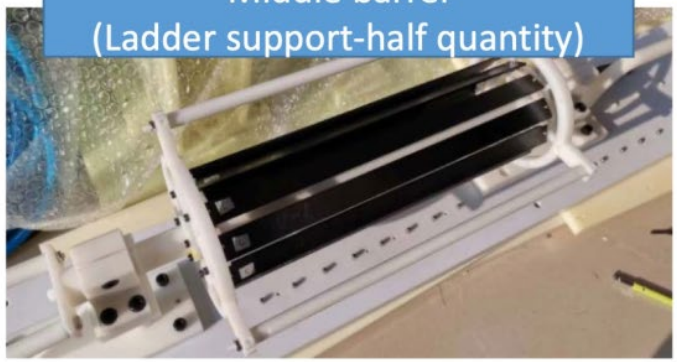
- **Production of ladder support with carbon fiber is in good progress**
  - Half of the ladder support has been produced
  - The yield of first batch of production is a bit low (~30%)
  - New batch of production has higher yield
  - Expected 120 good ladder support in this production

New batch ladder support



Inner barrel

Middle barrel
(Ladder support-half quantity)

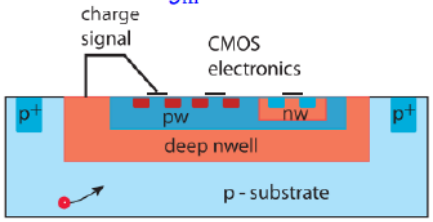


Planar monolithic - Depleted MAPS

Depleted MAPS/HVCMOS offer an alternative to hybrid sensors as timing detectors – aiming for better S/N

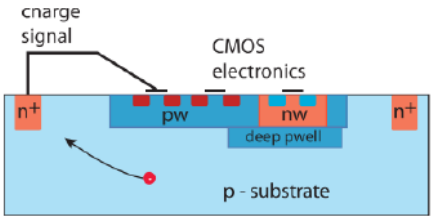
taken from N. Wermes

$\tau \propto \frac{C}{g_m}$, $ENC_{thermal} \propto \frac{kTC}{g_m}$ compensated by power (g_m)



- Large electrode: $C \approx 300$ fF
- Strong drift field, short drift paths, large depletion depth
- Higher power, slower
- Threshold $\sim 2000\,e^-$

σ_{wf} - small, σ_j, σ_{lf} - large



- Small electrode: $C \approx 3$ fF
- Low analogue power
- Faster at given power
- Difficult lateral depletion, process modifications for radiation hardness
- Threshold $\sim 300\,e^-$

σ_{wf} - large, σ_j, σ_{lf} - small

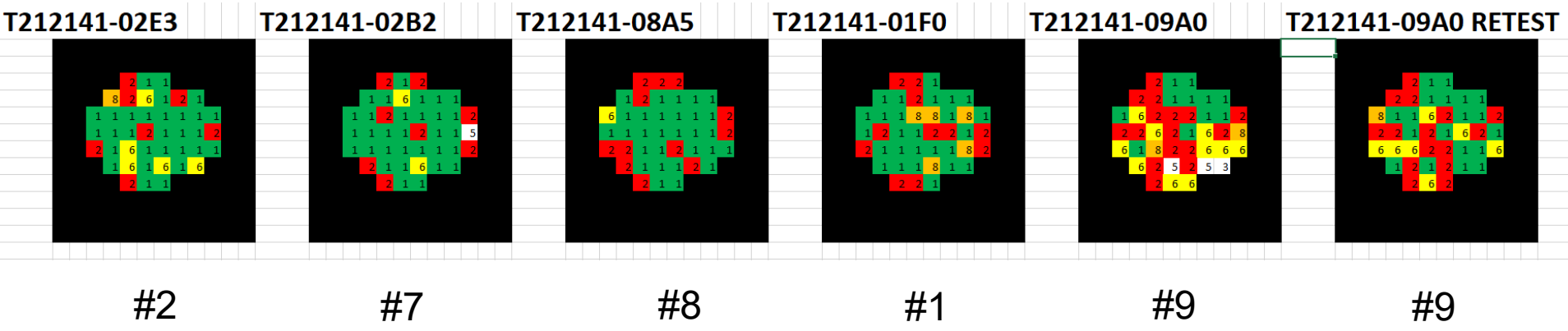
The limits set for the planar detector are still valid:
CACTUS D-MAPS *(Y. Degerlia et al. JINST 15 (2020) P06011)*

LFoundry-150 nm, high resistivity substrate
thickness=100 µm-> ~7500 e for m.i.p.
simulated channel noise ENC~ 300 e
τ_r~1 ns -> σ_j ~ 50 ps
σ_{wf}~0 (pixel of 1x1 mm^2)
σ_{lf}~40 ps

σ_t~65 ps -> also aimed by the designers (60 ps)

Wafer test result

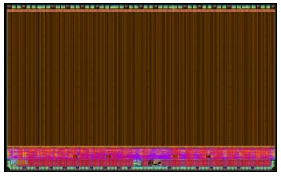
- **5 wafers tested**
  - Wafer #1-3 standard process
  - Wafer #7-9 modified process
- **It seems modified process wafer has a lower yield**
  - Substrate of modified wafer should be biased by a negative voltage, but not the case in the wafer test, may affect the result



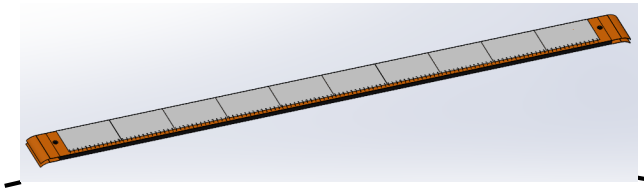
Ladder readout design

- **Detector ladder required for detector assembly**
  - Sensor chips, readout electronics, mechanical support, etc.

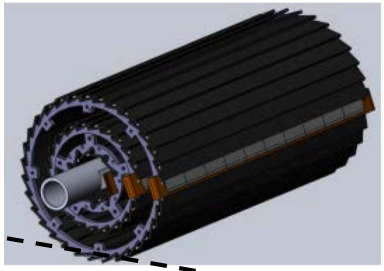
CMOS imaging sensor prototype

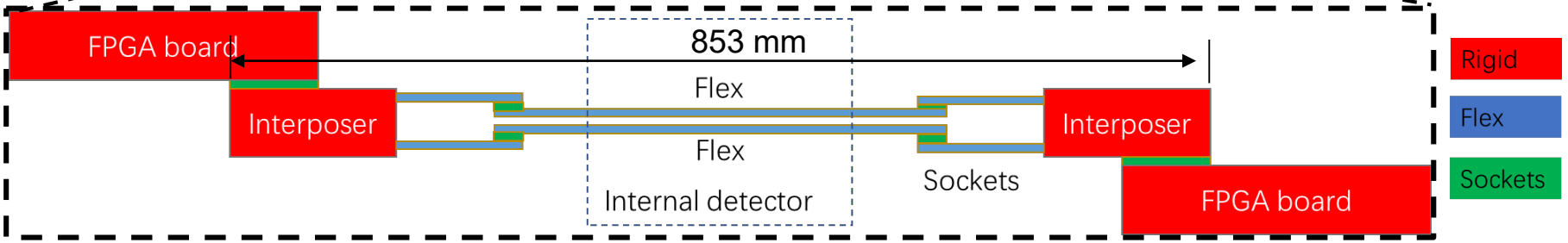


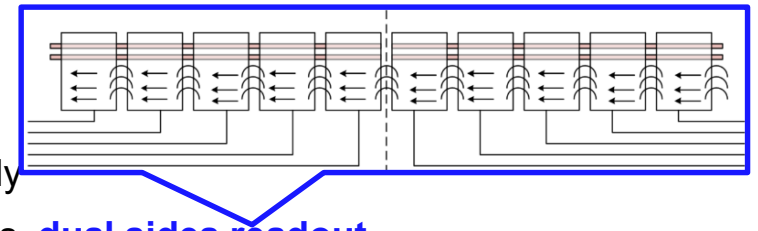
Detector module (ladder) prototype



Full size vertex detector Prototype



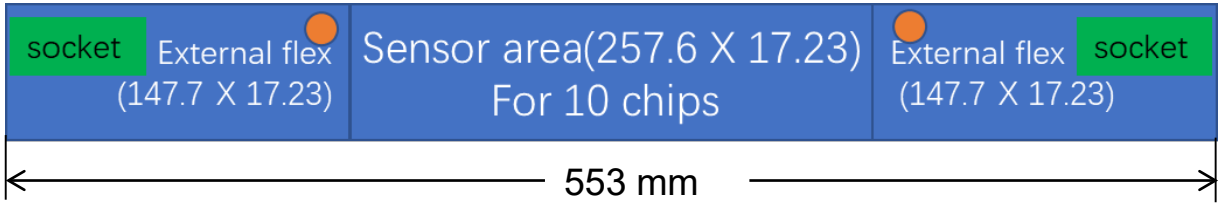




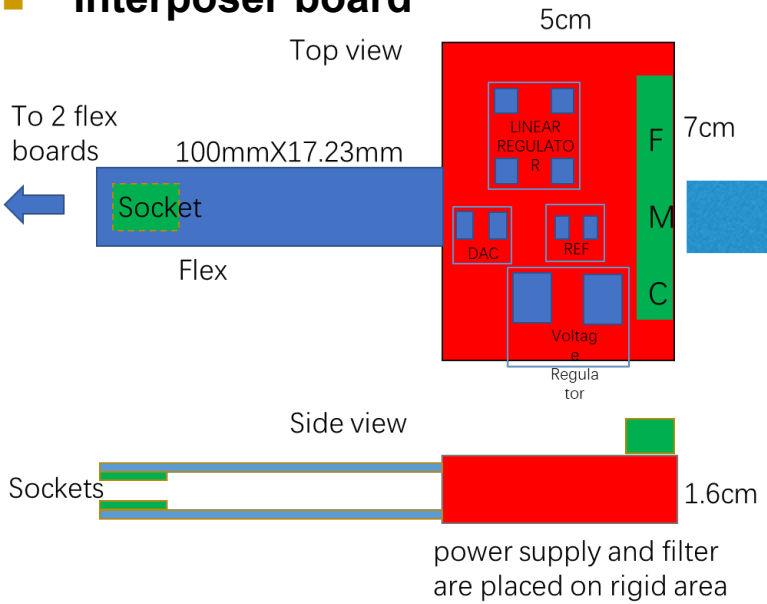
- **Ladder readout structure**
  - Containing 3 boards for easier production & assembly
    - Flex board：Assembled with 10 TaichuPix chips, **dual sides readout**
    - Interposer board：FMC mezzanine rigid and flex board, in production
    - FPGA board：FMC carrier board, available in the lab

Ladder readout design

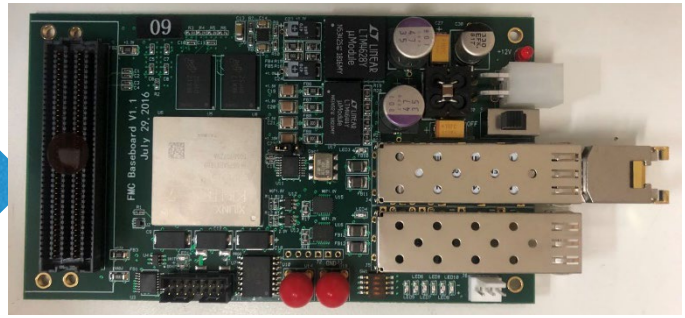
- **Two versions of flex board designed**
  - Version 1 (baseline): 2 layers, **less material**, limited layout space leads to **worse signal integrity**, thickness ~0.2 mm, in production
  - Version 2: 4 layers, **more material** dedicated GND and power plane gain **better signal integrity,** thickness ~0.4 mm, production done



- **Interposer board**



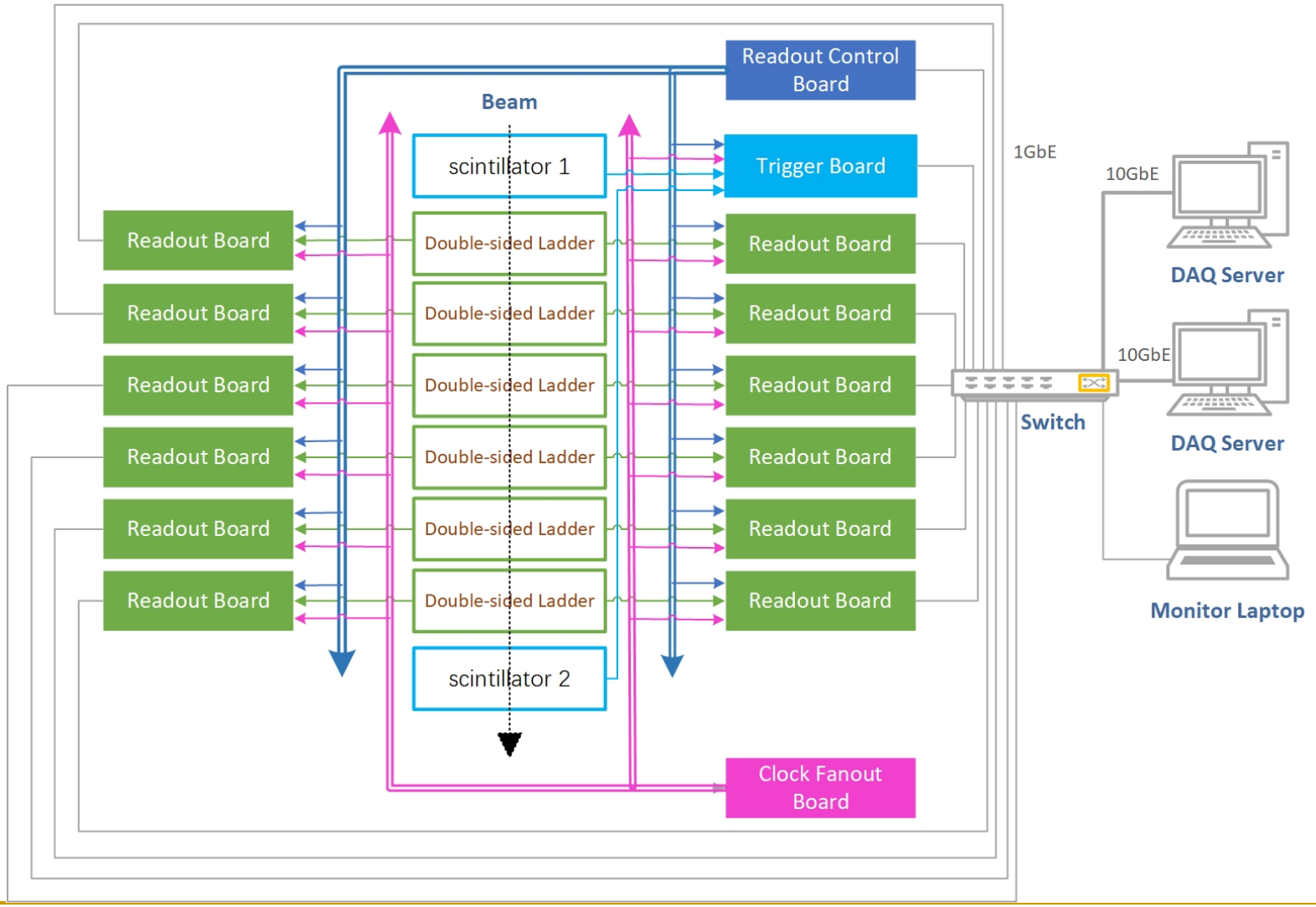
- **FPGA board**



  - Communication with chips
  - Data processing and package data
  - Readout to PC via 1Gbps Ethernet
  - Capability of 6 Gbps readout and 2GB internal DDR memory

Design of DAQ

- **Considering 6 double-sided ladders**



MOST2 project requirements on pixel chip

Silicon Vertex Detector Prototype – MOST (2018–2023)

Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
- Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program

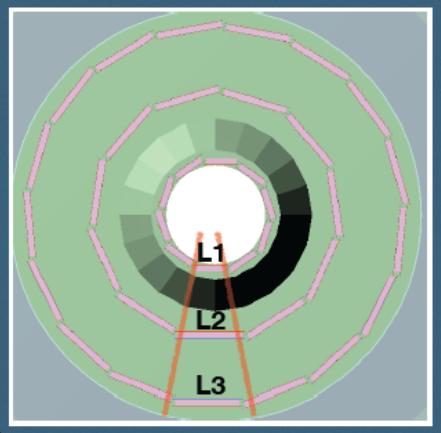
Double sided ladder

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm

3 X 2 layer = 6 chips

Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

3-layers
same size
same chip

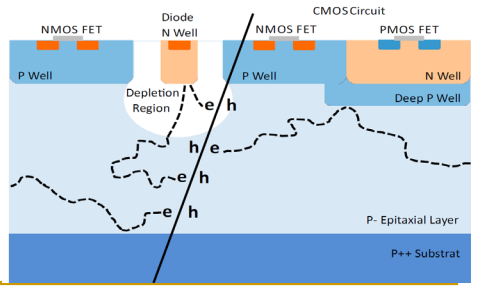
Goals:
1 MRad TID
3-5μm SP resolution

Integrate electronics readout

Design and produce light and rigid support structures

8

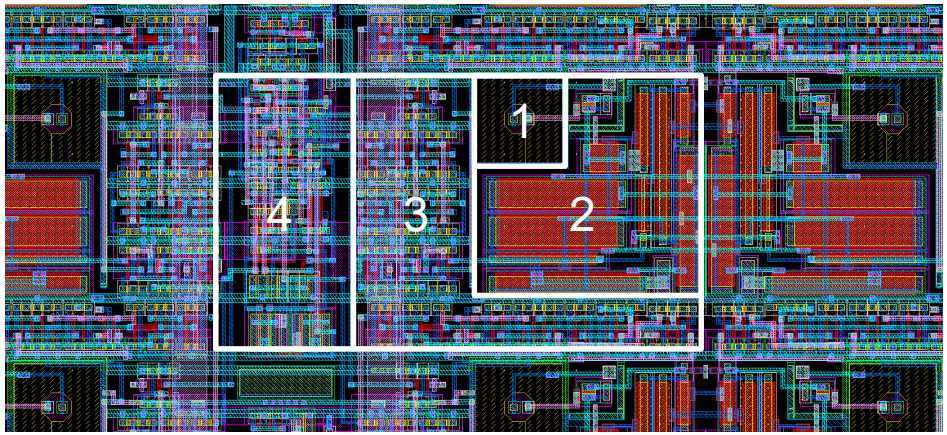
- **Motivation for TaichuPix chip design**
  - Large-scale & full functionality pixel chip
  - Fit to be assembled on ladders with backend Elec. & DAQ



CMOS pixel sensor

Design of JadePix-4/MIC5

- **Key component verified and reused from JadePix-3**
  - Diode
  - Analog frontend
  - Hit register
- **Asynchronized Encoder and Reset Decoder (AERD) ***
  - Generating col. and row address from hit pixel
  - Tracing back to reset hit pixel
- **Final layout of pixel matrix**
  - pixel array: 356 row × 498 col.
  - Pixel size: 20 μm × 29 μm

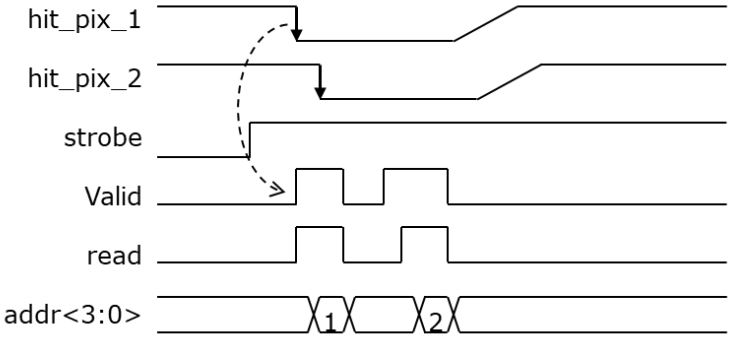


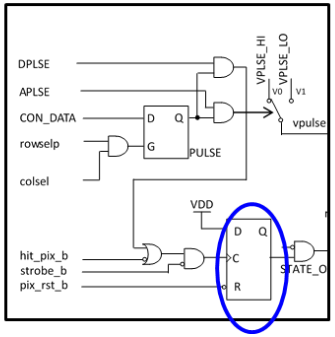
JadePix-4 pixel layout
(MET4 and above not shown)
1. Diode
2. Analog frontend
3. Digital logic
4. AERD shared by 2 col.

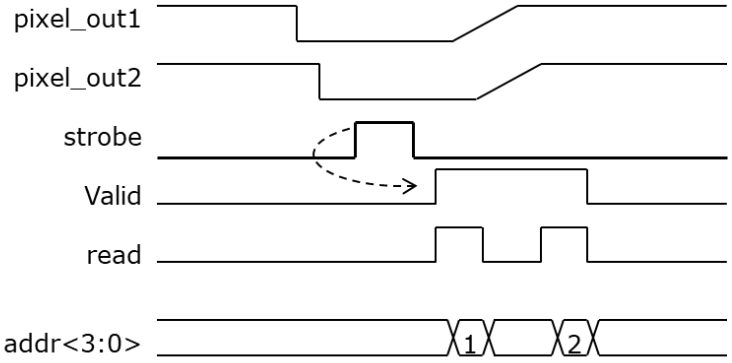
*P. Yang, etc., NIMA 785 (2015) 61-69

Readout of JadePix-4/MIC5

- **Triggerless mode**
  - Global gate signal, **strobe==1**
  - All hits registered at their leading edge
  - 0.2 hits/μs per double col. with the estimated hit density of inner most layer
  - Occupancy 0.02% @ integration time = 1 μs
- **Trigger mode**
  - Global gate **controlled by trigger signal**
  - Hits registered only when overlapped with a trigger (analog buffer)
  - Capable to handle very high hit density with a dead time for readout, 50 ns/hit







Layer Stackup

- Option1 （baseline）
  - 2 layers
  - Less material
  - limited layout space lead to worse signal integrity
    - Crosstalk
    - Large voltage drop
    - Ground bounce
  - Thickness: ~0.2mm （+0.1mm stiffener）

- Option2
  - 4 layers
  - Dedicated GND and power plane gain better signal integrity
  - More material
  - Thickness: ~0.38mm （+ 0.1mm stiffener ）
  - For study the ASIC chips and electronics performance

The design of the 2 options is similar， and the production has been started at the same time.