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R&D on the SOI technology for the vertex detector of CEPC

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On behalf of the SOI study group

from IHEP

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Outline

- Requirements of the CEPC Vertex detector
  - In perspective of the pixel sensors
- A floor planning in pixels
  - CPV-2, an explorer on the position resolution
- First trial with the SOI process + 3D integration technique
  - CPV-4, a principle prototype for 3D-SOI
- Summary & acknowledgements

Requirements of the CEPC Vertex detector

- Impact parameter resolution $\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}(\mu m)$
- Low occupancy < 1%
- Low material budget 0.15%/ X_0/layer

First detector layer at different colliding modes

Operation mode	H (240)	W(160)	Z (91)
Hit density (hits · cm^{-2} · BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%) (at 10 us)	0.08	0.25	0.23

Baseline design parameters

	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	0.15%/X_0
Layer 2	18	62.5	6	0.15%/X_0
Layer 3	37	125.0	4	0.15%/X_0
Layer 4	39	125.0	4	0.15%/X_0
Layer 5	58	125.0	4	0.15%/X_0
Layer 6	60	125.0	4	0.15%/X_0

Physics driven requirements → **Running constraints** → **Sensor specifications**

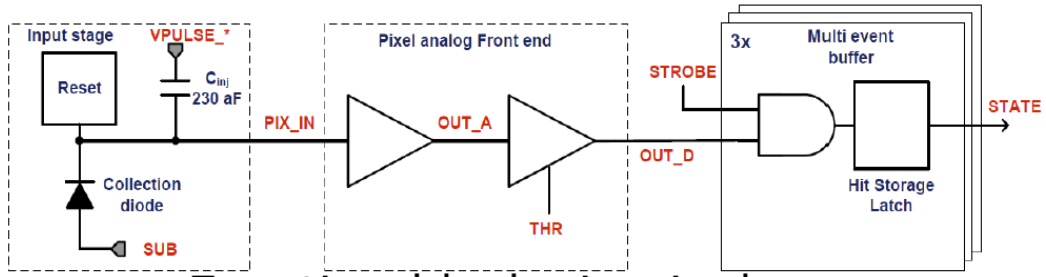
- $\sigma_{s.p.}$ (2.8um) → Small pixel (~16 μm), Thinning to (50 μm)
- Material budget (0.15% X_0/layer) → low power (50 mW/cm^2)
- r of Inner most layer (16mm) → Air cooling → low power (50 mW/cm^2)
- beam-related background → fast readout (~1 μs)
- radiation damage → radiation tolerance (≤ 3.4 Mrad/year, $\leq 6.2\times10^{12} n_{eq}$/(cm^2 year))

Pixel design: **contradictory** optimize direction

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

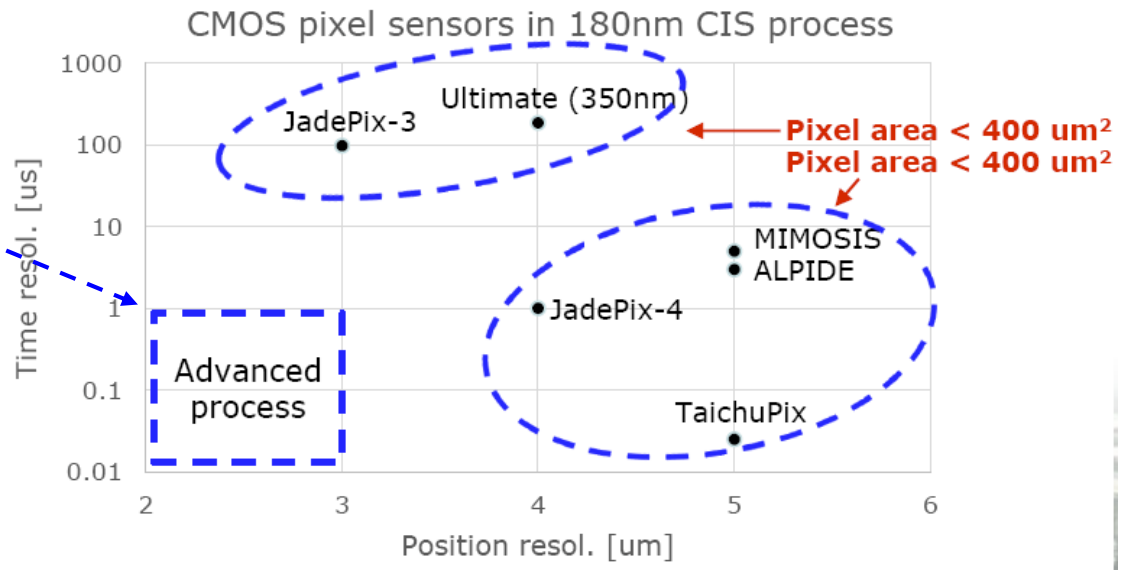
Trade off between Position resolution & Time resolution

- Rules of thumb concerning the pixel (learned from the R&D on 180 nm CIS process)
  - **Sensing diode + Analog FE**: 16×16 μm² = 256 μm²;
  - **Hit registers and logic gates**: 16×7 = 112 μm²;
  - **Readout structure:**
    - **Rolling shutter:** < 430 μm² ; (for Position resolution)
    - **Data driven:** > 580 μm²; (for Time resolution)
- More advanced process or new techniques to accommodate **more transistors (more functionalities)** within a pixel area < 400 μm² (e.g. 16×25)
  - 65nm CIS process
  - **200nm SOI + 3D integration**

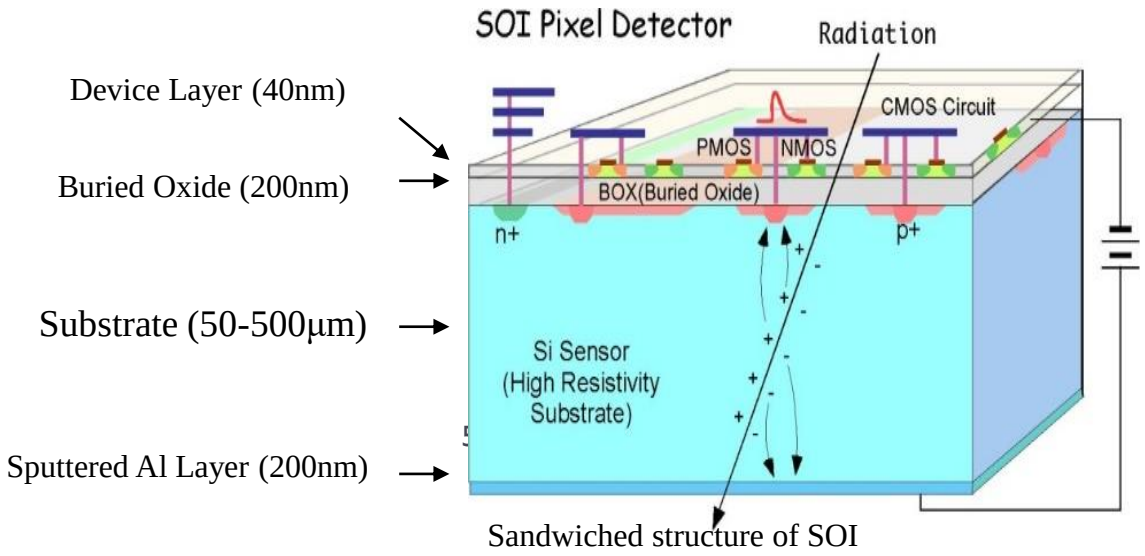


Function blocks in pixels

Name	Pixel size [um²]	Position Resol. [um]	Time Resol. [us]	Readout scheme	Pixel area
MIMOSIS	26.88x30.24	5	5	Data driving	812
ALPIDE	28x28	5	3	Data driving	784
TaichuPix	25x25	5	0.025	Data driving	625
JadePix4	20X29	4	1	Data driving	580
Ultimate	20.7x20.7	4	186	Rolling shutter	428
JadePix3	16x23.11	3	98.3	Rolling shuter	370



SOI Pixel Sensor



SOI: Silicon-on-Insulator technology

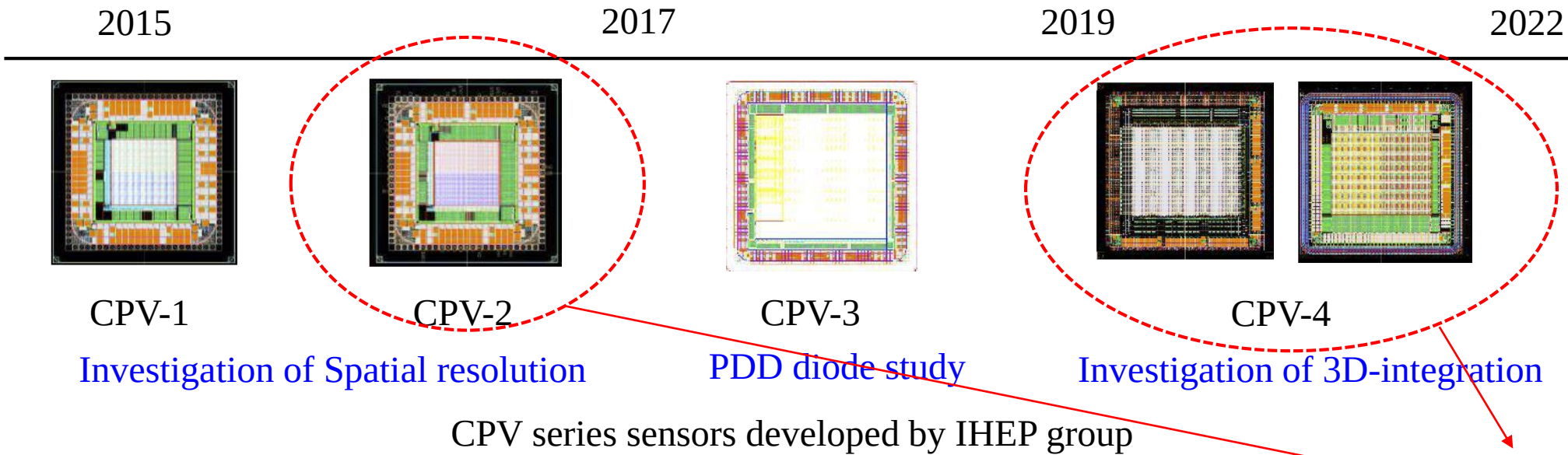
- Utilize 0.2μm FD-SOI CMOS process by lapis Semiconductor Co. Ltd.

SOI pixel detector: monolithic type detector

- **High resistivity** （>1 kΩ·cm），**thick** (50-500 μm) **sensitive layer**; *more signal charges, low material budget possible;*
- **Fully depleted** (high basing voltage > 100V possible); *fast collection*
- **Low power dissipation**
- **Almost no single event effects (SEE) probability**; *radiation tolerance*
- **Low cost**

A promising candidate to be used in high energy particle detection

R&D of SOI pixel sensor for Vertex (In China)



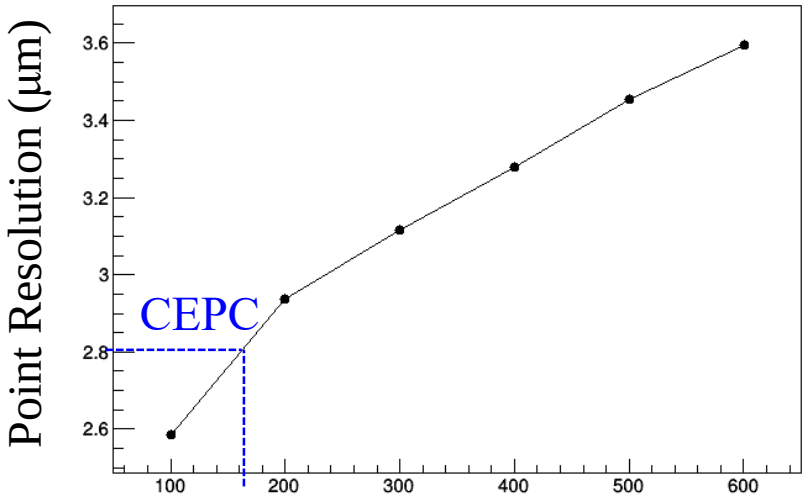
CPV series sensors developed by IHEP group

Design guideline in general: adopted 1-bit binary readout in pixel

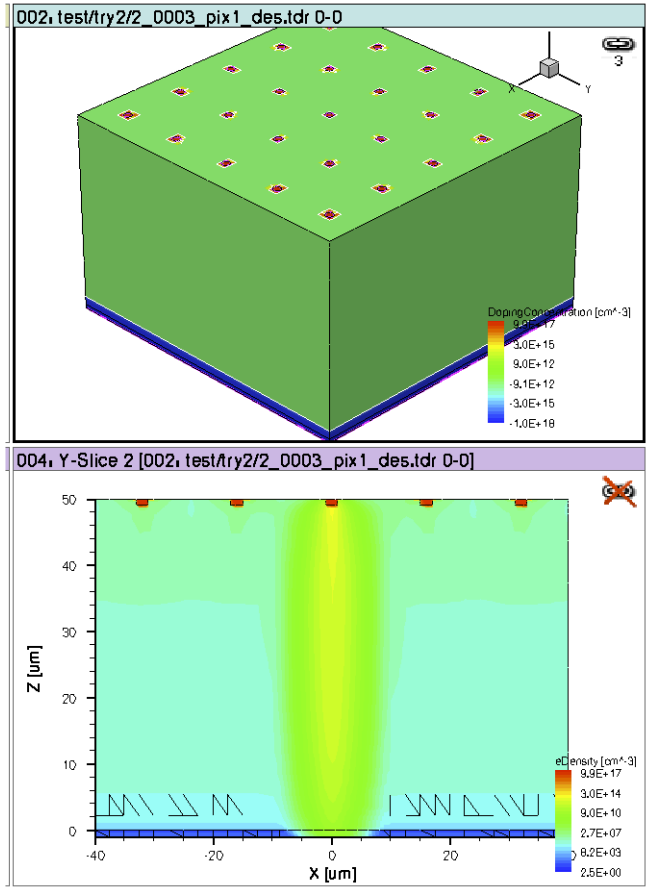
- Small pixel size to enable spatial resolution < 3μm;
- In-pixel discriminator to eliminate the excessive driven current;
- In matrix zero-suppression to minimize data load;
- Hit processing within ~1μs to keep low occupancy;

Investigation on the position resolution

- **16μm pixel pitch size** & **50μm sensor thickness**
- **Low threshold** is essential for the high position resolution
  - Threshold < 200 e-
  - ENC ~ 20 e-



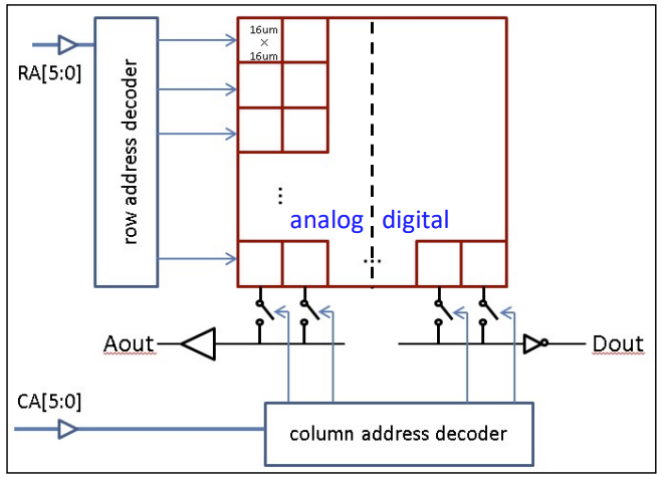
Threshold (e^-)

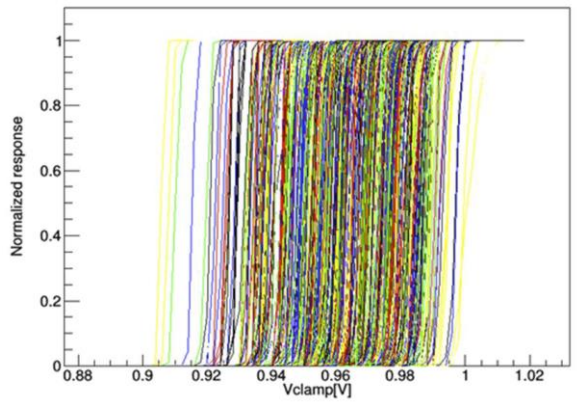


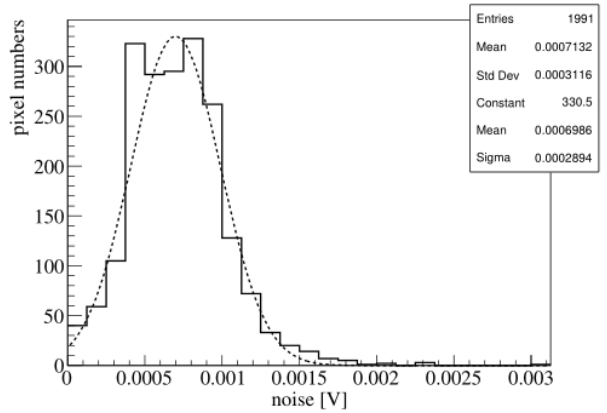
TCAD simulation of the charge carrier transportation

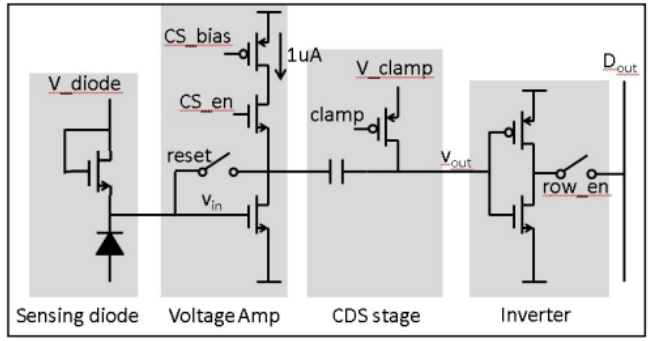
Investigation on the position resolution: CPV-2

- **CPV-1/2 dedicated to validate the simulation**
  - **Simplified in-pixel architecture to keep pixel pitch = 16 μm;**
    - Sensing diode + Analog FE + Inverter (as a discriminator);
    - No hit register or logic gate;
    - Rolling shutter readout of HIT state;
  - In-pixel CDS to **eliminate** the KT/C reset **noise**;
  - **Thinned to 75 μm** and characterized electrically;
    - Minimum threshold < 200 e^-, ENC = 6 e^-



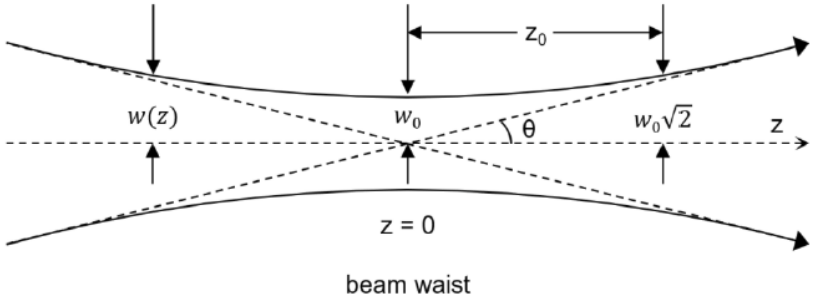


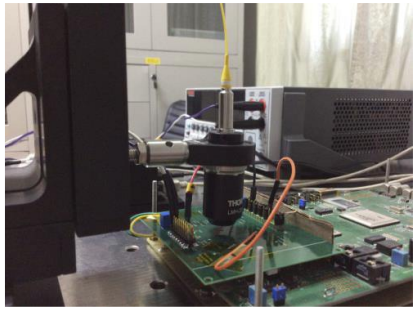


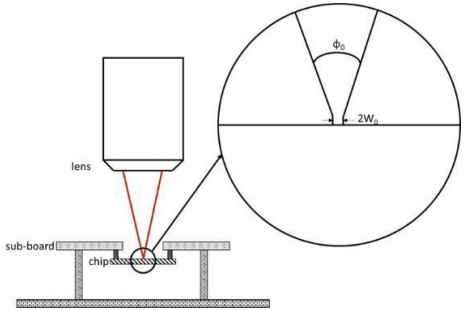


Investigation on the position resolution: CPV-2

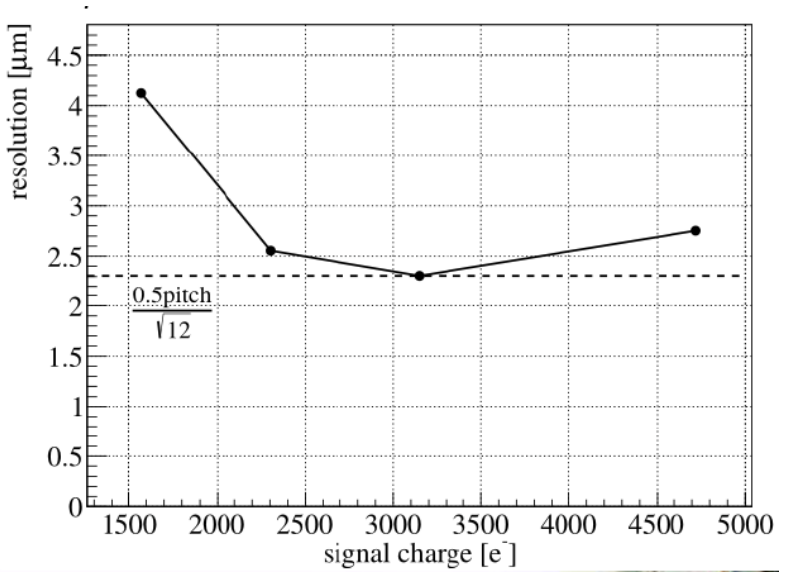
- Infrared laser test setup
  - Wavelength 1064 nm
  - Pulse energy adjustable 0 – 60 pJ
  - Focused to W_0 = 1.7 μm
  - 3-dimension motion stage, repeatable positioning resolution 1μm



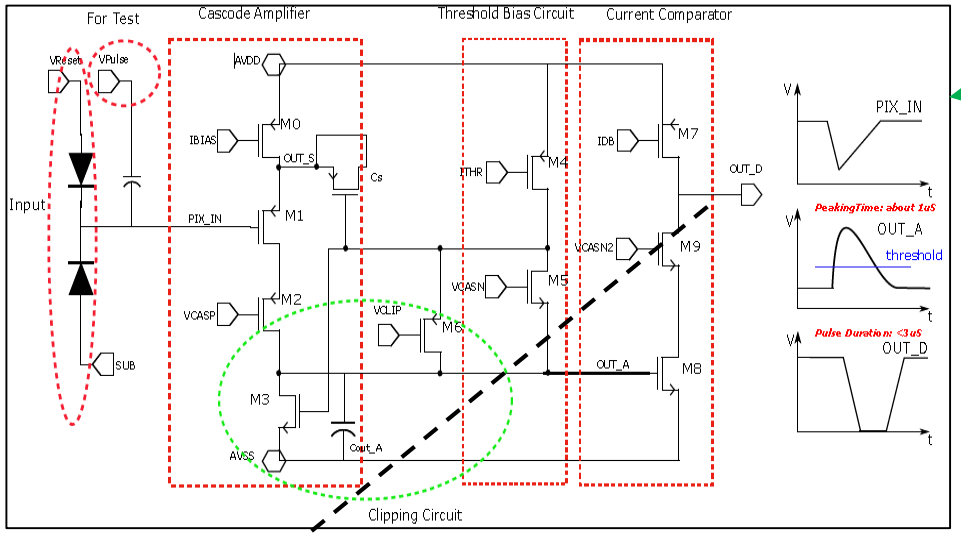


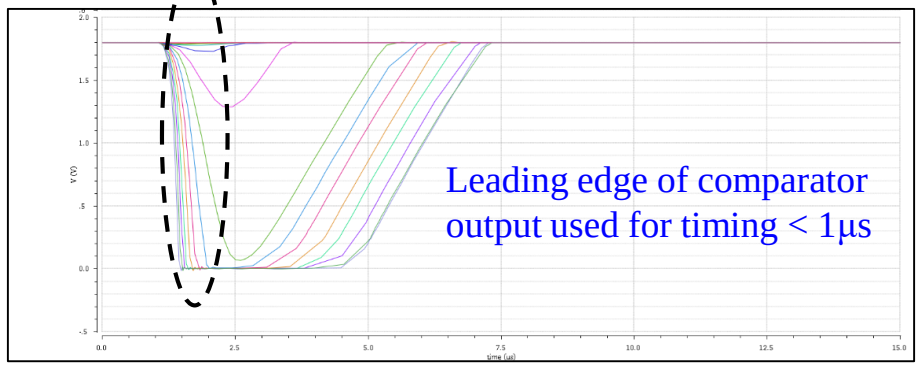


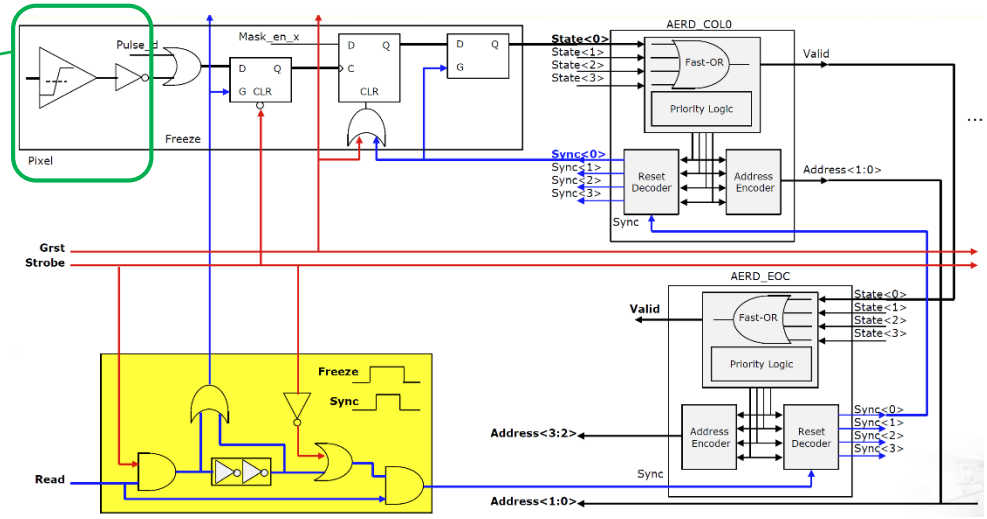
- The position resolution was related to the cluster size
  - Pixel pitch size, depletion, charge collection
  - Signal charge/ threshold optimized with threshold fixed to 200 e^-
- **Position resolution < 3μm achieved** with Pitch = 16μm, threshold < 200 e^-



CPV-4 architecture







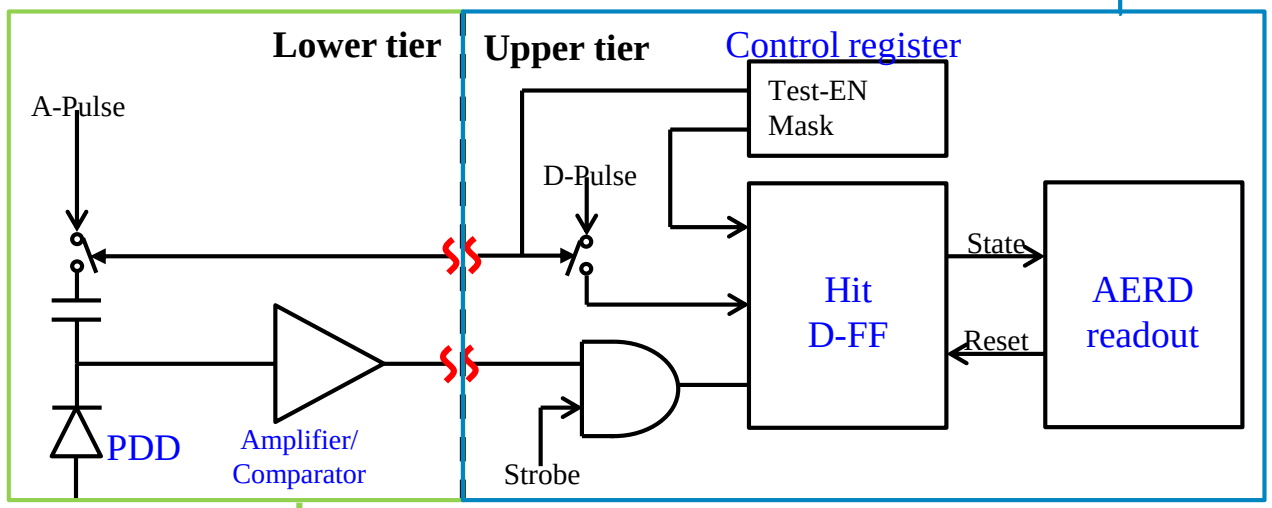
Data readout structure (simplified) of CPV4

*Ping Yang, NIMA 785 (2015) 61-69

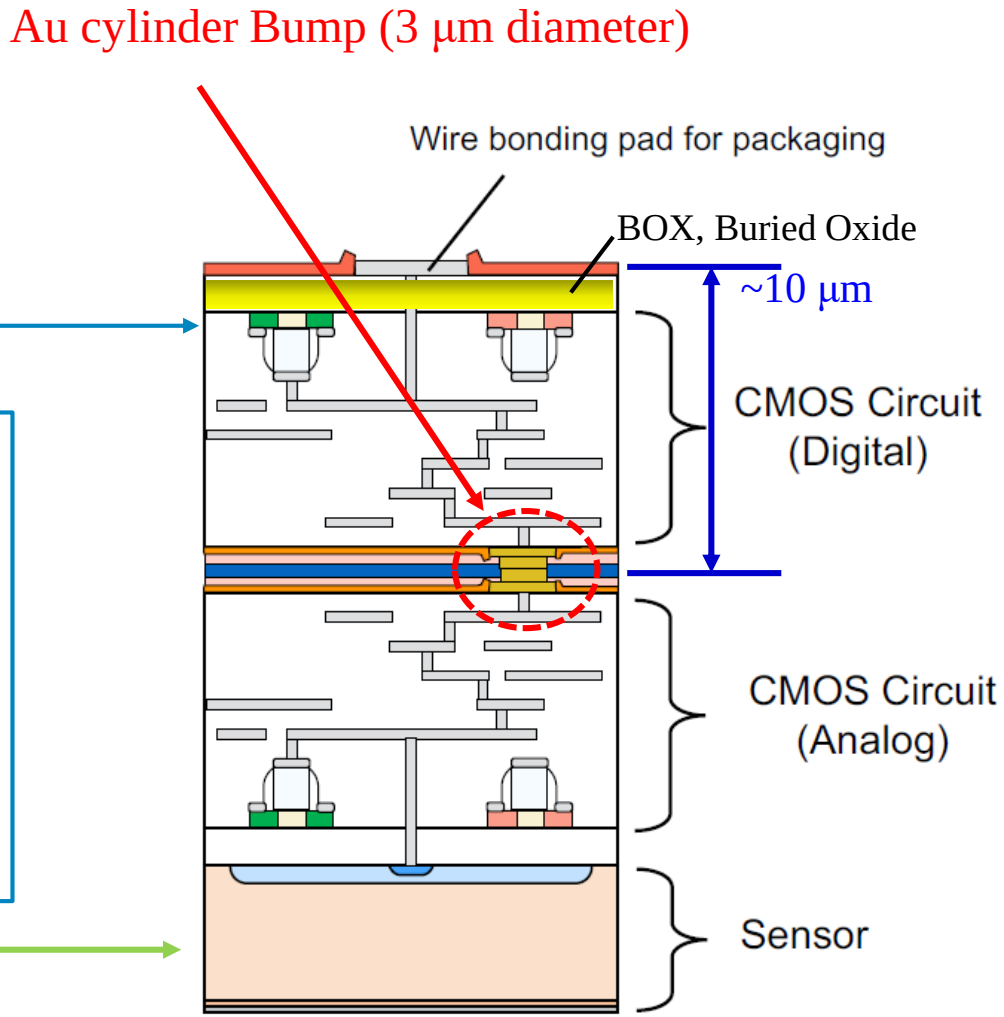
- Low power front-end:
  - Topology same as JadePix-3/4 (originally from ALPIDE);
  - Compatibility with PDD diode to be verified;
- Data-driven readout (Asynchronous Encode Reset Decode*)
  - Targeting time resolution < 1μs
- Pixel area targeting < 400 μm^2

CPV-4: 3D implementation

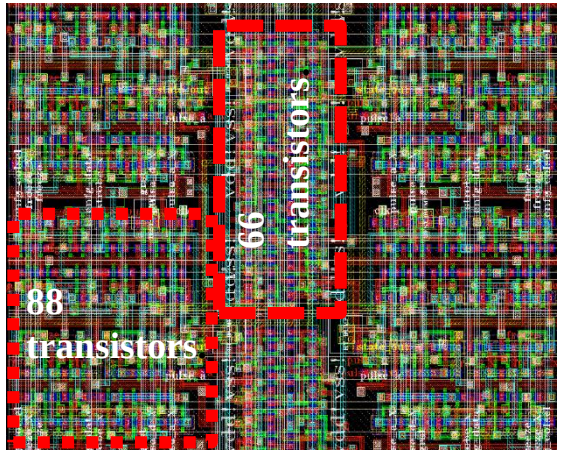
- Vertical integration of
  - Lower tier: PDD sensing diode + amplifier/comparator;
  - Upper tier: Hit D-Flipflop + Control register + AERD readout;
  - 2 Vertical connections in each pixel: comparator output and test switch;
- Pixel size: 17.2×21 = 361 μm^2
  - Resources of layout area and metal layers for routing ×2
- Thickness of the upper tier: ~ 10 um



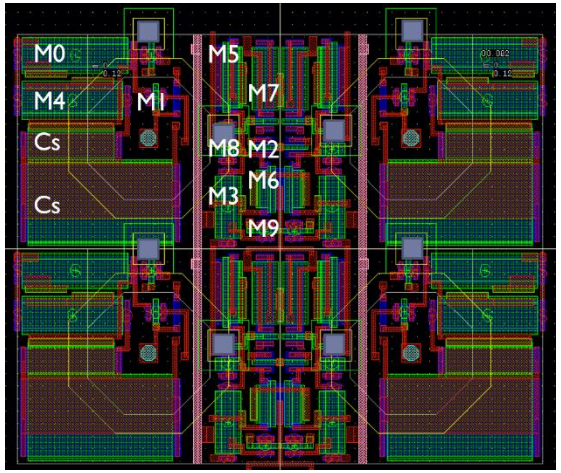
Division of upper and lower functionalities



CPV-4: pixel layout implementation

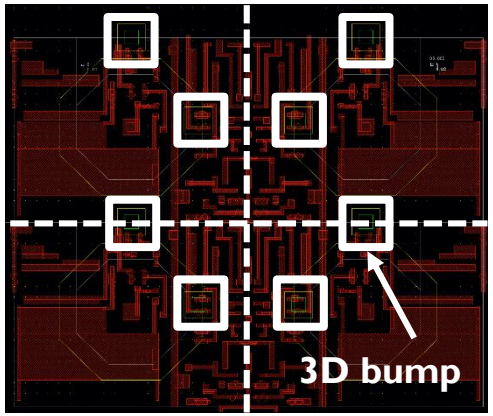


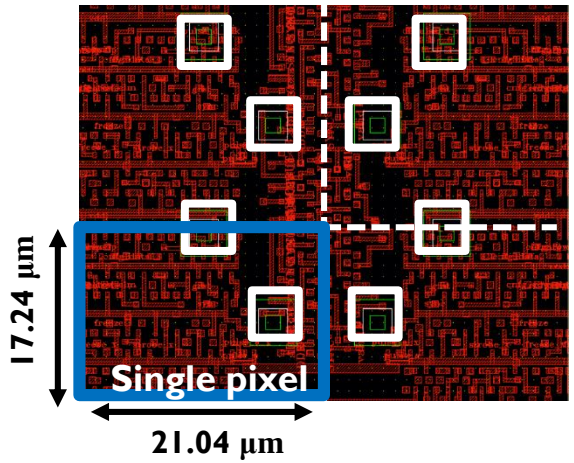
Layout of 2*2 pixels in upper tier



Layout of 2*2 pixels in lower tier

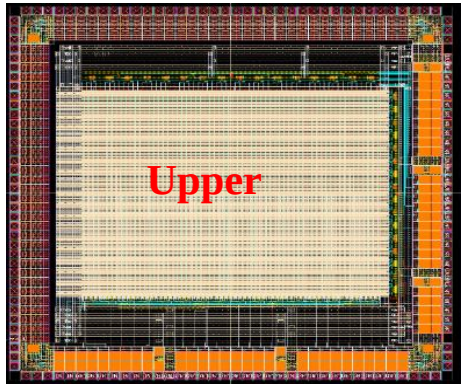
- A lot of efforts to minimize the layout size: 21.04 μm * 17.24 μm
  - Upper tier: 88 transistors for in-pixel control registers;
    66 transistors for a single stage of AERD;
  - Lower tier: Compromise between noise and transistor size;
    Y-axis mirrored, sensitive input node protected
    against the output node to minimize the crosstalk





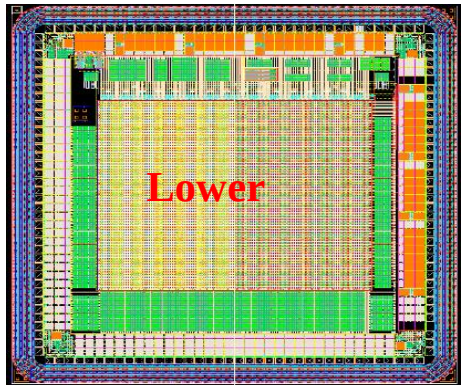
3D bump positions in 2*2 pixels of upper and lower tier (Metal_1 only).
2 bumps for each pixel (Comparator output & test switch)

CPV-4: upper and lower chips verified before 3D integration

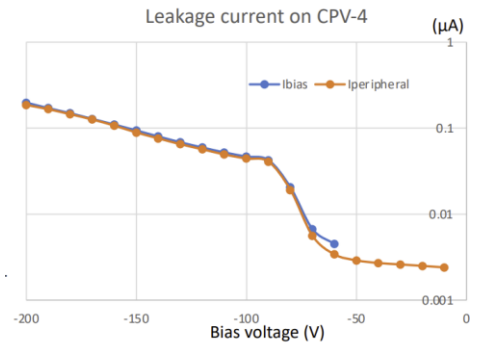


Pixel size	17.24×21.04 μm^2
Time resolution	~1 μs or ~3 μs in different operation mode
Pixel array	128×128
Chip size	4.5mm×4.5mm

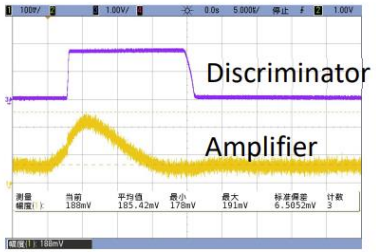
- Characterization of Upper and Lower chips separately
  - I-V curve of the sensor;
  - Waveform of analog Front-end;
  - Digital control and readout of the upper chip;



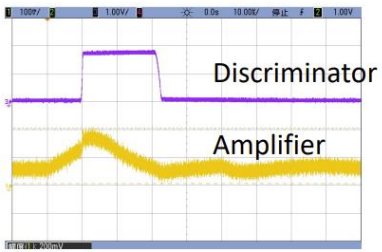
Layout of CPV4-3D



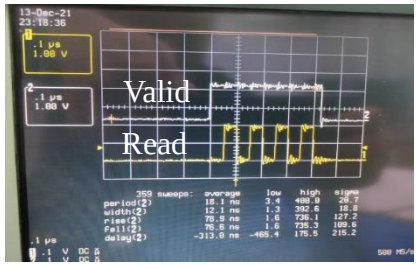
I-V response of the lower chip. Indicate the sensor can be biased at -200V.



Analog frontend w/o PDD
Test charge injected ~ 100 e$^-$



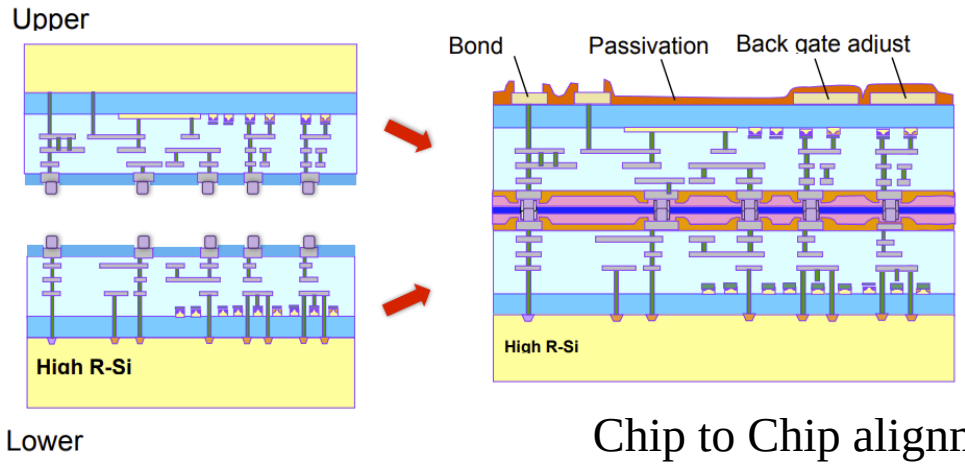
Analog frontend with PDD
Test charge injected ~ 750 e$^-$

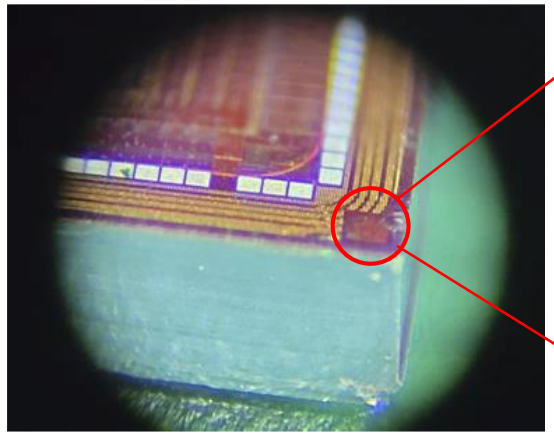


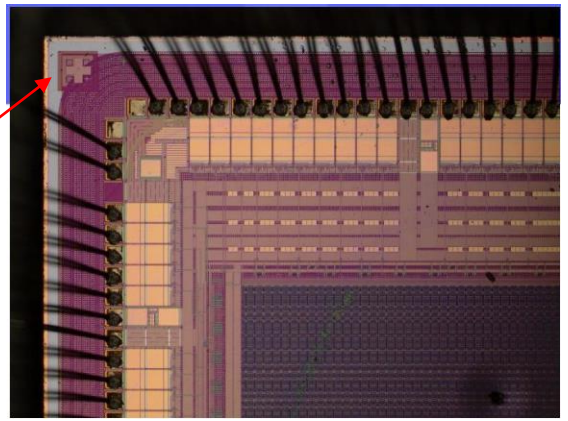
Output of the upper chip (Valid):
low -> High: test pulse injected to 4 pixels;
High ->Low: all the addresses of the 4 pixels readout (Read),;

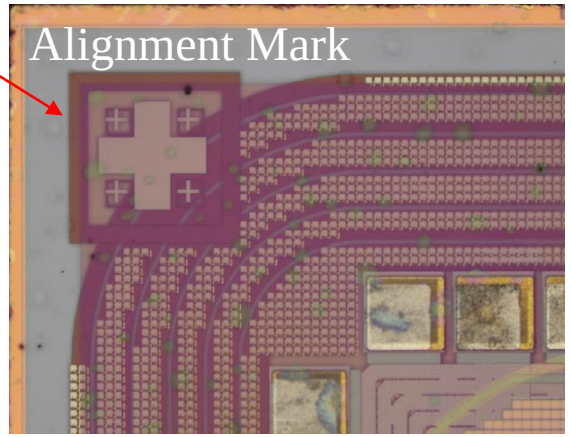
CPV-4: chip to chip 3D implementation

3D chips delivered in Aug. and Oct.

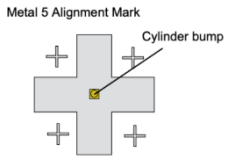


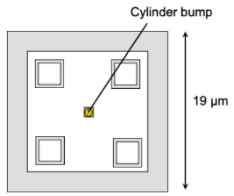


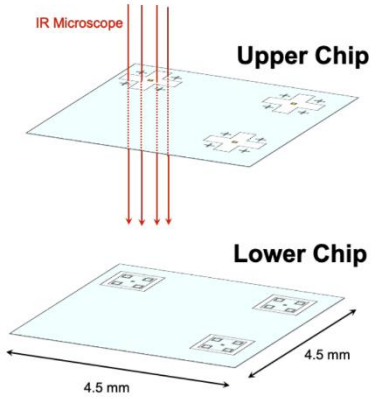


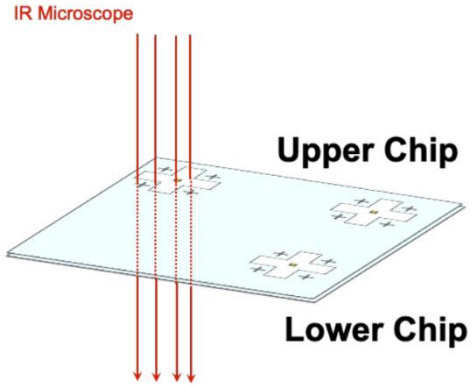


Chip to Chip alignment

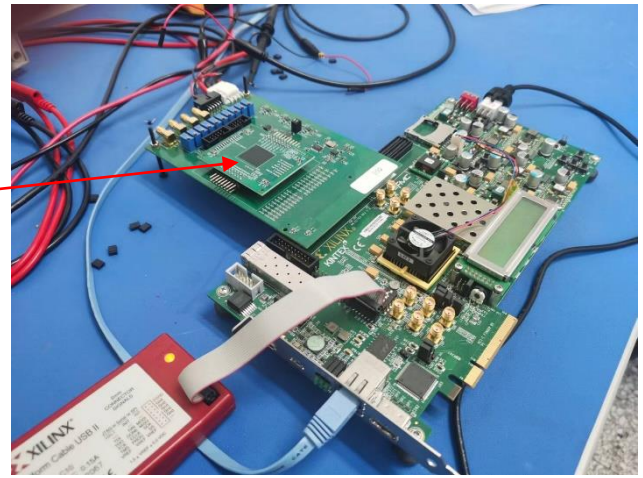






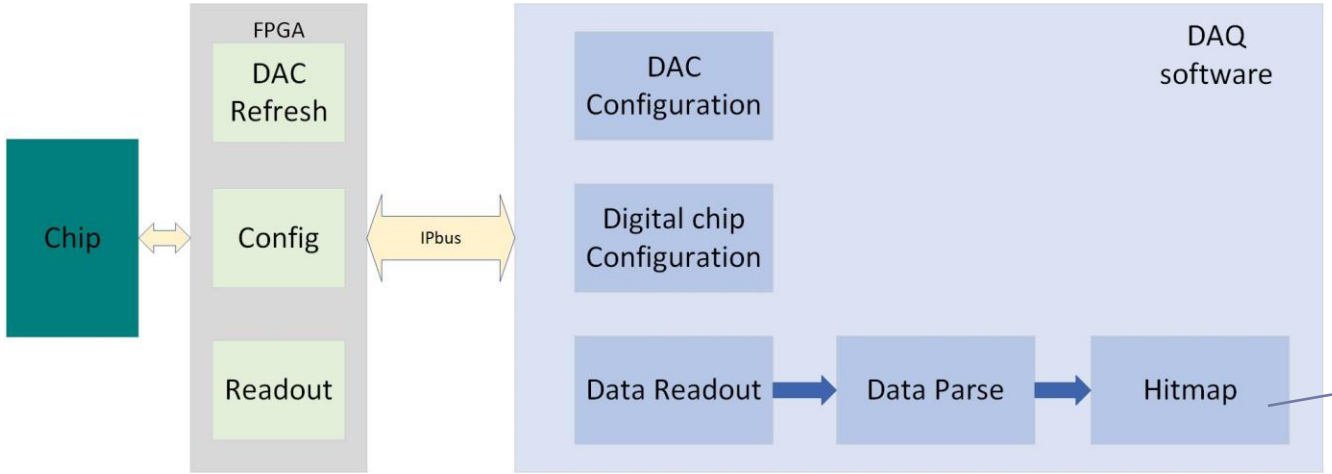


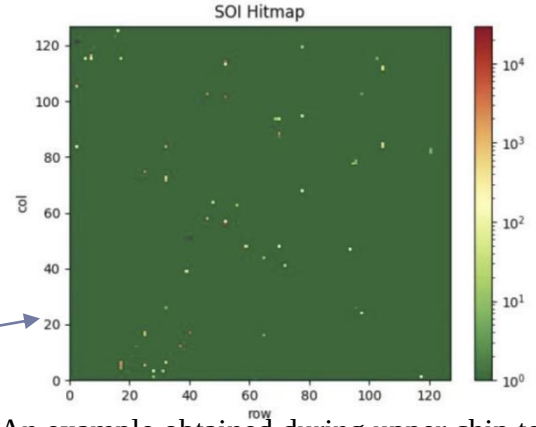
CPV-4-3D: ready for the 3D chips test



A test system is ready for the 3D chips tests:

- Firmware and DAQ system have been verified during the upper & lower tiers separate tests;
- Wire bonding has done on some **3D chips for conditioning**
- For the **formal 3D chips,** wire bonding and tests are underway;





An example obtained during upper chip test

Summary and Outlooks

- The position resolution < 3 μm is required by the physics programs at the CEPC experiments, along with
  - Time resolution < 1μs for low occupancy;
  - Low power consumption < 50mW/cm^2 for low material budget;
- Trade off between position and time resolution due to the pixel circuit floor
  - Pixel area < 400 μm^2 is critical for the position resolution;
  - More advanced processes than 180 nm, or new techniques needed;
- CPV-2 explored the position resolution of binary readout
  - Pixel size 16 μm × 16 μm, threshold < 200 e$^-$
- 3D implementation of the CPV-4 design, targeting Position and Time resolution simultaneously
  - Pixel size: 17.2 × 21 = 361 μm^2; Resources of Layout area and metal layers for routing × 2
  - Data driven readout: ~ 1 μs
- Recent progress on the 3D-SOI:
  - Upper and Lower chips have been characterized separately
  - Test on the 3D chips is underway

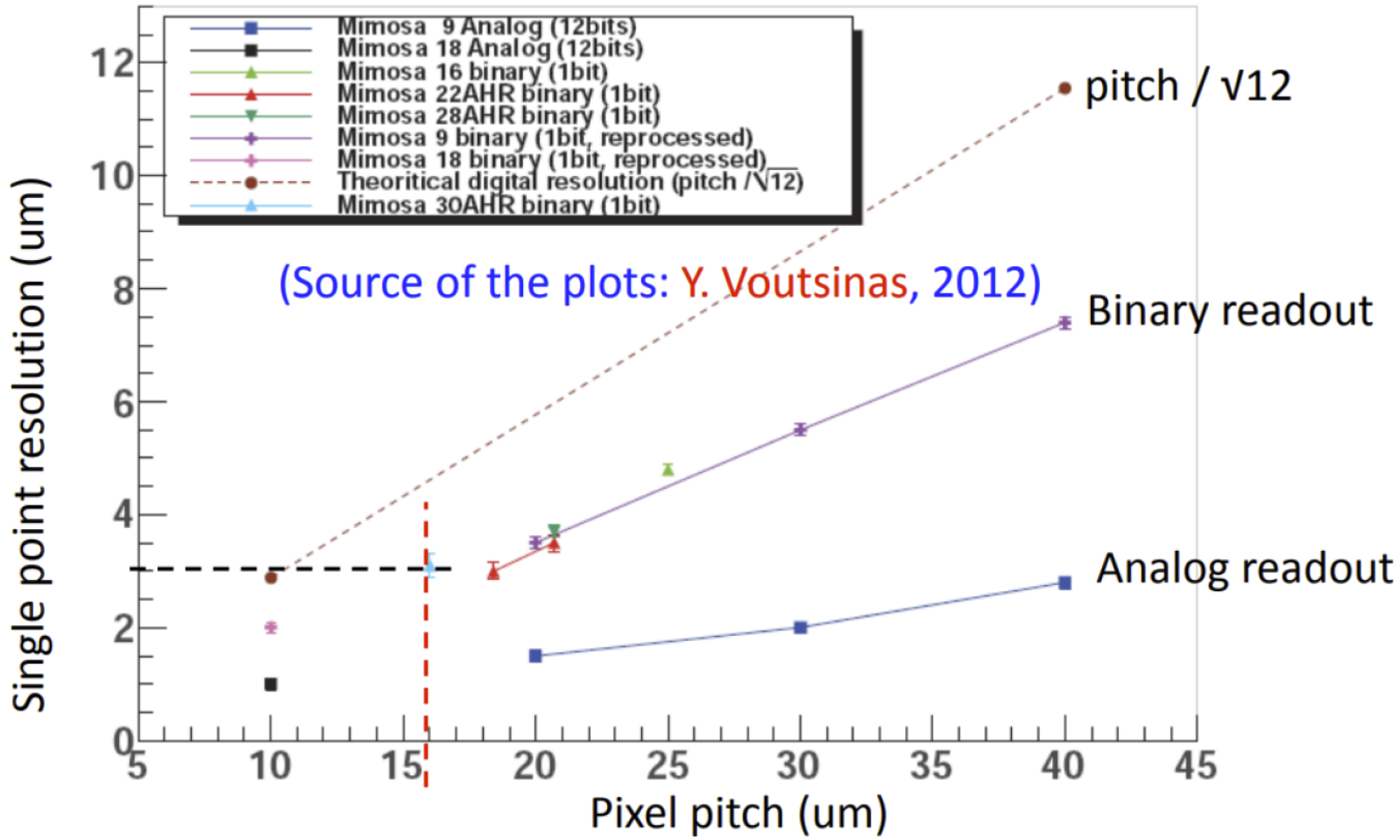
Acknowledgements

This work is supported by

- The National Natural Science Foundation of China (11935019, 11575220, 11375226);
- The State Key Laboratory of Particle Detection and Electronic, IHEP;
- The CAS Center for Excellence in Particle Physics (CCEPP)

Thank you for your attention!

Backups

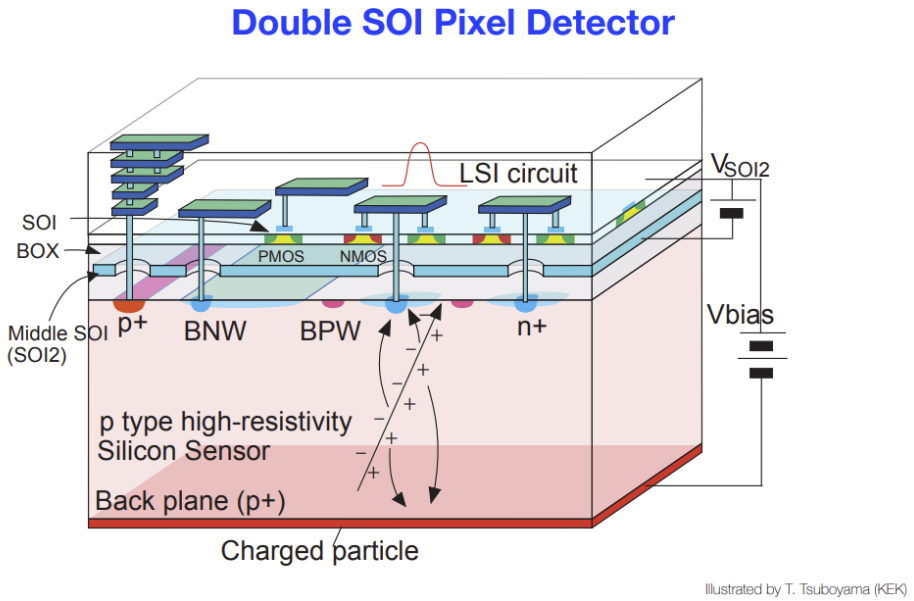

Mimosa 9 Analog (12bits)
Mimosa 18 Analog (12bits)
Mimosa 16 binary (1bit)
Mimosa 22AHR binary (1bit)
Mimosa 28AHR binary (1bit)
Mimosa 9 binary (1bit, reprocessed)
Mimosa 18 binary (1bit, reprocessed)
Theoritical digital resolution (pitch /√12)
Mimosa 30AHR binary (1bit)
pitch / √12
(Source of the plots: Y. Voutsinas, 2012)
Binary readout
Analog readout
Single point resolution (um)
Pixel pitch (um)
0
2
4
6
8
10
12
5
10
15
20
25
30
35
40
45

Double SOI

Double SOI Pixel Detector

Middle Si layer suppresses

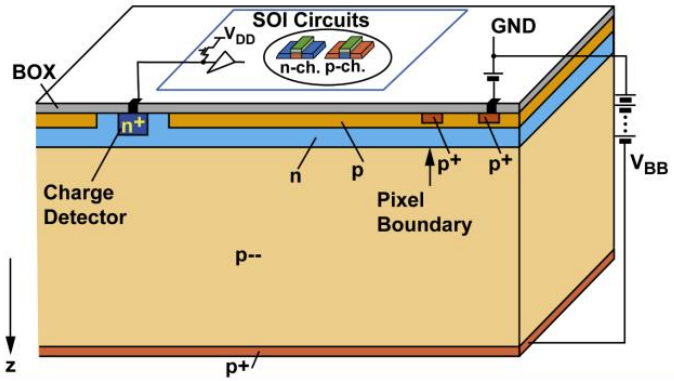
- Back gate effect
- Sensor-Circuit cross talk
  - Middle Si layer shields coupling between sensor and circuit.
  - It is useful for analog and digital mixed circuit in pixel.
- Radiation damage (TID)
  - It is able to compensate electric field generated by trapped holes in the BOX.
  - It can be used in high radiation environment (~1MGy).
  - (K. Hara, Vertex2017, Sep. 11-15, 2017, Las Caldas)



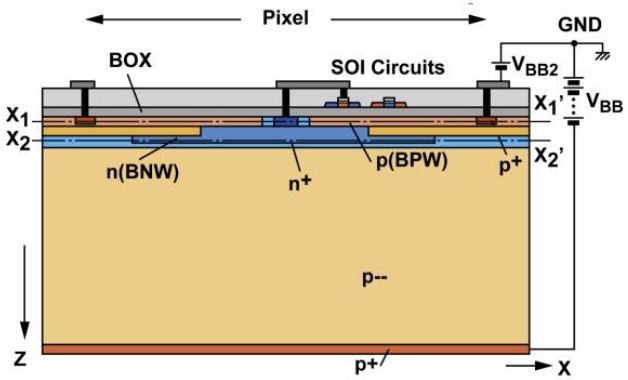
Sensor thickness: 50 - 500 μm
Sensor Resistivity: > 1 kΩ·cm
SOI2 thickness: 150 μm (*n*-type)
SOI2 Resistivity: < 10 Ω·cm

PDD (Pinned Depleted Diode)

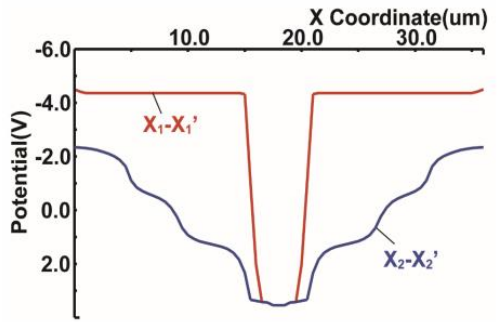
A SOI Pixel Detector Using Pinned Depleted Diode Structure (SOIPIX-PDD)

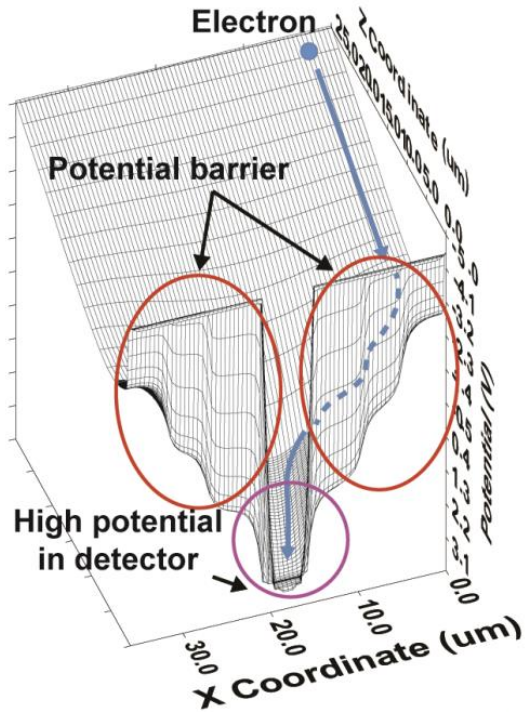


- Pinned Surface of Si Substrate with High Density Holes
  → Very Low R-G Dark Current
- Buried Channel → No Carrier Loss Due to Si-SiO_2 Interface Traps
  → Nearly 100% Charge Collection Efficiency
- Lateral Electric Field to Gather Electrons into an n^+ Sensing Node
  → High Sensitivity and Low Noise Due to Small Sensing Capacitance



VBB=-15V
VBB=-4V
25kΩcm, 200μm
36μm x 36μm

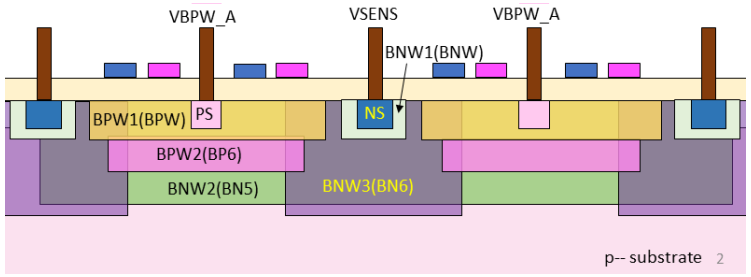




Shizuoka University, University of Kyoto, University of Miyazaki and KEK of SOIPIX R&D Group

CPV4-3D: PDD sensing diode system

CPV4-3D employs the PDD (Pinned Depleted Diode) sensing diode system for charge collection



Schematic view of PDD diode structure.

Composed of several layers of doped structures with different depths interface:

- Sensing node (NS) and the buried n-well (BNW1) form a charge collector;
- BPW1:shielding layer between circuits and the charge collector;
- BNW2, BPW2, BNW3 form a lateral gradient electrical field, benefit to charge collection efficiency;
- High negative voltage is backside applied to obtain a fully depleted substrate.

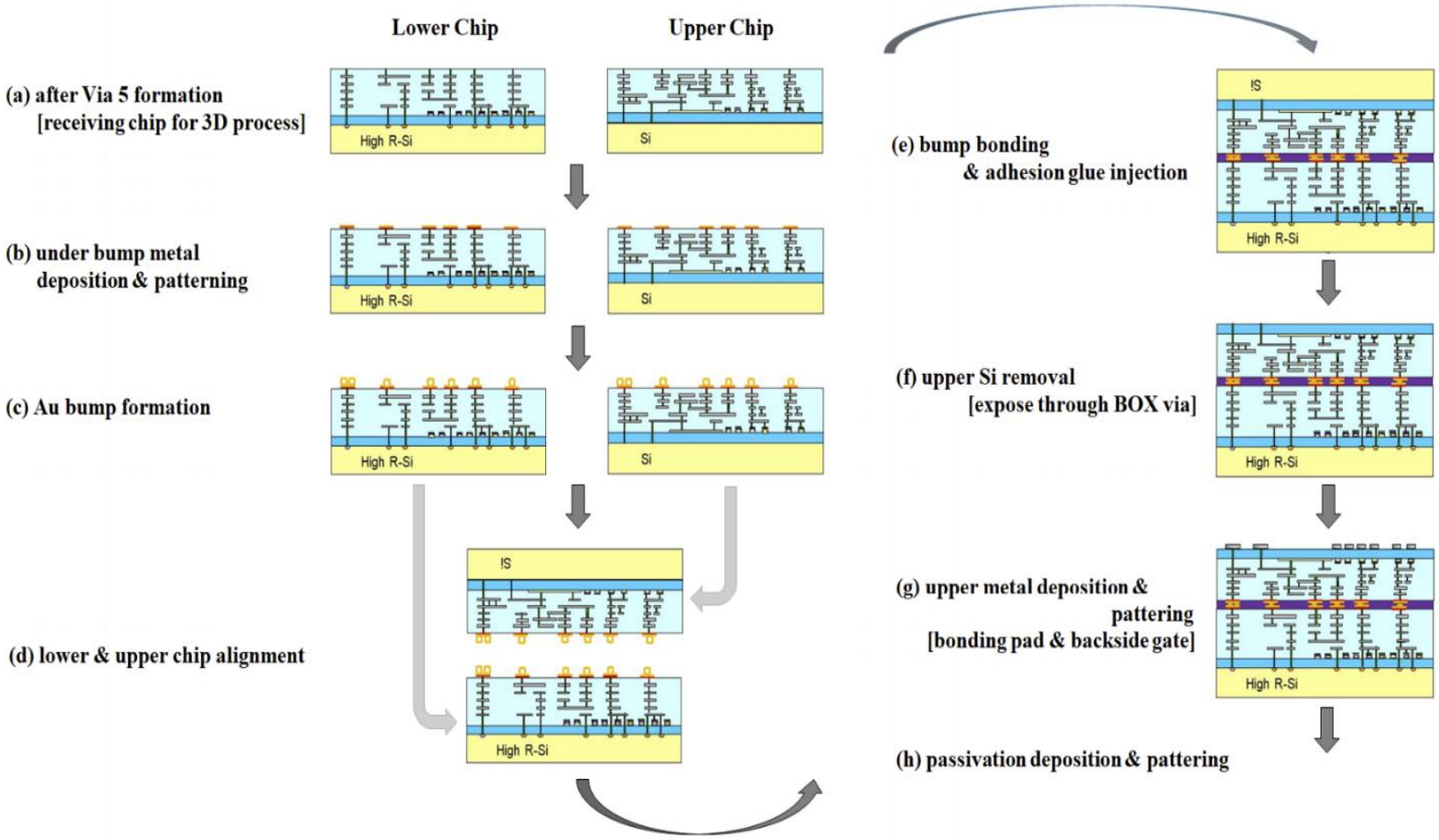
◆ Not 3D-specific, but the most active part of study in SOI pixel **sensor** technology

- Evolution of years' development: BPW, Nested-wells, Double SOI, and PDD (Pinned Depleted Diode)

◆ **All-in-one solution** in the sensor part:

- Control back-gate of transistors
- Maximize charge collection efficiency
- Suppress leakage current of Si-SiO_2 interface
- Minimize the capacitance of electrode (Cd)
- Shield the capacitive coupling between the sensor and pixel circuit

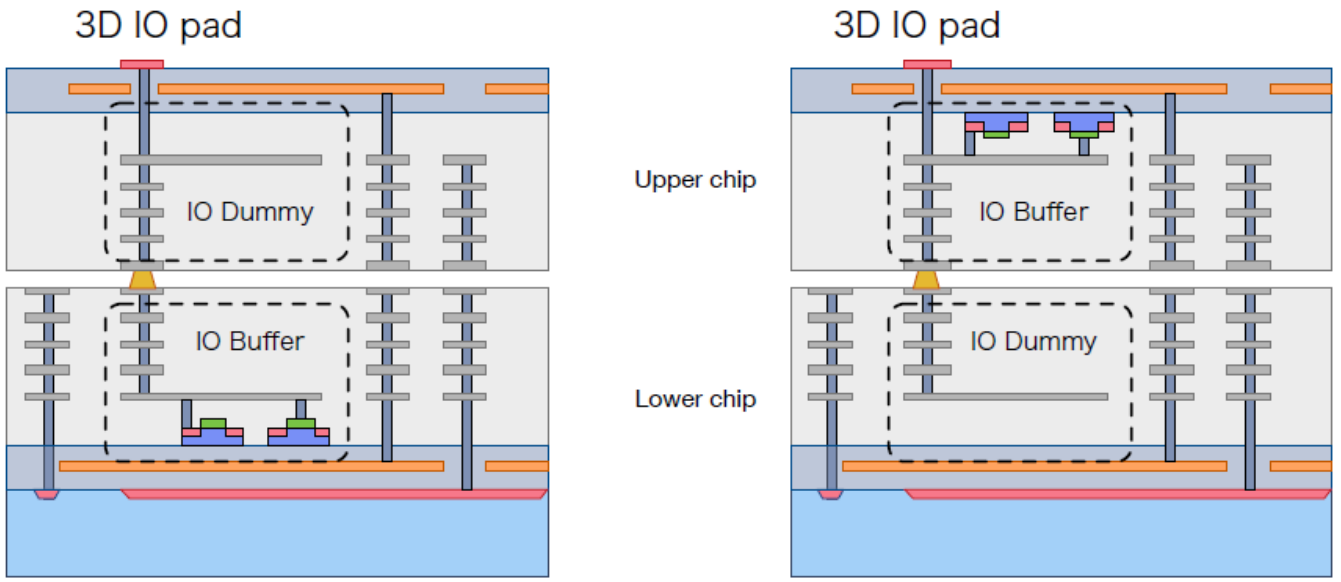
3D chip stacking process



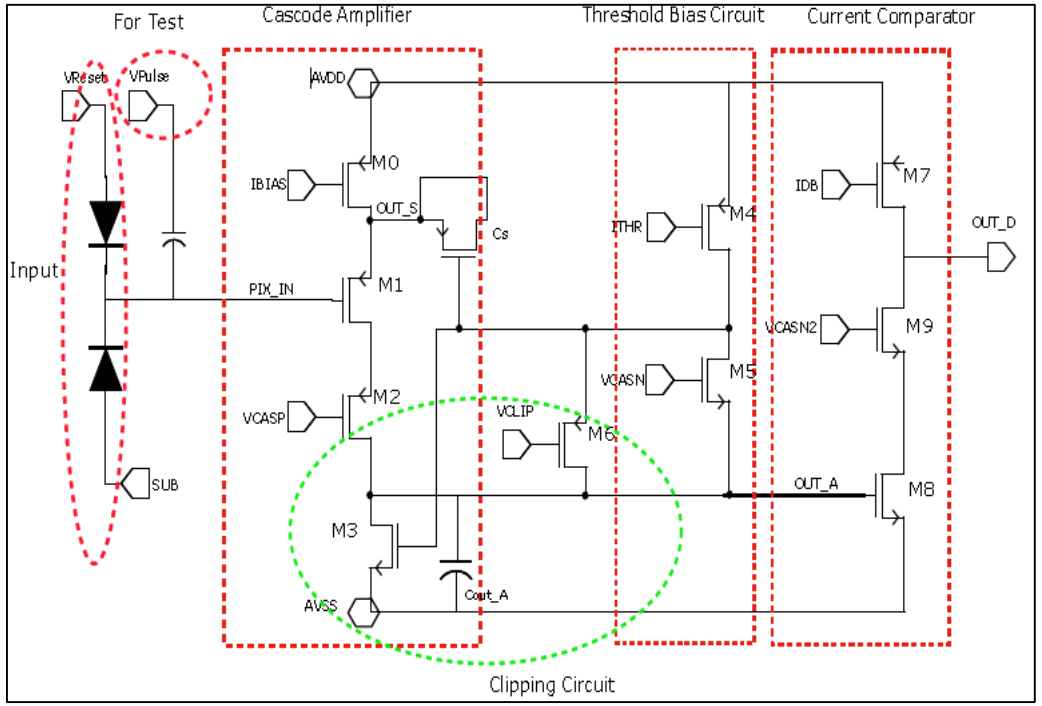
3D chip stacking process *@*Ikuo Kurachi，et all, Oct.7, Vertex 2020*

3D IO pad

Configuration for the signal of lower tier(left) and upper tier(right)



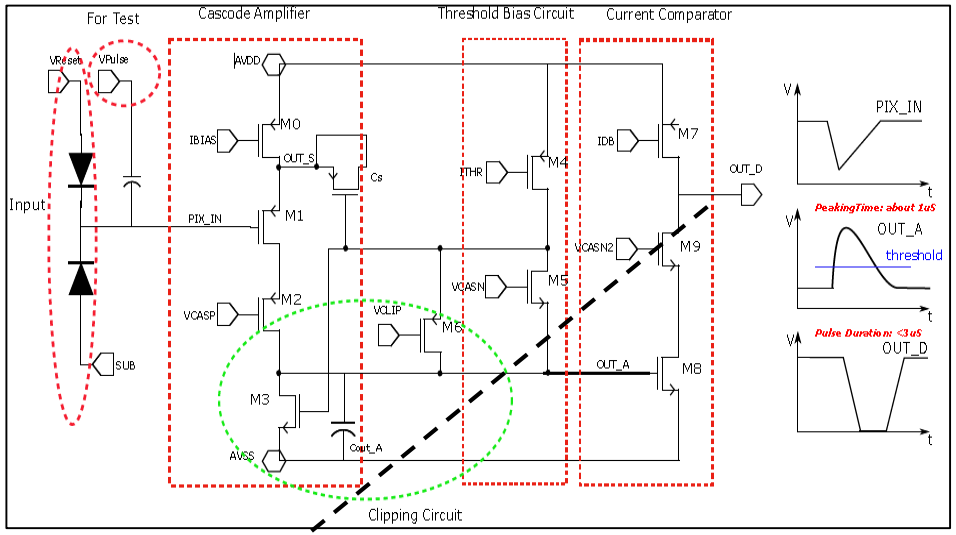
CPV4-3D: Lower tier pixel

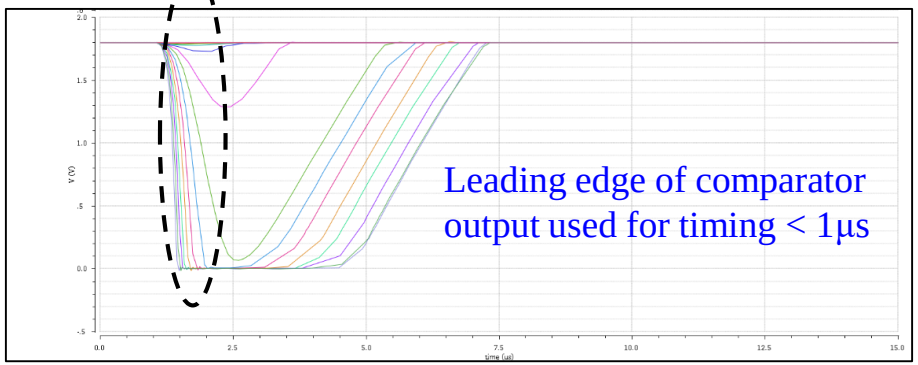


Pixel schematic of CPV4-3D lower tier. The *structure original from ALPIDE designed by CERN for ALICE*

- **Lower tier pixel integrate the functions of**
  - Charge collection;
  - Amplification;
  - Digitization;
  - Threshold tuning;
  - Structure for pulse inject test;
- -4V on the **back-gate** of MOS transistors required (BPW shown last page) in order to minimize electrode capacitance Cd.
  - Vth decreased 70 mV for PMOS and increased 50 mV for NMOS
  - Characterized and modeled in HSPICE by KEK
- Influence on the front-end assessed
  - Current mirror matched and placed in a -4V N-well (Counter-part branch of M0, M4, M7)
  - The other transistors compensated by proper offset on their bias voltage (VCASN e.g.)
  - **Confirmed by simulation**

CPV4-3D: Lower tier pixel





◆ **Transistor size** selected according to ALPIDE design* to minimize FPN as a first order approximation

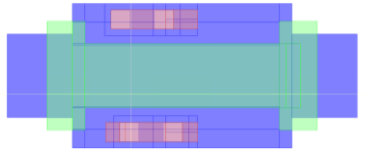
Transistor	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9
W/L	1.8/8.5	1/0.4	1/0.4	1/5	2/8.05	0.63/4.94	0.63/3	1/5	1/0.4	1/1

◆ Simulation results of **threshold and noise**

	Threshold	Gain@Thr	Vnoise@Thr	ENC
Pre-layout	75 e^-	32mV/10e^-	4.33 mV	1.34 e^-
Post-layout	**125 e^-**	8.6mv/10e^-	2.92 mV	**4 e^-**

◆TID radiation enhancement

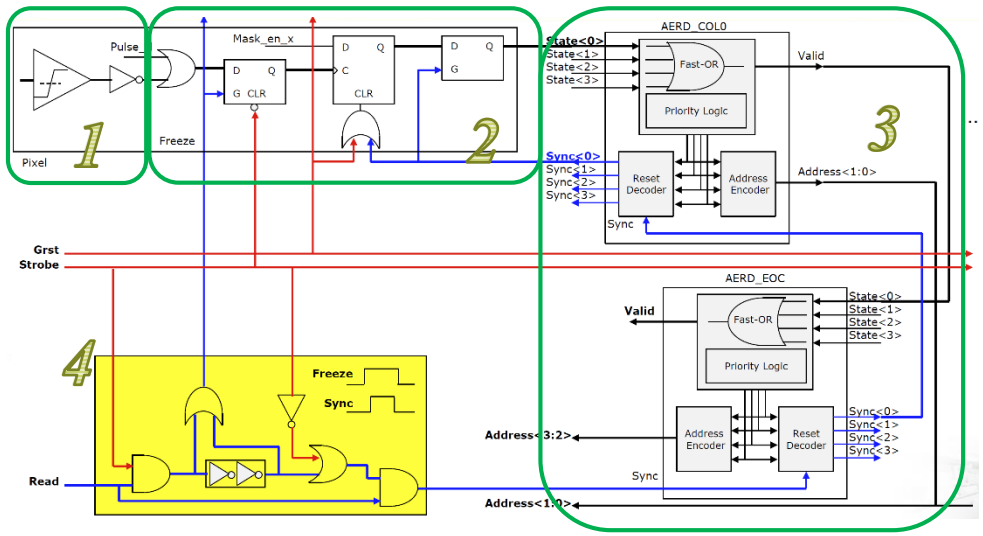
- Smallest working current path at M5 = 0.5nA, the same order of magnitudes with leakage after radiation (TID: ~1-10 Mrad)
- H-gate transistors used for M5 in test pixels for TID
- Compensation of TID-induced Vth shift to be applied on the BPW layer



H-gate NMOS layout used in this design

*Ref: D. Kim et al., 2016 JINST 11 C02042

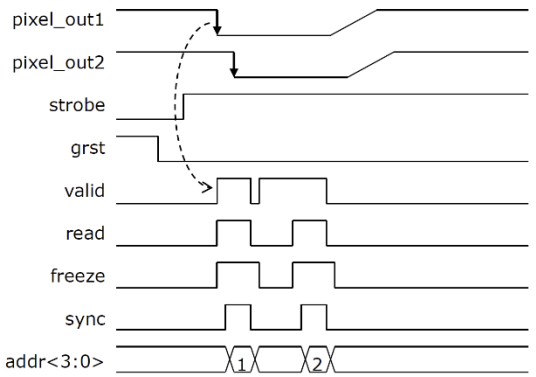
CPV4-3D: upper tier



Data readout structure (simplified) of CPV4-3D

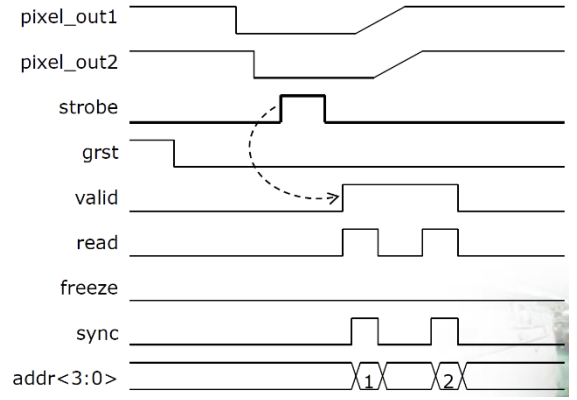
Continuous readout mode:

- Strobe == 1;
- Timing by falling edge ~ 1μs resolution
- New hits are freeze while reading



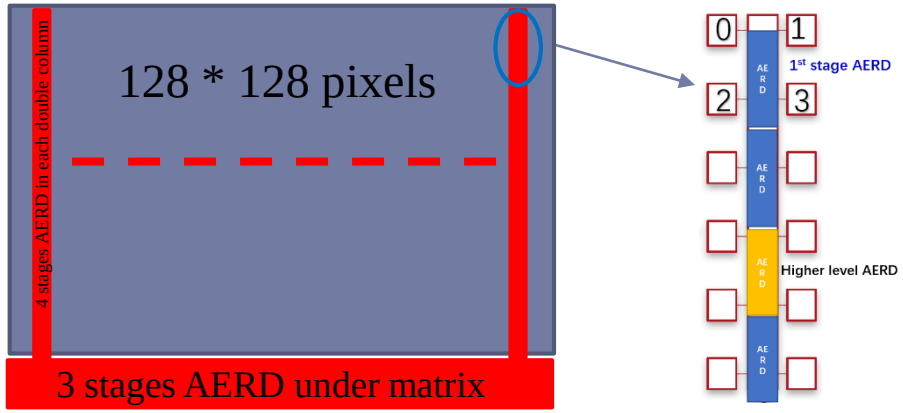
Triggered readout mode:

- Strobe as gate signal;
- Timing by trigger ~ 3μs resolution
- Read after trigger



1. Lower tier pixel: convert hits information into digital signals
2. Upper tier pixel: Hit D-Flipflop + Control registers (Musk/D_test/A_test/hit_response)
3. Data-driven readout (Asynchronous Encode Reset Decode*)
   - 4 stages AERD in each double column for 128 rows
   - 3 stages AERD under matrix for 64 double columns
4. SYNC/FREEZE generation block: outside the matrix
   - Continuous readout mode
   - Triggered readout mode

**Ping Yang, NIMA 785 (2015) 61-69*



14-bit output for fired pixel address information