Radiation-Tolerant High Speed Links

Readout challenges in future high-granularity high luminosity trackers

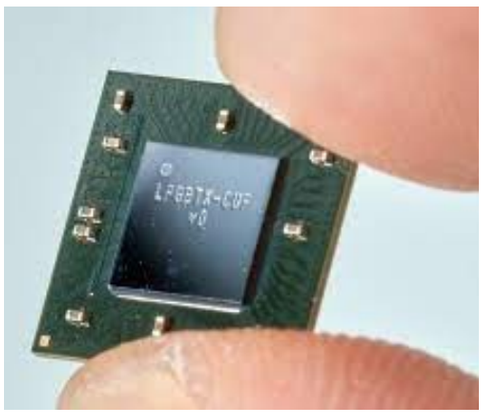
Stefan Biereigel, CERN, 24/10/2022

Introduction

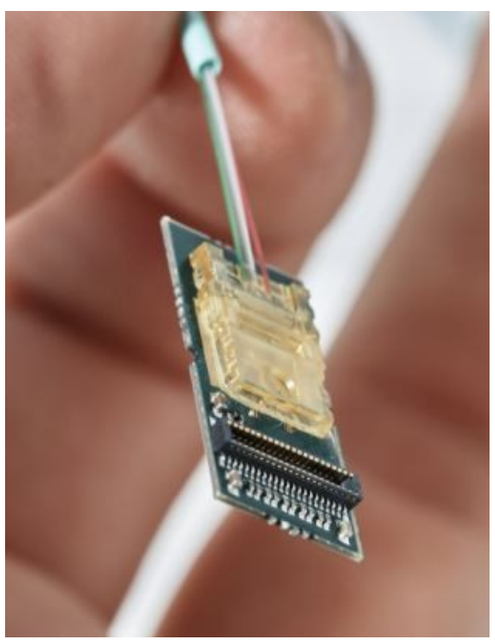
- Studies of future high-granularity trackers ongoing
  - Readout challenges for **>100 Gb/s per ASIC** on the horizon
- Solutions / feasibility currently explored within CERN experimental physics R&D program
  - Study of future high-speed links
  - Strongly connected with CMOS technology (rad-hardness, co-packaging, integration) research

State of the Art

- Common development for HL-LHC experiments: *Versatile Link Plus (VL+)*
  - Radiation-tolerant data aggregator ASIC (lpGBT, 65 nm CMOS)
  - VCSEL-based transmitter on optical module (VTRx+)
  - Throughput: 10 Gb/s per lane
- Data aggregation typically performed on module level
  - Limited data rate between front-end ASIC and aggregator
- Limited radiation hardness of VCSEL-based optics
  - Constrains location/use of optical modules



lpGBT ASIC



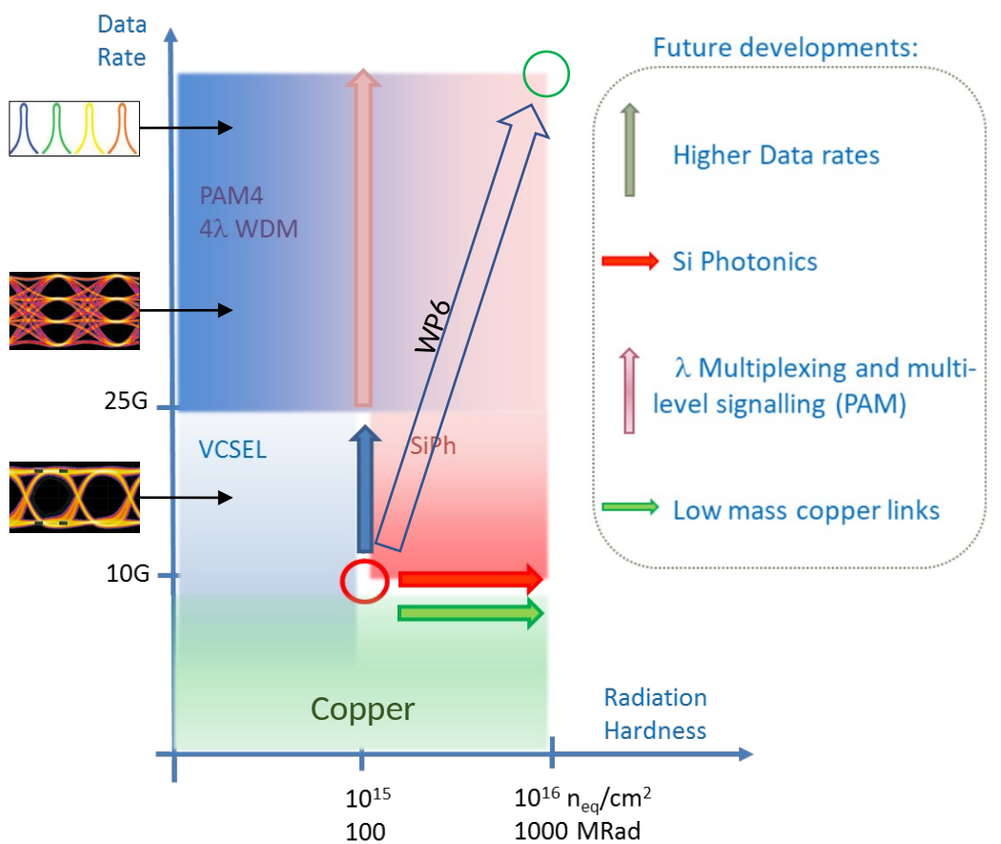
VTRx+ Transceiver Module

Future Challenges

- Expecting 10x increase of data produced **per ASIC**
  - Very high data rate links need to come closer to front end
- Desired TID tolerance up to/beyond 1 Grad (10 MGy)
- R&D focus: development of flexible IP blocks for future experiments
  - Can be used to assemble aggregator/concentrator ASICs
  - Reuse in low-granularity environments

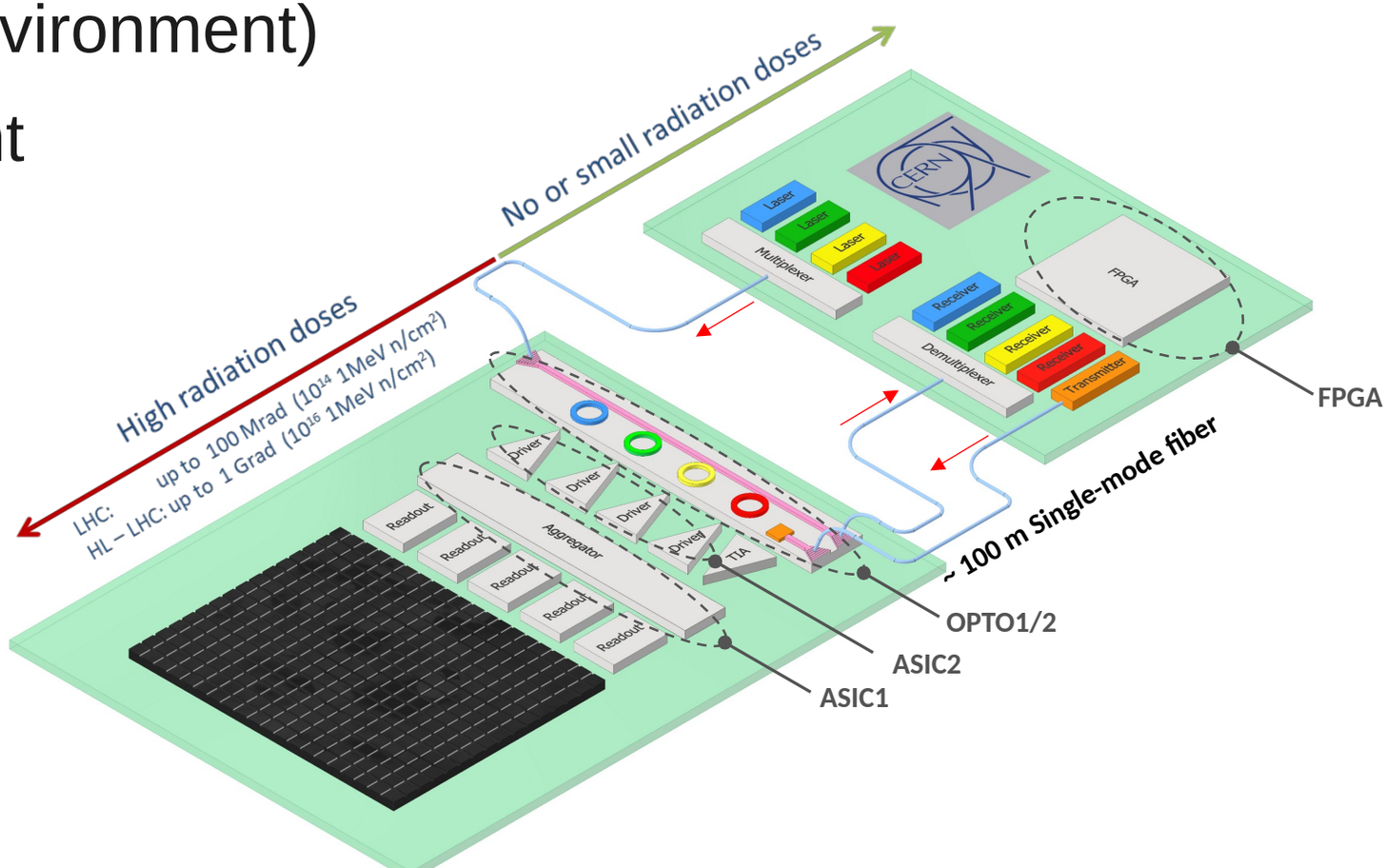
Evolution

- Goal within R&D program: Increase link bandwidth and radiation tolerance
- Dimensions for increasing bandwidth
  - Increase **symbol rate per link**
    - High-speed circuit design
  - Increase **modulation order**
    - Move from NRZ to PAM-4: 2 bit per symbol
  - **Multiple links within one fiber** (Wavelength Division Multiplexing)
- Increasing radiation tolerance
  - Adoption of 28 nm CMOS
  - Silicon Photonics replacing VCSELs



Silicon Photonics

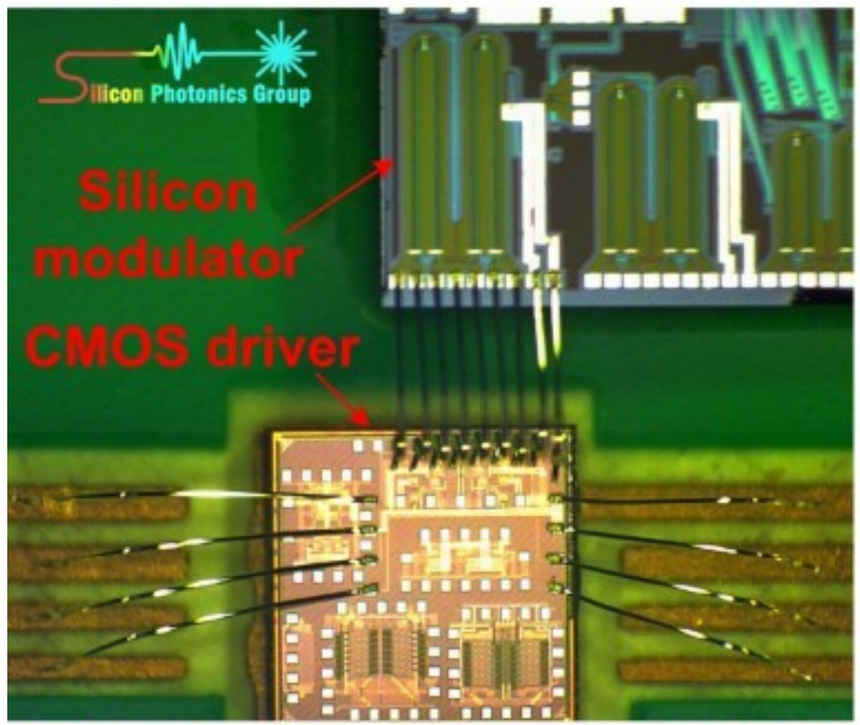
- Silicon Photonics replacing VCSELs
  - Laser source can be moved to back-end (outside of radiation environment)
  - SiPh used to implement integrated rad-hard modulators



Silicon Photonics

- Two-component system
  - SiPh integrated circuit (PIC)
    - Specialized photonics process
  - Transmitter/driver ASIC
    - High-speed CMOS process
- Integration challenges
  - Wirebonding – bondwire parasitics
  - Flip-chip (3D packaging, technological challenge)

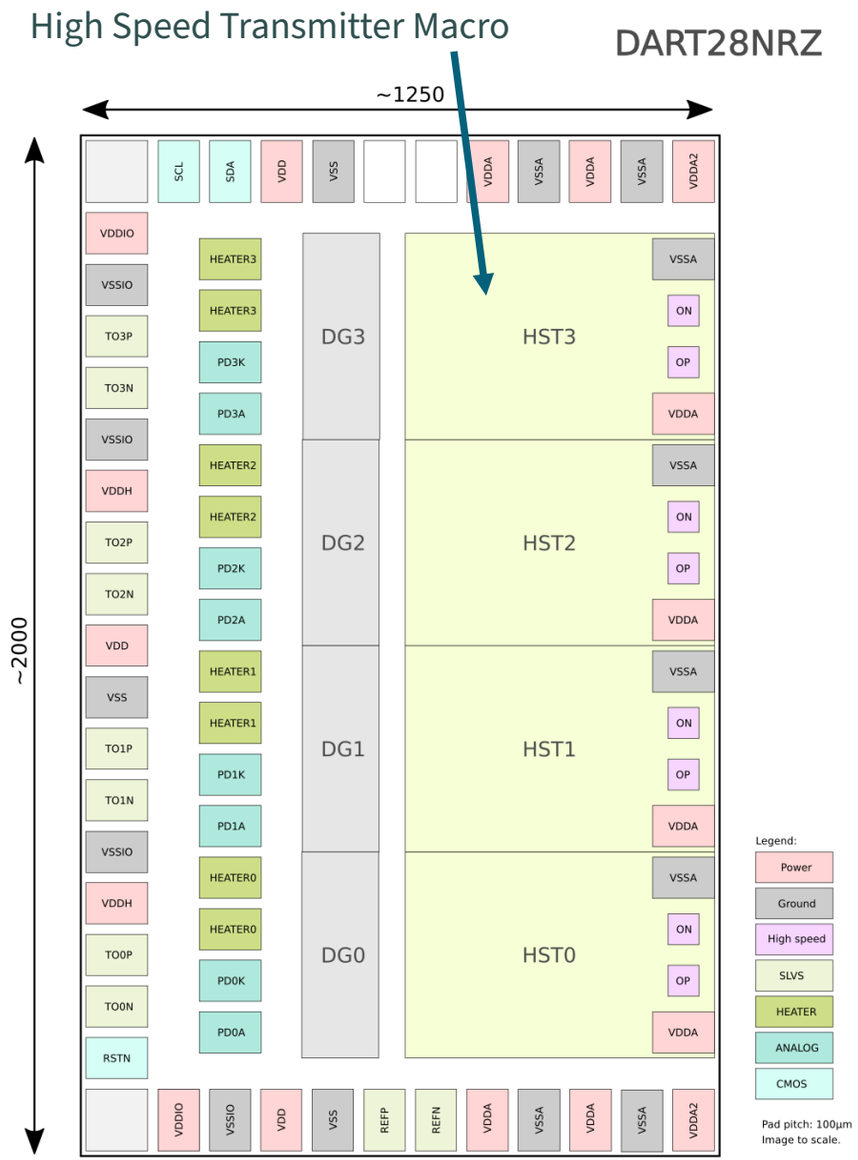
https://europractice-ic.com/tsmc28-si-photonics/



Example Silicon Photonics System (Driver + Modulator)

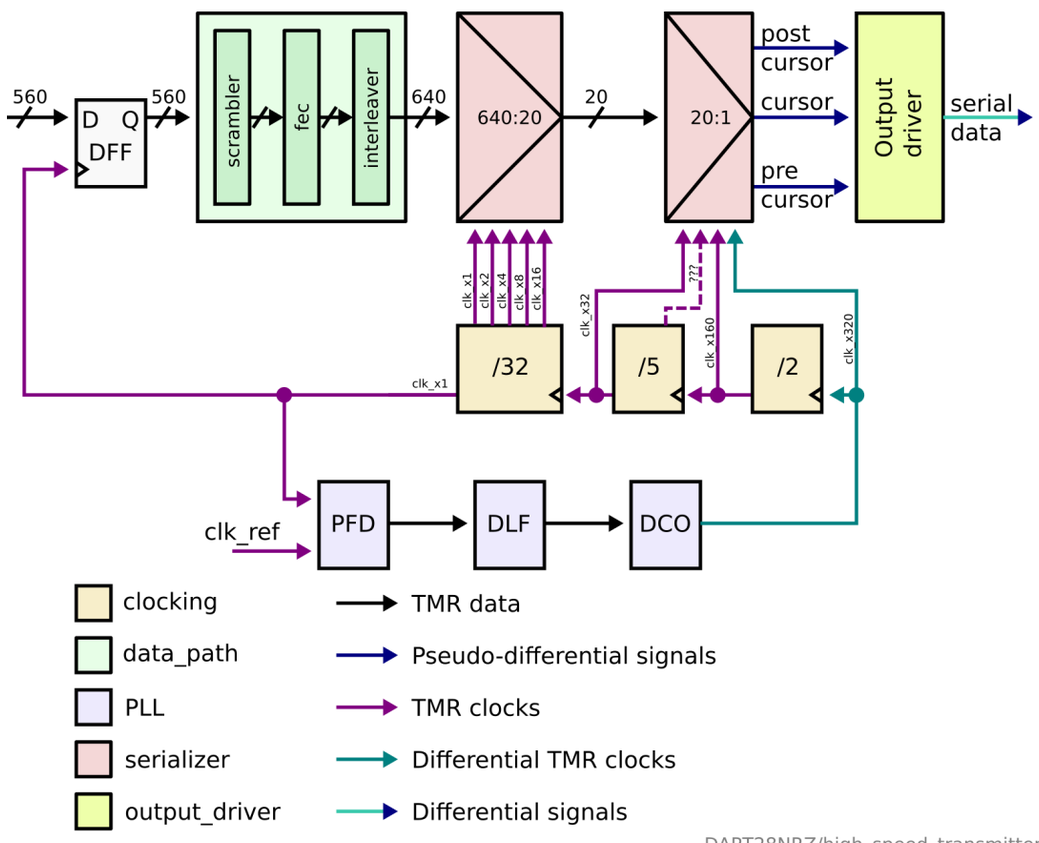
Demonstrator ASIC Transmitter

- First test chip (DART28NRZ), main goals:
  - **Demonstrate 26 Gbps NRZ** multi-lane transmission using on-board data generators
  - **Electrical characterization** & wirebond **integration with SiPh**
- Current baseline design: two electrical & two optical transmitters
  - Four abutted “IP Blocks” – simulating real-world integration scenario
  - Data generators included on-chip



High Speed Transmitter Macro Block

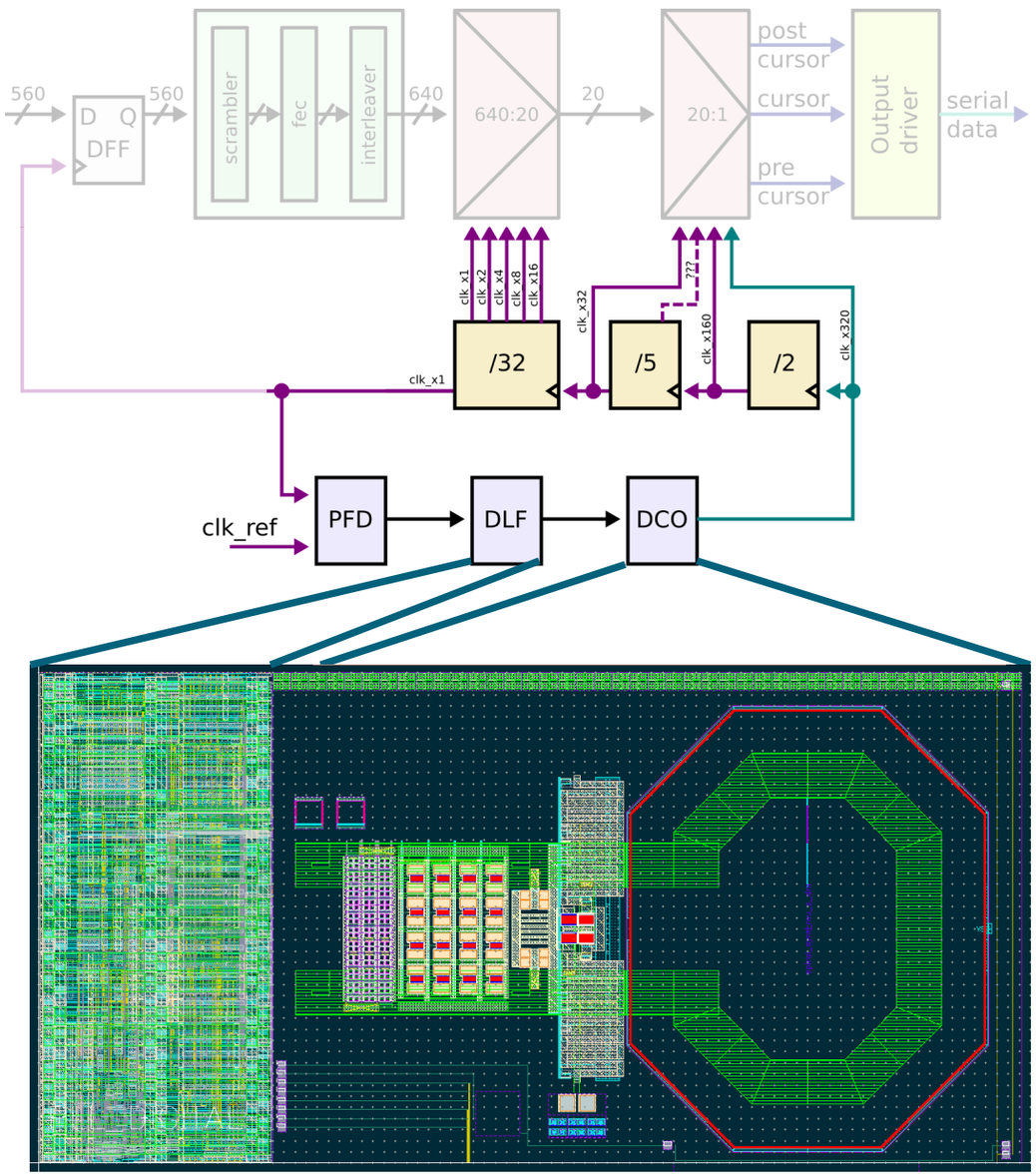
- Individual transmitter channels designed as self-contained IP blocks
- Encapsulates all critical functionality
  - Rad-tolerant data path
  - High-frequency PLL
  - High-speed Serializer
  - Output Driver
- User Interfaces
  - PLL reference clock, user data & clocks



DART28NRZ/high_speed_transmitter

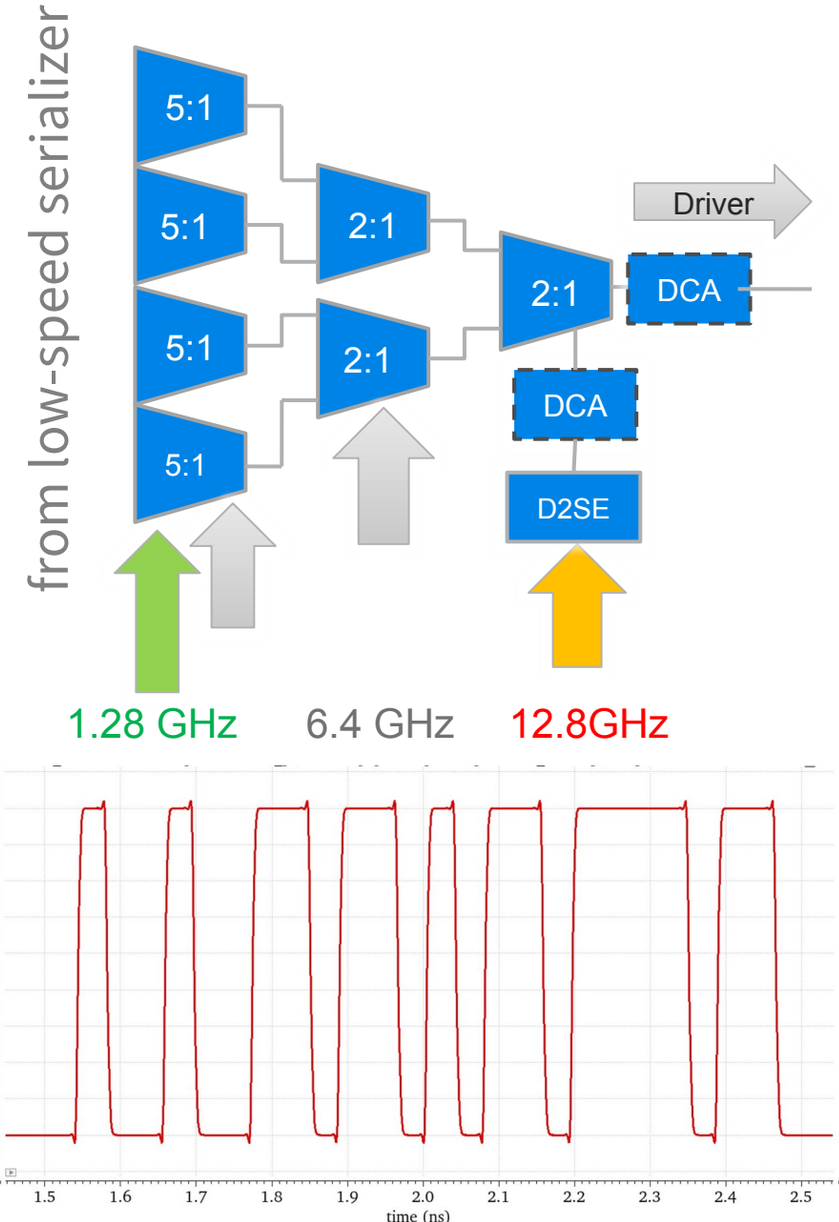
High Speed Transmitter – Clocking

- NRZ transmitter uses **highly synchronous clocking architecture**, similar to VL+
  - Target: 25.650 Gbps, 1 UI ≈ 40 ps
- Using a **half-rate serializer**, requires generation of **12.8 GHz clock**
- Stringent jitter requirements: **<1 ps rms**
- **LC oscillator PLL** for low-jitter local clock generation
  - Adoption of **All-Digital PLL architecture**
- TMR dividers shared between PLL and serializer



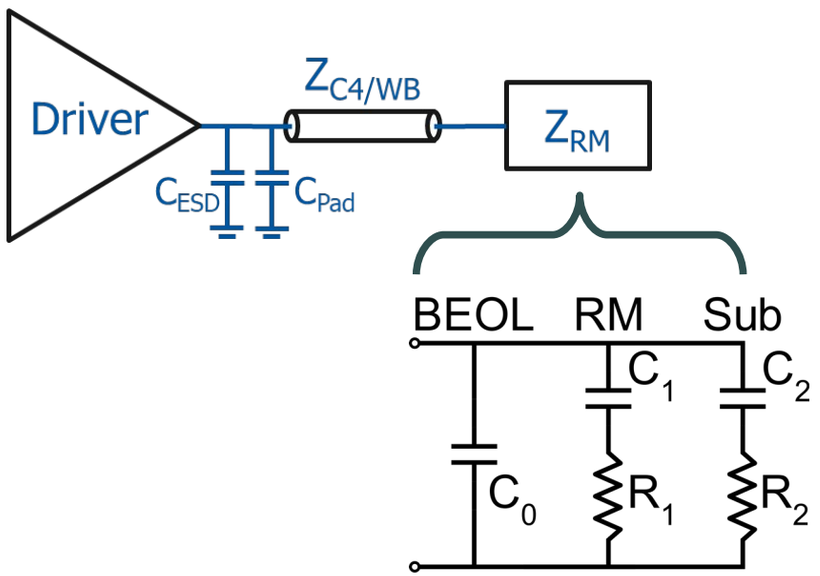
High Speed Transmitter – Serializer

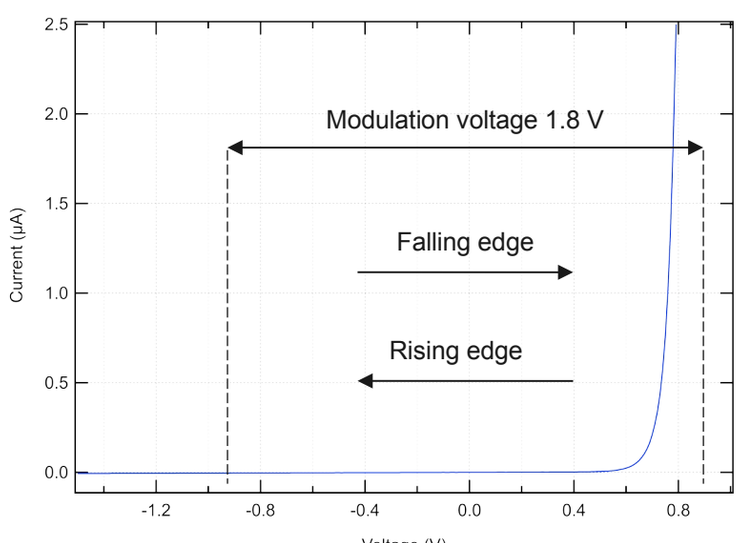
- Serializer converts parallel user data bus into serial, high speed data stream
- **Ciritical: High-speed serializer (20:1)** - full-custom design flow
  - High data rate (careful design of clock and data distribution, balanced layout, etc)
  - Tight specifications for duty cycle distortion and even-odd jitter performance
    - On-chip clock duty cycle adjustment necessary
- Low-speed serializer stages implemented using digital design flow



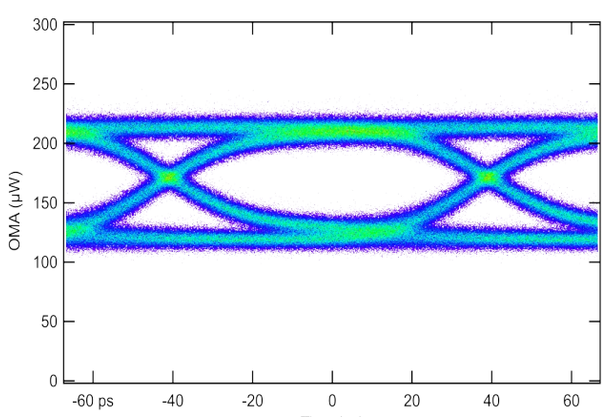
High Speed Transmitter – Output Driver

- Designed to drive ring modulator on SiPh IC – (mainly) **capacitive load**
- General Design Challenges
  - High bandwidth with large ESD/pad capacitance and wire-bonding
  - Maximize drive amplitude, while avoiding forward-bias of the ring modulator

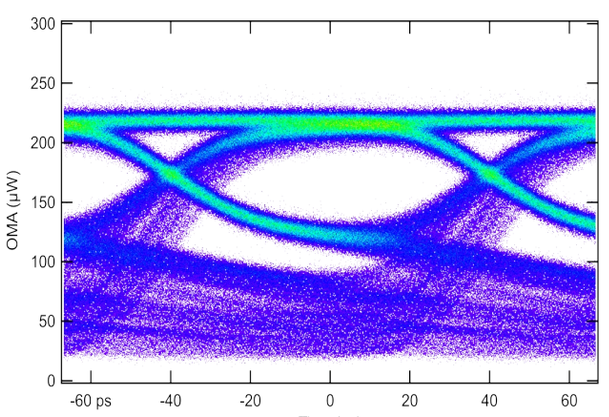




RM Transfer Function



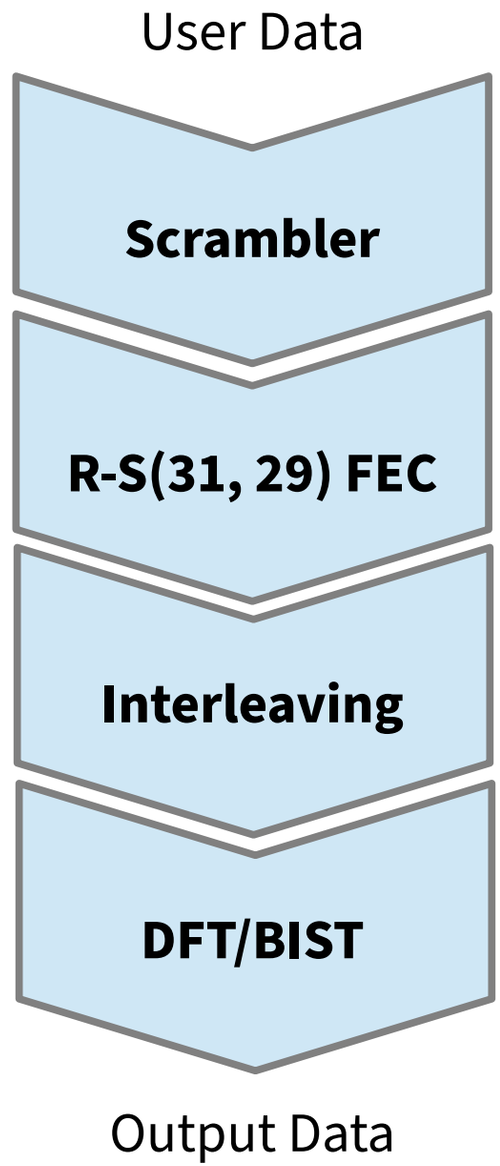
$V_{forward}$ = 0.5V



$V_{forward}$ = 0.9V

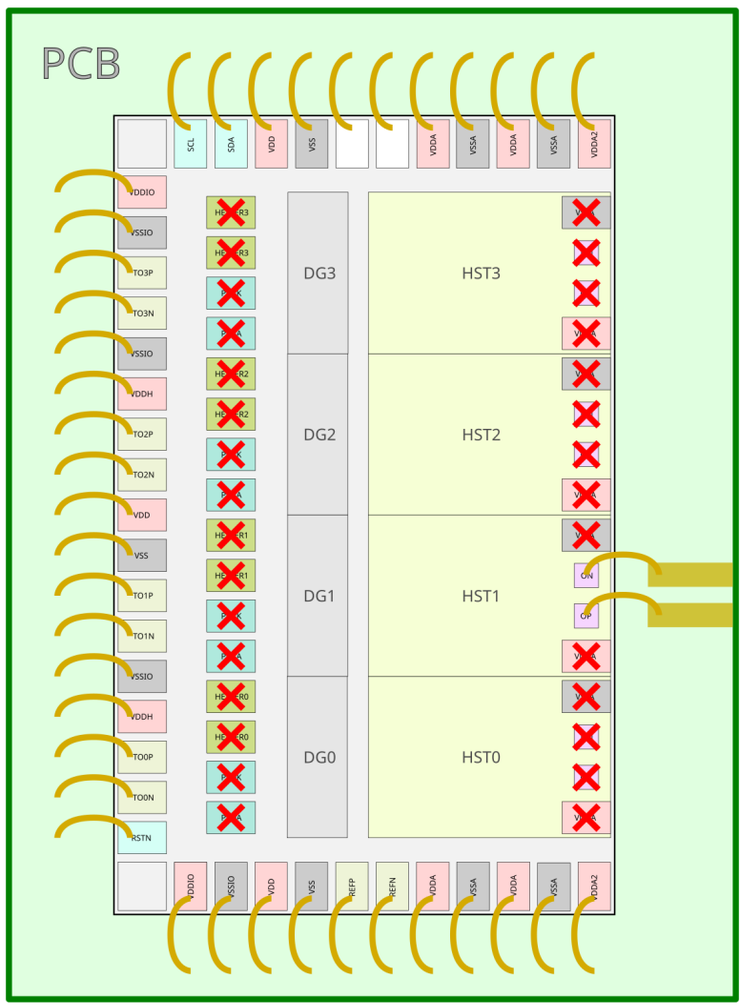
High Speed Transmitter – Data Path

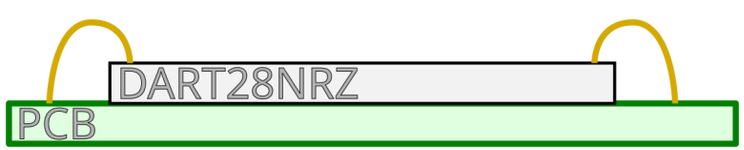
- Similar to VL+ data path
  - **Scrambler** for DC balancing of data
  - FEC: **Reed Solomon (31, 29)** code
  - **Interleaving** to improve burst error resiliency
  - **560 user bits → 640 link bits per frame**
  - **User bit rate: 22.44 Gbps**
- Integrated **DFT/BIST** features
  - PRBS / fixed pattern generation
  - Error injection
  - Flag injection (for latency measurements)



DART28NRZ Demonstrations

- **Single Channel, Electrical**
  - Demonstrate correct operation of high-speed transmitter
  - Characterization across voltage/temperature
  - TID (X-ray) / SEU (Heavy Ion / Laser) tests
- Single Channel, Optical (w/ PIC)
  - Demonstrate SiPh integration, end-to-end optical link
- Dual Channel WDM Demonstration
  - Demonstrate two NRZ over one fiber using existing PIC





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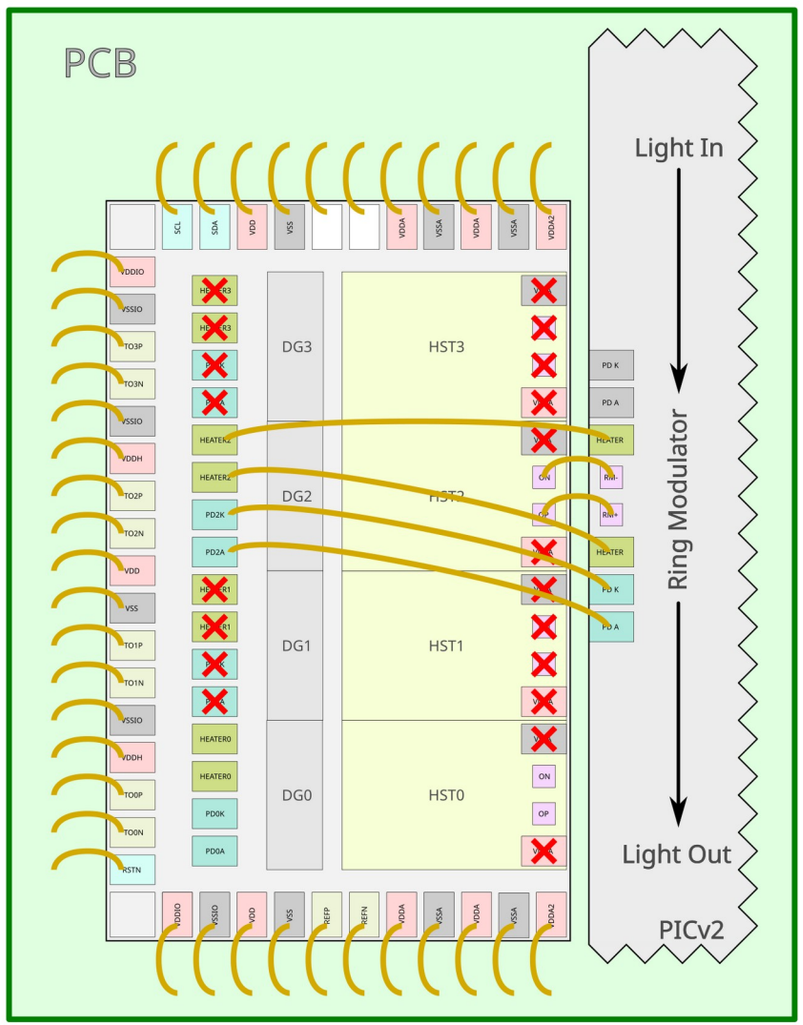

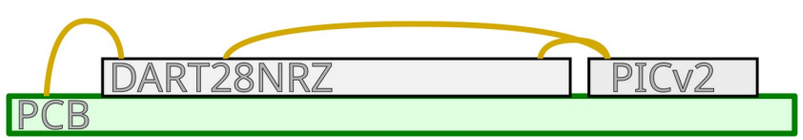

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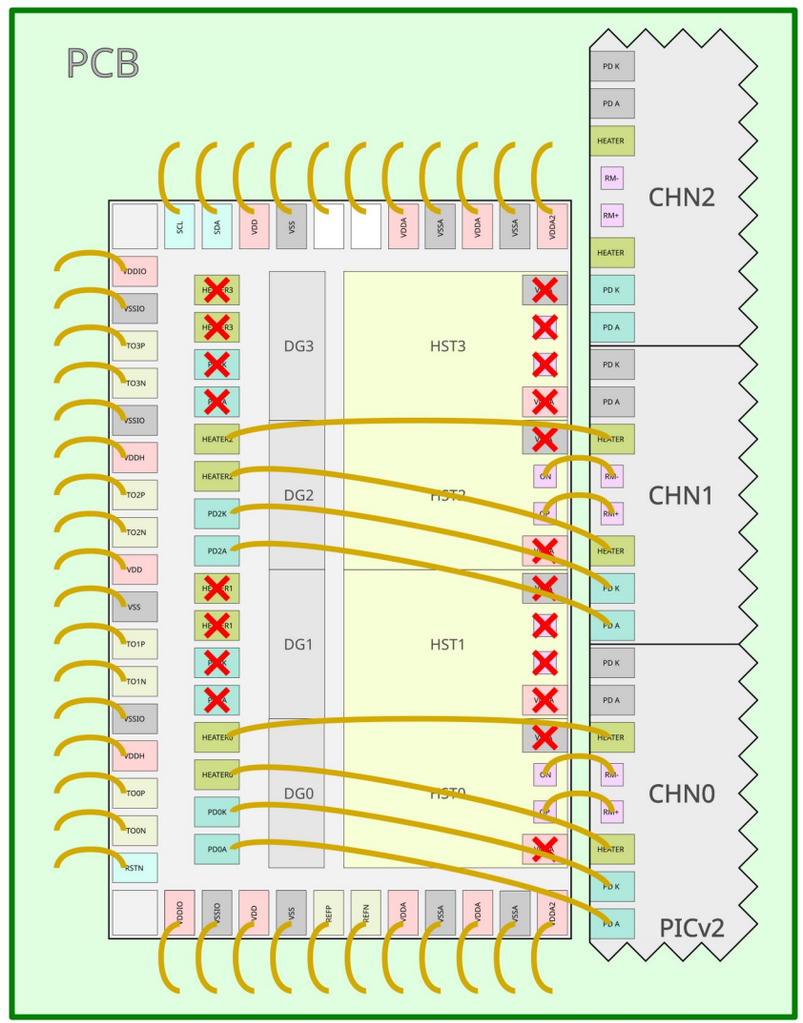
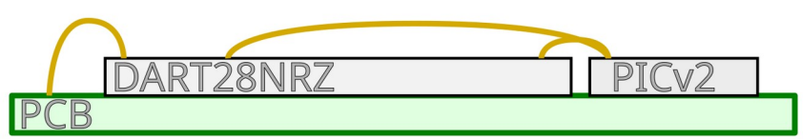
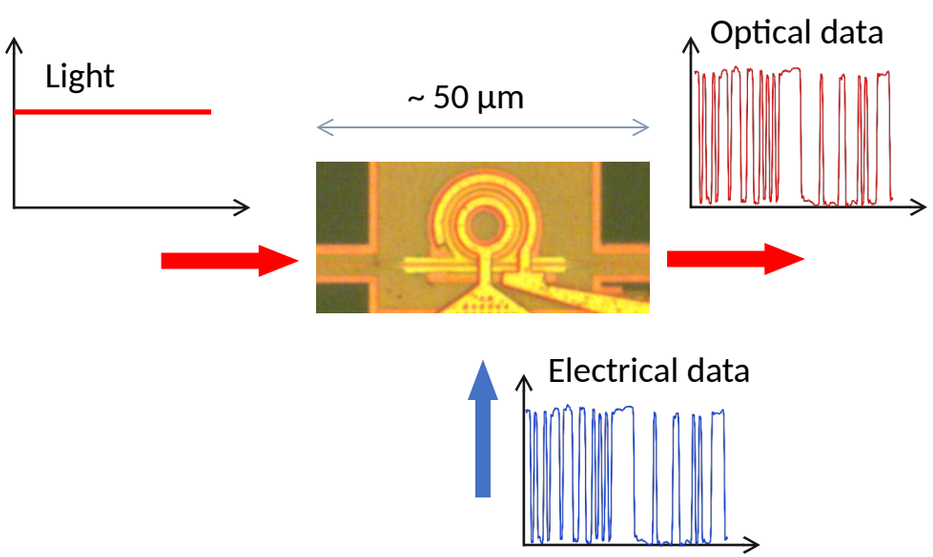
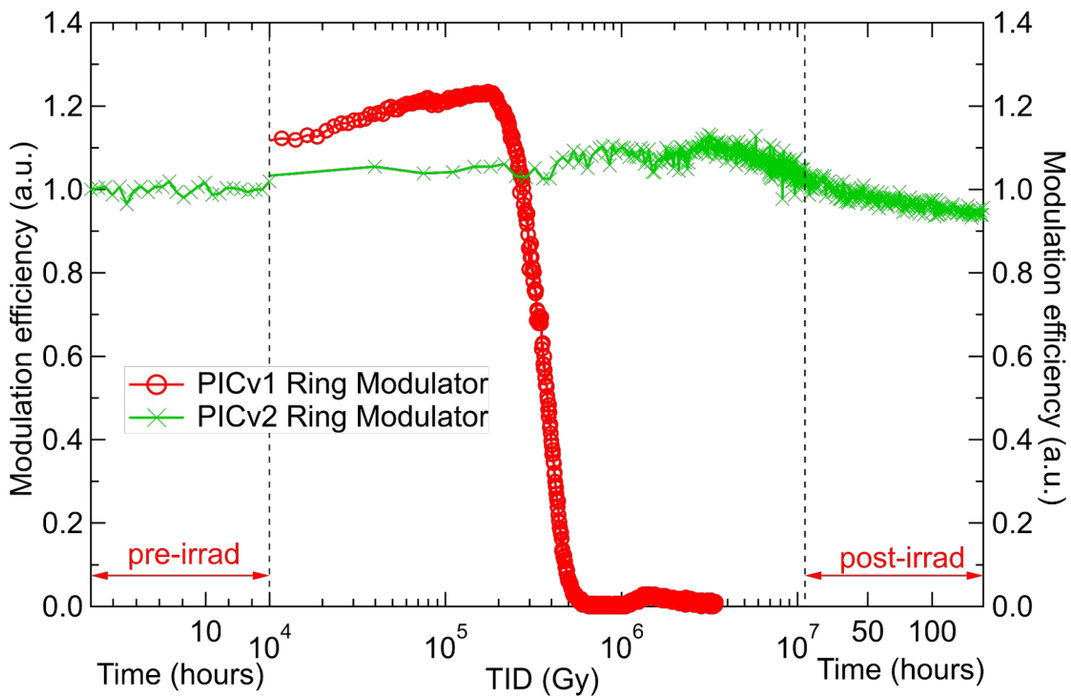




Silicon Photonics – Radiation Tolerance

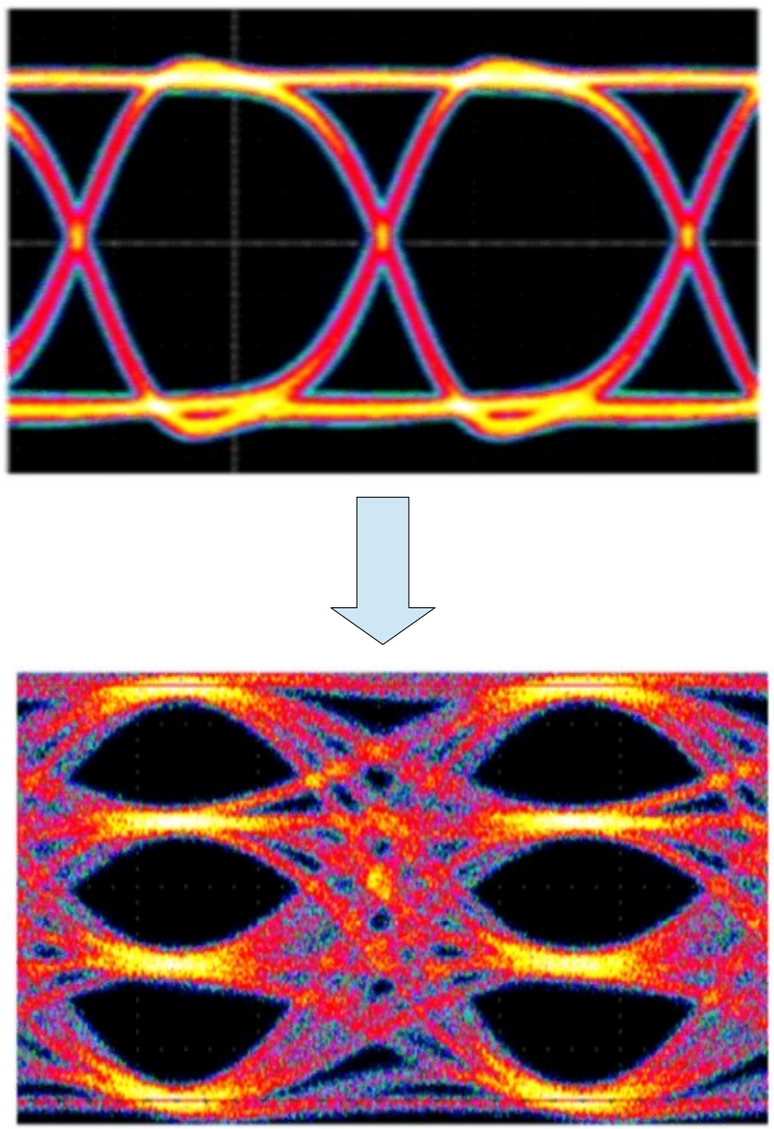
- Design and characterization of SiPh components in progress
  - Various components (e.g. photodiodes) intrinsically rad-hard
  - Optimization of micro ring modulator structures
    - Very promising radiation response (exceeding 10 MGy target for optimized design)





Towards 100+ Gb/s per ASIC

- First milestone: Demonstration of 26 Gbps NRZ link, will be a stepping stone for
- Exploration of WDM schemes
  - Foreseen with first demonstrator ASIC
  - Challenges: Co-packaging, integration
- Exploration of PAM-4
  - Compatibility with commercial modules (SFP) constrains the transmitter implementation (data rate restrictions)
  - Design challenge: PAM-4 output driver – large swing, high speed
  - Requires different approach to channel coding
- Exploration of 50+ Gbps NRZ
  - Possible favorable trade-off with SiPh
  - Challenges: co-packaging (multi-die flip-chip, ...)



Conclusions

- Goal to demonstrate a first **evolution of high speed links for future experiments in 2023**
  - Development as reusable IP-block, bringing links closer to the front-ends
- Multiple avenues for scaling into the 100 Gb/s realm need to be explored
  - Challenging in many domains: circuit design, co-packaging/integration, COTS back-end compatibility, etc

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