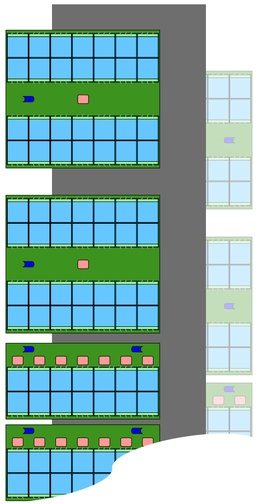
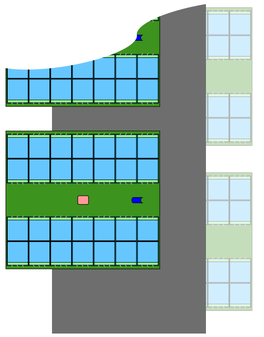
MAPS-based Upstream Tracker at LHCb Upgrade II





Quan Zou (邹全)[1] on behalf of the LHCb UT upgrade team

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[1]Institute Of High Energy Physics (IHEP), Beijing, China

Introduction

LHCb starts data-taking at L=$2\times10^{33}\ cm^{-2}s^{-1}$ in 2022 with upgraded detector. Upstream Tracker (UT) is located just upstream of the magnet and covers the full detector acceptance.

- Provide **fast track reconstruction** to speed up trigger decision
- Reduce **ghost rate** in long tracks
- Improve **momentum resolution**

But with L = $1.5\times10^{34}\ cm^{-2}s^{-1}$ in Upgrade II after 2032, it can not cope with the **data rate** and the **high occupancy** (up to ~ 10%) would significantly compromise the UT performance.

The proposed design for the upgraded UT detector is discussed using **CMOS MAPS technology** and give results from preliminary performance studies, together with an R&D plan.

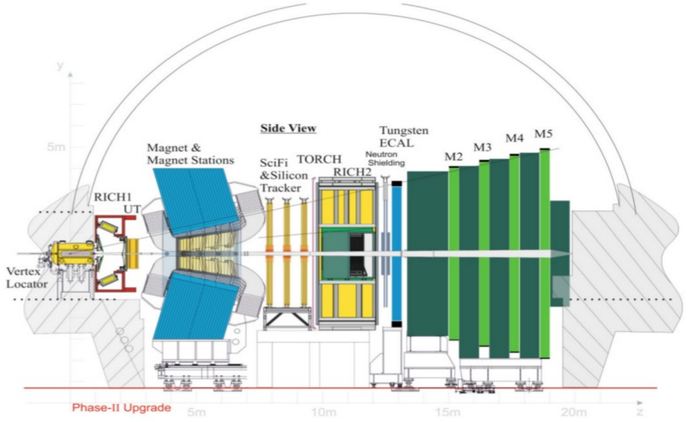


Fig. 1: LHCb Detector at Upgrade II

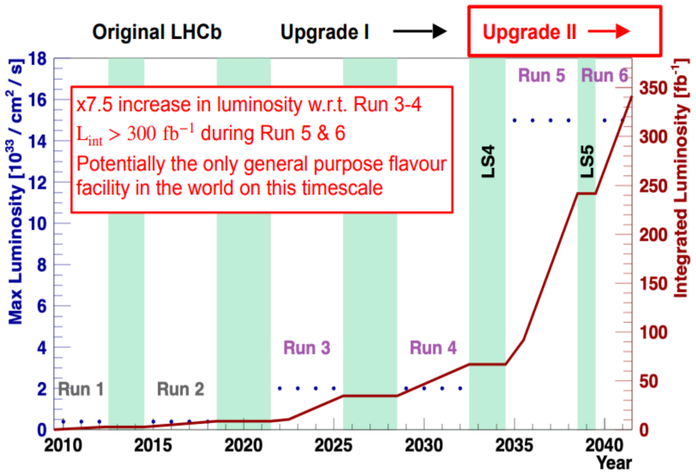


Fig. 2: Upgrade II timeline

Upgrade II Luminosity Simulation

Performance studies are based on simulation samples generated in Upgrade II conditions using the available Run 3 UT material and design in Geant4.

The two relevant occupancy related quantities for the future UT design are the **mean and maximum hit density per bunch crossing**, respectively.

Figure 3 shows the average hit densities per bunch crossings in p-p and Pb-Pb collisions.

- In p-p running conditions, the average density is **5.9 hits/cm^2/BX** in colliding bunch crossings, or 4.0 hits/cm2/BX in all bunch crossings, while it is **2.9 hits/cm^2/BX** for colliding Pb-Pb bunch crossings
- The maximum hit density in a central Pb-Pb events can reach ~ **52.5 hits/cm^2** , much larger than in p-p collisions
- For a pixel size of 50 × 150 μm^2 , the corresponding occupancy rate is 3.9 × 10^{-3}

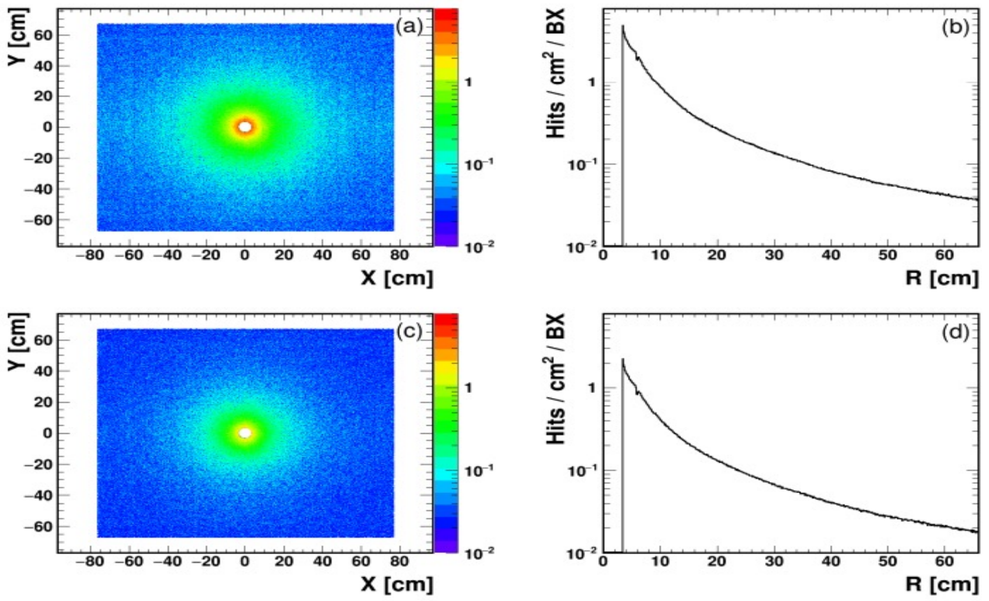


Fig. 3: The mean UT hit density per BX at the first plane per beam-beam colliding bunch in (a and b) the p-p programme, and (c and d) the Pb-Pb programme. All four plots use the same scale for direct comparison. The colour map of the 2-D plots are also shown.

CMOS Sensor Options

The ongoing R&D studies indicate that **Depleted Monolithic Active Pixel Sensors** (DMAPS) can be considered as very strong candidates for UT. Other technologies such as LGADs, that add timing capability, are optional choices.

To achieve substantial depletion in the sensing volume and improve the speed and radiation tolerance of the detector, DMAPS implementations follow two different approaches, namely large fill-factor or high-voltage (**HVCMOS**) and low fill-factor or low-voltage (**LVCMOS**).

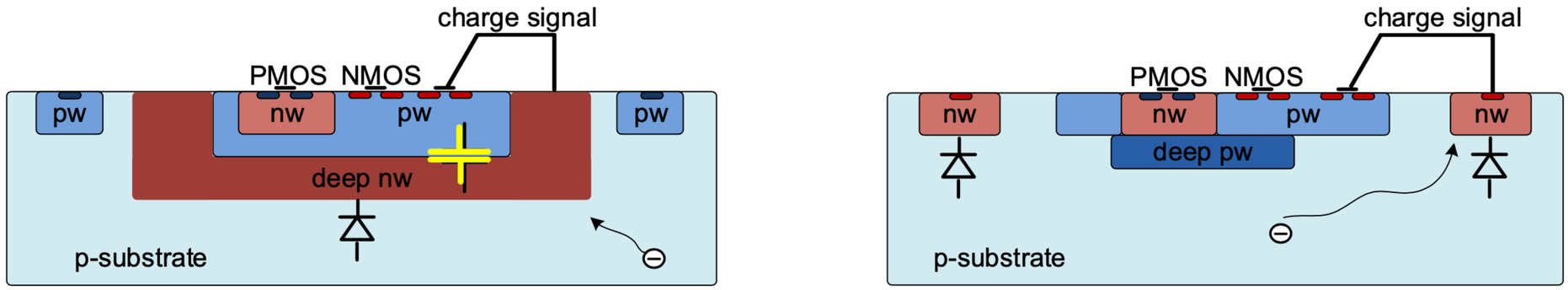


Fig. 4: The schematic of HV-CMOS (left) and LV-CMOS (right)

Detector Layout

A four-plane detector based on HVCMOS is proposed. Layout using other MAPS technology like LVCMOS is similar.

A potential detector layout is illustrated in Fig. 5. The basic element from which the overall detector plane is constructed is the stave, which is composed of modules containing the MAPS chips.

- **Fourteen chips in a 7 × 2 array** are interconnected to a flex circuit to form a module.
- The common **HL-LHC radiation tolerant ASIC** for data, timing, trigger and control applications, known as the lpGBT, will be utilized for data concentration and transmission.
- **A total of 36 modules** are mounted alternately on both sides of a supporting bare stave, **in total 12 staves**.
- The inner staves differ in design, with their innermost modules consisting of only 5 × 2 sensor chips each due to the beam hole.

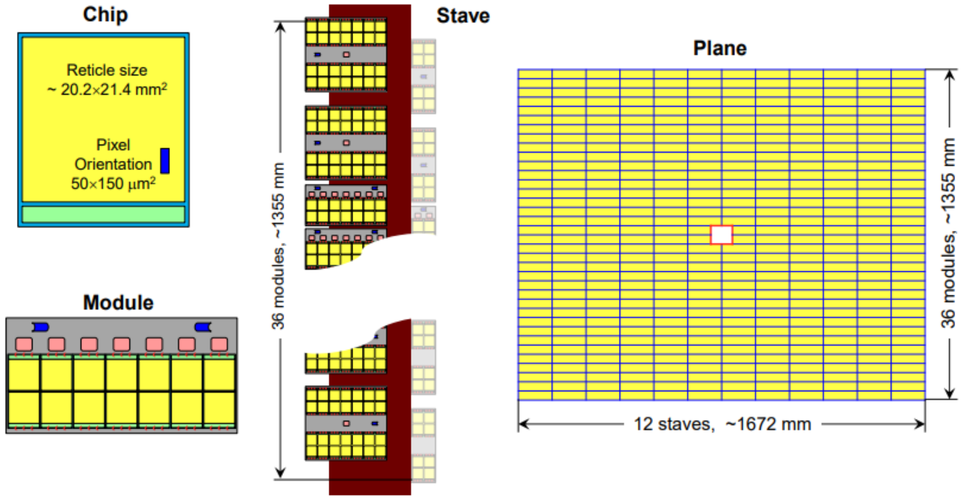


Fig. 5: A possible configuration for the Upgrade II UT detector.

Detector Layout

Geometry modeling is under development **based on HVCMOS.**

- Sensor chip: the HV-CMOS geometry
- Module: 6 types, to match with different data rates
- Stave: 4 different types
- Plane: 4 planes

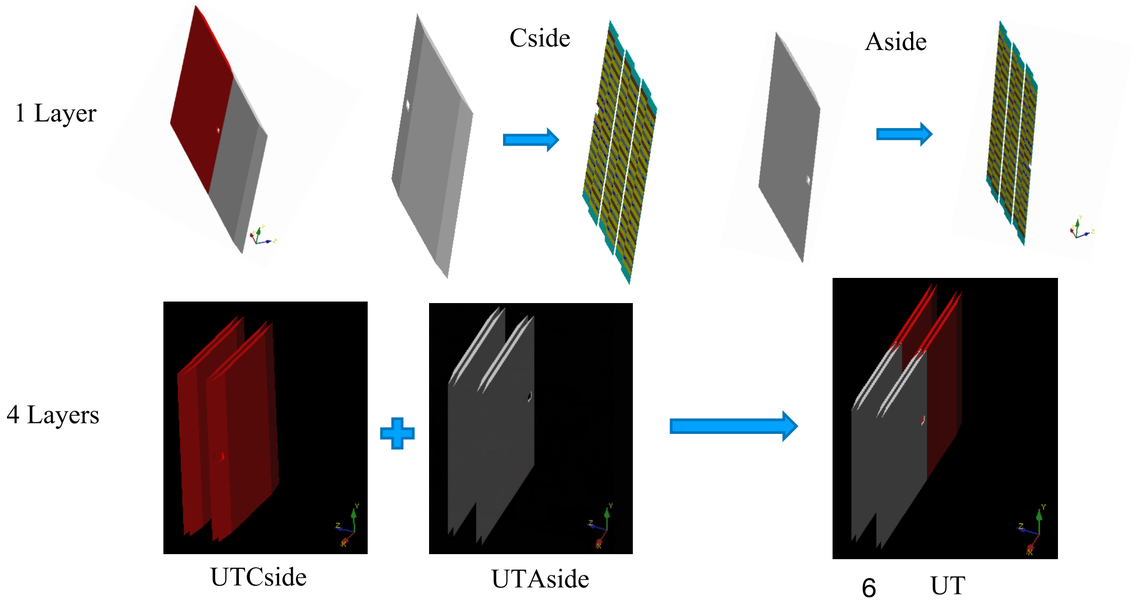
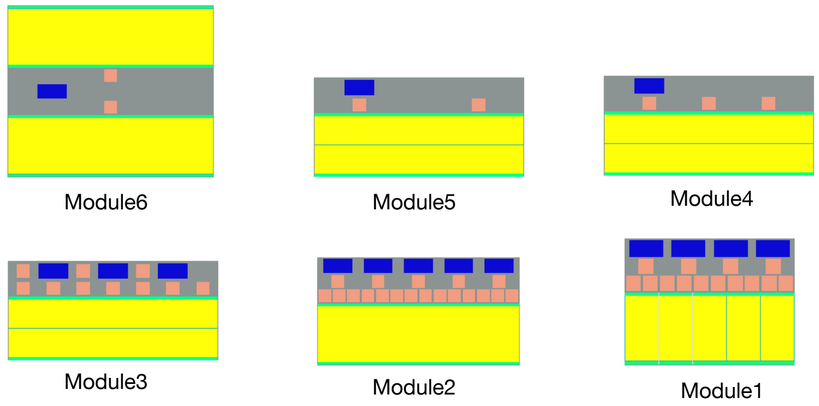
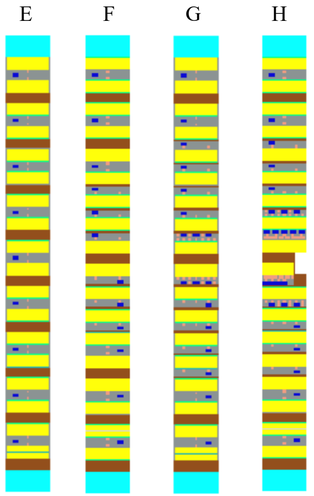


Fig. 6: Geometry construction using DD4hep





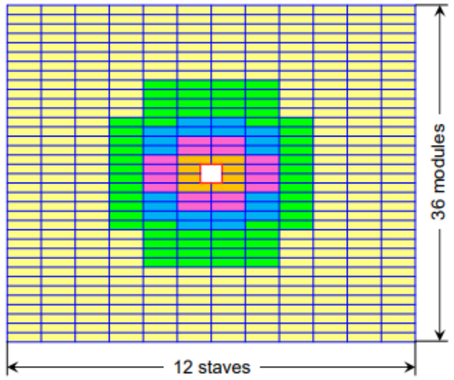
Mudules and staves

Readout Electronics Design

The UT has a significantly high occupancy, with the hottest chip requiring a data rate of about 9.0 Gbps. In total, **the UT has a data rate of about 6.8 Tbps**.

Fig. 7 shows an illustrative plan, based on simulation studies at the peak luminosity, of how many lpGBT readout links (e-links) will be required on the chips in different regions of the detector.

- The e-links of lpGBT can be set to **1.28, 0.64, or 0.32 Gbps** bandwidth.
- The hottest chip needs at least **8 e-links of 1.28 Gbps** for event data.
- In the outer regions of each plane, **one link of 0.32 Gbps** bandwidth is sufficient. Thus dual-modules can be constructed for 28 sensor chips that share a single lpGBT.
- In total, about **1888 event data lpGBTs** are deployed. An extra **1312 lpGBTs** are used for fast and slow control.



Ring	5	4	3	2	1
e-links / chip	1	1	1	1-3	2-7
Gbps / e-link	0.32	0.64	1.28	1.28	1.28
lpGBT / module	0.5	1	2	7	14/10
Num of modules	1312	240	80	64	32
Num of lpGPTs	656	240	160	448	384

Fig. 7: The lpGBT allocation and configuration plan.
Only lpGBTs for event data are listed

THANKS !

If you have any questions,
please mail me by zouquan@ihep.ac.cn