Characterization and operation of ATLASPix3

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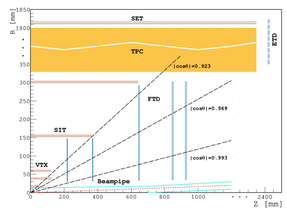
Abstract

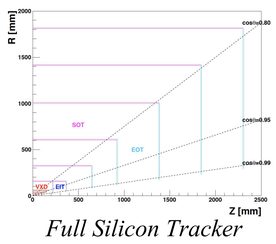
The CEPC is proposed as an $e+e-$ collider and operates at center-of-mass energy of 90–240 GeV to produce Z (around 91.2 GeV), W (around 160 GeV), and Higgs bosons (240 GeV). For the resolution/multiple scattering requirement (especially for momentum measurement $\sigma_{1/pt} = 2 \times 10^{-5} \oplus \frac{1 \times 10^{-3}}{p \sin^{3/2}\theta}\ GeV^{-1}$) and the financial constraint, the CEPC physics program demands a high-resolution, fine-pitch, low-material, fast-readout and economical tracking system with a large-area coverage, and the monolithic pixel sensor with the High Voltage Metal-Oxide-Semiconductor (HVCMOS) technology has the potential to satisfy requirements. Latest development based on ATLASPix3 sensor prototypes will be reported, including the lab test setup and cosmic ray test based on telescope module and the trimming optimization method at the software level.

Introduction

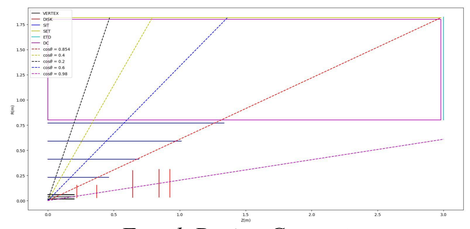
☐ Si Tracker for CEPC



Baseline Design (TPC/Si)



Full Silicon Tracker



Fourth Design Concept

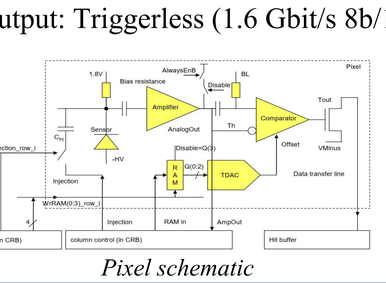
To address the physics requirements of the CEPC, a baseline and two alternative tracker designs as shown in the figure above. They all have some pros and cons, but all of them use large area silicon. Over 70m² for silicon + TPC/DC designs, and about 140m² for full silicon design. For silicon sensor, HVCMOS technology with an industrial process is an economical and effective candidate.

☐ Sensor technology

The High-Voltage CMOS pixel sensor ATLASPix3 designed by KIT, and have two versions (ATLASPix3.0 and ATLASPix3.1) now

- Pixel size 50 × 150 µm² (or smaller)
- 132 columns × 372 rows (reticle size 20.2 × 21 mm²)
- 25ns timing compliant
- TSI 180 nm process on 200 Ωcm substrate
- Pixels contain amplifiers and comparator with threshold tune circuit
- Material budget for tracker layers: ~0.65% (TPC/Si)/, ~1% (Full Si) X0 / layer
- Data output: Triggerless (1.6 Gbit/s 8b/10b) /triggered (1.28 Gbit/s 64b/66b)

HV-CMOS structure



Pixel schematic

Block scheme of the pixel matrix and column circuits

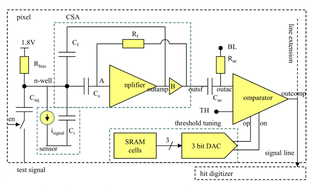
Trimming

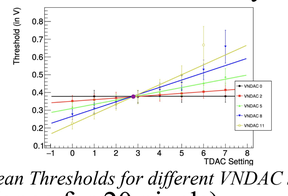
☐ To equalise the detection thresholds of the pixels

☐ Done by the in-pixel tuning circuits by varying the TDAC(tuning DAC) value

- Each pixel contains a 3 bit TDAC and a disable bit
- The correlation between TDAC and the threshold is linear
- The parameter VNDAC adjusts the amount of current drained by the TDAC

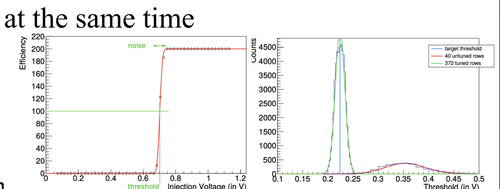
☐ Steps

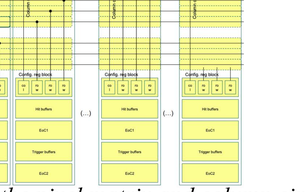




Mean Thresholds for different VNDAC setting

- Configure injection and measure scurves (once for 20 pixels)
  - Configure injection to activate pixels
  - Measure scurves for all activated pixels of the chip at the same time
- Get target threshold
  - Target thresholds are $\mu+3\sigma$ of untuned distribution
- Fit scurve to get the threshold
- Determine the best TDAC value for each pixel through a binary search





☐ Optimization on trimming duration

Trimming the whole chip took a lot of time (7.5 hours)

- Time duration of each process:
  - Configure injection (2ms for one time) and fit scurve (1ms for one scurve) are fast
  - Measure scurves (2s for one time) took a lot of time
- Approaches of optimization:
  - Increase the number of the max simultaneous pixels
  - Reduce the number of pixels with TDAC = 7 (0) through setting a lower (higher) target threshold
  - Add a mode to customize the target threshold in software
- 7.5 hours to 5.5 hours when max simultaneous pixels (20 to 22) and target threshold at (1% to 0.1%) of untuned distribution

Lab test set up

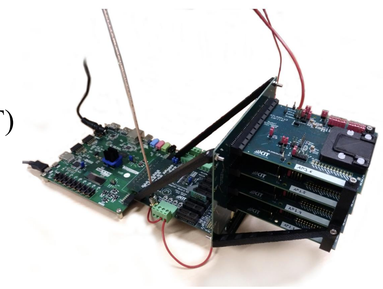
ATLASPix3 – Working with the GEneric Configuration and COntrol System (GECCO) Setup

GECCO can be used with a single board or 4 boards (telescope configuration)

☐ Hardware

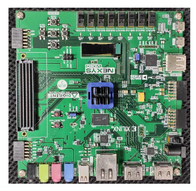
- Telescope module

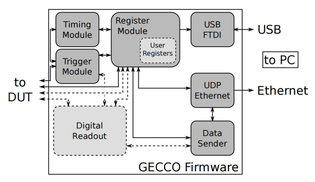
  One GECCO board can readout four sensors
  - DUT (Device Under Test) Carrier boards (KIT)
  - Telescope board (KIT)
  - GECCO board (KIT)
  - NexysVideo board (Digilent)



☐ Firmware

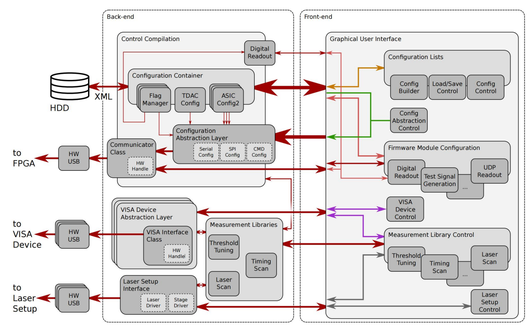
- The target device is the Digilent NexysVideo board
- Program FPGA via Vivado
- Contents of base project:
  - USB communication with PC
  - Communication protocol with registers read and writable from PC
  - Timing modules for test signal generation
  - Data sender module for Gigabit Ethernet





☐ Software

- Based on C++ with Qt framework
- Communication via USB is implemented, user just calls read or write methods with register address
- Contents of base project:
  - Configuration Data Containers
  - Configuration Abstraction Layer
  - Communication with FPGA
  - Digital Readout of the DUT
  - Measurement and Test Routines
  - User Interface and Transmission

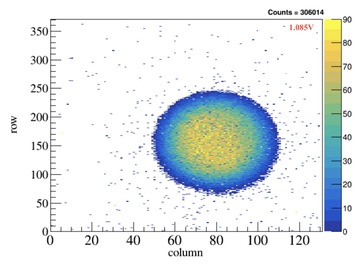


Radioactive Source Test: Fe55 (5.9keV EC)

☐ Use single chip module

☐ To calibrate the Threshold with Energy

☐ Tape the source at the back side of the chip (with collimation)

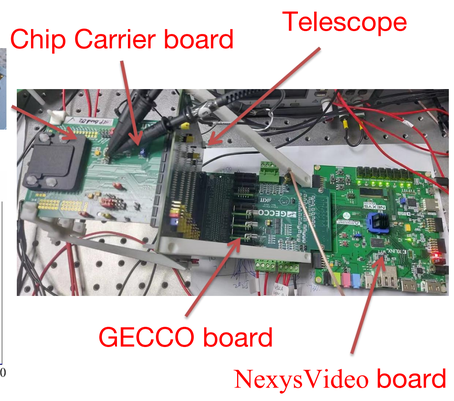


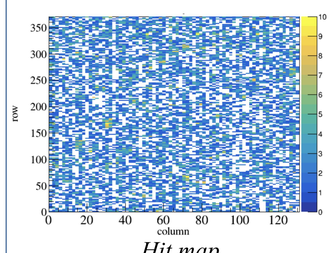
Hit map

Cosmic Ray Test

☐ Use telescope module with L4 alone

- ATLASPix3.1 for 24 hours





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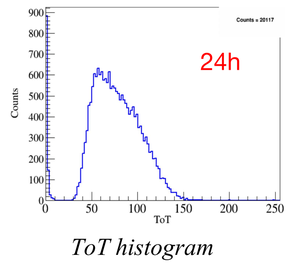

ToT histogram

The 2022 International Workshop on the High Energy Circular Electron Positron Collider, 24-28, October, 2022