Characterization and operation of ATLASPix3

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on behalf of the CEPC silicon tracker team

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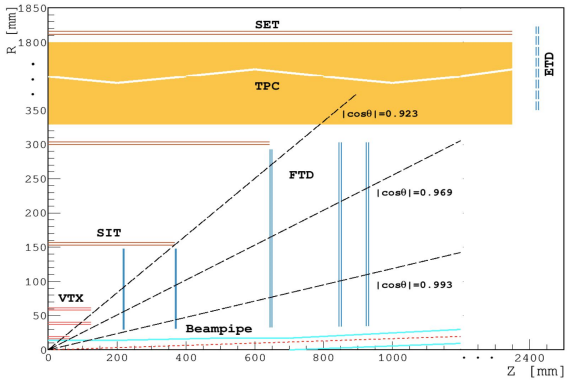
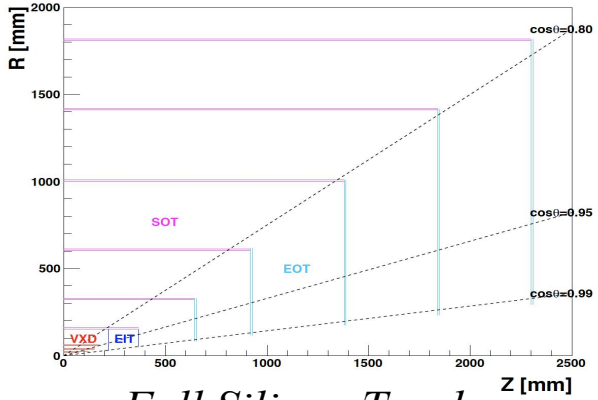
Silicon Tracker for CEPC

To address the physics requirements of the CEPC, a baseline and two alternative tracker designs are being considered

- Baseline Tracker Design
  - Vertex detector (VXD) with six layers
  - Time Projection Chamber (TPC)
  - Two inner and one outer barrel layers (SIT and SET)
  - Five disks in forward region (FTD)



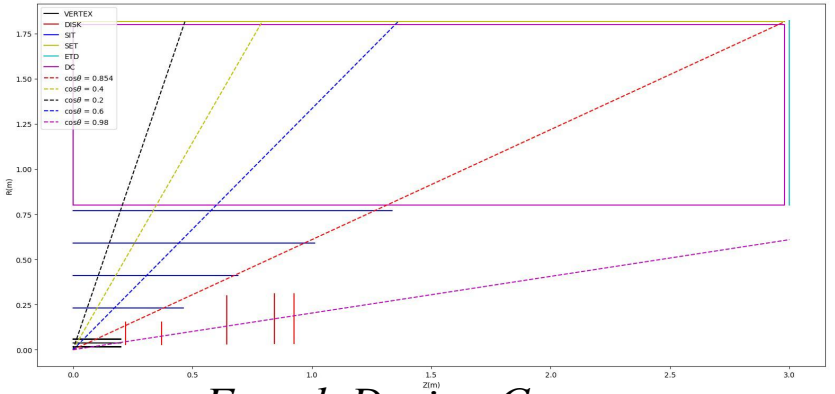
Baseline Design (TPC/Si)



Full Silicon Tracker

- Full Silicon Tracker Design
  - Vertex detector (VXD) with six layers
  - Silicon Tracker (SOT, EIT and EOT)

- Fourth Design Concept
  - Similar but not identical VXD with five layers
  - Drift Chambre (DC)
  - Outer silicon wrapper



Fourth Design Concept

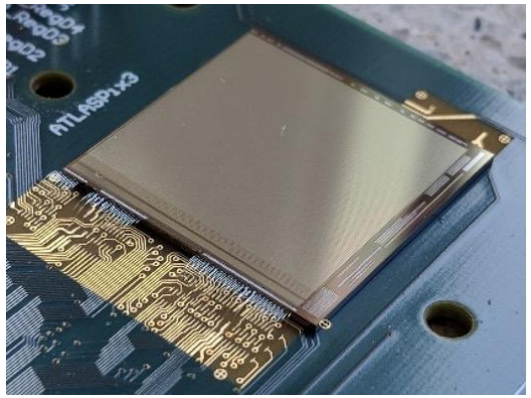
- All of them use large area silicon (Over 70m² for silicon + TPC/DC designs, about 140m² for full silicondesign)
- HVCMOS technology is an economical and effective candidate!

ATLASPix3 – Working with the GECCO Setup

- ATLASPix3

  The High-Voltage CMOS pixel sensor ATLASPix3 designed by KIT, and have two versions(ATLASPix3.0 and ATLASPix3.1) now

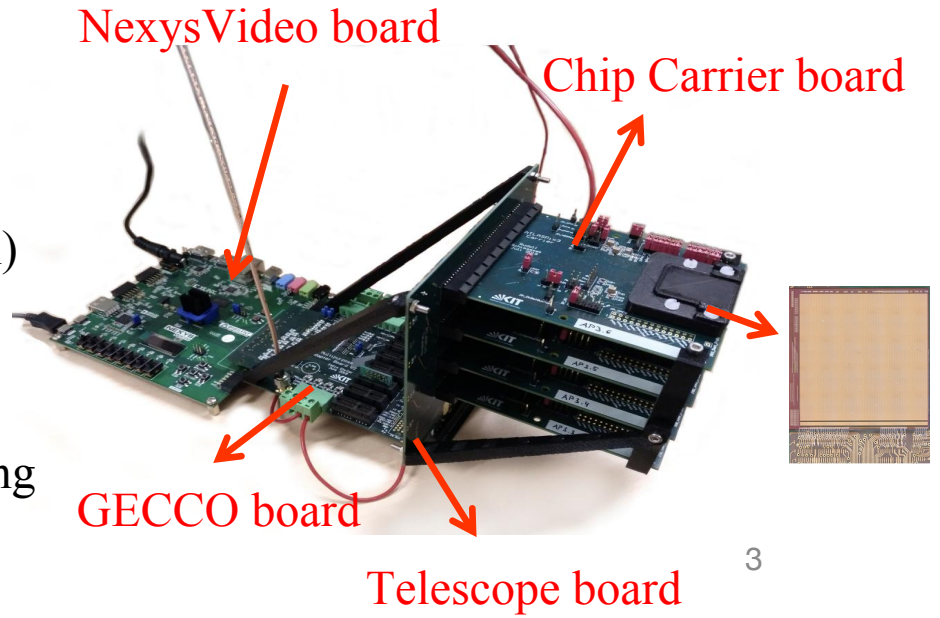
  - Pixel size: 50 × 150 μm^2(or smaller)
  - 132 columns × 372 rows (reticle size 20.2 × 21 mm^2)
  - Pixels contain amplifiers and comparator with threshold tune circuit
  - Data output: triggerless(1.6 Gbit/s 8b/10b) /triggered(1.28 Gbit/s 64b/66b)
  - 25ns timing compliant
  - TSI 180 nm process on 200 Ωcm substrate



- Readout using GEneric Configuration and COntrol System (GECCO)

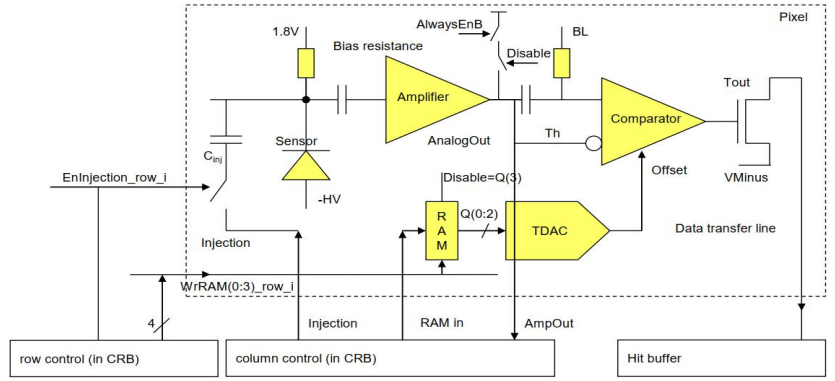
  GECCO can be used with a single board or 4 boards (telescope configuration)

  - Telescope module
    - One GECCO board can readout four sensors
    - KIT produced telescope cards carrying 4 sensors with ~2.5 cm spacing

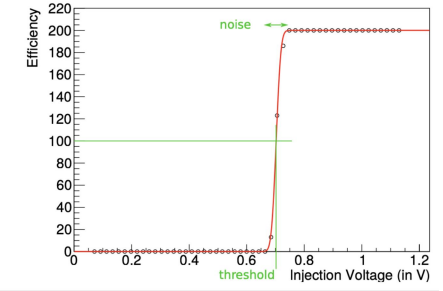


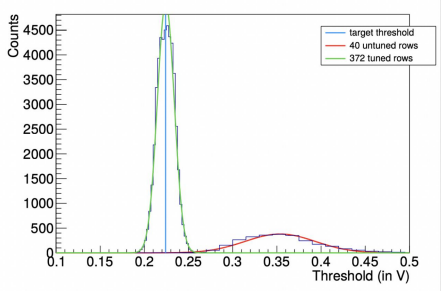
Trimming

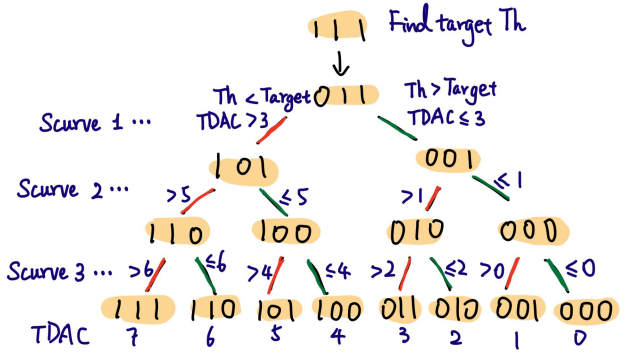
- To equalise the detection thresholds of the pixels
- Done by the in-pixel tuning circuits by varying the TDAC(tuning DAC) value
  - Each pixel contains a 3 bit TDAC and a disable bit
  - The correlation between TDAC and the threshold is linear
  - The parameter VNDAC adjusts the amount of current drained by the TDAC



- Steps
  - Configure injection and measure scurves (once for 20 pixels)
    - Configure injection to activate pixels
    - Measure scurves for all activated pixels of the chip at the same time
  - Get target threshold
    - Target thresholds are $\mu+3\sigma$ of untuned distribution
  - Fit scurve to get the threshold
  - Determine the best TDAC value for each pixel through a binary search



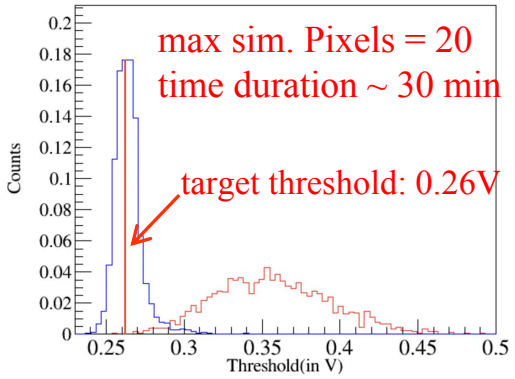


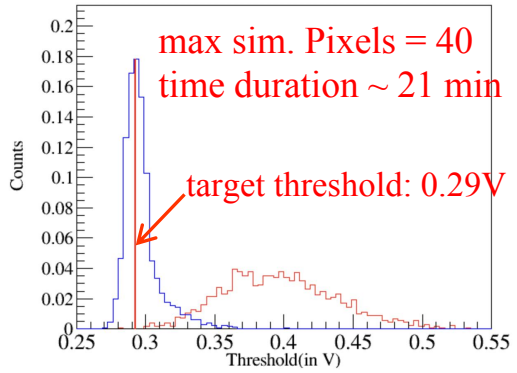


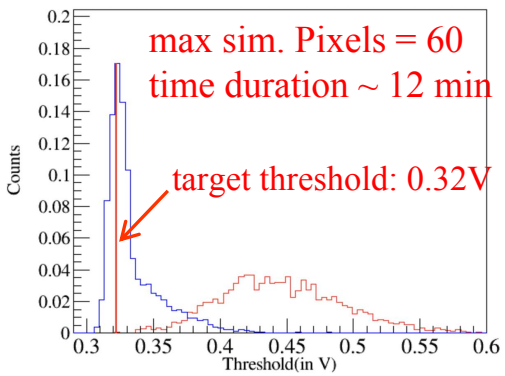
Optimization on trimming duration

- Trimming the whole chip took a lot of time
  - 7.5 hours when max simultaneous pixels = 20 and target threshold at 1% of untuned distribution
- Time duration of each process
  - Configure injection (2ms for one time) and fit scurve (1ms for one scurve) are fast
  - Measure scurves (2s for one time) took a lot of time
- Approaches of optimization
  - Increase the number of the max simultaneous pixels

  (Caveat, the signal size of the charge injection is affected when increase the number of pixels measuring at once)
  - Reduce the number of pixels with TDAC = 7 (0) through setting a lower (higher) target threshold
  - Add a mode to customize the target threshold
- 5.5 hours when max simultaneous pixels = 22 and target threshold at 0.1% of untuned distribution
- Subset: conducted for 3600 pixels:

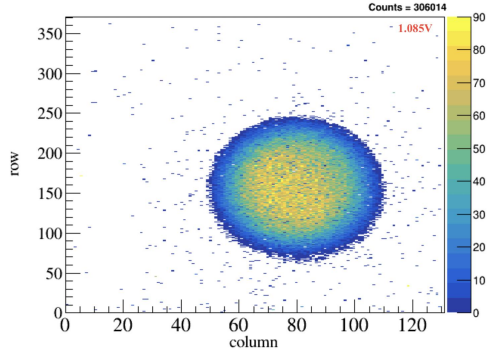






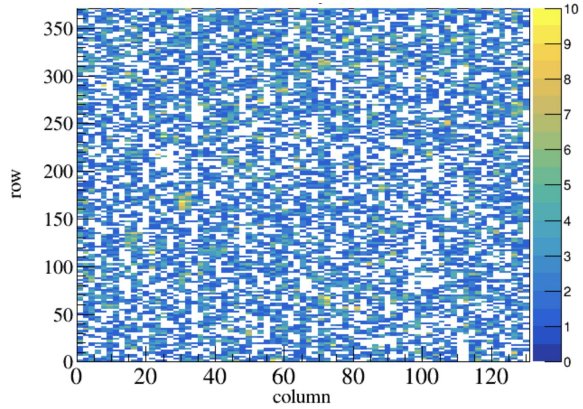
Response of ATLASPix3 to radioactive source and cosmic rays

- Radioactive Source Test: Fe55 (5.9keV EC)
  - Use single chip module
  - To calibrate the Threshold with Energy
  - Tape the source at the back side of the chip (with collimation)

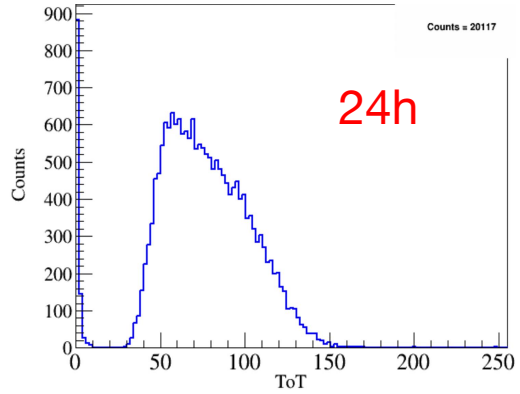


Hit map

- Cosmic Ray Test
  - Use telescope module
    - ATLASPix3.1 for 24 hours



Hit map



ToT histogram