DAQ towards a HVCMOS-based tracker for CEPC

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1. Introduction

High-voltage CMOS (HVCMOS) pixel sensor is a promising candidate for particle tracking in CEPC, due to its high performance and cost effectiveness. A HVCMOS pixel sensor is being designed specifically under 55 nm technology. A pixel matrix with dozens of columns and rows is integrated and each pixel is able to make time and charge measurement separately. The result is given out by a certain output port from the chip, which maximum data rate could reach up to Gbps.

To acquire the test data, a specific Data Acquisition System (DAQ) is also being designed based on the DAQ system for ATLASPix. The ATLASPix DAQ can support the data acquisition of four ATLASPix sensors simultaneously. It is highly automated and highly integrated which includes various functions such as configuration, decoding and trimming. For better expansibility and higher data rate, a new readout method based on a Gbps transceiver is proposed. This DAQ can achieve higher data rate to cope with the condition when more sensors are integrated, and meanwhile inherit the highly integrated characteristic of the previous one. This poster will give more introduction on CEPC HVCMOS DAQ.

2. Pixel Sensor for CEPC

HVCMOS pixel sensor is an advanced research area in particle tracking. HVCMOS pixel sensor is designed as an analog-digital mixed application specific integrated circuit (ASIC). A pixel matrix and readout circuit are integrated in a single chip. Comparing with the traditional readout method, pixel sensor can gives out hit information for each pixel point directly, instead of information with analog summation only from corners or edges. This readout method eliminates the error in hit position reconstruction process, which inevitably happens due to the analog circuit inconsistency. This advantage leads to a high performance of pixel sensor in particle tracking.

ATLASPix, which is designed under 180 nm technology, is one of the HVCMOS pixel sensor and it was initially designed for the upgrade of ATLAS Inner Tracker[1]. Based on ATLASPix, a prototype pixel sensor for CEPC (called CEPCPix in below) is being designed under 55 nm technology for the aim of researching its performance under a promoted technology.

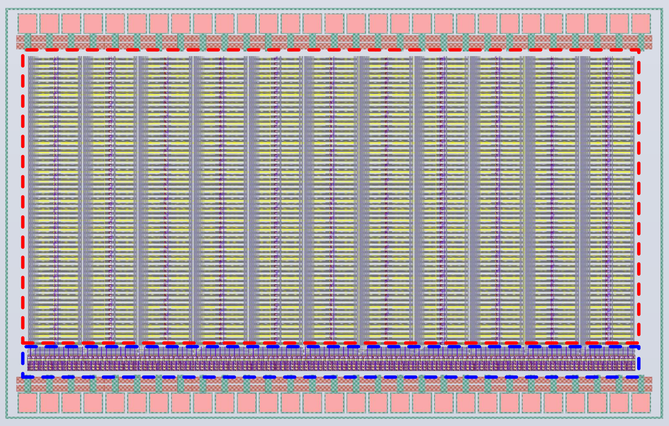

Fig. 1. Prototype layout of CEPCPix

The prototype layout diagram of CEPCPix is shown in Fig. 1. It consists of three parts, 1) the pixel matrix for time-over-threshold measuring of the particle track, 2) the digital logic for data serializing and transmitting, and 3) the control logic for configuration and debugging. The pixel matrix size is 60 row × 11 column while each pixel size is 252 μm × 22 μm. When a pixel is hit by particle, a current pulse is generated, amplified and sent to a comparator for over threshold detecting. A pulse is given out onto the hitbus which turns on the serializer to record the pixel address, together with timestamps of its leading and trailing edge. At the final end, the data is sent out through a serial transceiver with 8b/10b (or 64b/66b) coding. The configuration of CEPCPix is based on shift register chains. Debug mode, which allows self-generating hit pulse for trimming, is also compatible under different configuration.

3. DAQ Design for CEPCPix

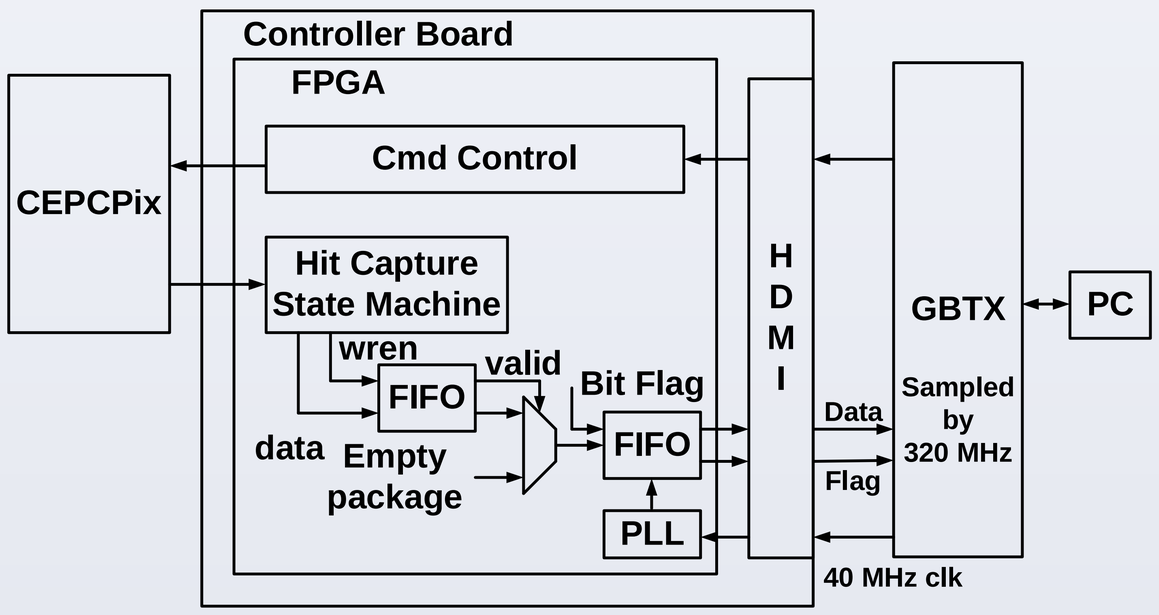

Fig. 2. DAQ hardware for CEPCPix

The block diagram of CEPCPix DAQ hardware is shown in Fig. 2. A subsidiary Field Programmable Gate Array (FPGA) is employed for data receiving from 4 sensors. A state machine is set to capture and assemble data package into certain order. The data is pushed into an asynchronous FIFO for clock domain crossing. When there is no hit data valid, an empty data package is sent out continuously for instead to keep the data stream speed as stable.

To adapt the system for more sensors, a high-speed data transmission tunnel has to be established. GBTX is a radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gbps user bandwidth) bidirectional optical links for data transmission. It can be employed for data aggregation from different subsidiary controller board. Controller boards and GBTX are connected by HDMI cables and the data can be sampled by 320 MHz clock at maximum. Finally, GBTX uploads the data to PC by optical fibers.

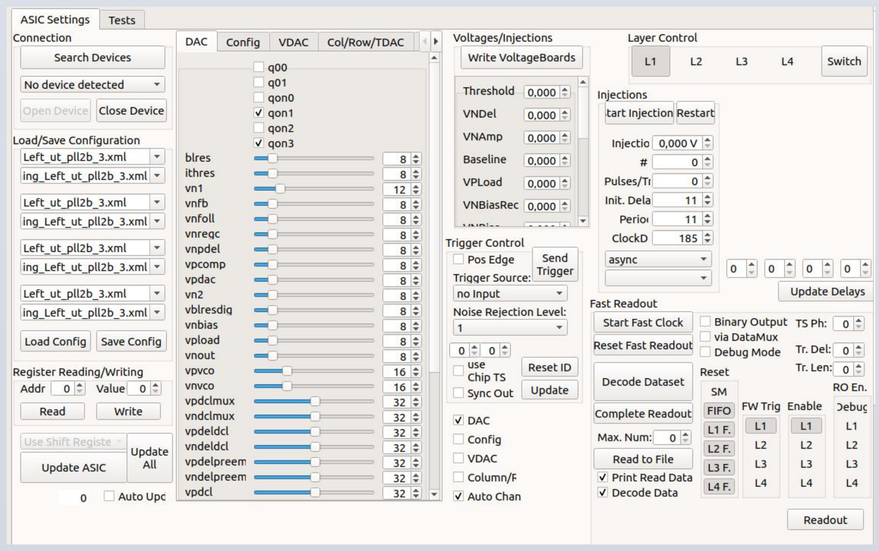

Fig. 3. DAQ software interface for controller board

Fig. 3 shows the software interface for controller board at present. Preset configuration files can be imported for setting the value of threshold voltage, bias voltage and working mode. The data readout function can either save raw data or the data already being decoded which give out the hit channel number and timestamps directly. In future, the interface between PC and GBTX will be integrated into the software to control more sensors simultaneously.

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