DAQ towards a HVCMOS-based tracker for CEPC

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CEPC SILICON TRACKER COMMUNITY

Pixel Sensor for CEPC - CEPCPix

▶ Pixel Matrix
- ◇ Designed in 55 nm technology
- ◇ 60 rows × 11 columns
- ◇ Pixel generate a negative pulse when hit

▶ Digital Readout Logic
- ◇ Hit pulse gives out pixel address and hitbus
- ◇ Hitbus signal starts the serializer for serial output
- ◇ LVDS output

▶ Configuration logic
- ◇ Shift register
- ◇ Partner clock and load latch signal for configuration stable
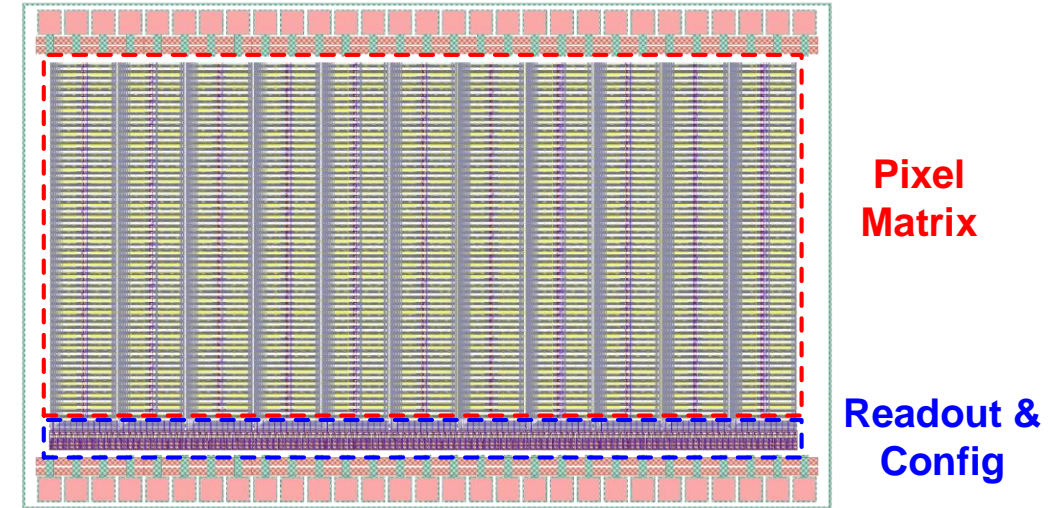
Pixel Matrix

Readout & Config

DAQ Design for CEPCPix - Hardware

▸ DAQ hardware consist of CEPCPix, Controller board and GBTX

▸ Controller Board

◇ Receive data from 4 CEPCPix, could be increased to 8

◇ Hit capture state machine for decoding LVDS data and package

◇ FIFO for crossing time domain from CEPCPix to local

◇ 2 stage FIFO for bit width adjustment
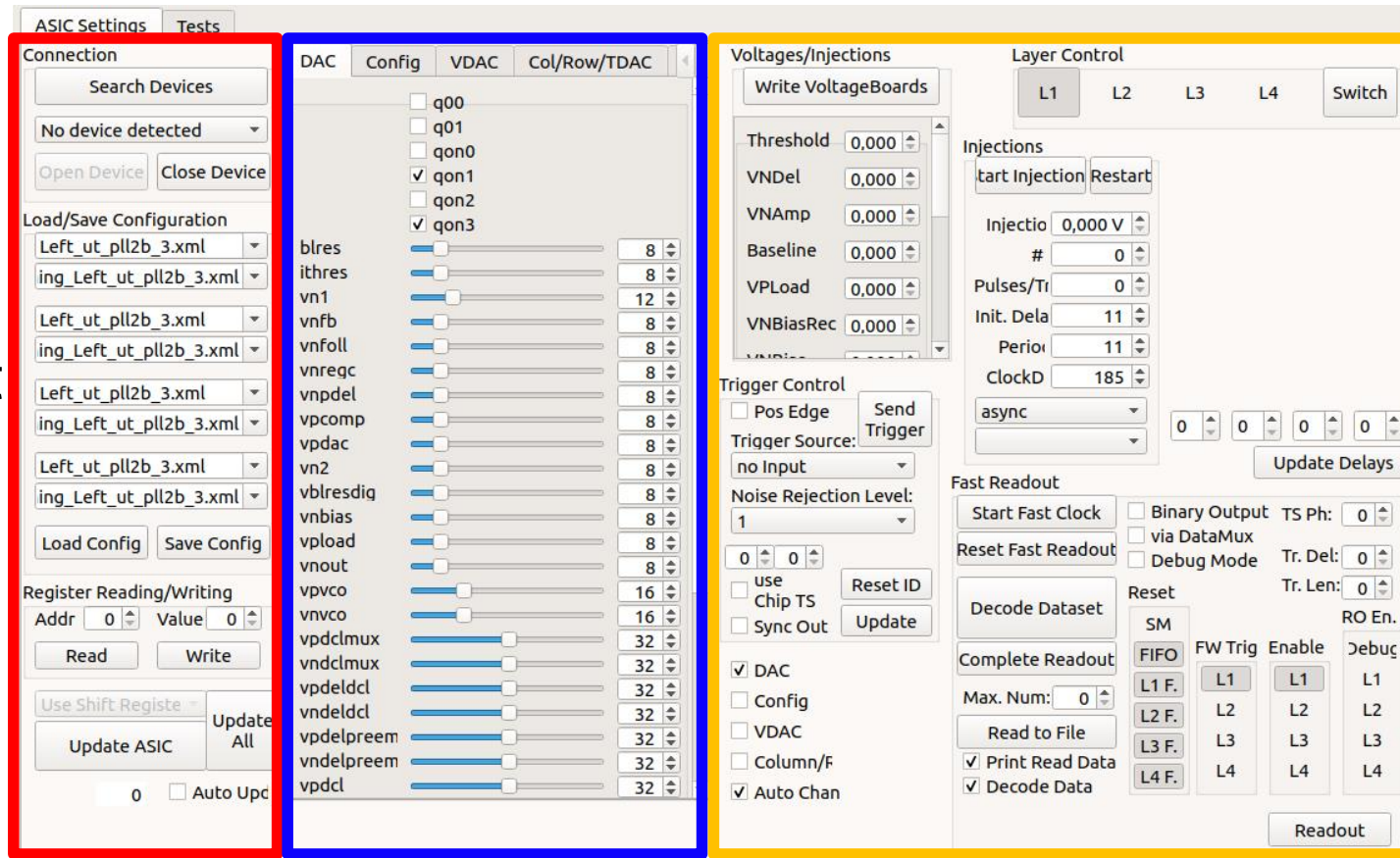
◇ Empty package when no hit data valid
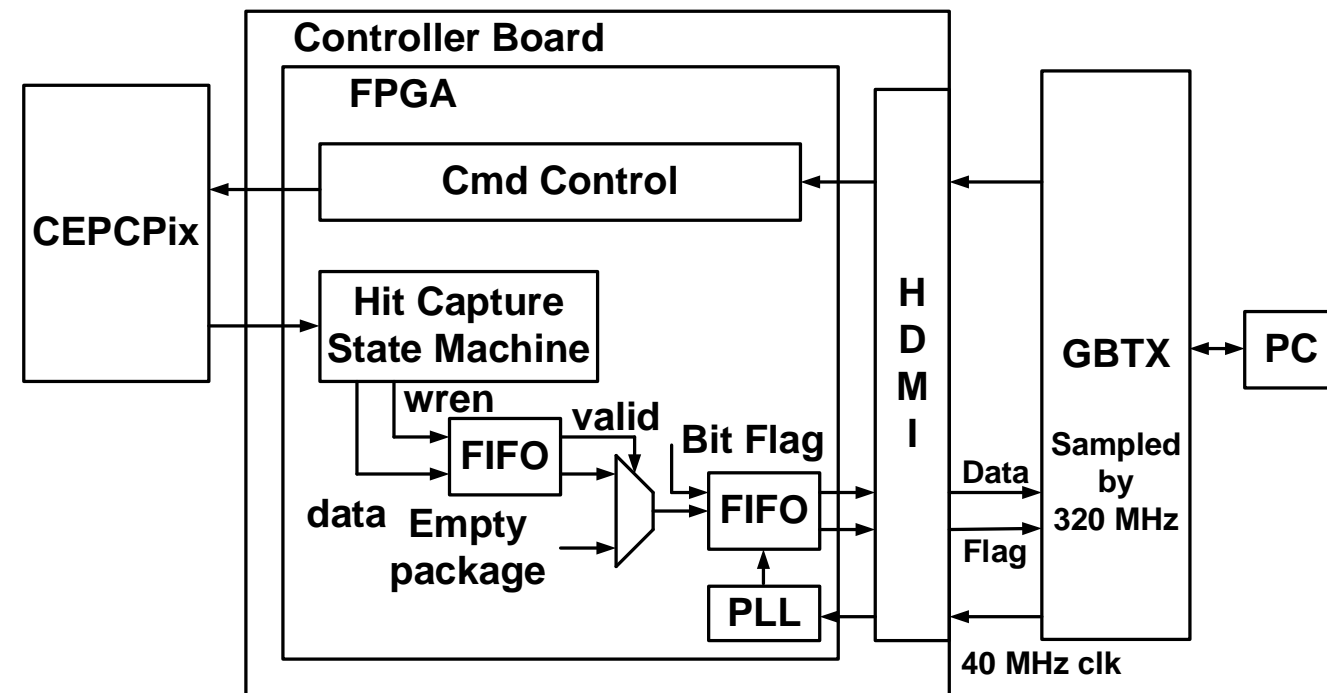
DAQ Design for CEPCPix - Hardware

▸ DAQ hardware consist of CEPCPix, Controller board and GBTX

▸ GBTX

◇ A radiation tolerant chip for high speed (3.2-4.48 Gbps user bandwidth) bidirectional data transmission

◇ Data, cmd, clk signal within a HDMI link

◇ Receive data and sampled with 320 MHz

◇ GBTX upload data to PC by optical fibers
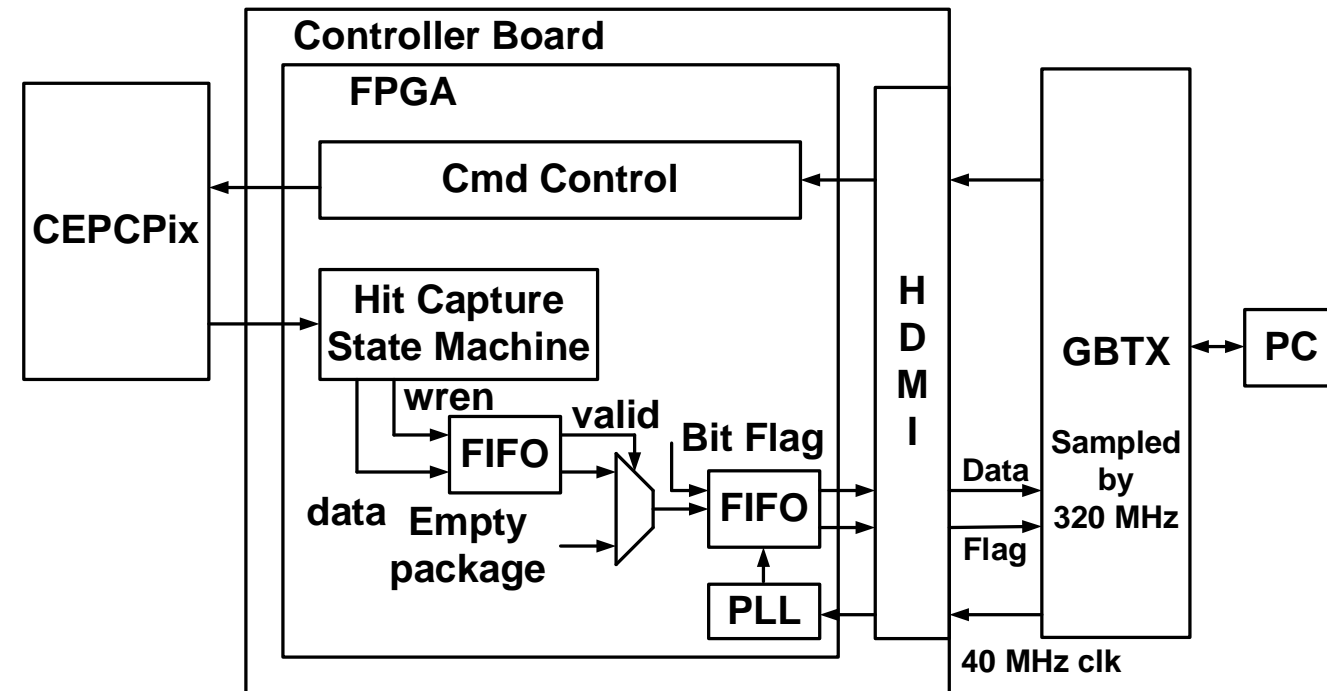
DAQ Design for CEPCPix - Software

▸ QTCreator platform based

▸ For 4 pixel sensor control and data receive at present

  ◇ Connection board for preset configuration parameter import and update config

  ◇ Setting board for adjusting each parameter, DAC, V_{th}…

  ◇ Readout board for setting data receive and decode mode

▸ To integrate the interface with GBTX in future

Connection   Setting   Readout