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The new LHCb GPU trigger

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From 2022 the LHCb experiment will use a triggerless readout system collecting data at an event rate of 30 MHz and a data rate of 4 Terabytes/second. A software-only High Level Trigger will enable unprecedented flexibility for trigger selections. During the first stage (HLT1), track reconstruction and vertex fitting for charged particles enable a broad and efficient selection process to reduce the event rate to 1 MHz. Tracking and vertexing at 30 MHz represents a significant computing challenge, and LHCb utilizes the inherent parallelism of the triggering process to meet throughput requirements with GPUs. A close integration with the DAQ and event building allows for a particularly compact system, with the GPUs hosted in the same servers as the FPGA cards receiving the detector data, which reduces the network to a minimum. This architecture also inherently eliminates latency considerations, allowing GPUs to be used despite the very high required throughput. We review the software and hardware design of this system, reflect on the challenges of developing for heterogeneous architectures, discuss how it meets LHCb's performance requirements, and show the commissioning status from LHC Run 3.

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