The CMS Level-1 Muon Trigger focusing on the RPC system

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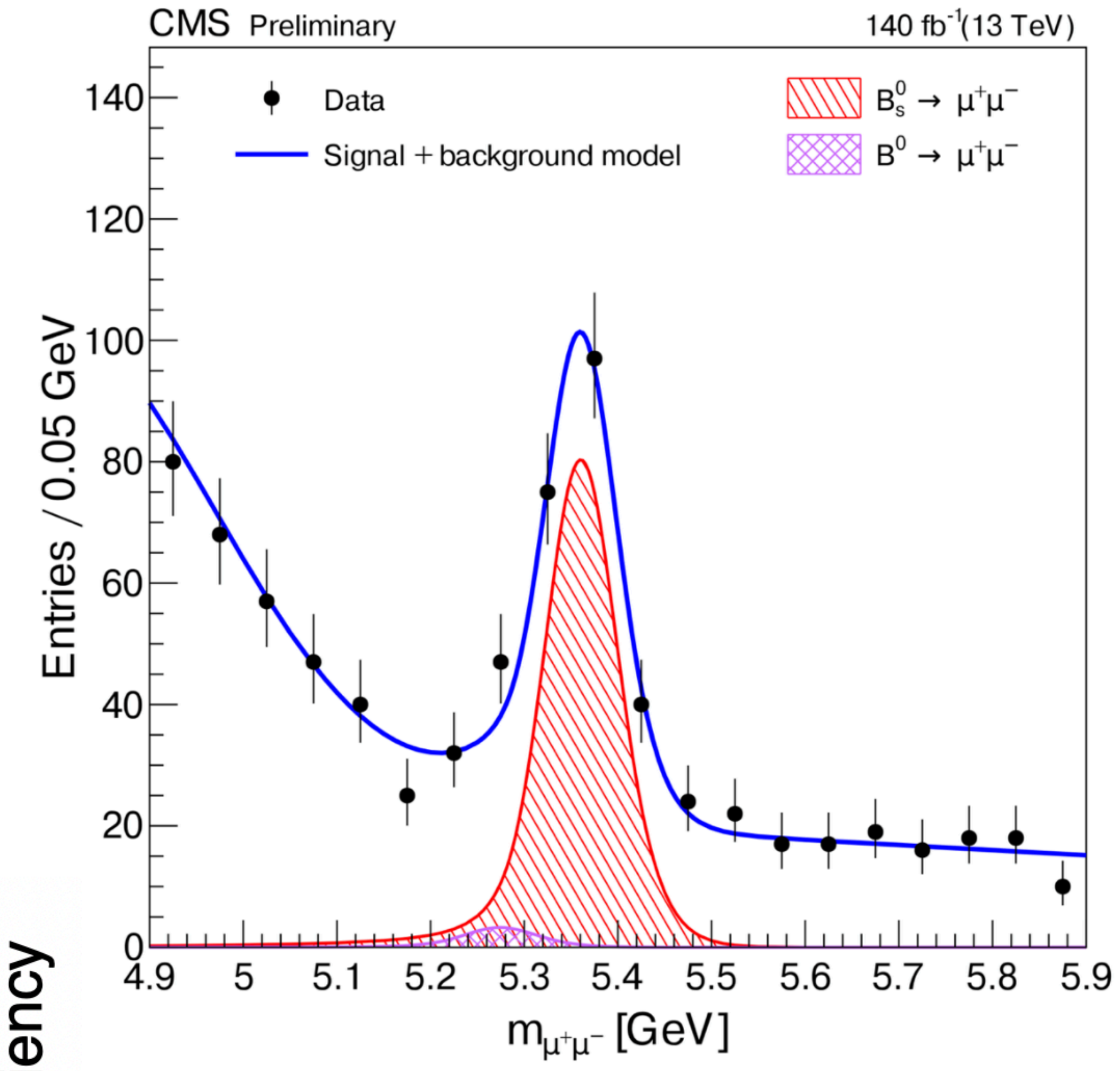
Physics Highlights

The Higgs boson was discovered via two-photon and four lepton decay modes in 2012 !

In July 2022, CMS makes the world's most accurate measurement of the decay of the B_s meson into a muon pair.



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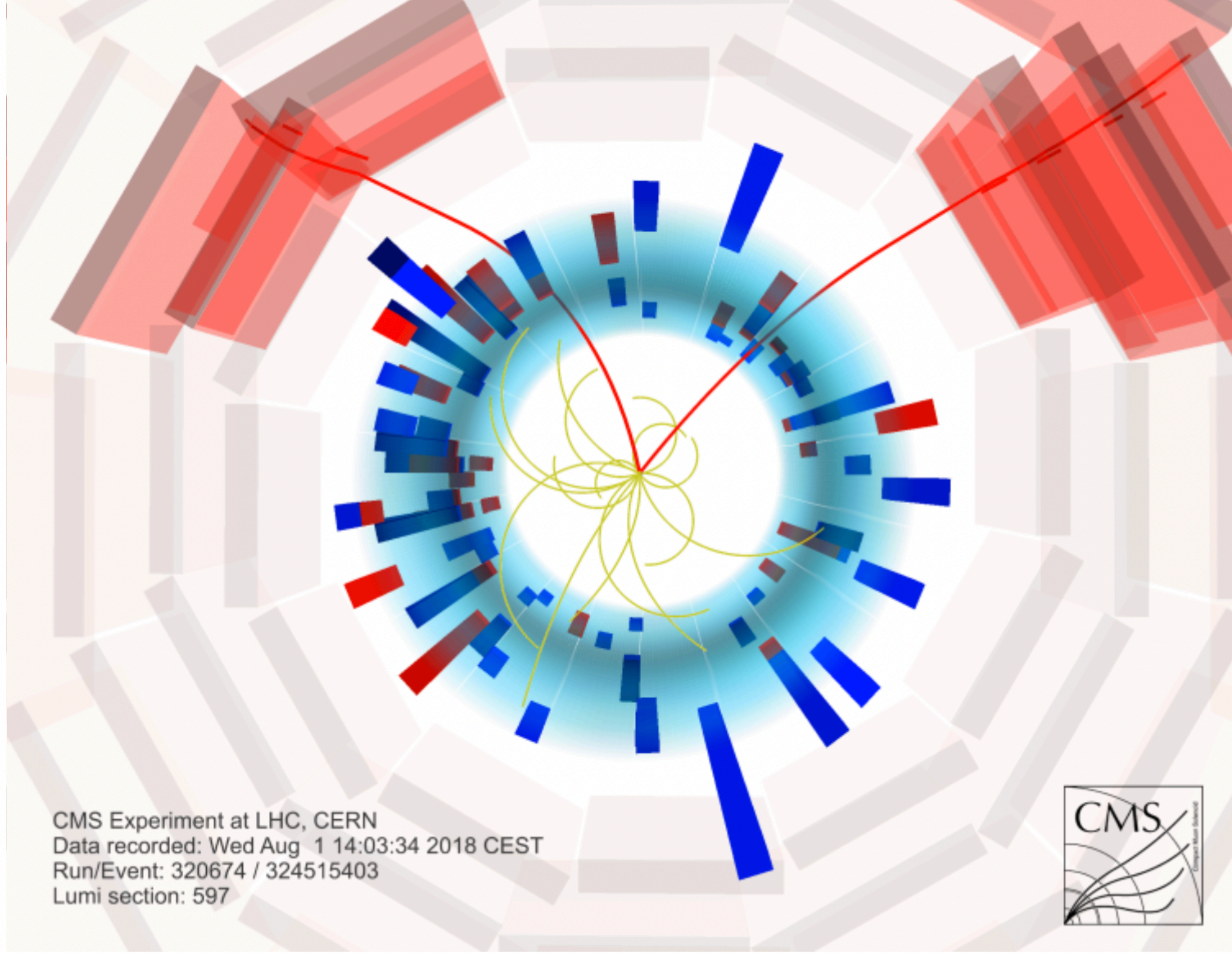
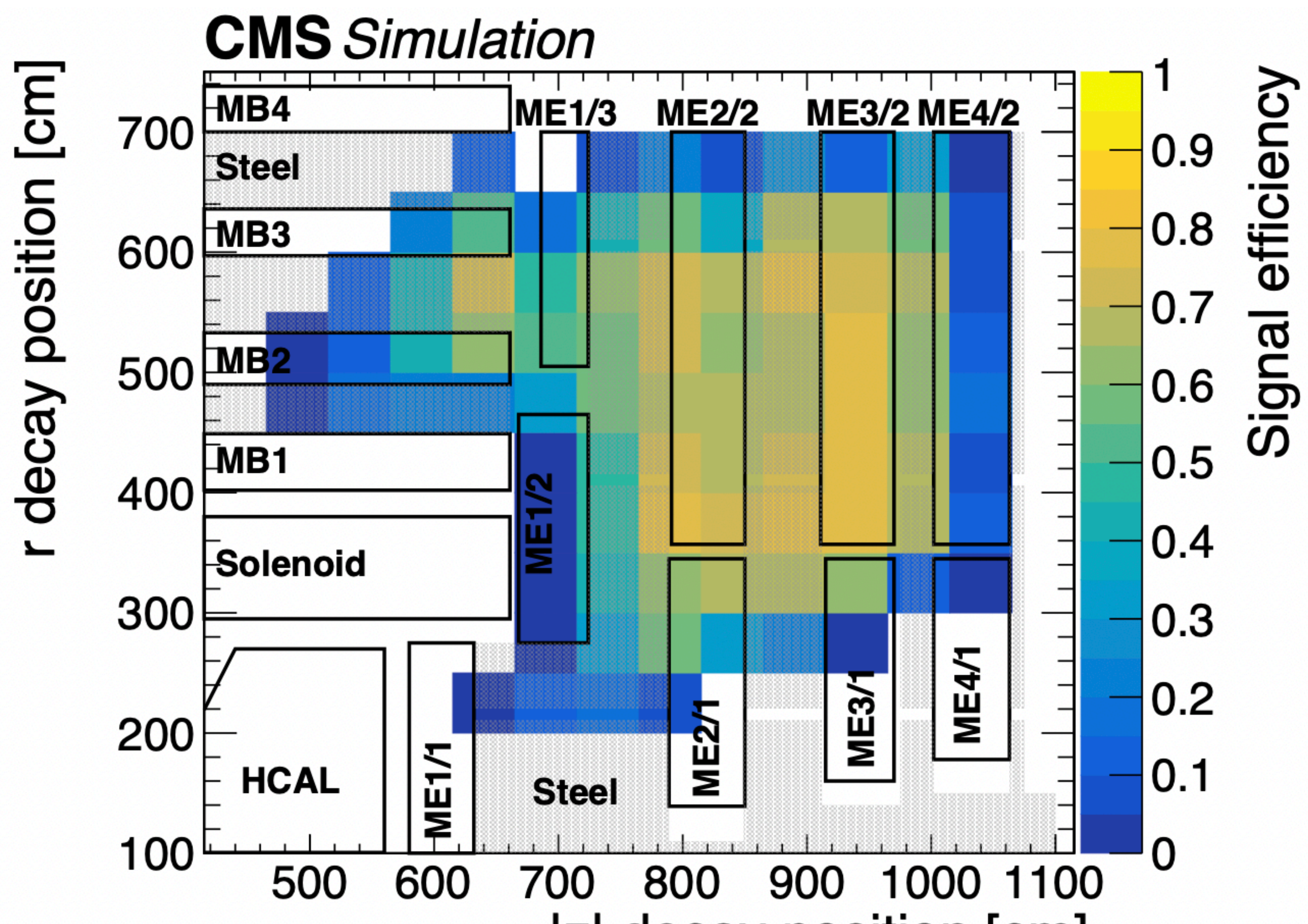




arXiv: 2107.04838

In December 2021, The first search at the LHC that uses a muon detector as a sampling calorimeter to identify showers produced by decays of LLPs. This search has been performed using the CMS Endcap Muon detectors.

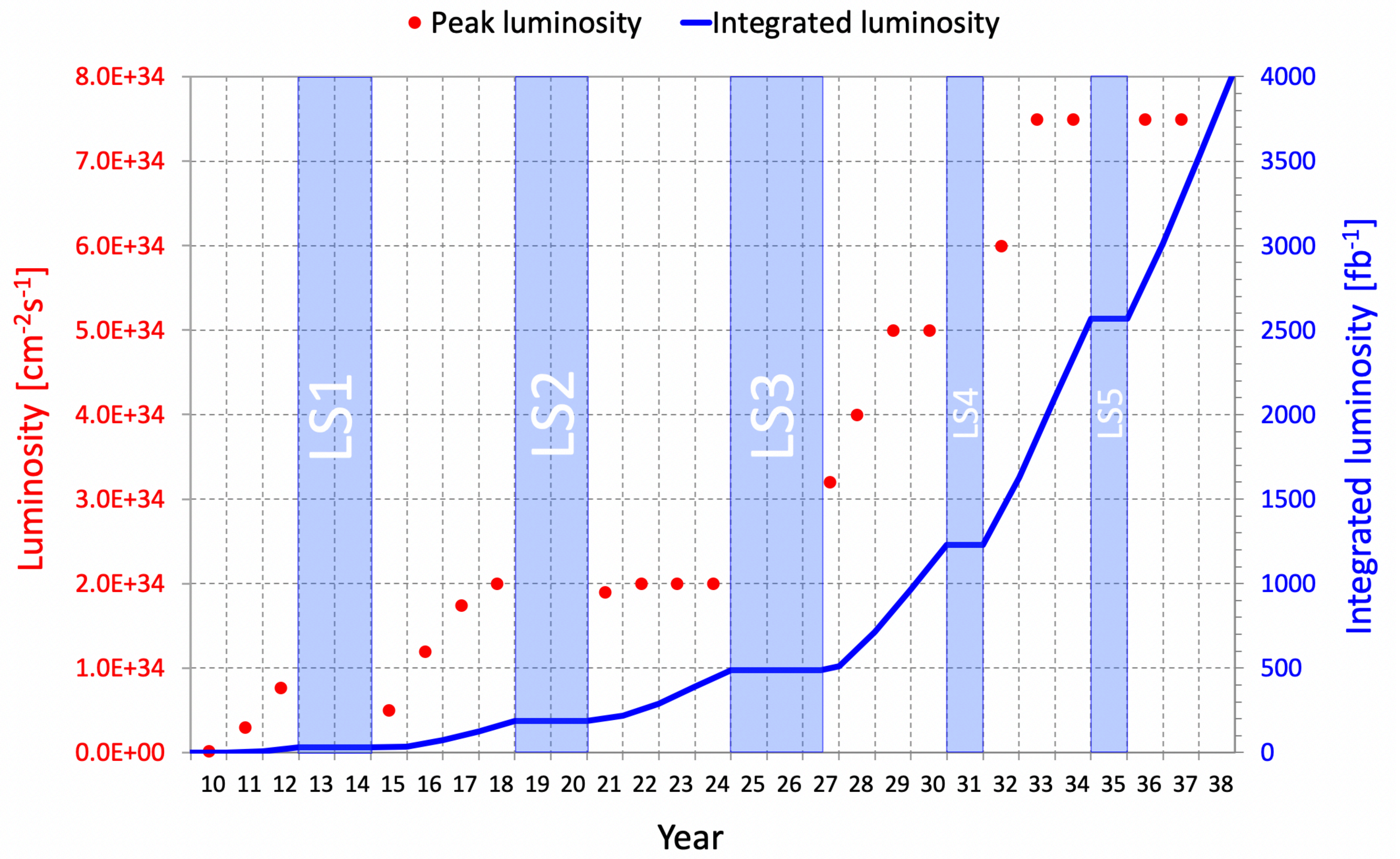
We need way more data to search for very very rare events : HL-LHC

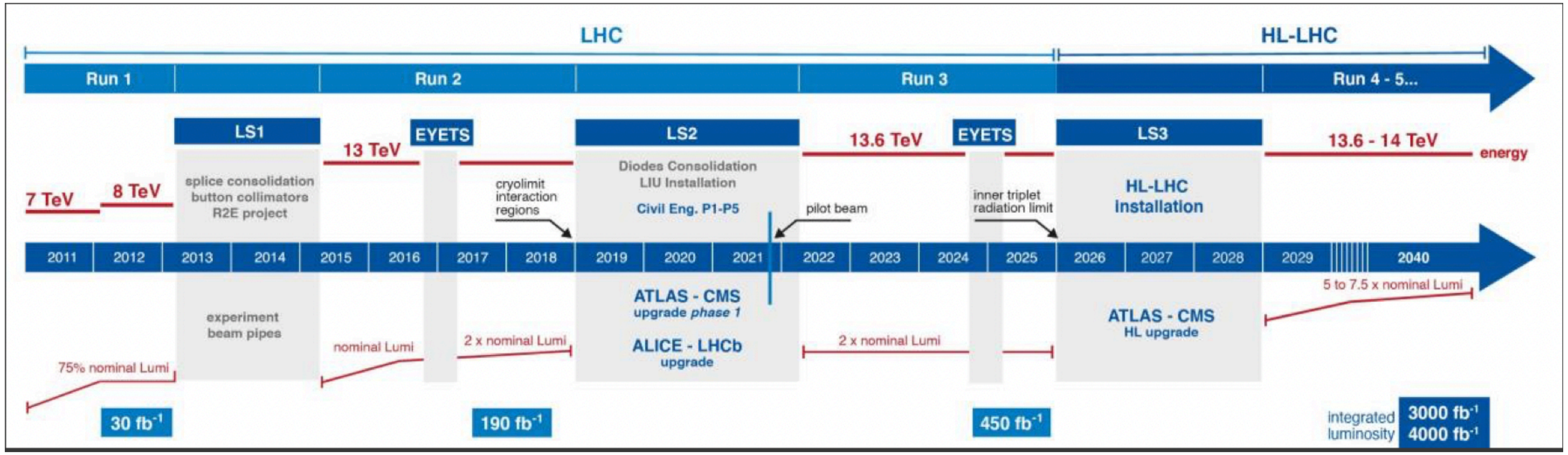
High Luminosity LHC: HL-LHC

LHC is being prepared to increase its integrated luminosity to around 3000 fb^{-1} to extend the sensitivity to new physics searches.

The center-of-mass energy is expected to be raised up to 14TeV.
> We are already taking data at 13.6 TeV.

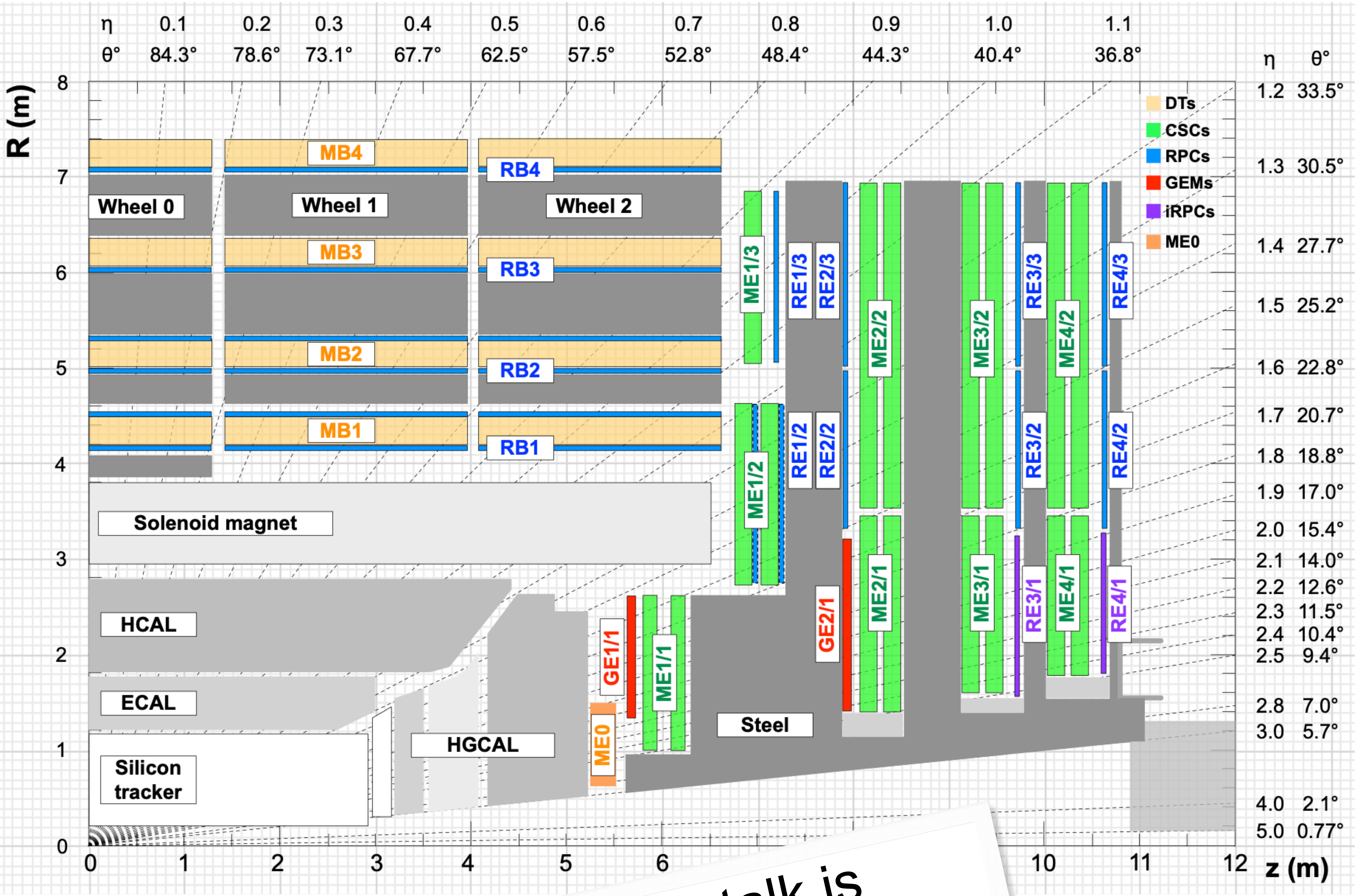
The current 'Phase-1' data taking period will end by the end of 2025 followed by a shutdown for the HL-LHC upgrade ending by the beginning of 2029.





Recipe for keeping the excellent performance in HL-LHC *in CMS Muon system*

- Repair / replace your aged detectors as well as its electronic components
- Update the trigger hardware and algorithms
    - Drift Tubes (DT)
    - Resistive Plate Chambers (RPC)
    - Cathode Strip Chambers (CSC)
- Make your readout electronics with deeper buffering and faster processing
- Add new detectors extending the eta coverage
    - Gaseous Electron Multipliers (GEM):
        - GE1/1 (already installed)
        - GE2/1
        - ME/0
    - Improved RPC (iRPC)
        - RE 3/1 , RE 4/1



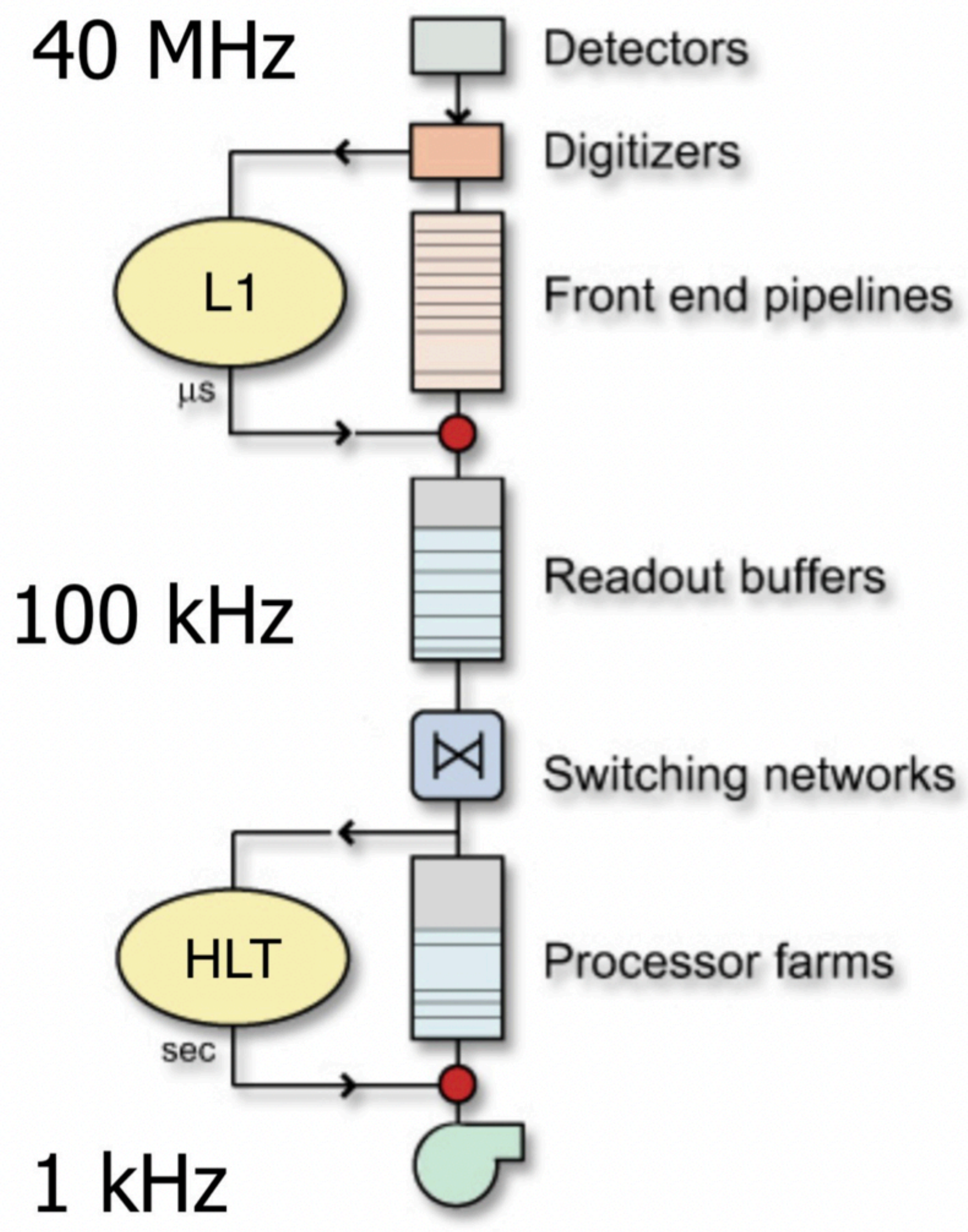
Focus of the talk is i/RPCs

CMS Trigger system

Phase I trigger system

CMS Trigger System is made of two components

- Level 1 Trigger (L1T)
  - Rate reduced by a factor 400
  - Decision taken in 3.6 μs
  - Custom hardware
  - Information from calorimeters and muon detectors
- High Level Trigger (HLT)
  - Rate reduced by a factor 100
  - Decision taken in hundreds of ms
  - Commercial server farm
  - Full detector information

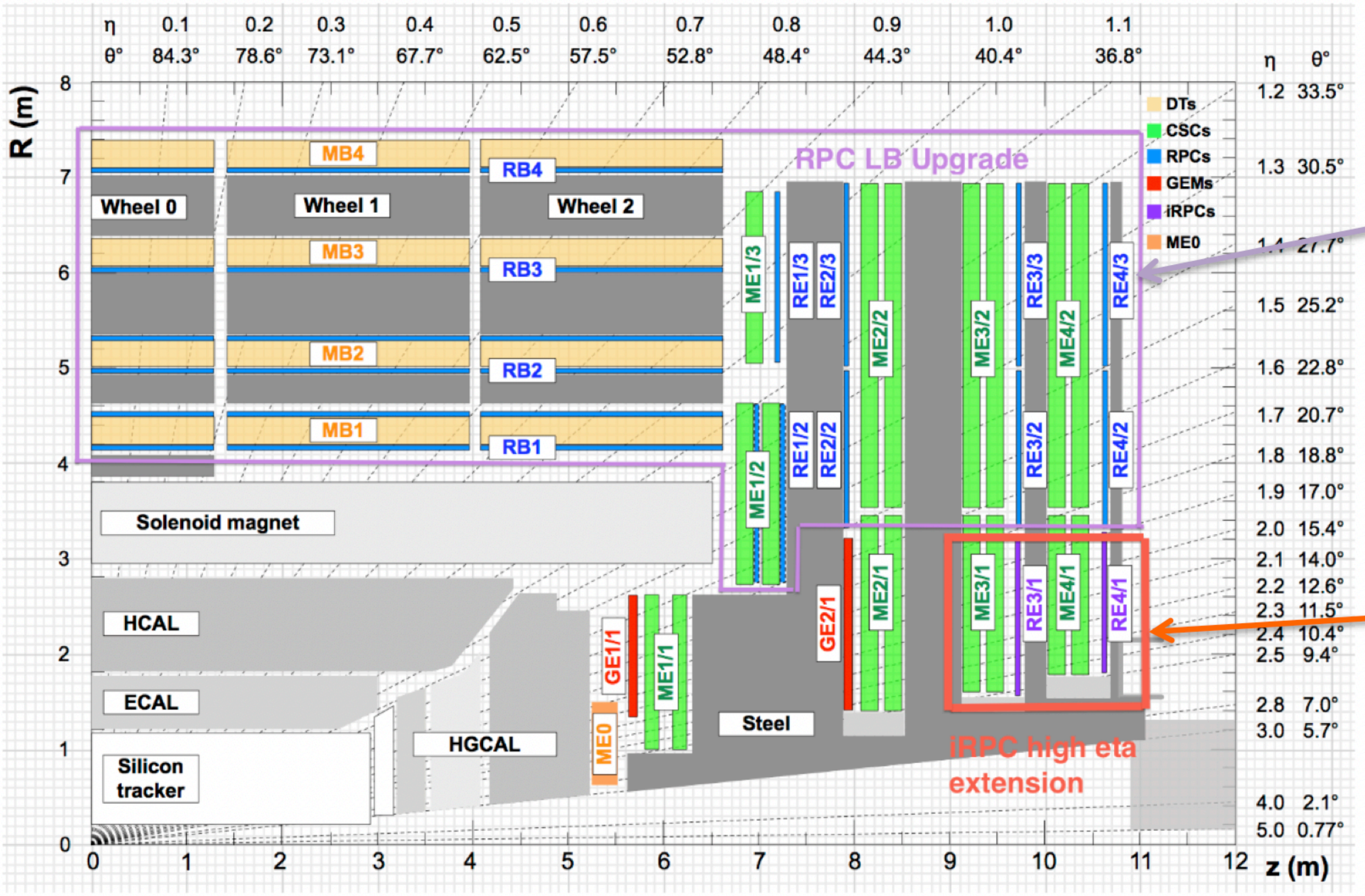


Phase II trigger system

Key aspects of the L1Trigger Upgrade

- 100 → 750 kHz **rate** to HLT
- 3.6 → 12.5 μs **latency**
- Refactored architecture
  - Merging sub-detectors information even earlier (DT and RPC **hits** available in the same boards)
- Increased **bandwidth**
- Availability of tracking information

RPC Upgrade Project

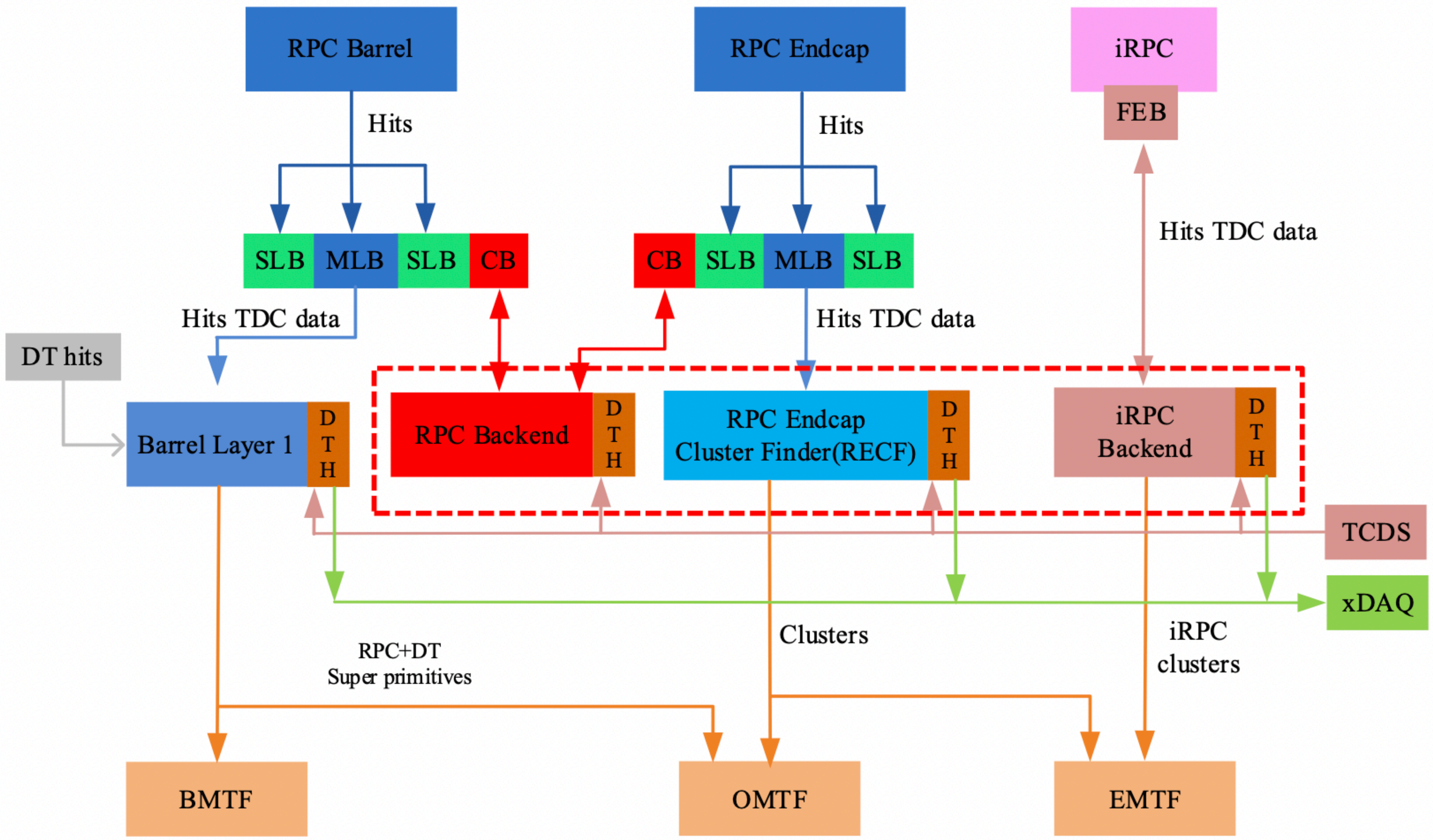


Upgrade of Link System to improve timing resolution for existing RPC system ($|\eta|<1.9$)

Extend the RPC coverage up to $|\eta|=2.4$ to restore redundancy in high eta region in stations 3 and 4

RPC Upgrade Project Trigger

- **iRPC backend:**
  - Fast/Slow control(TTC),
  - Monitor,
  - Data readout,
  - Trigger Primitive(Cluster) Generation
- **RPC Endcap Cluster Finder(RECF):**
  - Data readout,
  - Trigger Primitive(Cluster) Generation,
  - TP data Fanout
- **RPC backend:**
  - Fast control(TTC)
  - Slow control,
  - monitor,



SLB: Slave Link Board
MLB: Master Link Board
CB: Control Board
iRPC Hits: t1 and t2 to be transferred into Y position

RPC @ Barrel

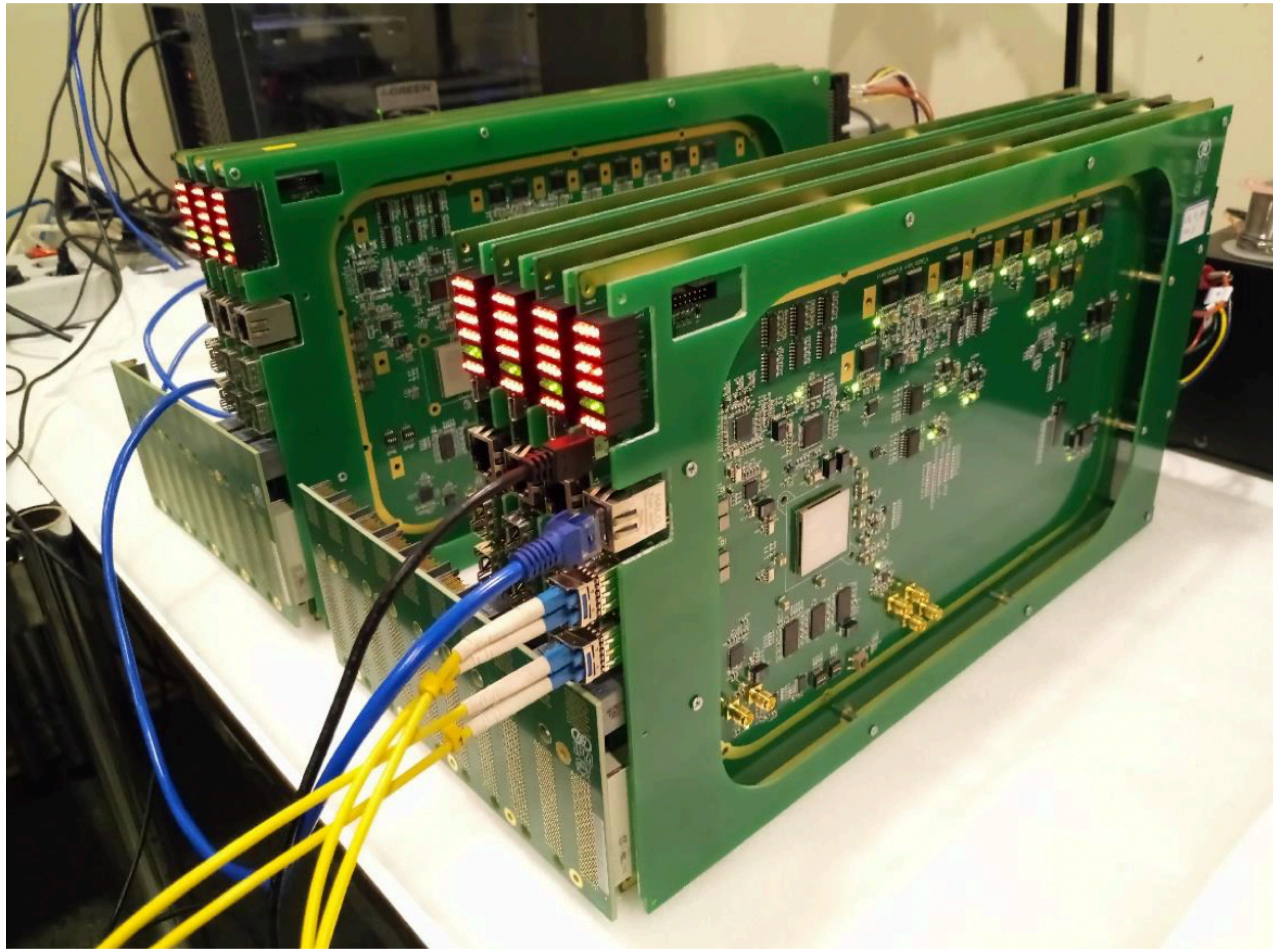
- The intrinsic time resolution of the RPC system: 1.5 ns
- To better exploit the time resolution and ensure the robustness of its readout during the HL-LHC era, the off-detector electronics (Link System) will be replaced during LS3.

- Level-1 Trigger : 40 MHz - > 640 MHz
  >introduction of sub-BX timing (1/16 Bx)

Expected maximum hit rate in RPC in Barrel at the HL-LHC conditions (3 safety factor): 600 Hz/cm^2

In general, a muon crossing an RPC chamber induces a signal in more than one strip.

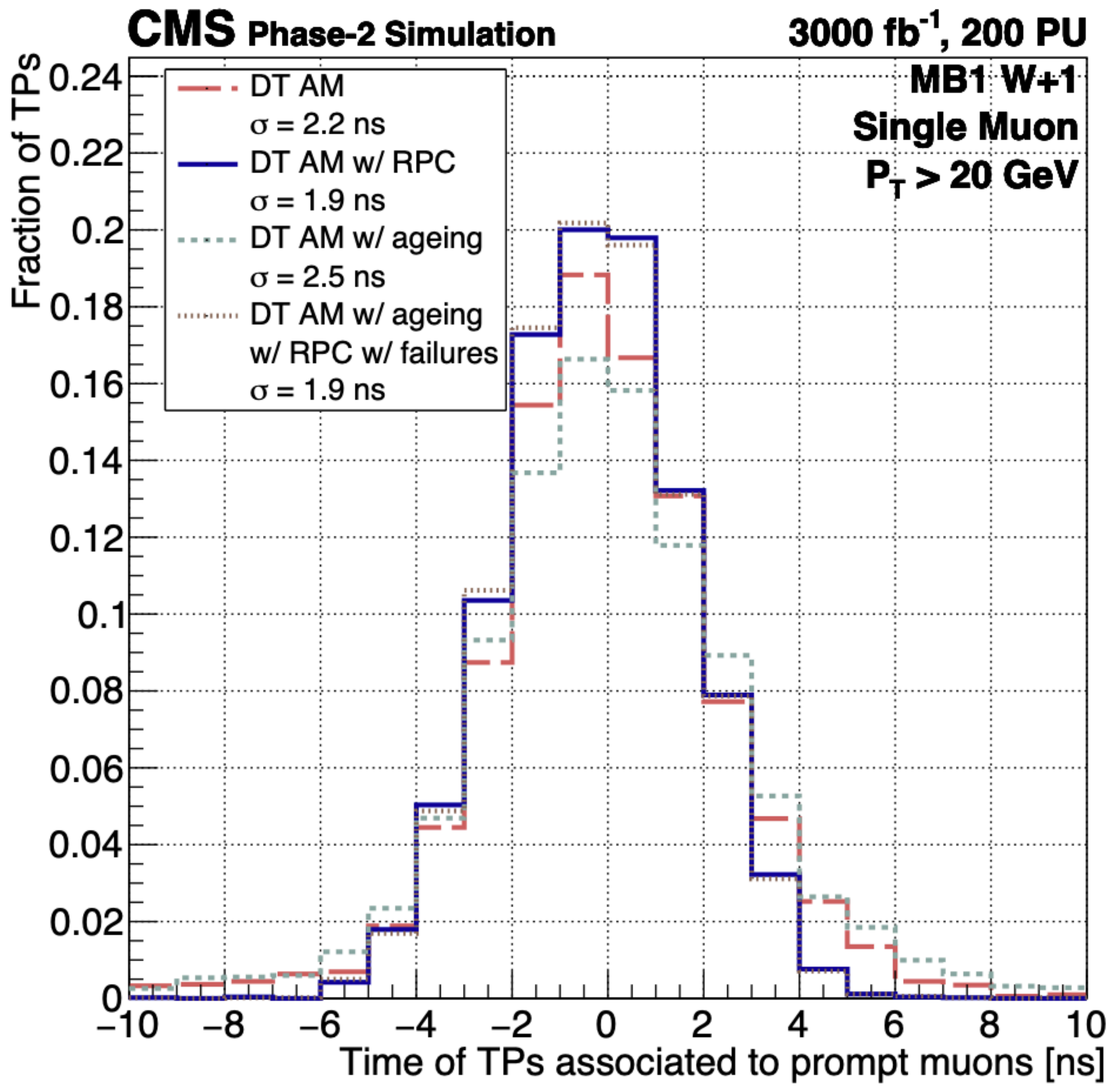
A clustering of the RPC single hits will be performed in the BMTL1 before using RPC information in the Level-1 trigger, together with the DT TP building.

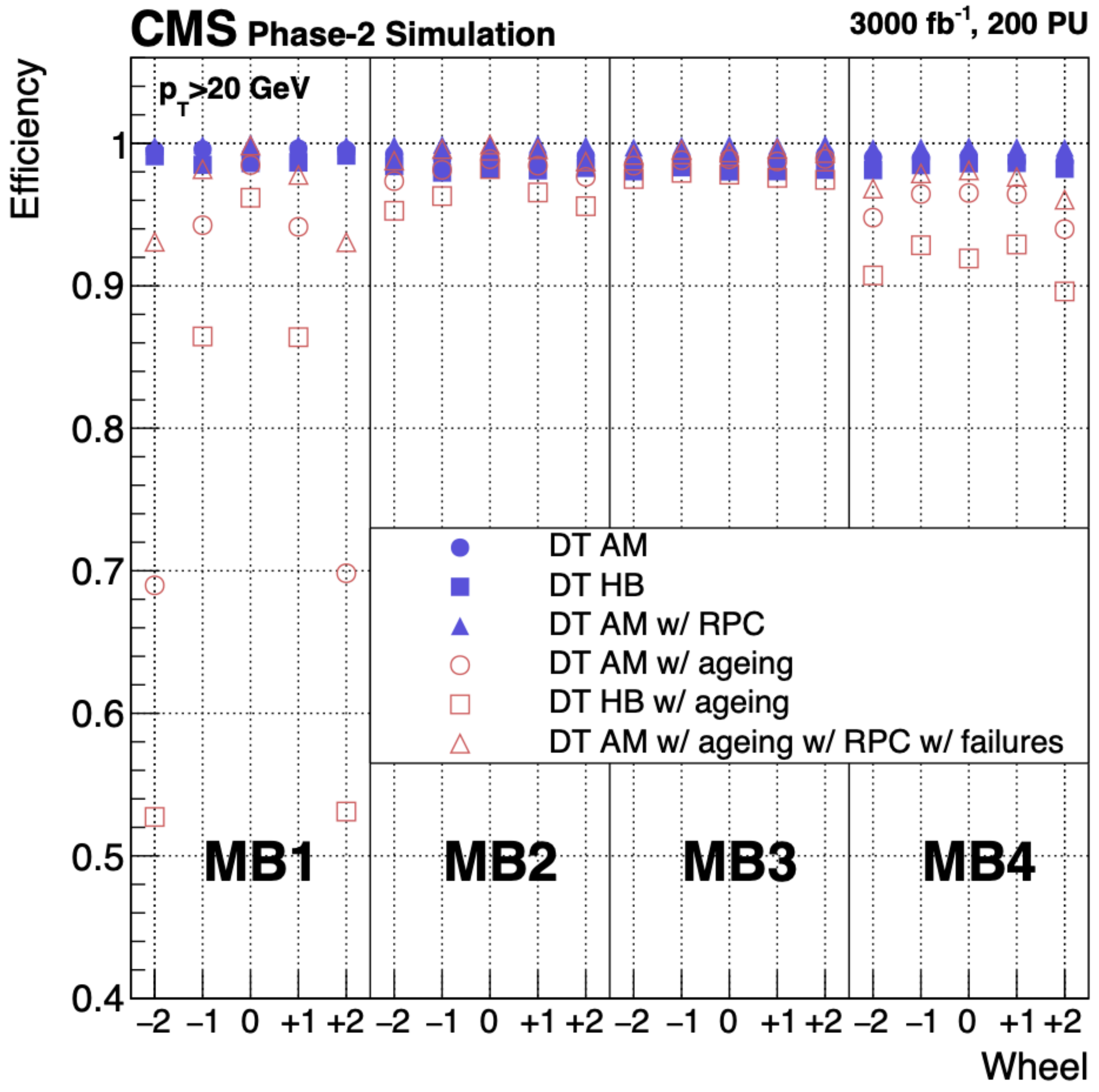


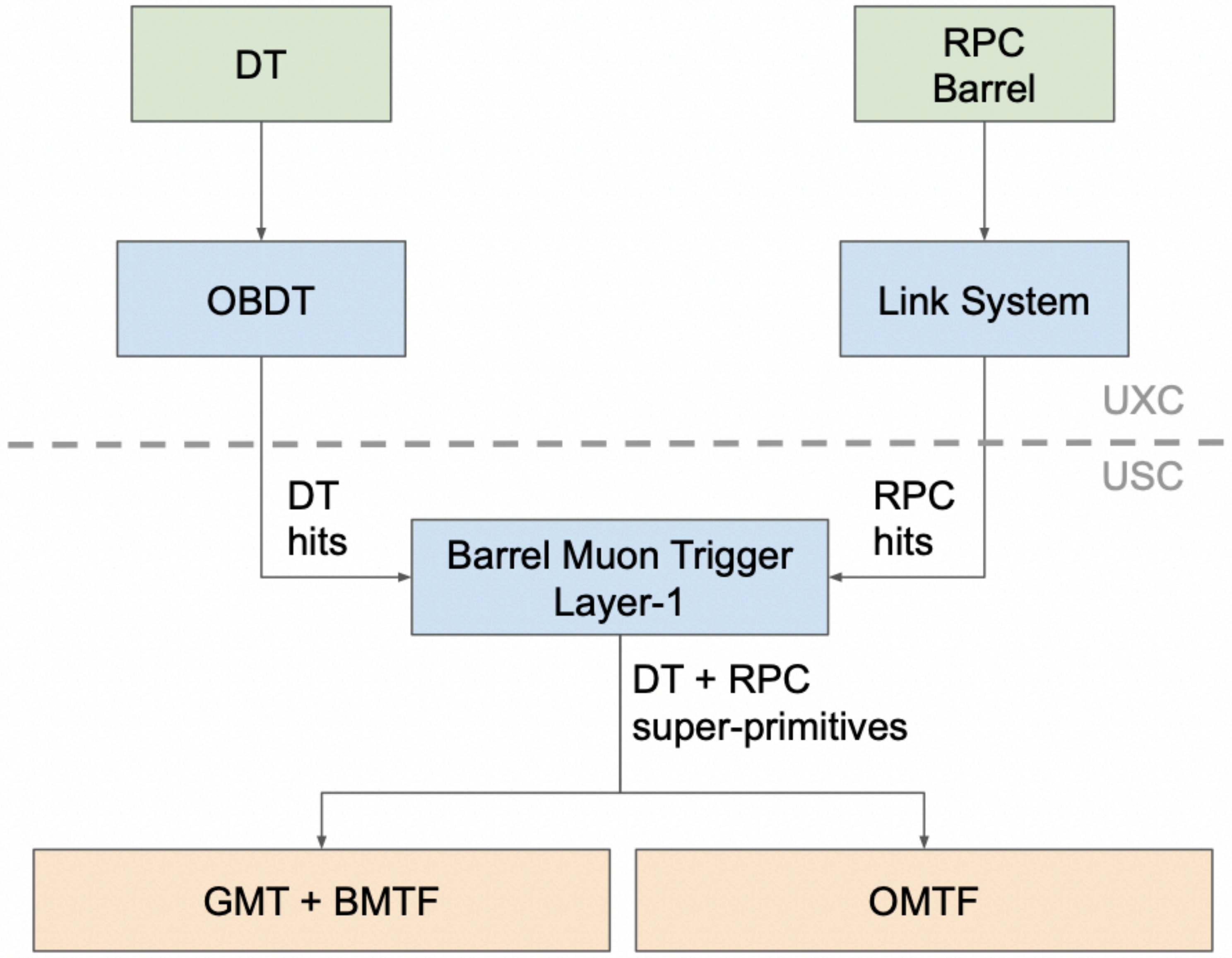
RPC @ Barrel: DT+RPC super-primitive combination

- After building the DT segments and clustering the RPC hits, the BMTL1 will merge information from both sub-detectors into combined super-primitives (SP)

- SP: space information from DT , time information from RPC

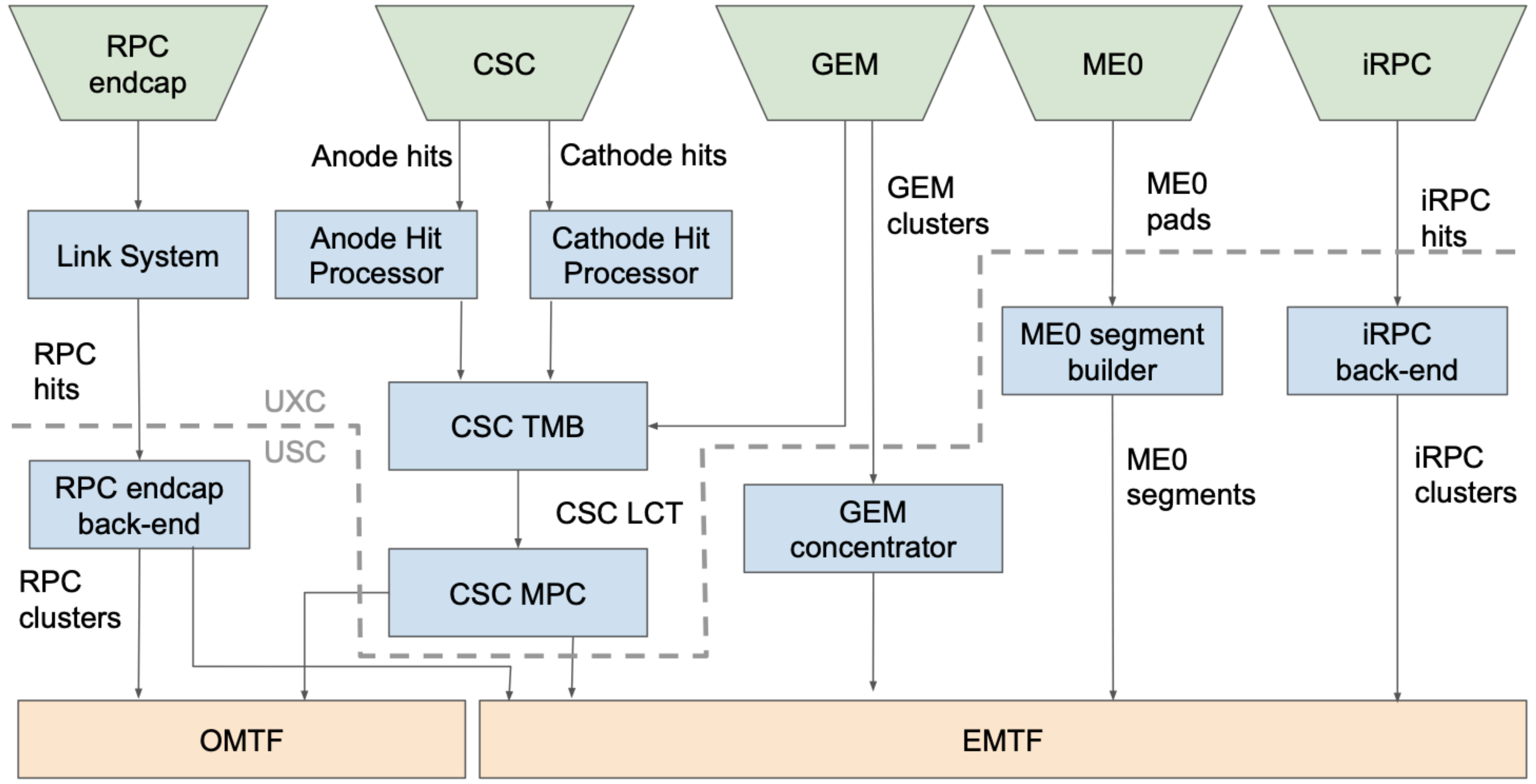


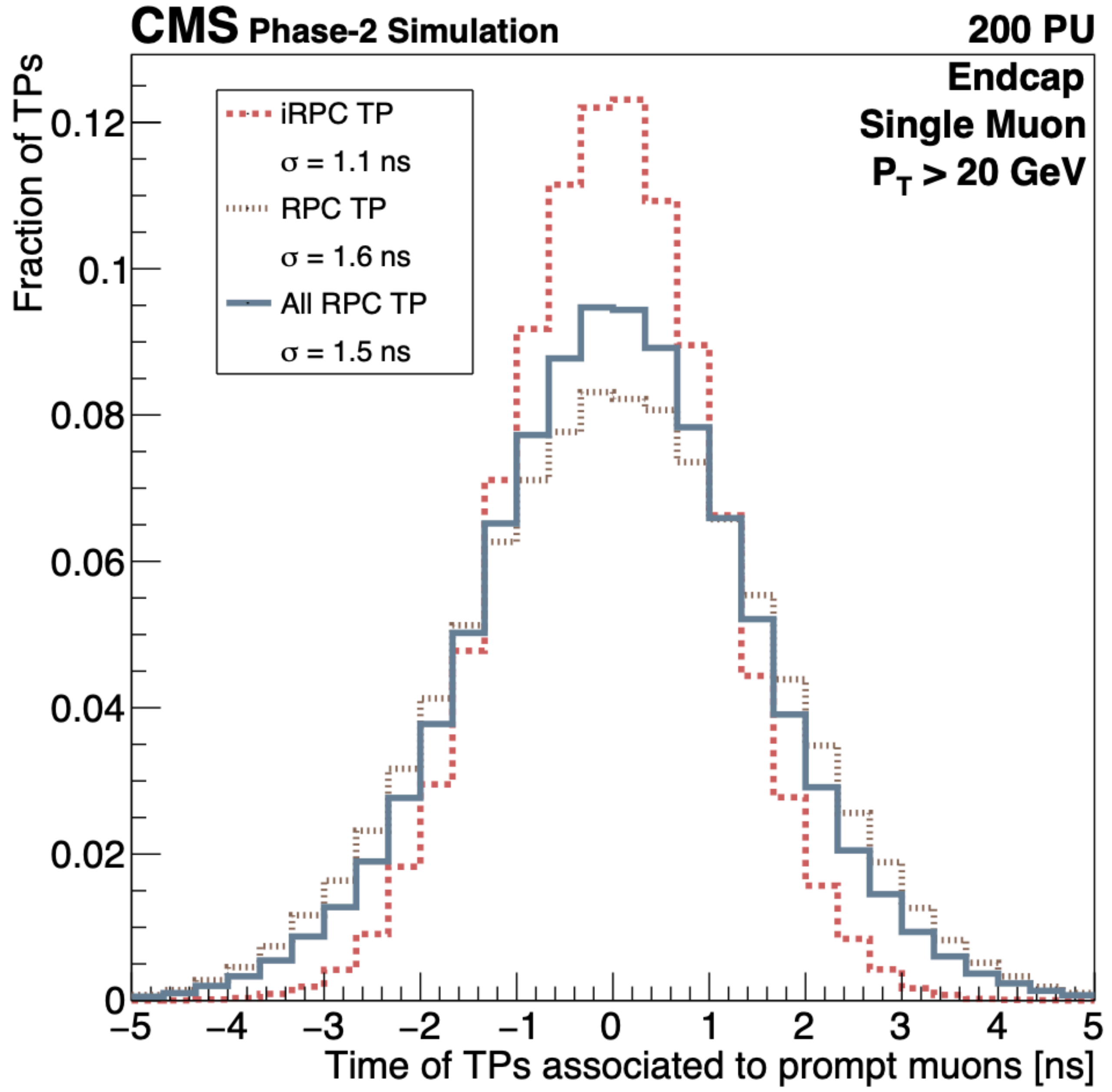




i/RPC @ EndCap: EMTF++/OMTF

For the existing RPCs
The same upgrade program as the barrel chambers
Latency will be the same as barrel as well

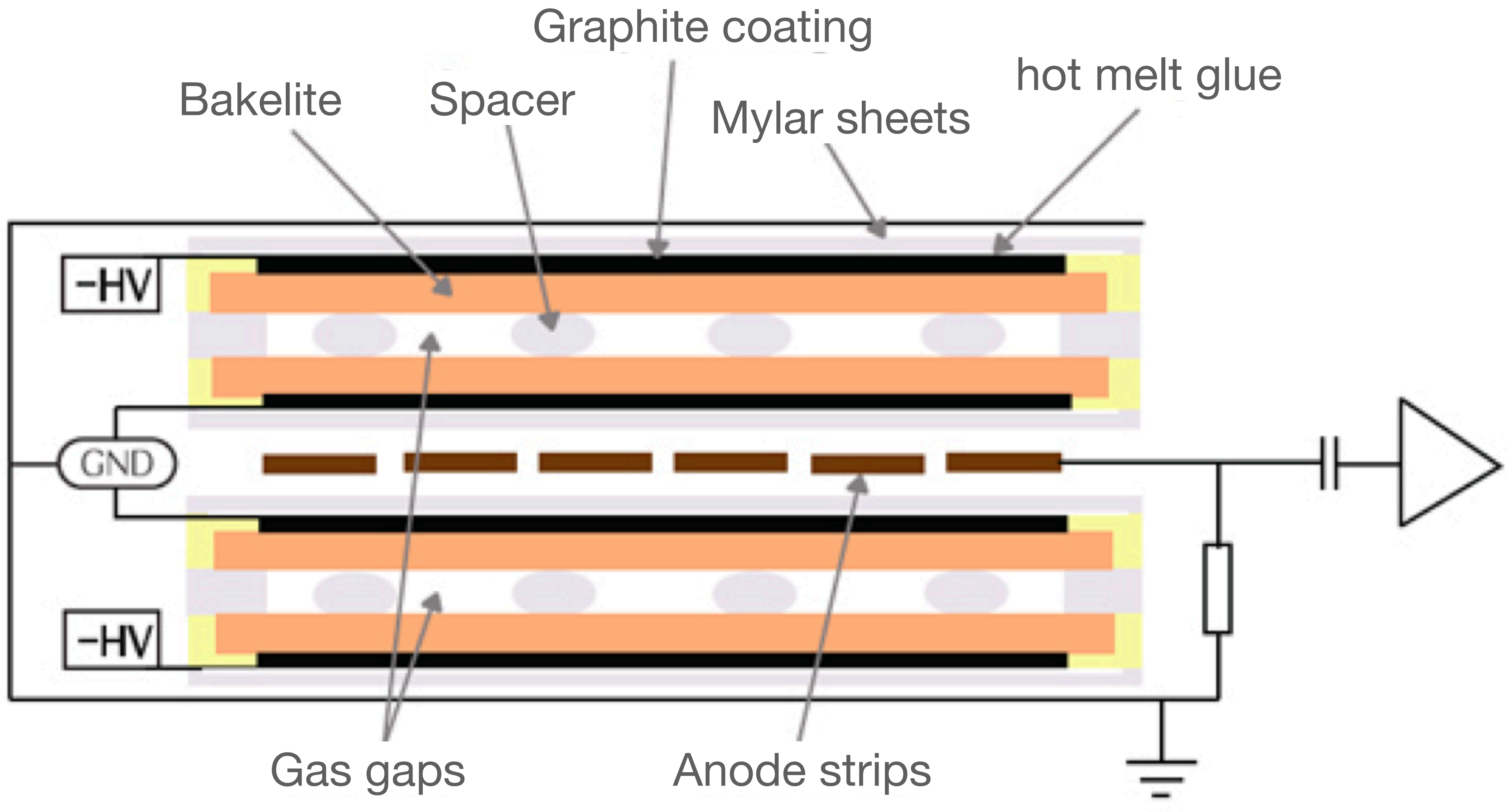




- EMTF++
  - A neural network that assigns pT and displacement will be used.
  - The TP information from all detectors CSC/GEM/(i)RPC will be input to the neural network
  - The algorithm subdivides the muon detectors fiducially into patterns consistent with muon trajectories
- OMTF
  - Currently a Bayesian algorithm, just using phi information and patterns, assigns pT to μ's
  - Currently moving into a similar neural network algorithm as EMTF
  - A similar input will be used for the network

Time distribution of the endcap (i)RPC trigger primitives associated to a generated muon track with *p*T > 20 GeV. The improved version of the front end electronics could not be included in the simulation.

The iRPC chamber



- Double-gap iRPC detectors
- Each gap made of two 1.4 mm low-resistivity (order of 10^{10} Ωcm)
- High Pressure Laminate electrodes Separated by a gas gap of the same thickness.

	Present system	iRPC
$\|\eta\|$ coverage	0 – 1.9	1.8 – 2.4
Max expected rate (Safety factor SF = 3 included)	600 Hz/cm²	2 kHz/cm²
Max integrated charge at 3 ab^{-1} (SF = 3 included)	~ 0.8 C/cm²	~ 1.0 C / cm²
ϕ granularity	~ 0.3 °	~ 0.2°
η resolution	~ 20 cm	~ 2 cm
T resolution	1.5 ns	< 1 ns

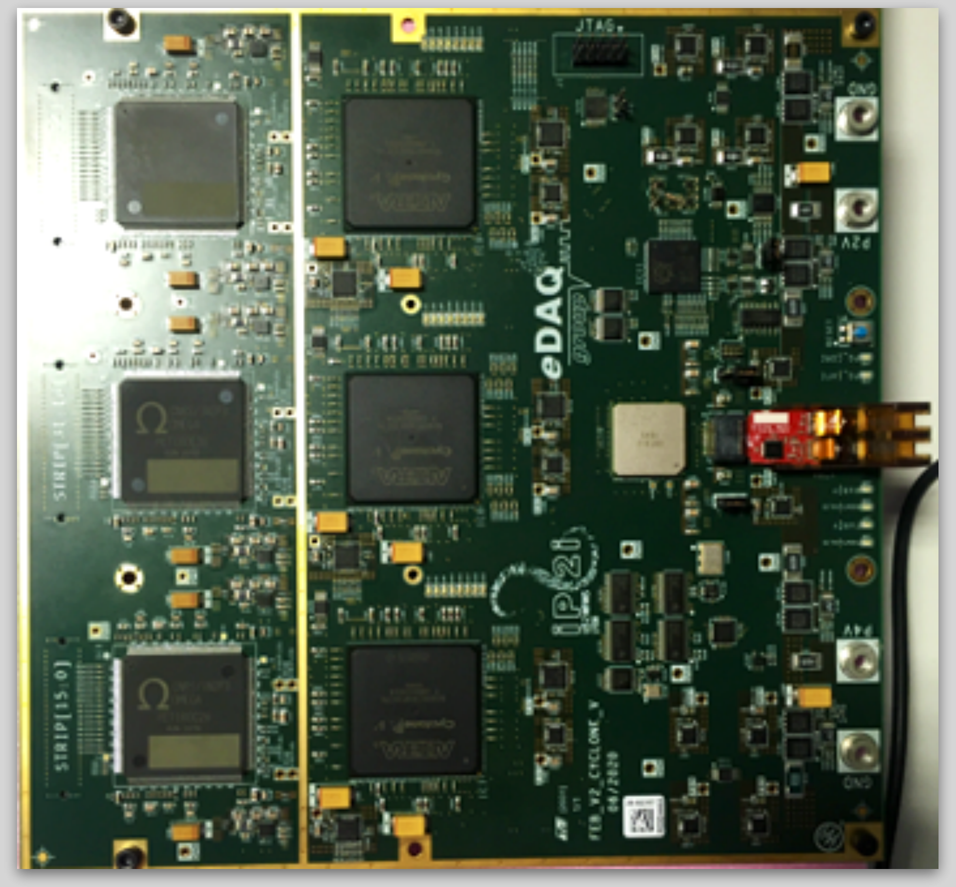
- The new layout reduces the amount of the avalanche charge produced by the passage of a charged particle through the detector.
- This improves the RPC rate capability by reducing the needed time to collect this charge.

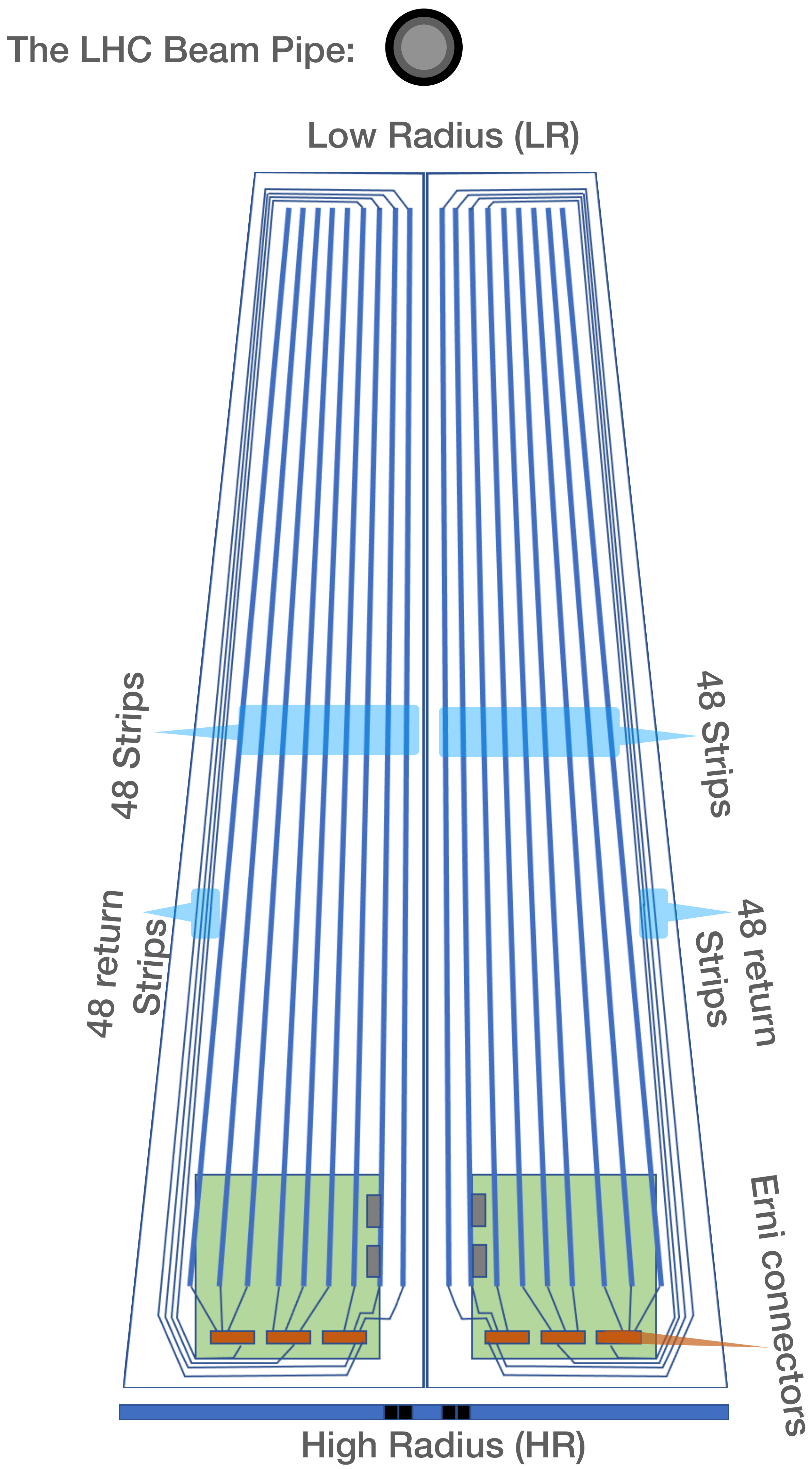
The new electronics and the readout principle

To cope with the lower charge signal of the iRPC at the same time to keep the iRPC efficiency high, the new front-end electronics are designed. The new FEB is sensitive, has low-noise and high time resolution.

The FEB composed of :

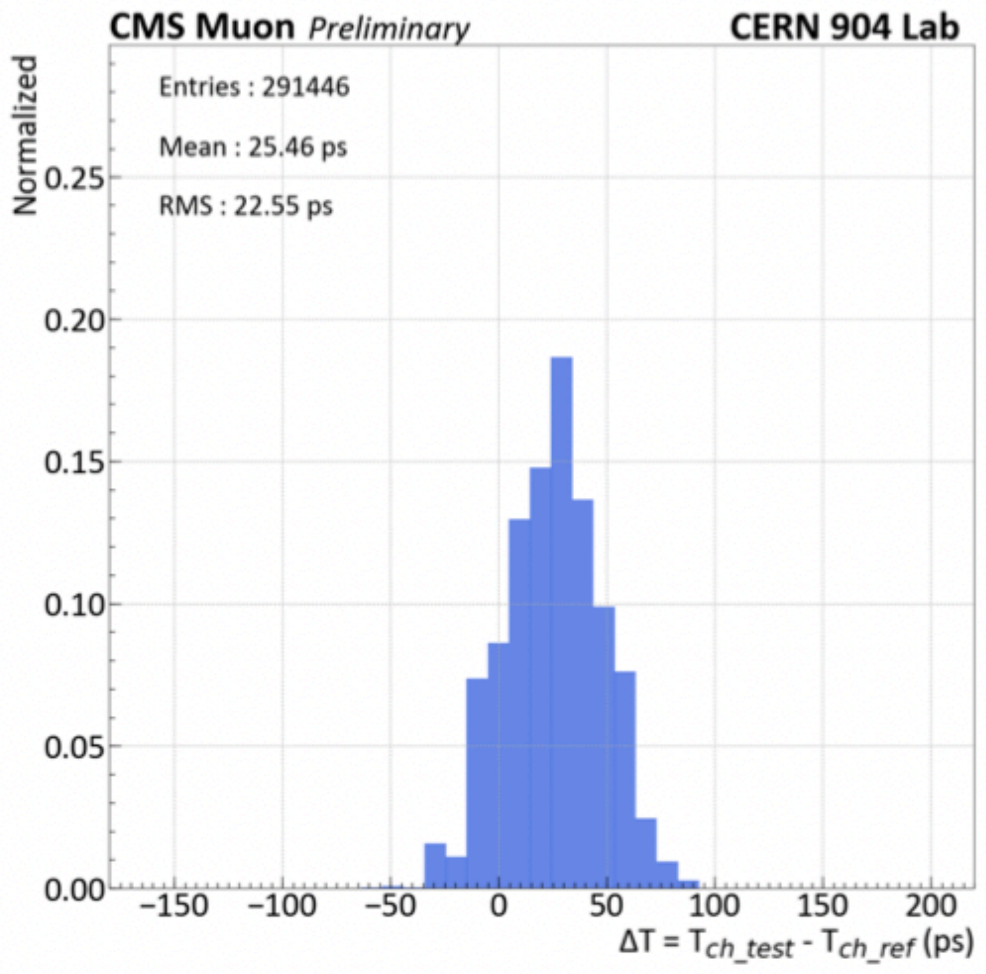
- 3 Erni connectors with 32 channels each
- 6 ASICs PETIROC 2C (top & bottom)
- 3 FPGAs Cyclone V (non rad-hard)
- GBTx/ GBT-SCA/VTRx.

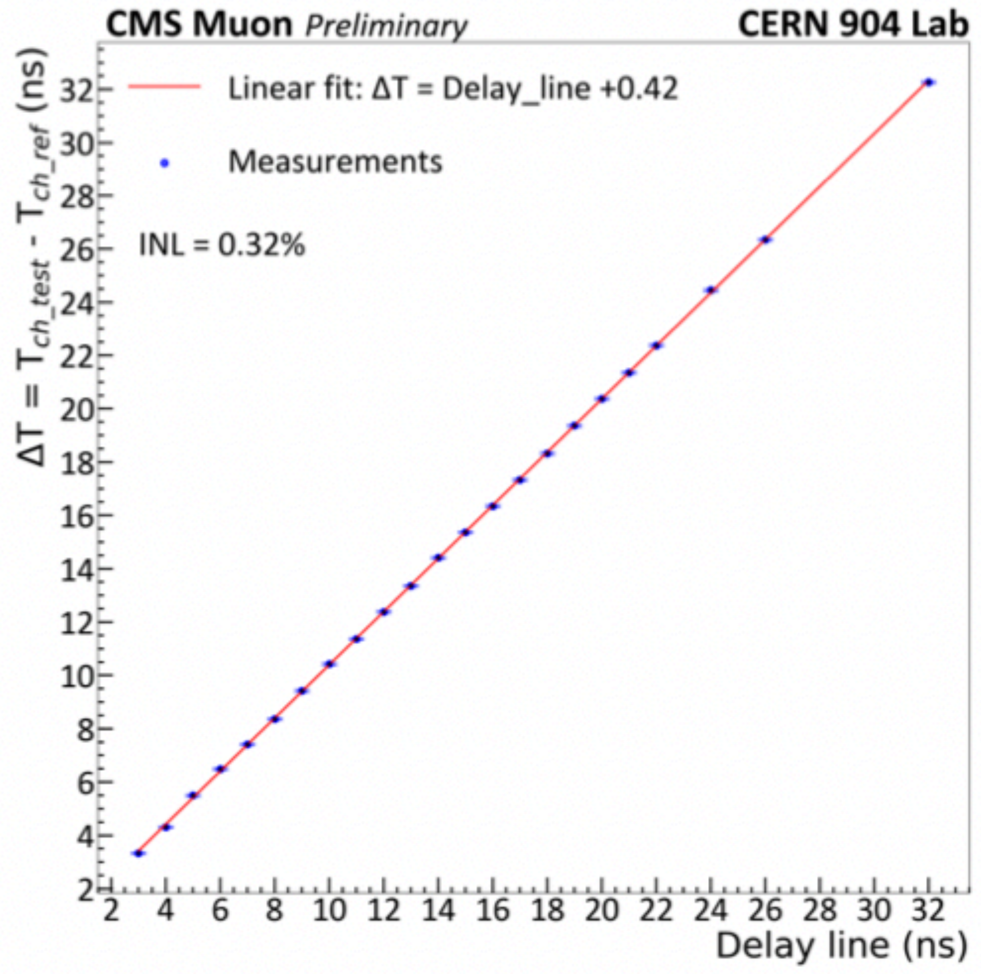


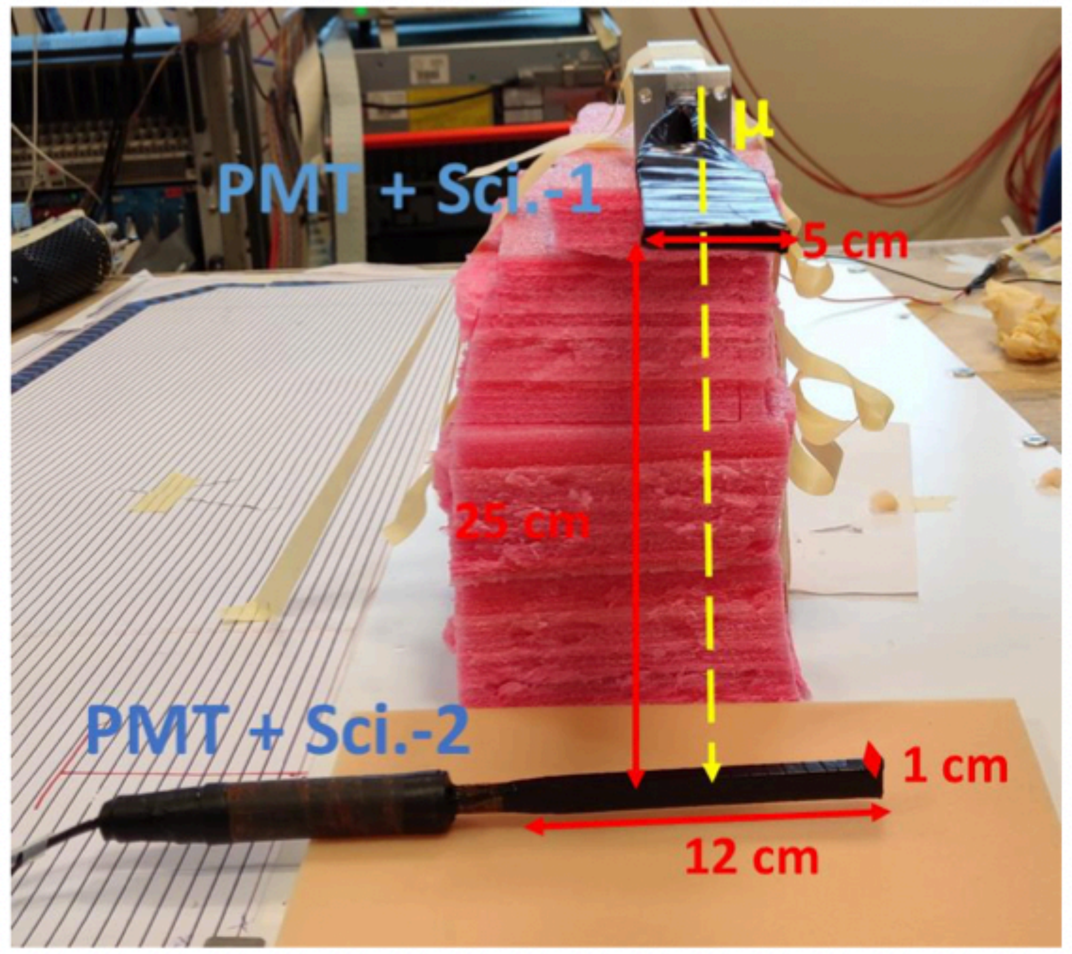


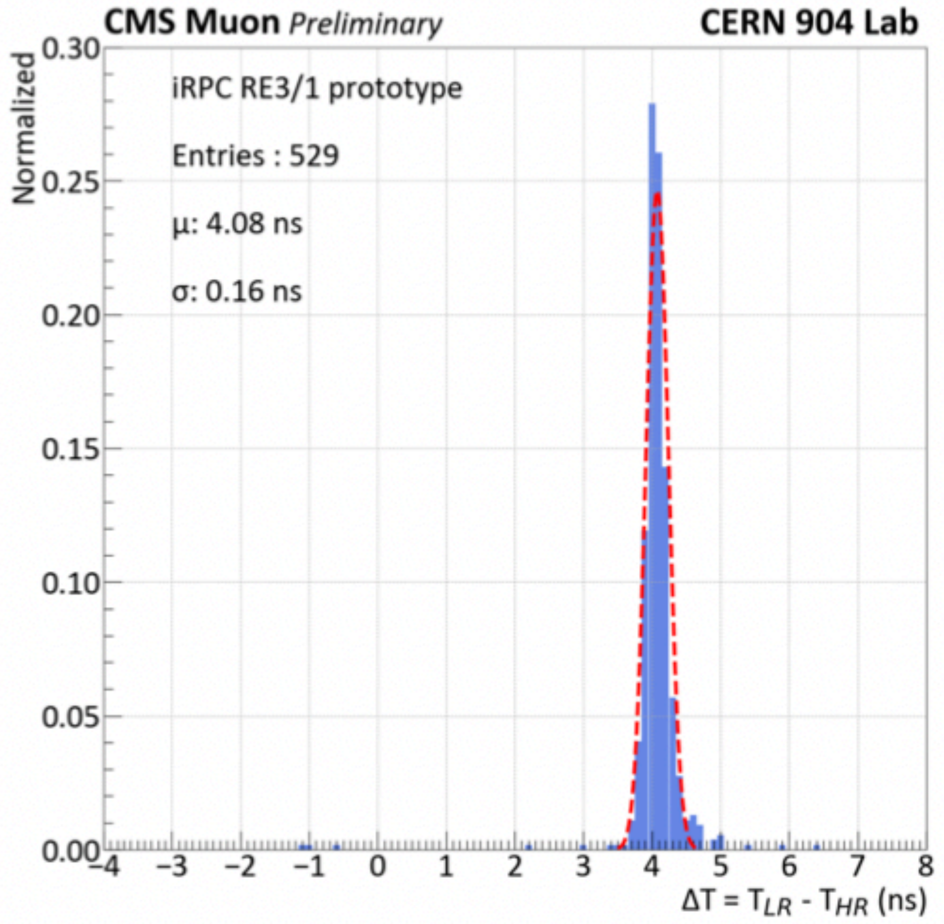
- Two readout panels: made of a thin (0.6 mm) Printed Circuit Board (PCB)
- Each PCB has 48 strips and equipped with a FEB.
- To identify the position along the strip, the read out of the iRPC detectors is from both sides of a strip end, low radius (LR) and high radius (HR).

Time and Space resolution

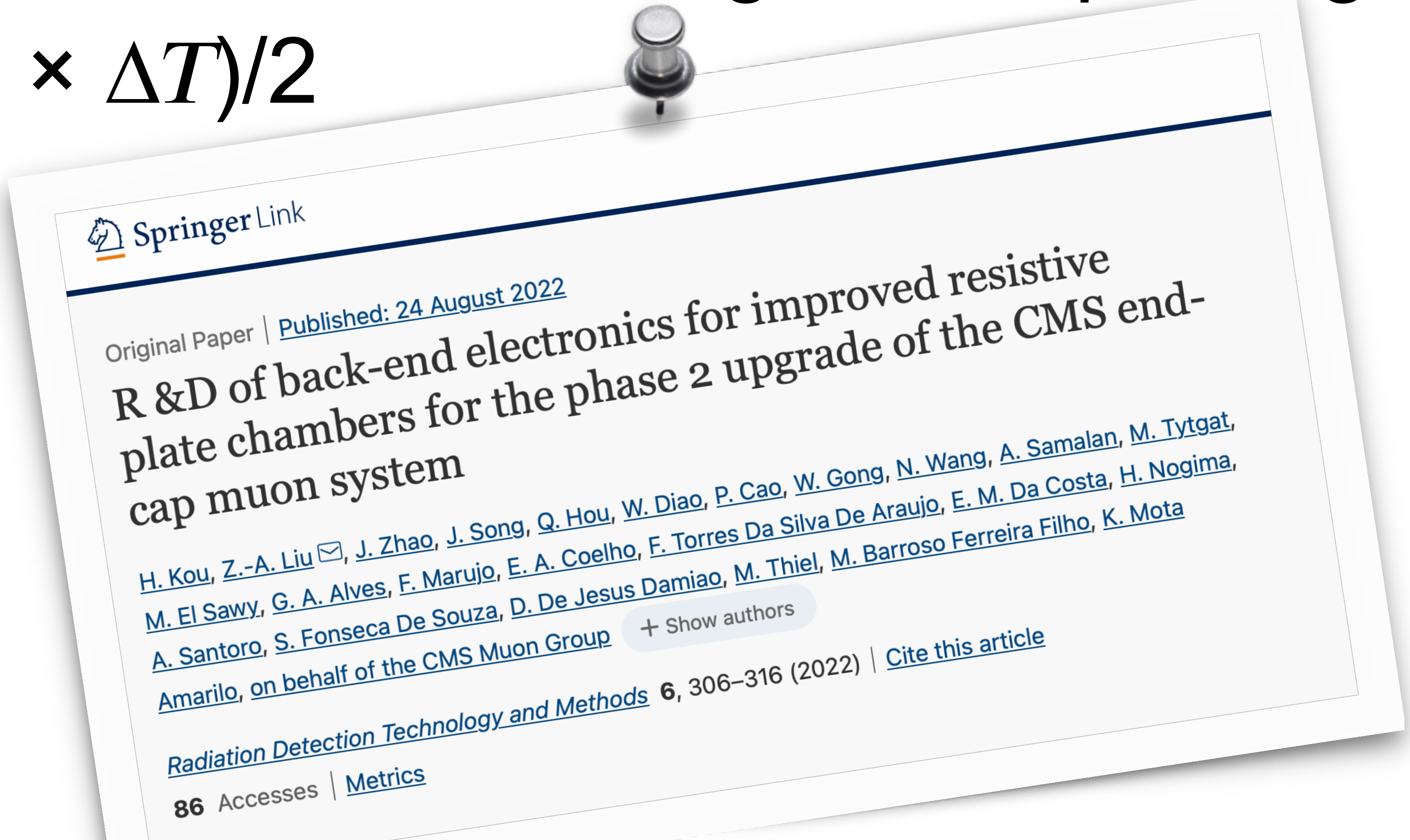






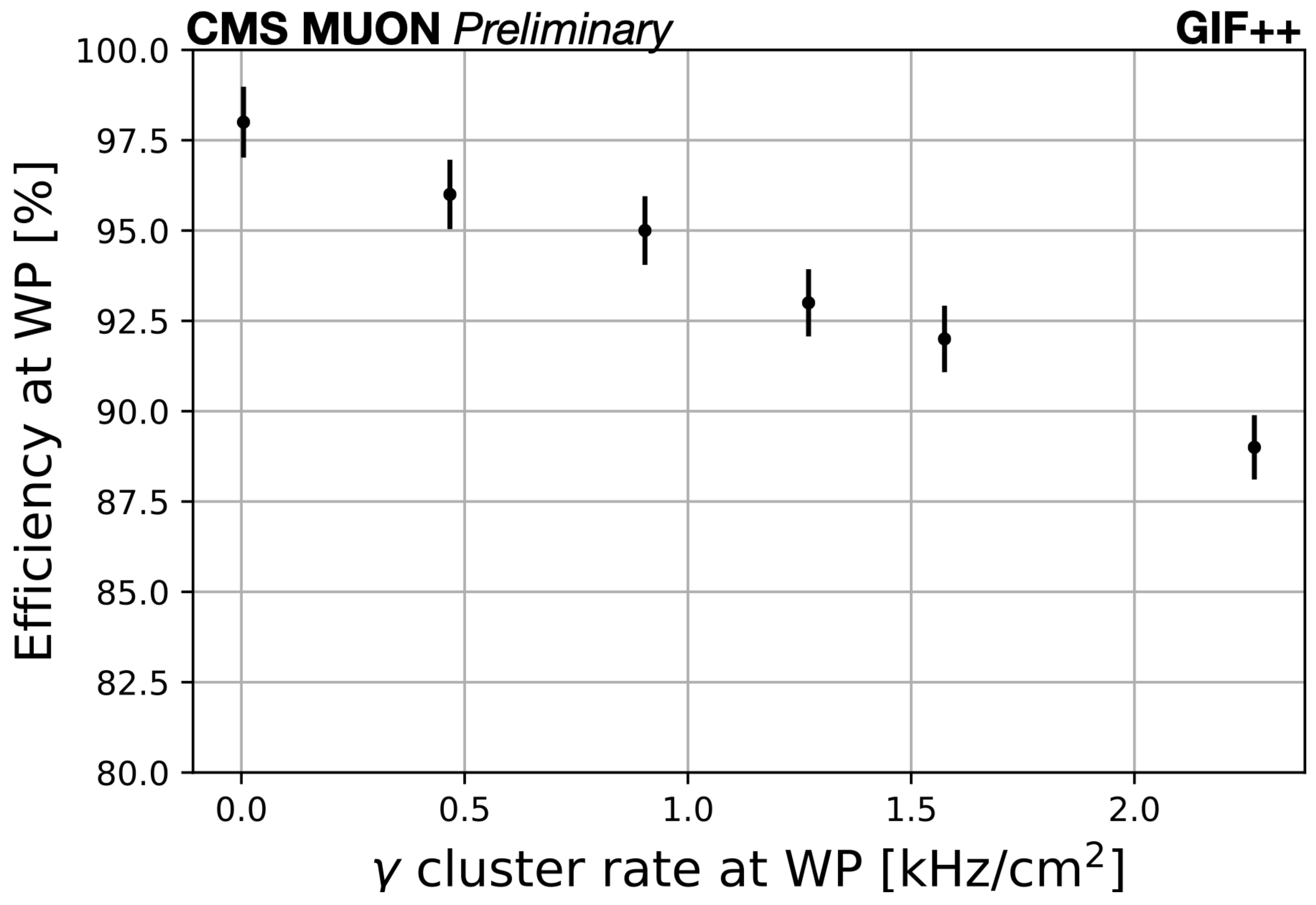


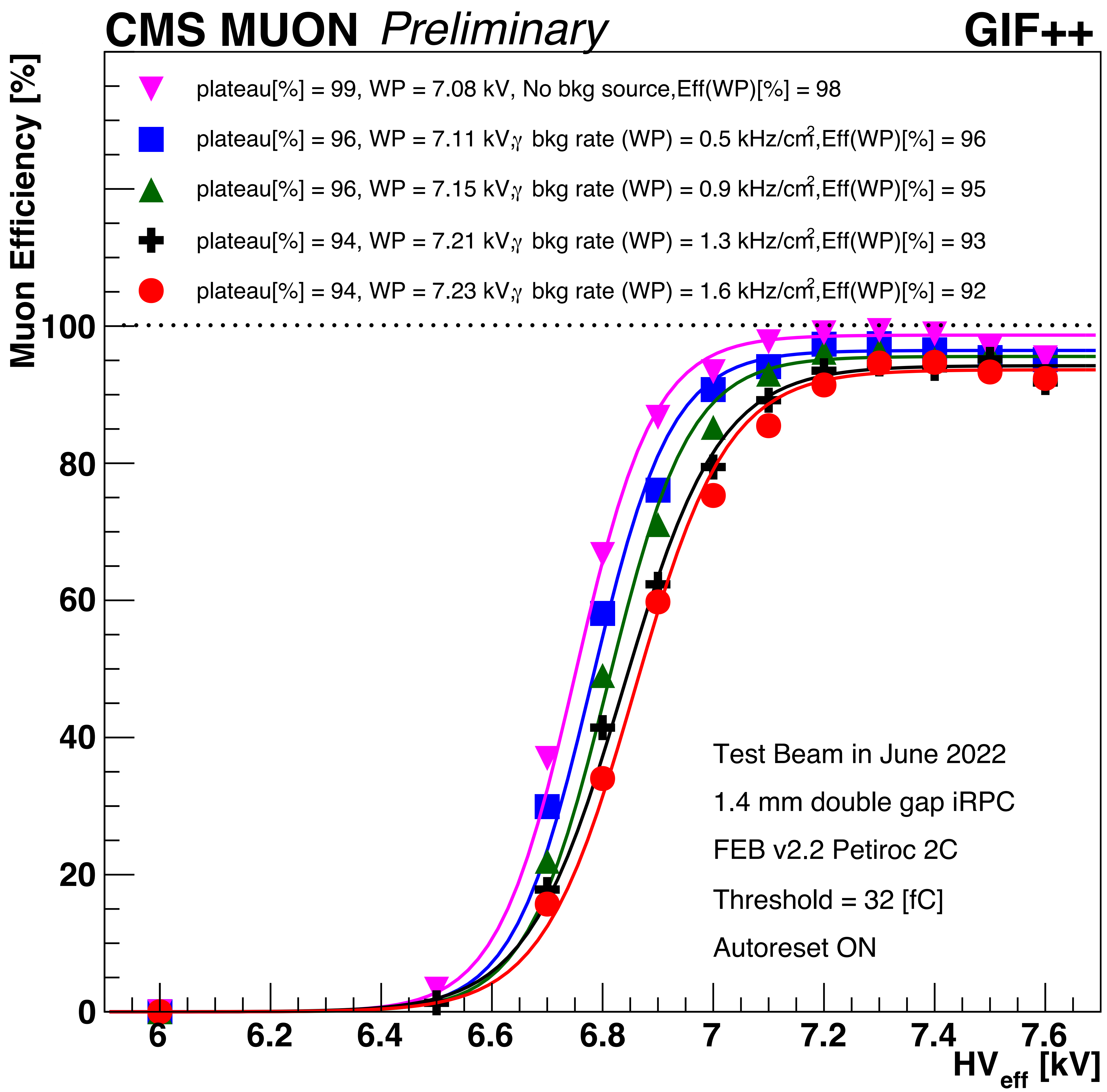
- The time difference between two channels without delay line is measured : RMS of 23 ps
- As the value of the delay line increases, the time difference between the two channels also increases linearly, with a maximum deviation of 0.1 ns.
- A strip is randomly chosen within the coincidence area of the two scintillators.
- The time difference distribution between both ends σ is 160 ps after rejecting the noise, which translates to a positional resolution of 1.5 cm along the strip using the formula $\Delta y = (v \times \Delta T)/2$



Performance of iRPC detector in GIF++

Efficiency versus effective high voltage with various background rates at WP.
At 0.9 kHz/cm² which is above the expected background rate of Phase II (0.7 kHz/cm²), the efficiency at WP is measured as 95%.
Estimated efficiency at 2 kHz/cm² is ~90%.





iRPC Backend µTCA Demonstrator

iRPC backend µTCA Demonstrator

µTCA compliant BE boards

- core board

a µTCA crate,

an AMC13 card,

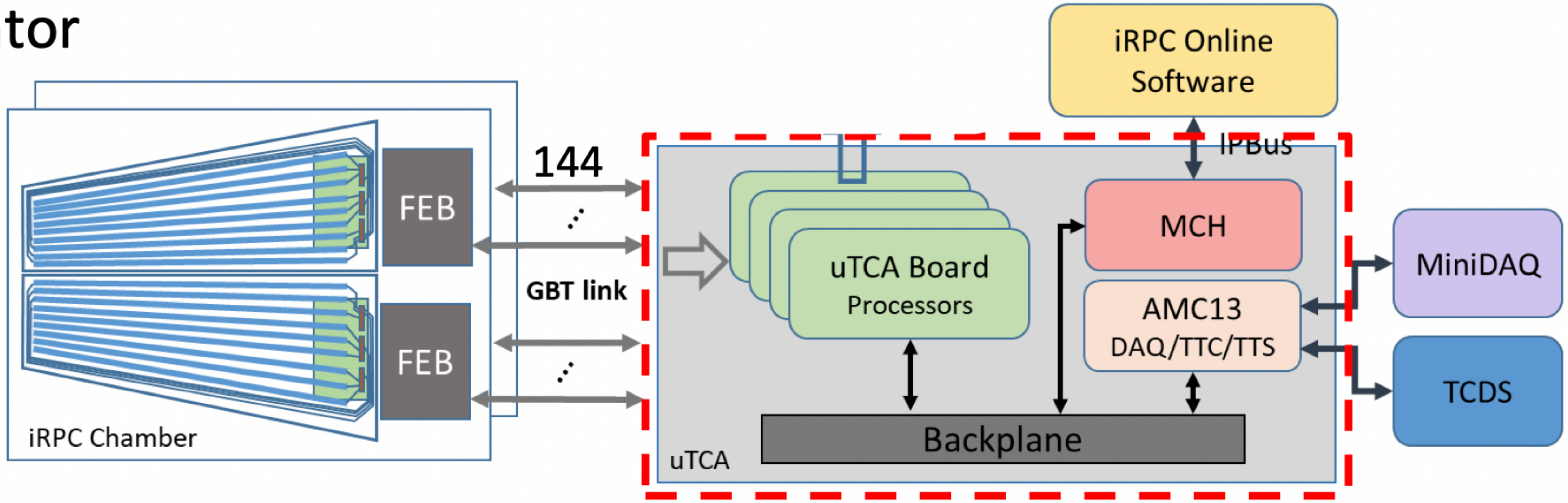
- system clock and fast control

a µTCA Carrier Hub(MCH),

- manage the whole system

a sever PC.

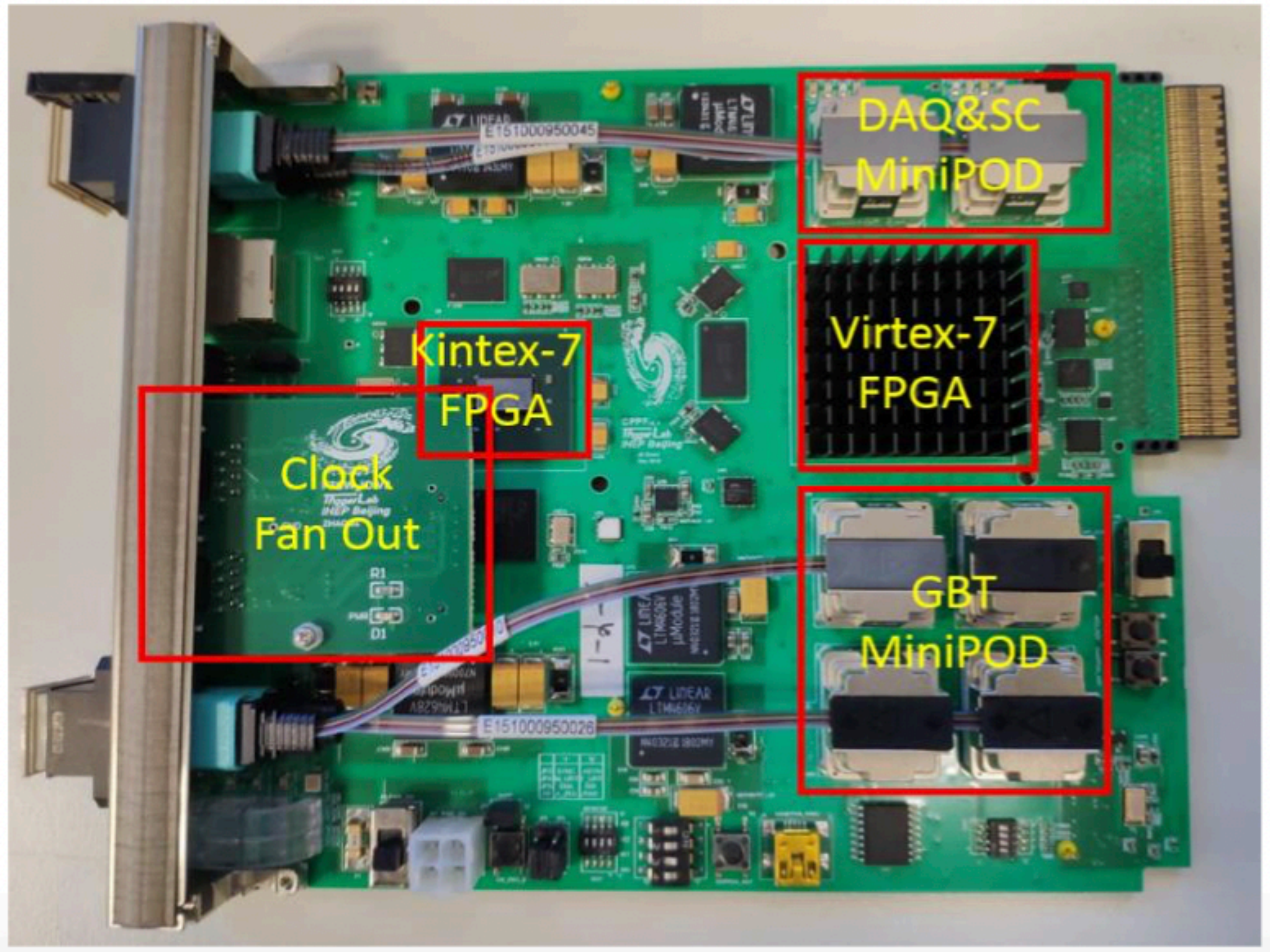
- slow control and DAQ



BE board

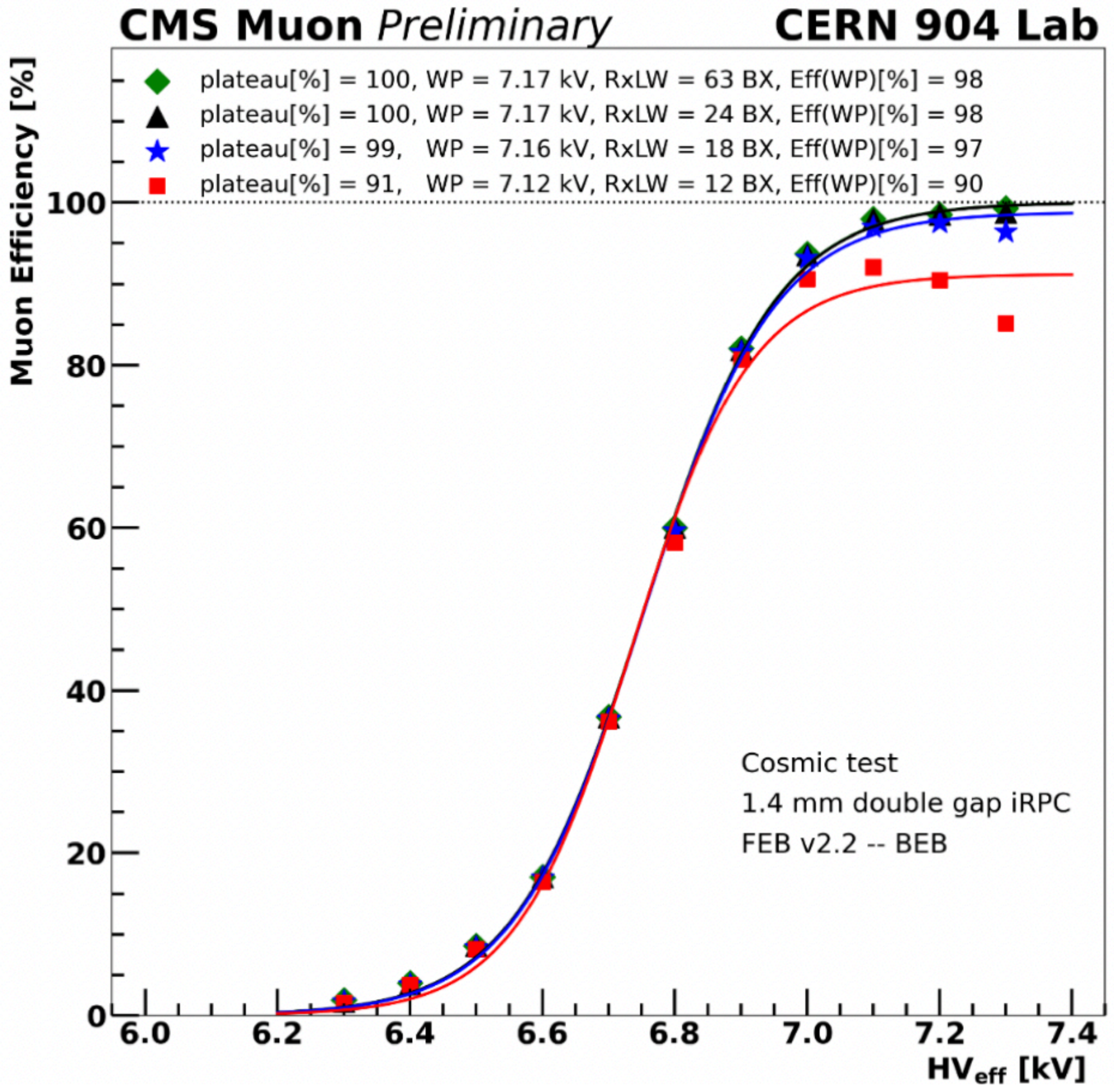
Virtex-7 FPGA： Core FPGA(GBT Communication with Feb + data processing);

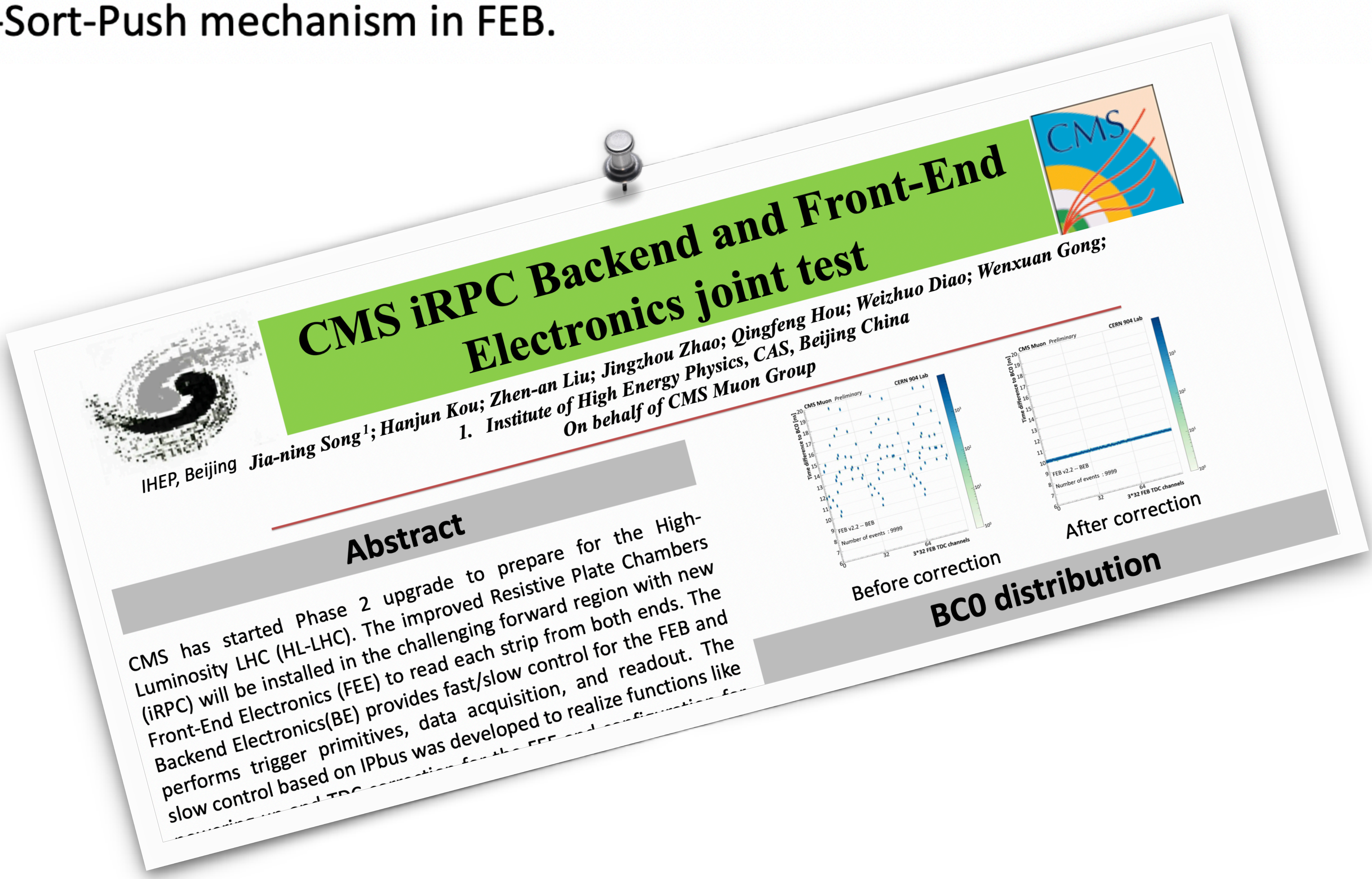
Kintex-7 FPGA： Control FPGA(clock configuration , SC)



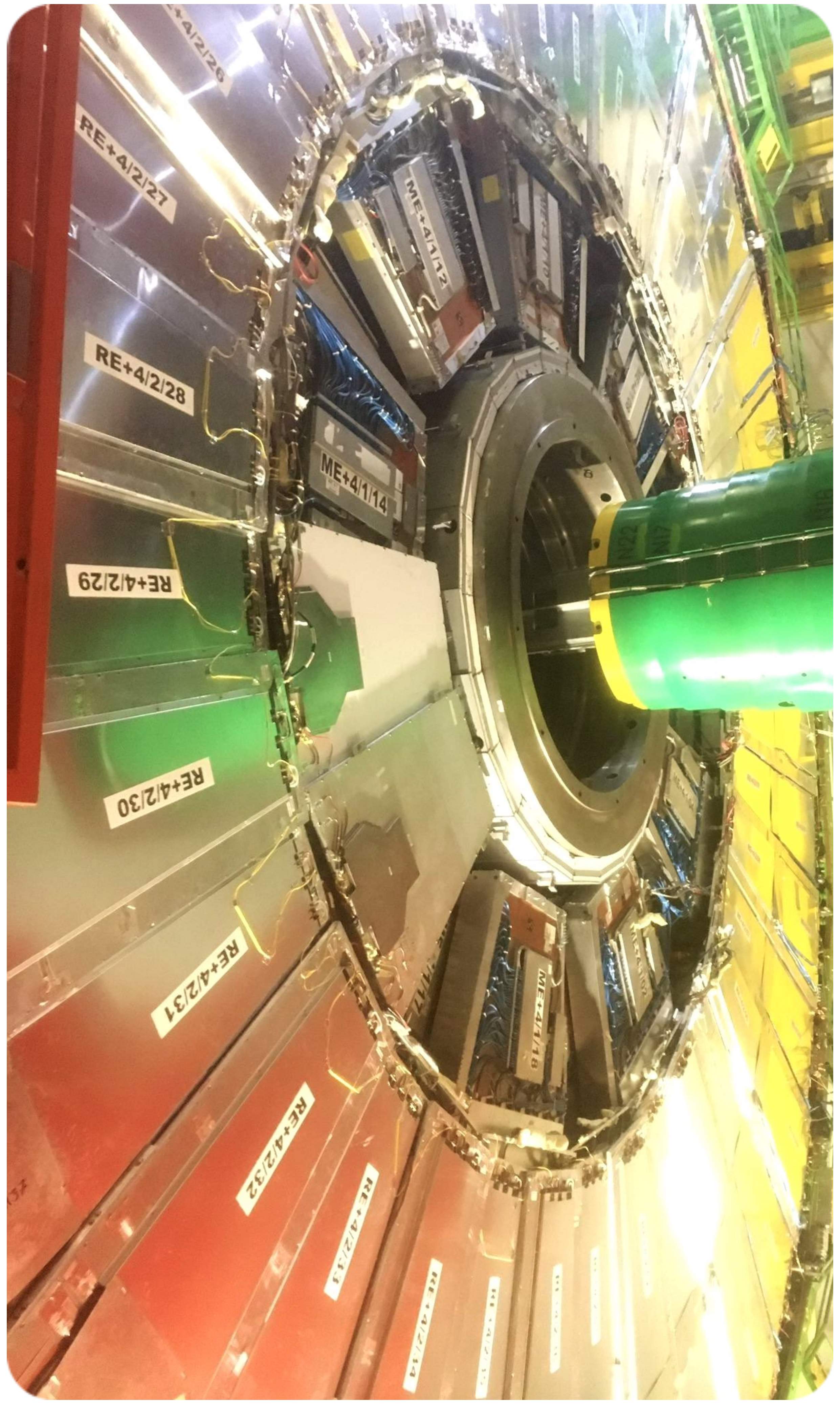
iRPC FEB-BEB joint test --Efficiency scan

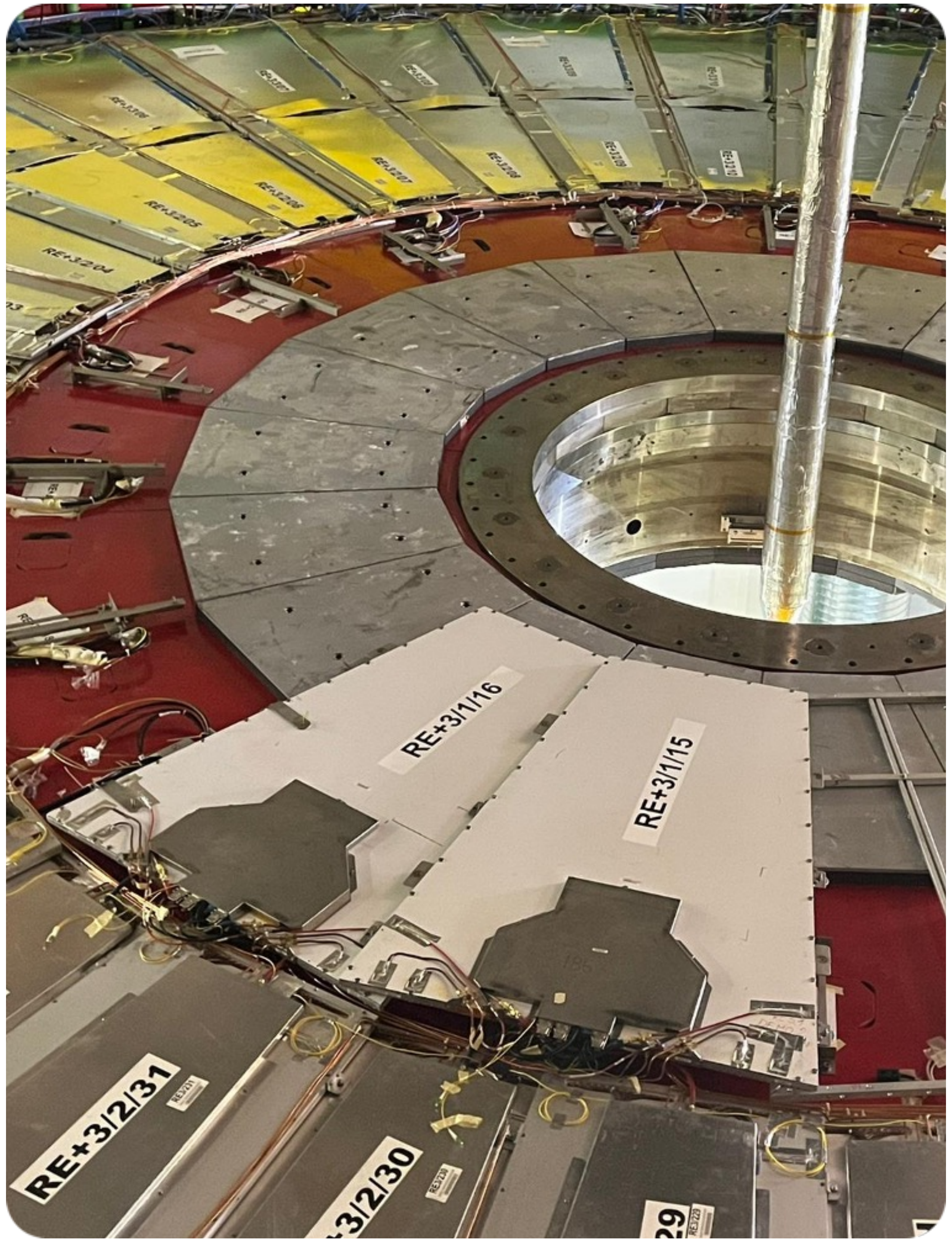
- This result was acquired using the present FEE parameters and backend system in 904.
  - When RxLW = 12 BX(25ns), the efficiency was not high.
  - And it increases to 100% when the RxLW set as 63 BX(25ns) (Extreme test situation, at the cost of 1 link per BEB).
- Shouldl be improved by implementing Check-Sort-Push mechanism in FEB.





Demonstrator iRPCs are installed

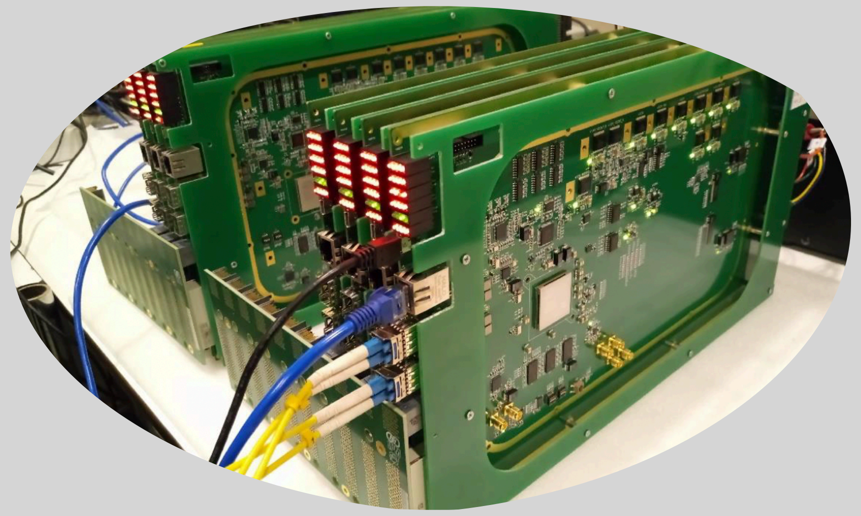




Four demonstrator chambers have just been installed in CMS cavern at the end of LS2. The picture on the left to right exhibit the final position of the demonstration chambers RE+4/1/15,16 and RE+3/1/15,16 respectively.

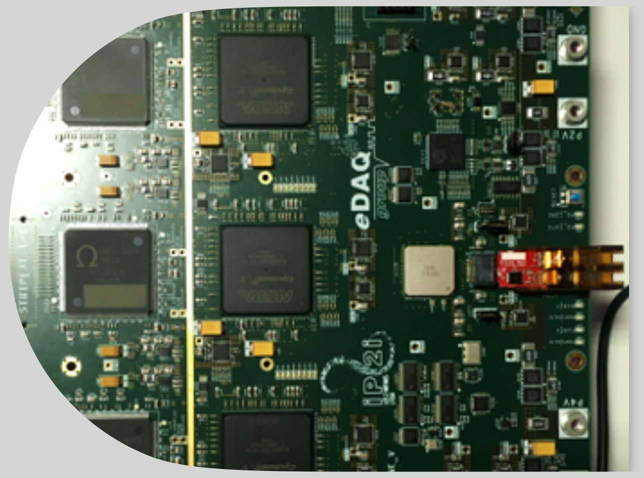
Conclusion

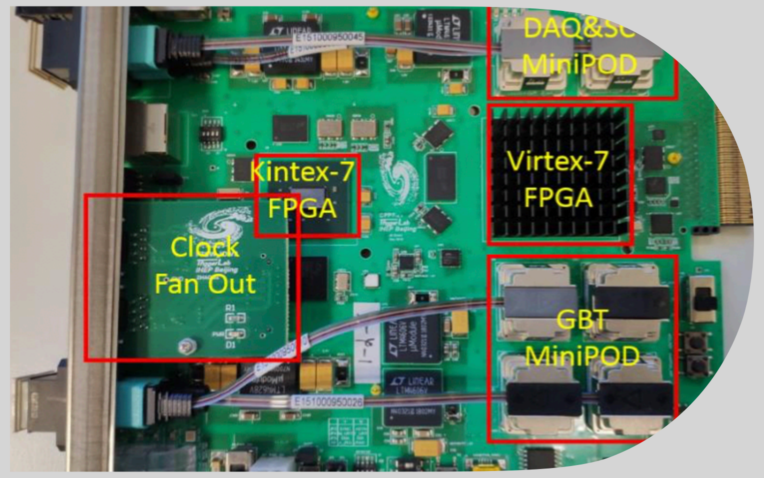
The existing RPC system



- Three of each prototypes Link Boards, Control Boards, Front Panel Boards has been ready since middle of February 2022.
- Firmware integration of MLB, SLBs, Slow Control emulator, and back-end electronics emulator have been finalised.
- Sophisticated Hardware Validation Tests is ongoing in Tehran IPM lab.
- Right at the moment, the New Link Board irradiation with charged/ neutral hadrons and thermal neutrons is ongoing at the CERN High Energy Accelerator Mixed-field using protons from PS.

The iRPC system





- The Front end electronic is validated.
- iRPC Validation with and without background are successful.
- Irradiation studies with gamma and neutron are successful.
- Commissioning of demonstrator chambers at the CMS Cavern is successful.
- Feb irradiation with charged/ neutral hadrons and thermal neutrons is ongoing at the CERN High Energy Accelerator Mixed-field using protons from PS.
- Front end board - Back end board joint tests in gamma irradiation facility with muon beam from SPS is ongoing.

Conclusion

As a result of successful performance at CERN 904 Lab, GIF++ and at the CMS cavern, currently, demonstrator iRPCs are getting ready for taking data during Run3 to further validate the performance for Phase II operations.

Phase II Upgrade brings new possibilities for RPC contribution to Level-1 Trigger

Increased synergies with other muon sub-systems to build more robust TP Increased trigger efficiency in forward region thanks to iRPC

Extended physics program thanks to the improved timing (HSCP)

References

- “Search for Long-Lived Particles Decaying in the CMS End Cap Muon Detectors in Proton-Proton Collisions at $\sqrt{s}$= 13 TeV”Phys. Rev. Lett. **127**, 261804
- CMS-PAS-BPH-21-006
- CMS Collaboration, “The Phase-2 Upgrade of the CMS L1 Trigger Interim Technical Design Report”, CERN-LHCC-2017-013. CMS-TDR-017.
- CMS Collaboration, “The Phase-2 Upgrade of the CMS Muon Detectors”, CERN-LHCC-2017-012. CMS-TDR-016.
- CMS Collaboration, “Level-1 Muon Trigger Performance”, CERN-CMS-DP-2018-044. CMS-DP-2018-044
- CMS Collaboration, “The Phase-2 Upgrade of the CMS Level-1 Trigger”,CERN-LHCC-2020-004 ; CMS-TDR-021

Back up slides

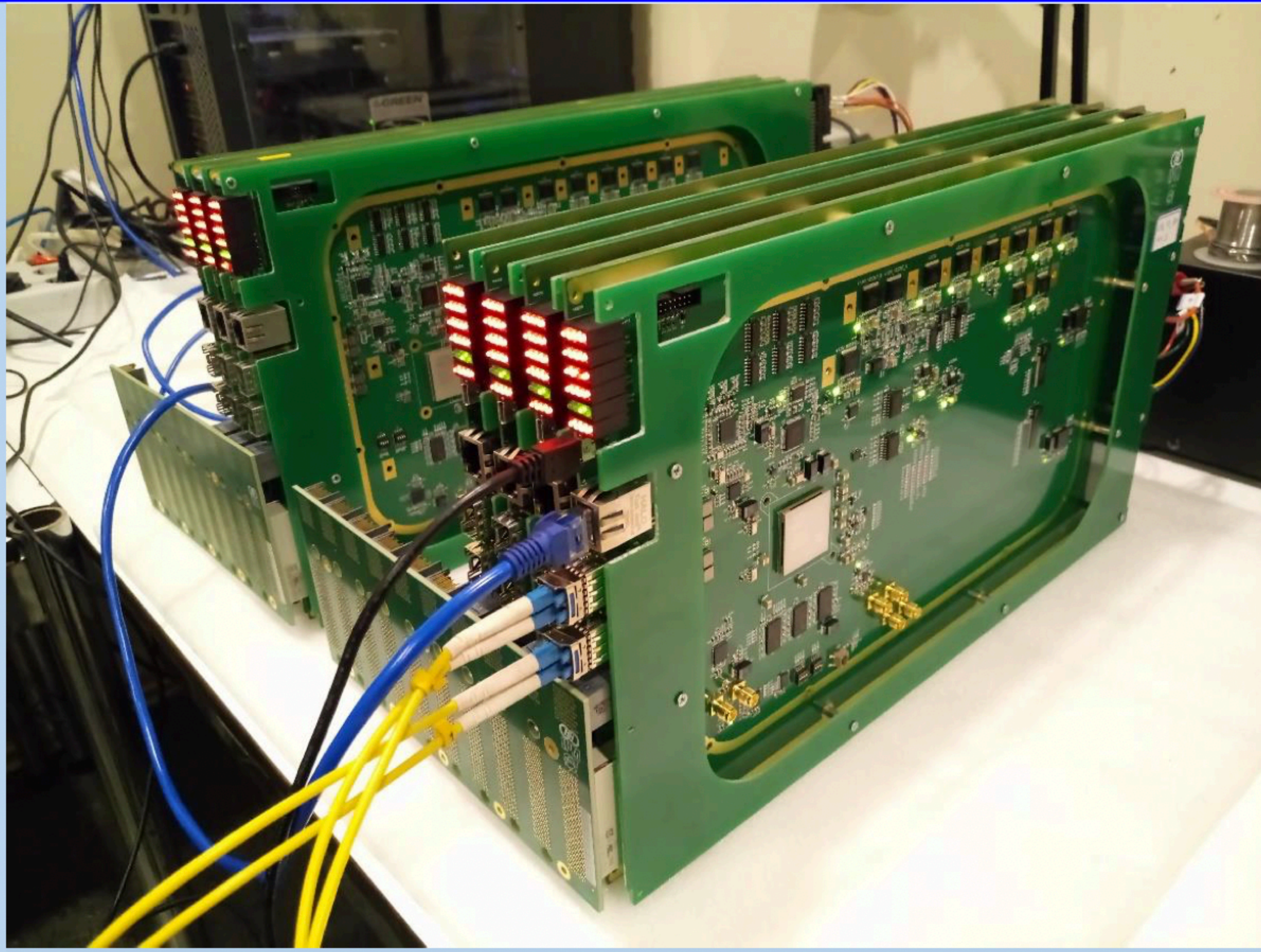
Gamma irradiation facility:GIF++

Located at the end of CERN SPS H4 line that provide 150 GeV Muon beam.

RPC Barrel and EndCap

New Link system Features :

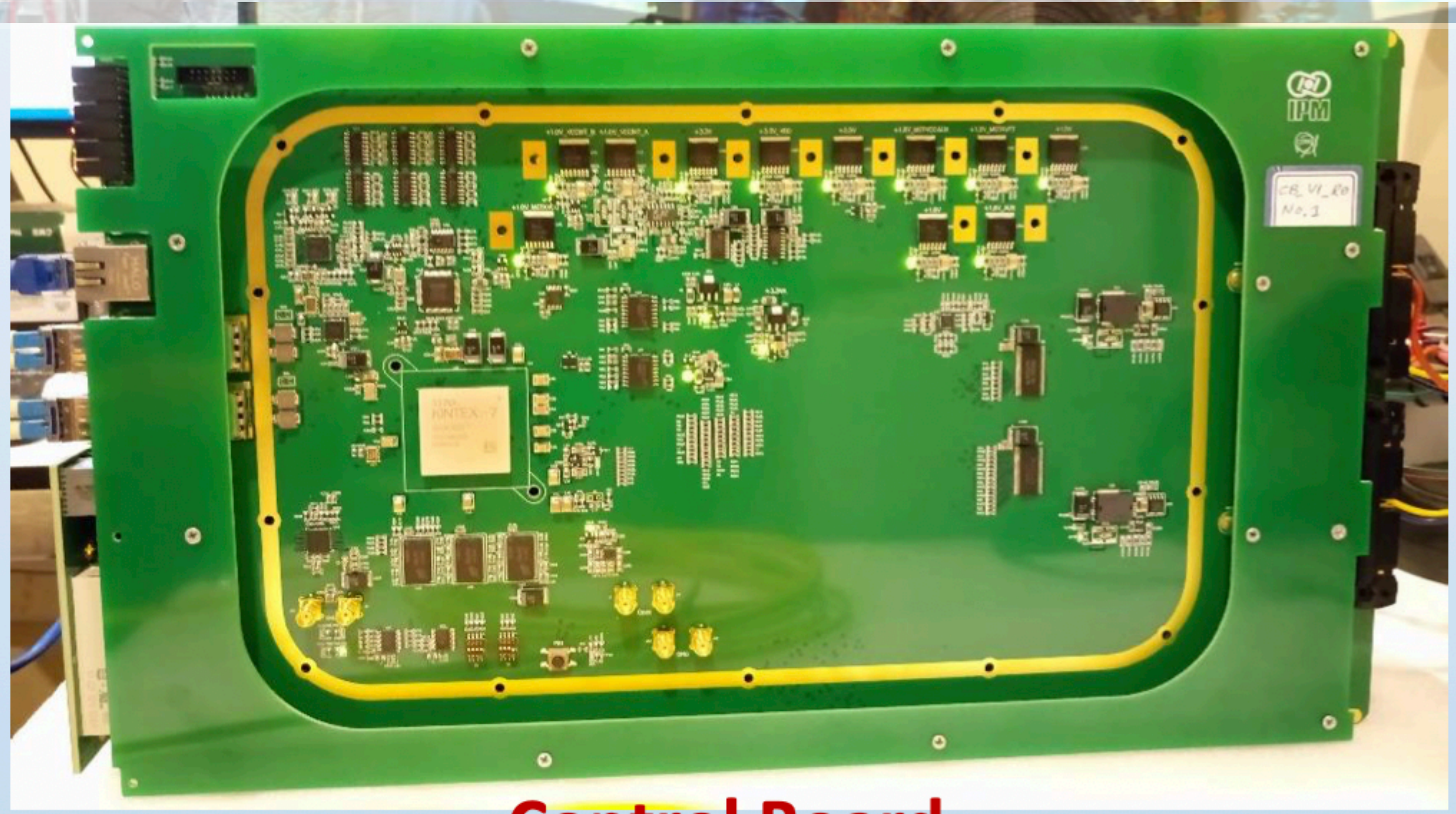
1. FPGAs are KINTEX-7, XC7K160T – Industrial Version
2. Muon hit time, TDC timing Resolution : 1.56ns
3. Master Link board output data rate : < 10.24 Gbps
4. Control Board communication with slow controller at < 10.24 Gbps
5. Embedded internal buffer (DDR3) : 4 GByte
6. Radiation Mitigation: TMR + Internal Scrubbing
   - Scrub Rate of entire FPGA (Real time SEU detection and Correction) : 13ms (31,770 times faster than the rate of SEU at the Balcony)
   - SEU at the Balcony : Every 413000 ms
7. Safety Systems:
   - Over & Under Voltage Protection
   - FPGA Over Temperature Protection
   - Transient Voltage Suppressor
   - ESD Protection (15 kV)



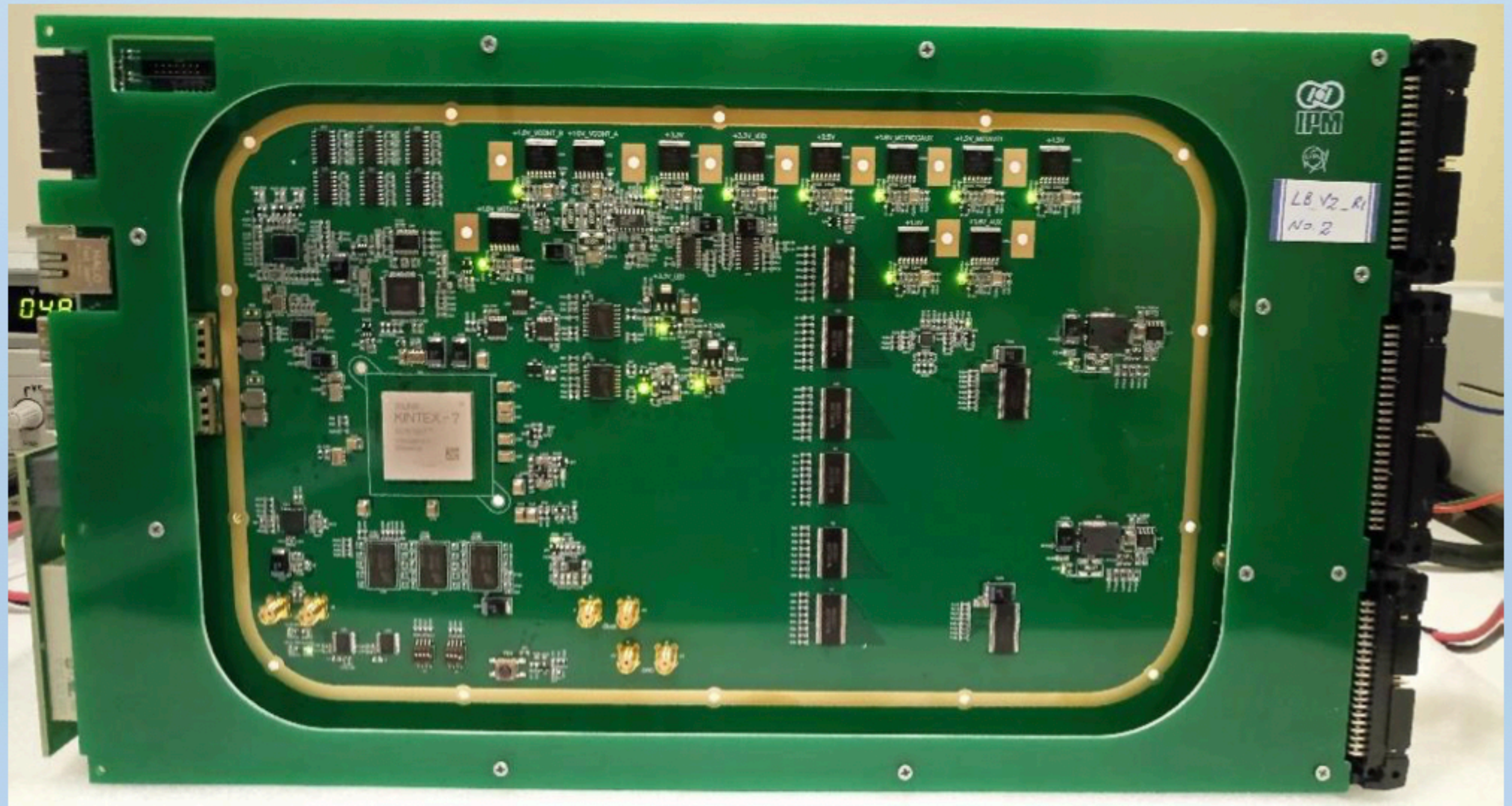
RPC Barrel and EndCap

• Control Board:

- The main bridge between Slow Controller and Link Boards
- Optical Links to receive TTC, Fast, and Slow commands. GBT-FPGA link driver.
- TTC clock and Fast BGo commands, BC0
- TTC Clock Phase shift adjustment
- FEB Parameter Configuration and Verification.
- Control and monitoring the Link Boards Histograms, Data Logs and Diagnostics through front panel bus.



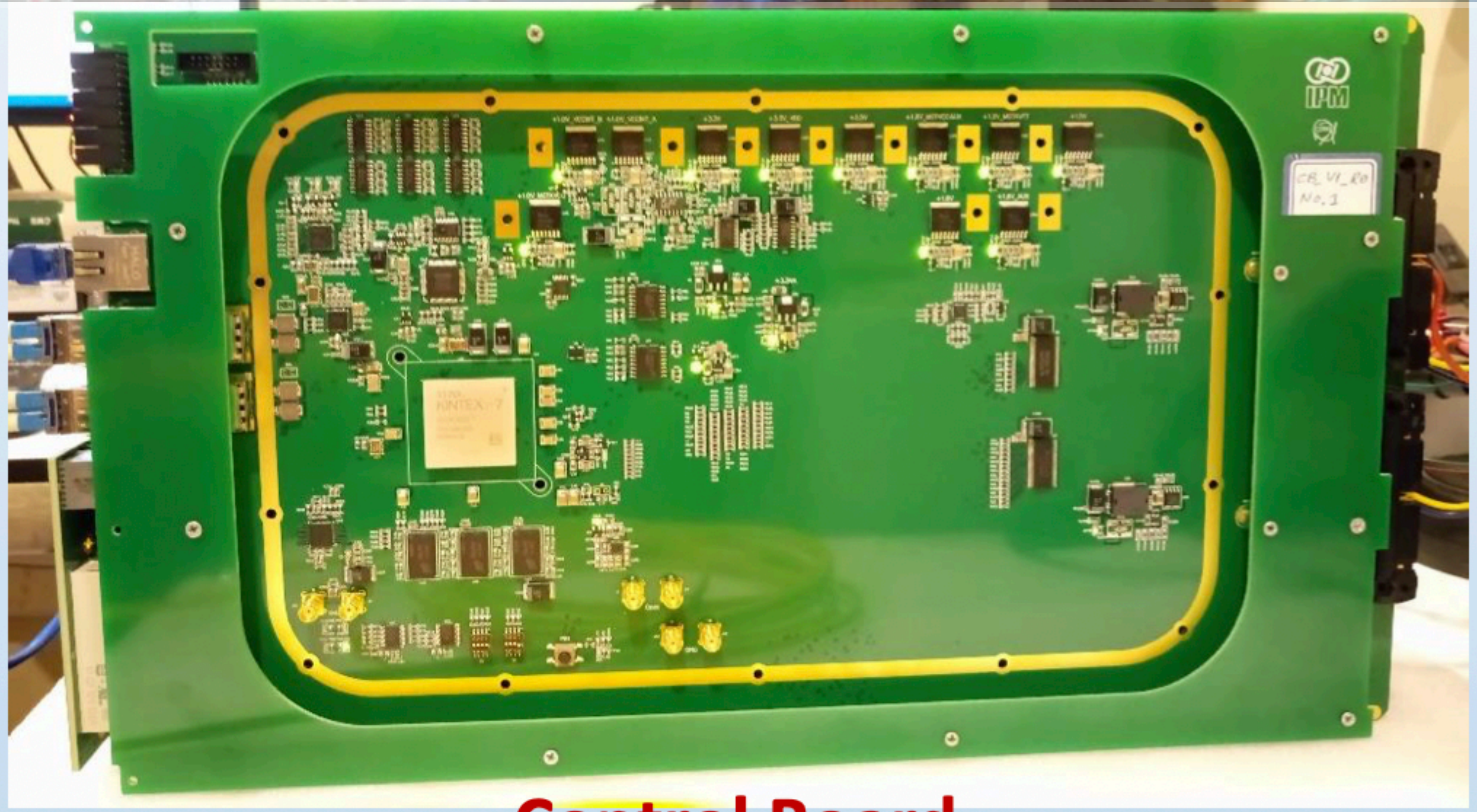
Control Board



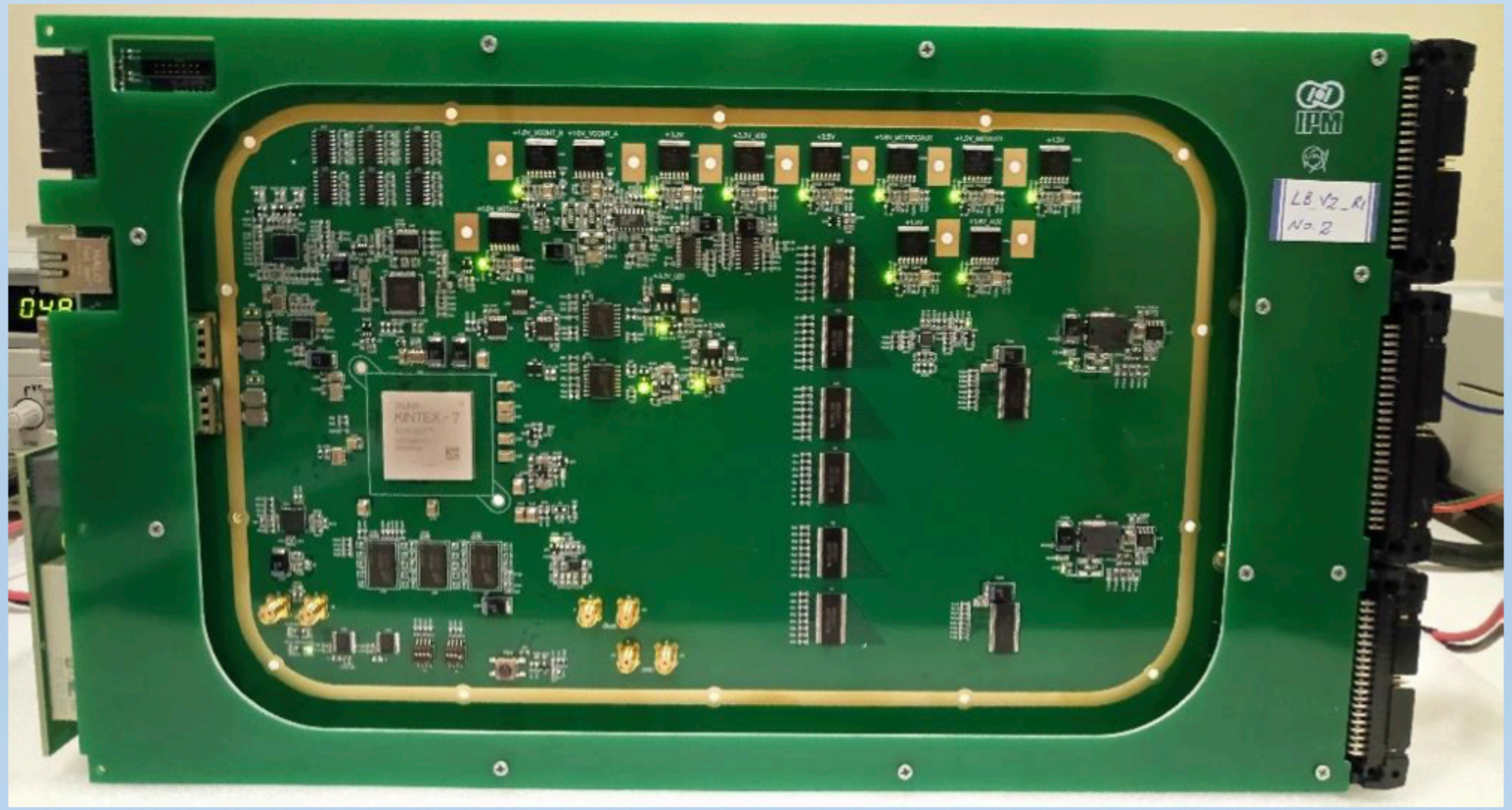
Link Board

RPC Barrel and EndCap

- **Link Board Main Functions:**
  - **96 Input Channels. 15 kV ESD protected.**
  - **24 output Channels to trigger the FEB to check the FEBs, Flat cables, and all interface connectors.**
  - **Detector Diagnostic and monitoring:**
    - **Full/Close window Histograms**
    - **RPC Data logging**
    - **Timing Histogram**
  - **Muon Hit time information with a TDC resolution of 1.5 ns.**
  - **Collects 42 hits per Bunch Crossing without buffer overflow and data loss.**
  - **Transmit 21 hits per Bunch Crossing to the L1T through 10 G optical Link.**
  - **Voltage, Current, temperature, and Radiation Protection features.**



Control Board

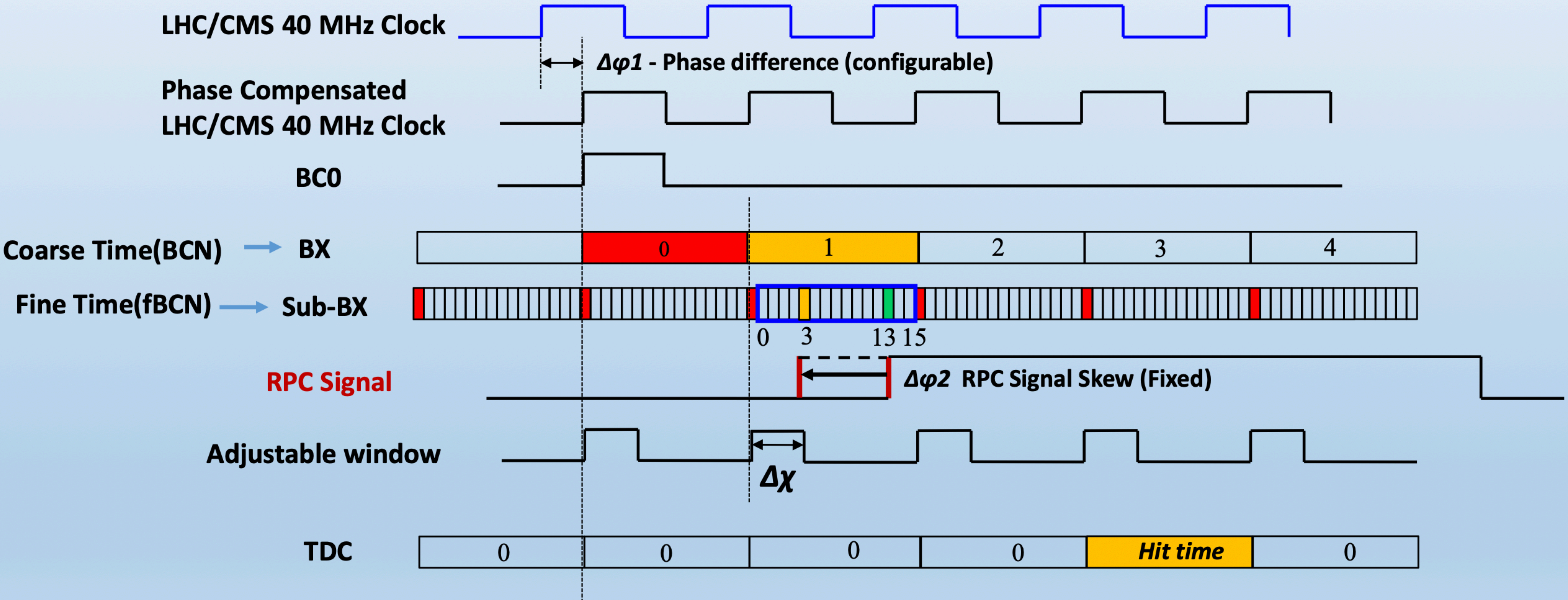


Link Board

RPC Barrel and EndCap

- **RPC signals time Stamp**

  The first step of the RPC signal processing is the measurement of RPC signal arrival time and assignment of this data to the phase compensated LHC/CMS clock (40 MHz) .



Hit time = BCN + fBCN ± Δφ1 ± Δφ2