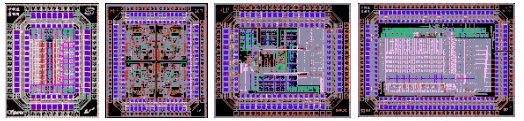


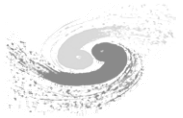
ASIC R&D Progress for ATLAS Silicon Pixel Detector Upgrade

CPPM & IHEP

W WEI (IHEP)
N Wang (IHEP) JP Luo(IHEP) Z WANG(IHEP)
RC Fei(CPPM) P Panguad(CPPM)
JC Clemens(CPPM) A Rozanov(CPPM)

9 April 2011

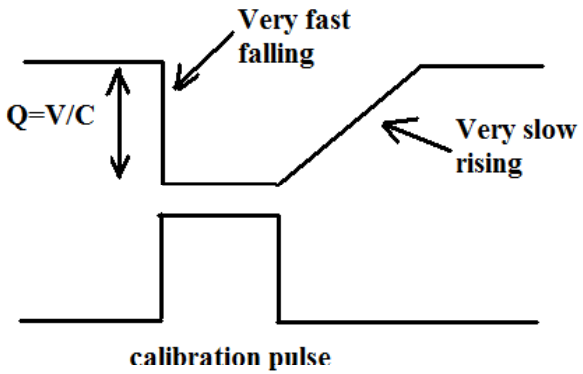
Details of Collaborations of 2010~2011



- **FEC4_P3C pulse generator (W. WEI)**
  - **Design**
  - **Single chip measurement result**
  - **FEC4_P3C associated with FEC4_P1 measurement**
- **Other Designs and simulation:**
  - **Design of power saving blocks for pixel unit (W. WEI)**
  - **Full chip functional evaluation of FEC4_P3 (W. WEI)**
  - **Power-on-reset block (N. WANG)**
  - **Modification of the SEU latch (N. WANG)**

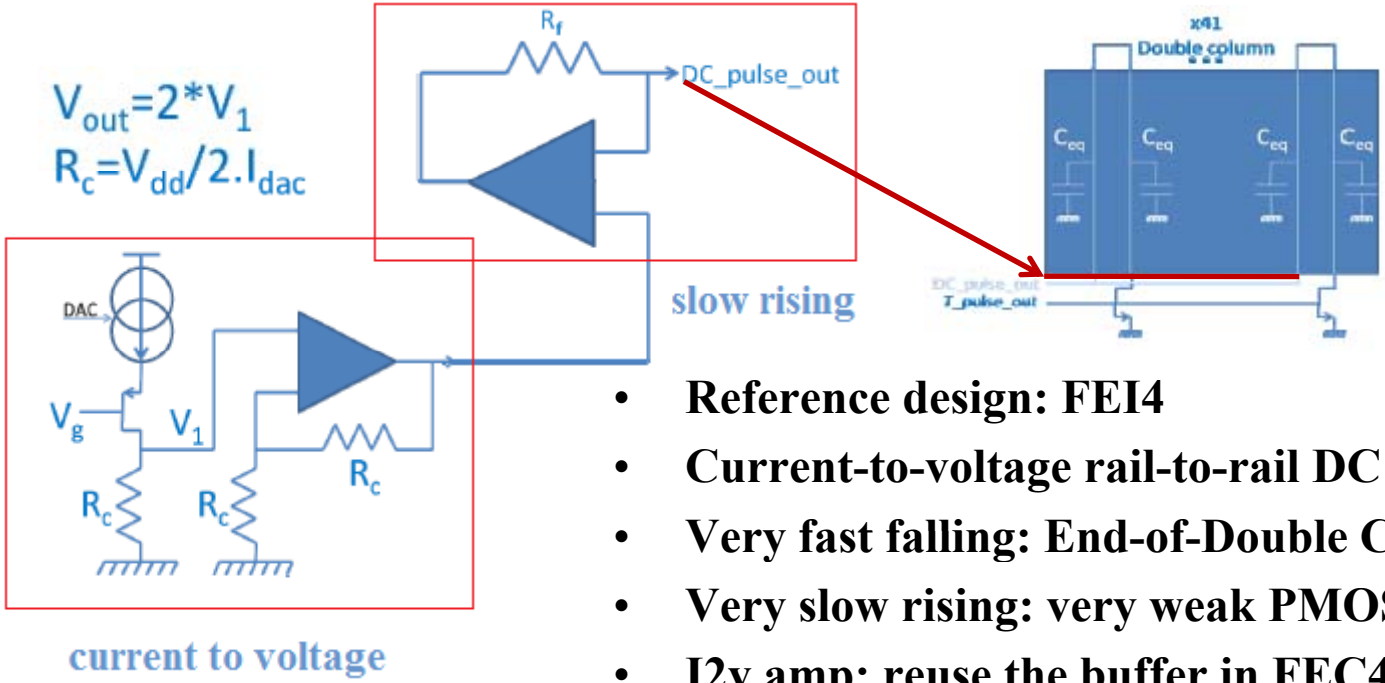
FEC4_P3C pulse generator

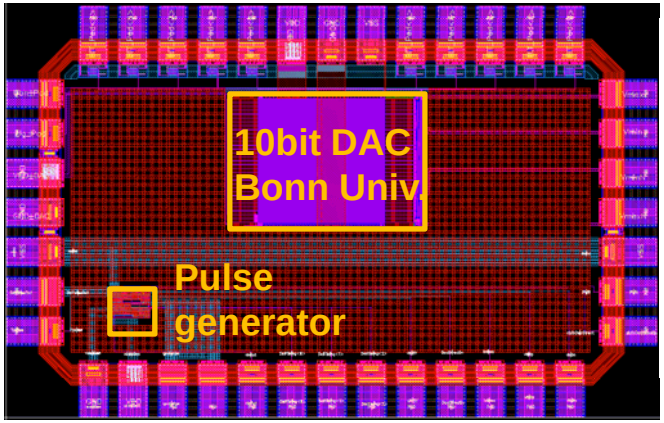
- **Provide a very fast and precise pulse to the pixel matrix**
- **Up to 30k pixels (FE_I4 case), parasitic capacitive load of 40pF~80pF**
- **A falling edge faster than 10ns to avoid ballistic deficit**
- **Rising time of hundreds of μs to avoid baseline shift**
- **Capable of pulse phase tuning and rising time tuning**



Dynamic range	0~1.5V (rail-to-rail)	Input DAC range	0~30 μA
Pixel matrix	53760 pixels	Load capacitance	53pF
EoDC switches	82	Falling time	< 2.5ns
Rising time	20μs~500μs	Rising time tuning	3 bits
Delay span	50ns	Delay tuning	6 bits
Output DC linearity (Full isolation)	< 1%	Output DC linearity (Shrunk isolation)	< 0.5%
Process corner endurance	all	Temperature corner endurance	-20~50
PSRR	40dB	Offset	< 9mV
Noise	<200μV rms	Power down	Yes

Design of the pulse generator

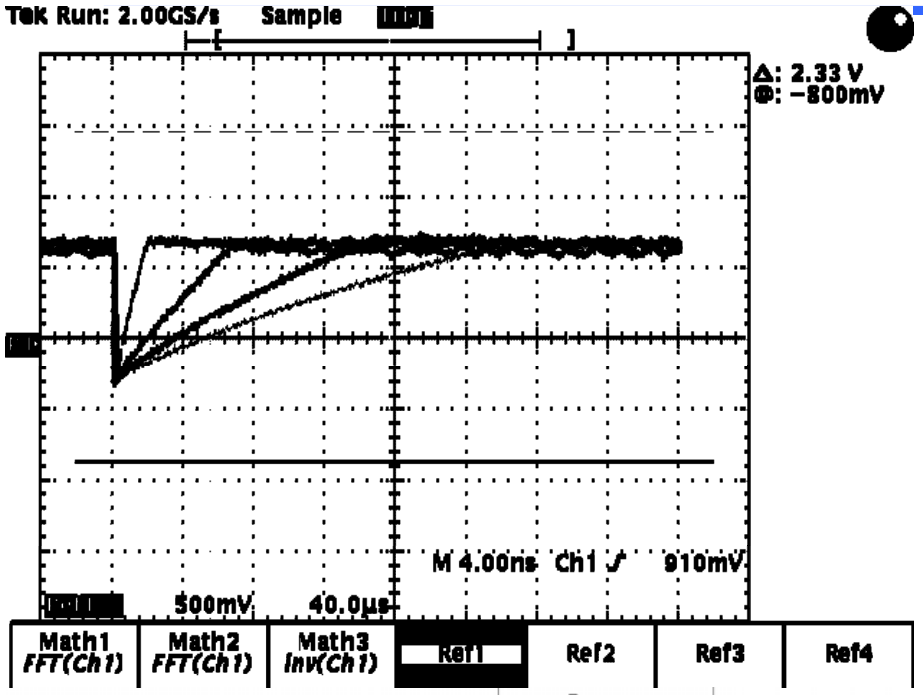




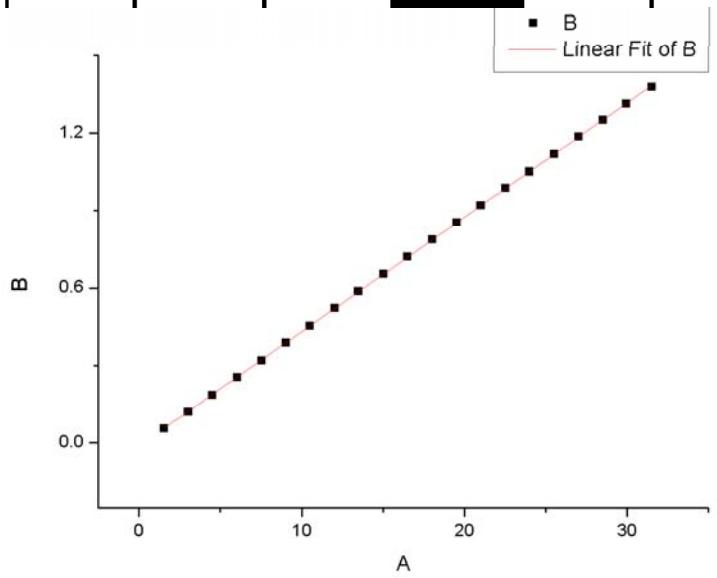
- Reference design: FEI4
- Current-to-voltage rail-to-rail DC output
- Very fast falling: End-of-Double Column Switches,
- Very slow rising: very weak PMOS and big resistor
- I2v amp: reuse the buffer in FEC4-P3 (designed by Jiangping)

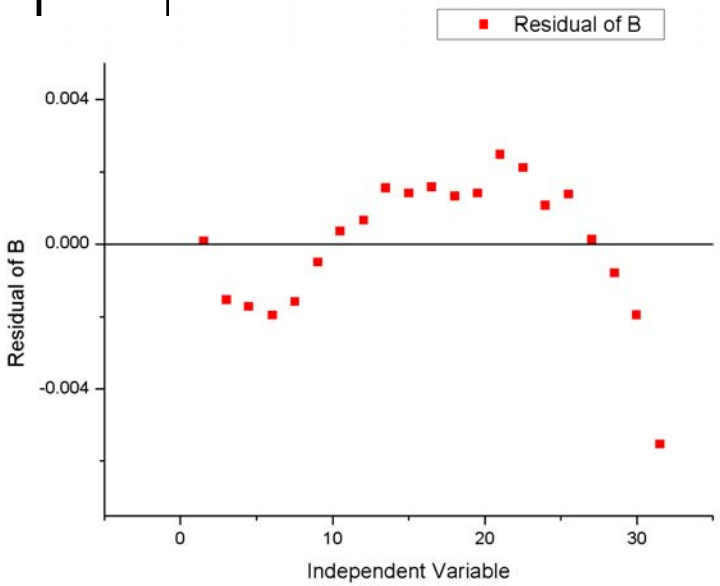
  Weak stage: modification on FEC4_P3 buffer
- Buiding blocks chip FEC4_P3C
- Tapeout: Nov. 2010, measurement: March, 2011
- Size of chip: 2.5 ×1.5 mm^2
- Area of block: 150 ×150 μm^2
- 20 pads (maximum sets)

Measurement for single block



- Falling time for charge injection: < 4ns @ 2ns stimuli pulse
- Rising time tuning:
  - Overlapped snapshots from four measured outputs with different tuning bits configuration(001/011/101/111)
  - Showing rising time is tunable 20~400 µs
- Dynamic range: Better than 1.4V
- Linearity: <±0.5%
- Similar results as in simulation





FEC4 P3C & P1 combined system

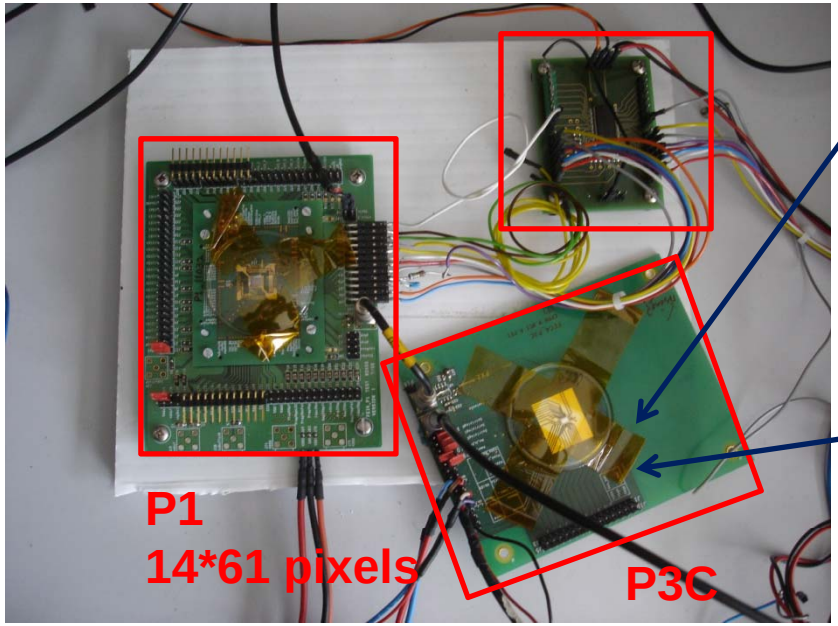
Volt controlled
by GPIB

Keithley 2410
V/I SourceMeter

CPPM current source module

USB
Interface

Current Output
Controlled by Keithley



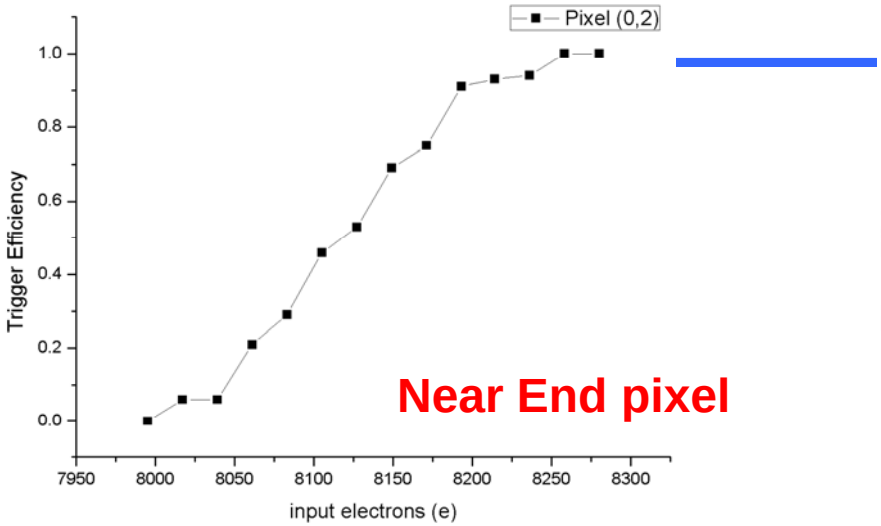
P1
14*61 pixels

P3C

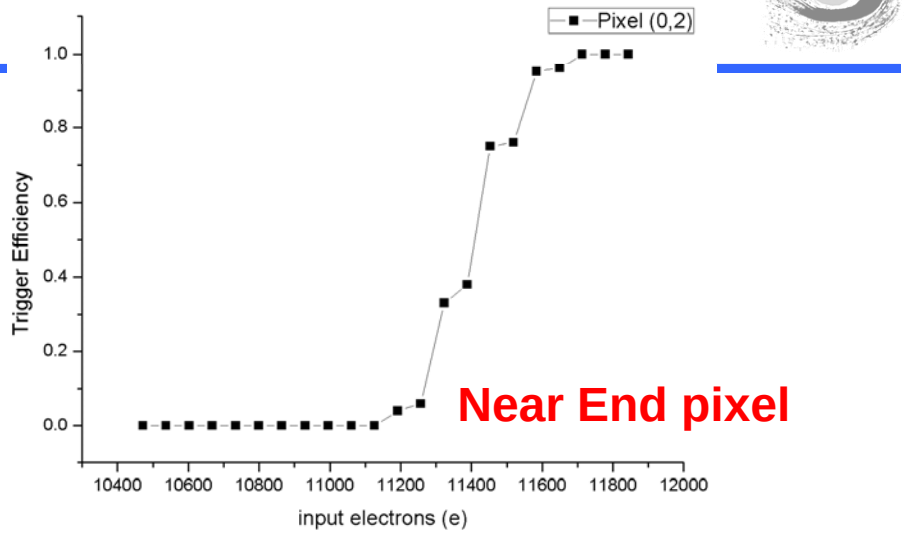
Calibration pulses output

HP8110A Pattern generator

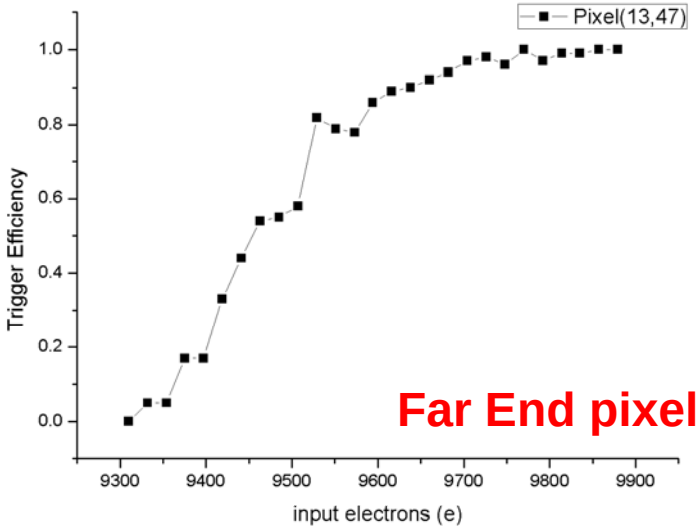
S-curve measurement



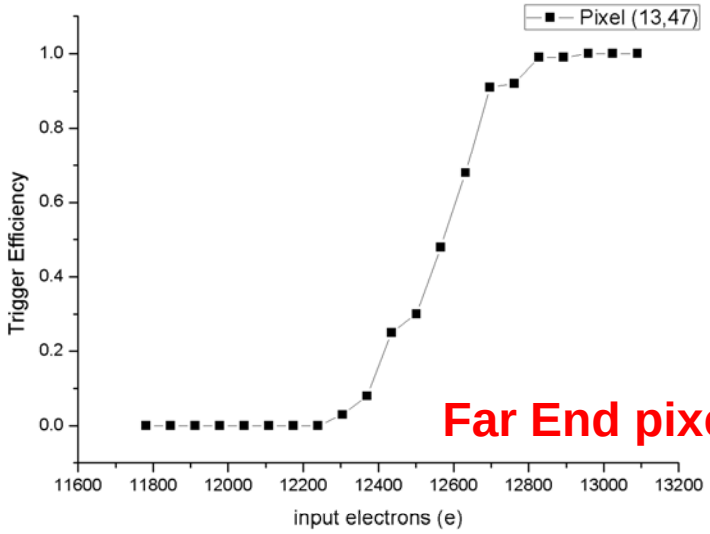
Pixel (0,2) HP generator + P1
Rms = 50e, 50% threshold =8117e



Pixel (0,2) P3C generator + P1
Rms = 104e, 50% threshold =11409e

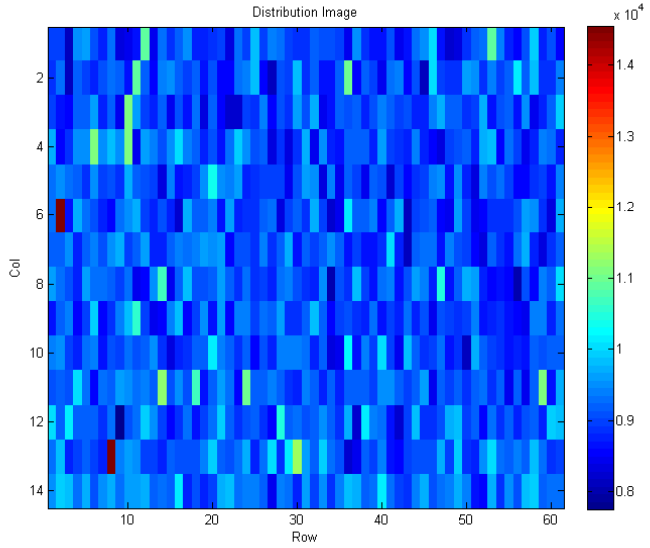


Pixel (13,47) HP generator + P1
Rms = 95e, 50% threshold =9454e

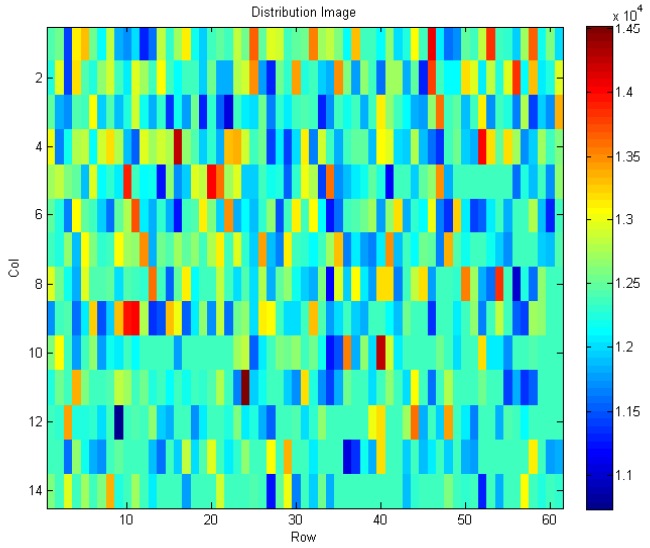


Pixel (13,47) P3C generator + P1
Rms = 109e, 50% threshold =12572e

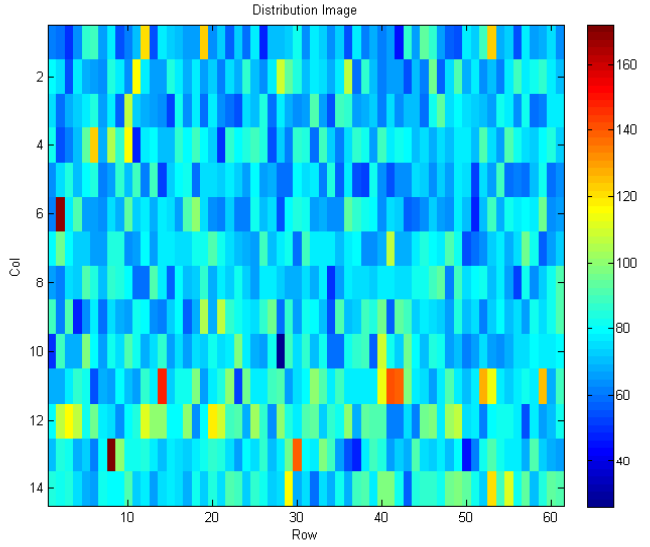
Full chip scan image



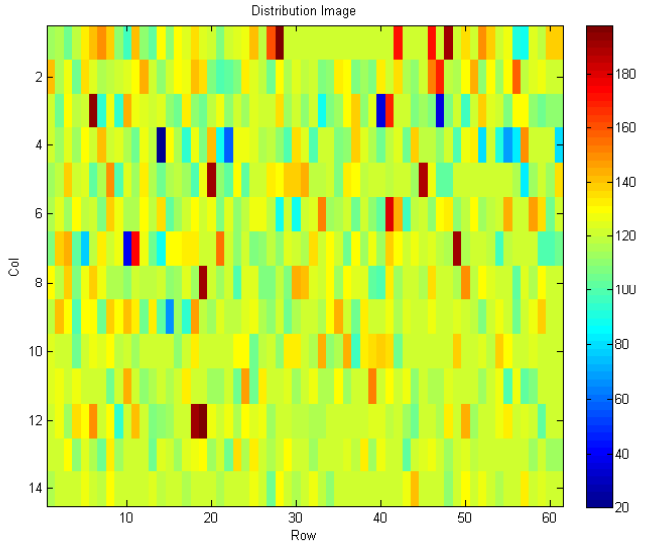
HP generator + P1, threshold distribution



P3C generator + P1, threshold distribution

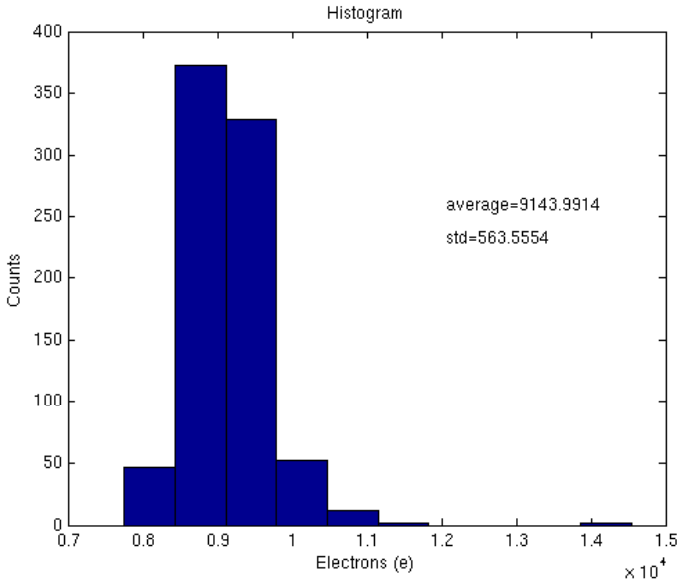


HP generator + P1, noise distribution



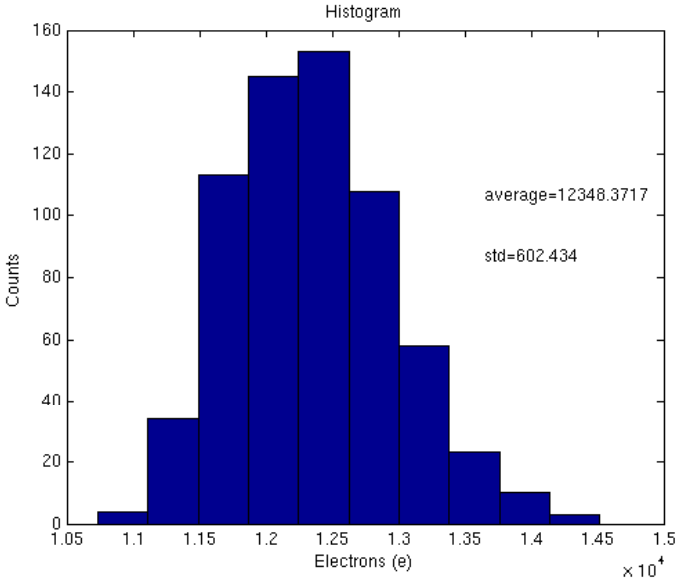
P3C generator + P1, noise distribution

Dispersion comparison



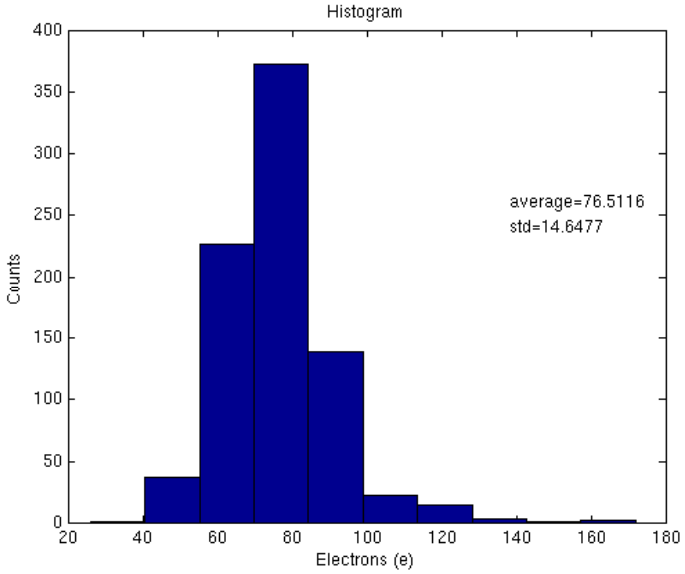
Aver=9.1ke
std = 563e

HP generator + P1, threshold histogram



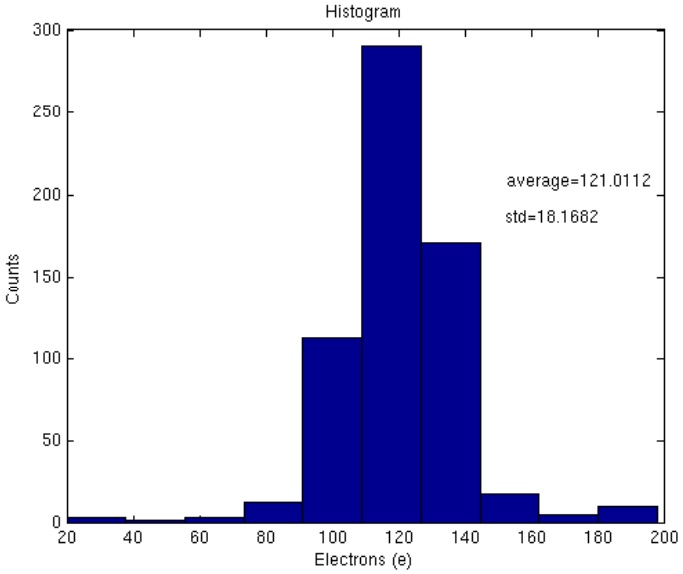
Aver=12ke
std = 602e

P3C generator + P1, threshold histogram



Aver=76e
std = 14.6e

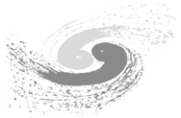
HP generator + P1, noise histogram



Aver=121e
std = 18.2e

P3C generator + P1, noise histogram

Summary of the measurement

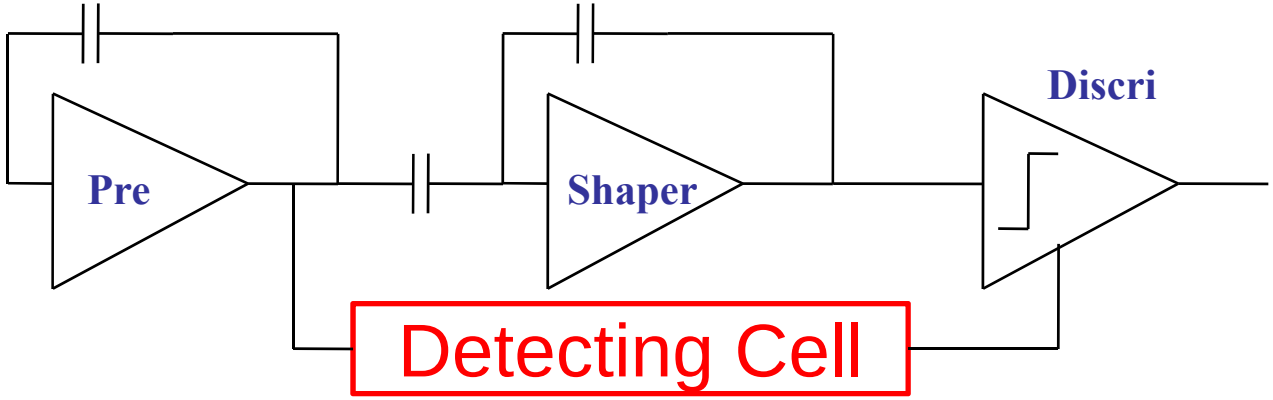


- **Single block**
  - **Functionality is good: fast falling, slow and tunable rising edge**
  - **Performance: linearity < ±0.5%, dynamic range: > 0~1.45 V**
  - **Unterminated problem because of the very high output impedance, expected to be solved in the final internal version**
- **Combined with P1 pixel matrix load**
  - **P3C pulse generator is compatiable with P1 load**
  - **No growing of threshold/noise dispersion was found**
  - **PCB connections a issue: reflections are hard to be eliminated – rms noise slightly increased**
  - **Expecting a better performance in final version if the generator is dwelled inside the chip**

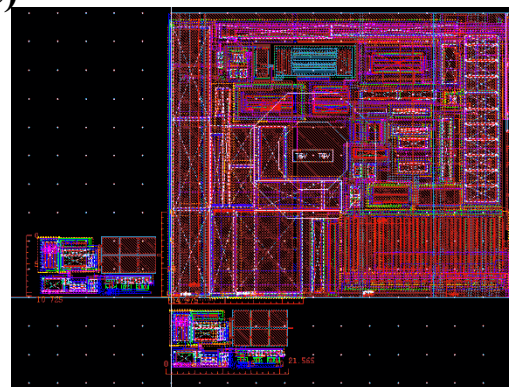
Details of Collaborations of 2010~2011

- **FEC4_P3C pulse generator (W. WEI)**
  - **Design**
  - **Single chip measurement result**
  - **FEC4_P3C associated with FEC4_P1 measurement**
- **Other Designs and simulation:**
  - **Design of power saving blocks for pixel unit (W. WEI)**
  - **Full chip functional evaluation of FEC4_P3 (W. WEI)**
  - **Power-on-reset block (N. WANG)**
  - **Modification of the SEU latch (N. WANG)**

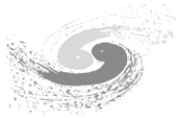
Design of the power saving blocks



- **Power consumption of Pixel: Analog 10 µA, Digital 10 µA**
- **FEC4_P3 pixel: half size of FEI4, 2X amount – 2X power**
- **To save power:**
  - **Design optimization (static)**
  - **Sleep – low power standby – wakeup – working – sleep (dynamic)**
- **A most power consuming block: discriminator (4 µA)**
- **Preamp output monitoring → Wakeup pulse for Discri**
- **Design issue:**
  - **Very large gain: Preamp output → Digital level**
  - **Speed: Wakeup pulse to be faster than TOT output**
  - **Area: very limited space in the exsiting FEC4_P3 design**



Full chip overall simulation and evaluation

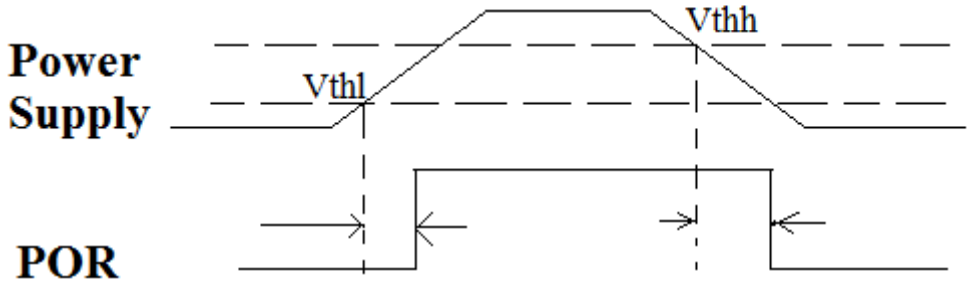


- **Full chip overall simulation**
  - **Common simulation: configuration of pixels are preset, configuration phase ignored**
  - **Real case of operation: configuration → normal operation time consuming in simulation**
  - **Overall simulation by FastSpice (Ultrasim):**
    - **Work as in the real case**
    - **Evaluate all the bias settling**
    - **Evaluate the configuration process and compatiability with PUC**
  - **Debug: Problems of HitEn, ClrGlobal, LdEn… were solved**
- **Full chip power network layout evaluation**
  - **Power distributed as a non-ideal grid with para. R**
  - **IR Drop: Bias condition may vary from near end to far end**
  - **FastSpice (Ultrasim Power Network Solver) with estimated R from layout extraction, to evaluate IR Drop and bias of all pixels**

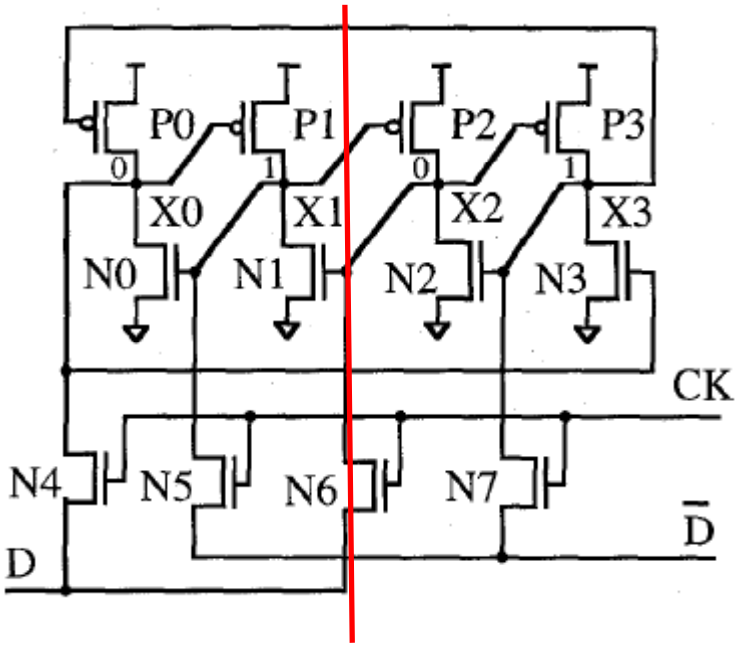
Power-on-reset block

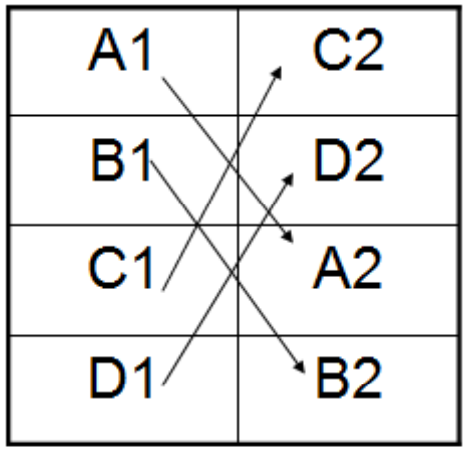
Designed by N. WANG

- Reset signals generated on both of the rising and falling edge of power supply
- Hysteresis of 100mV
- Implanted to Chrt 0.13 µm
- Compatiable with both 1.5V and 1.2V supply
- Layout is ready, to be embedded in the next tapeout



Modification of DICE latch for SEU





4-latch cell

by N. WANG

- **Included two latches in each cell**
- **SEU is restricted in one latch, the other one remains unchanged**
- **Capable of anti-SEU**
- **Modification:**
  - **Based on the 4-latch cell**
  - **Further separate the complementary node, enhance the anti-SEU capability**
  - **Layout size shrunk**
- **Expected to be evaluated in the next tapeout**

Summary and future

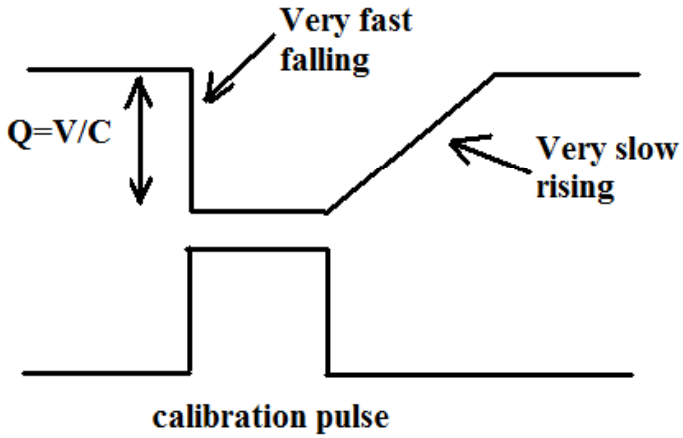
- **Collaboration between CPPM and IHEP was successful and fruitful in the past few years and will continue**

- **IHEP would like to contribute more on the coming ATLAS silicon pixel upgrades especially on the frond-end readout chips**

Thank you !

Backup Slides

Functionality

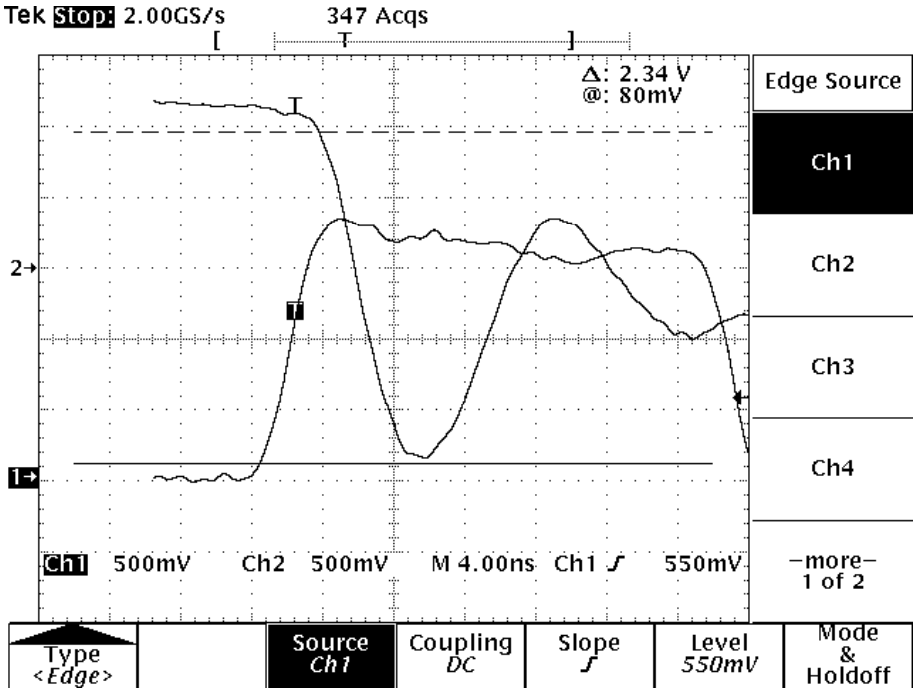


Output specification:

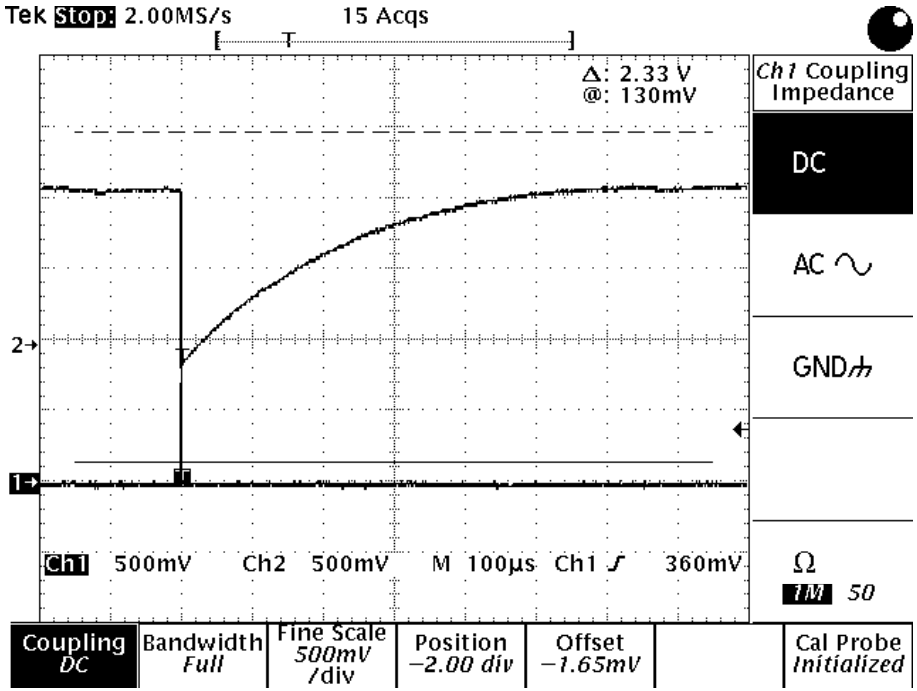
1. **Very fast falling edge -> charge injection**
   (less than 2.5ns @ 0.5ns input rising edge)
2. **Very slowing rising edge -> baseline restoration**
   (3-bits tuning, 20 µs ~ 500 µs)

Ringings detected due to the unterminated cable

Expected to be eliminated if dwelled inside the chip

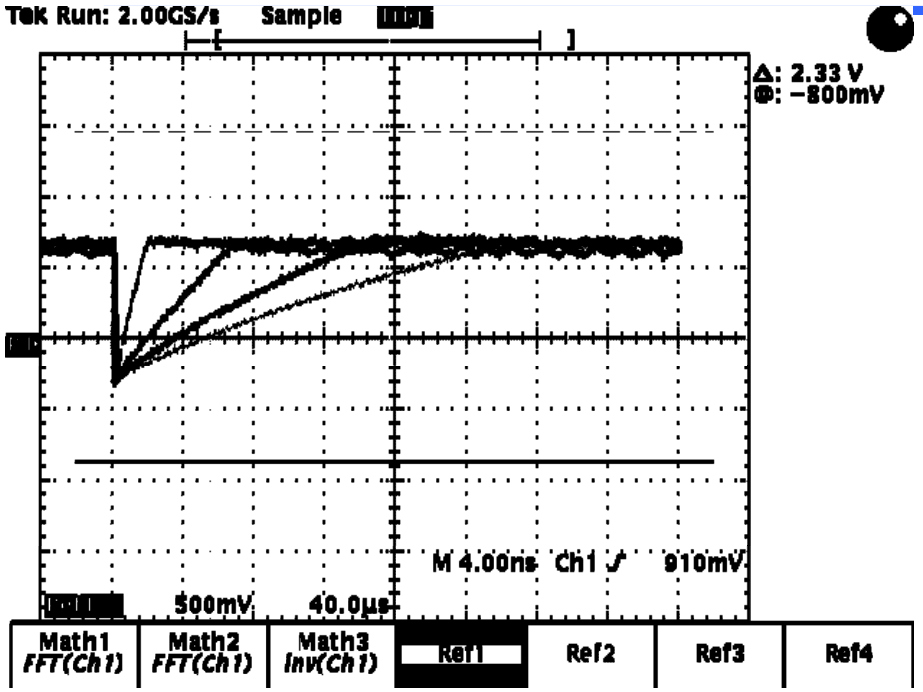


falling edge ~ 4ns @ 2ns input rising edge



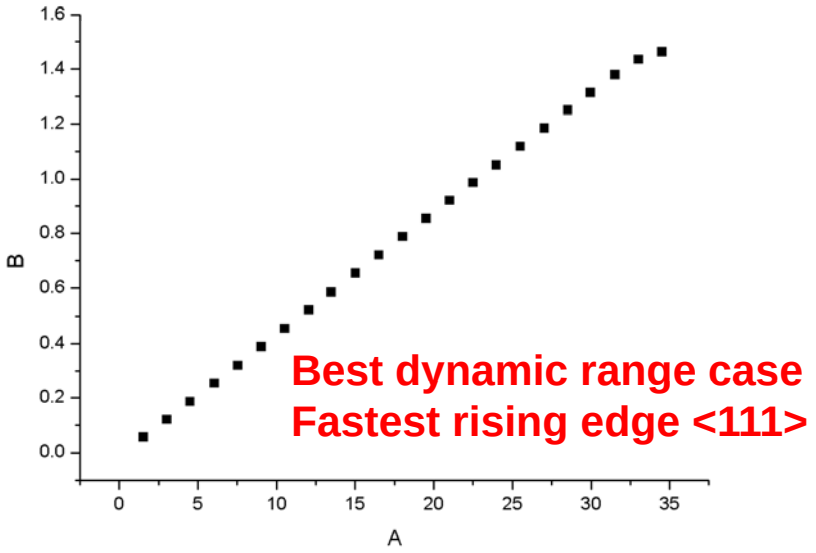
Rising edge ~500 µs @ 25uA input current

Performance

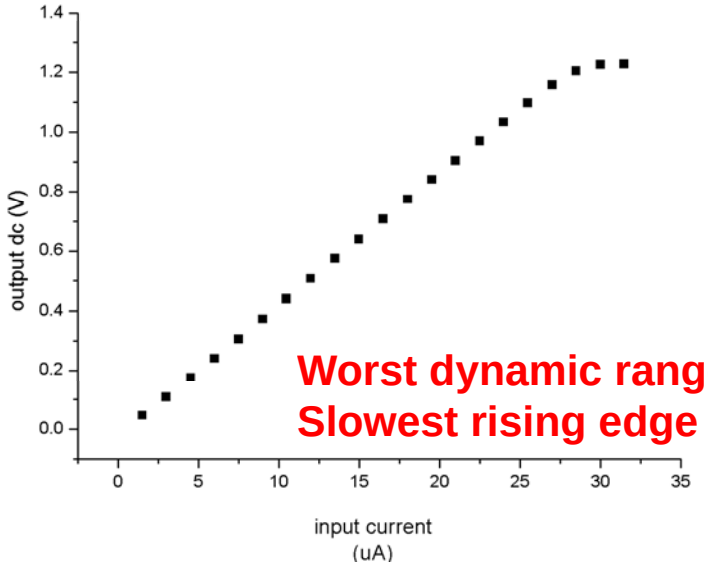


- **Rising time tuning:**
  - Overlapped snapshots from four measured outputs with different tuning bits configuration(001/011/101/111)
  - Same input current 20 µA, output 1 V
  - Same time scale 40 µs/div
  - Showing rising time is tunable 20~400 µs

- **Dynamic range:**
  - Best case: fastest rising: 1.45 V
  - Worst case: slowest rising: 1.3 V
  - Same result as in simulation

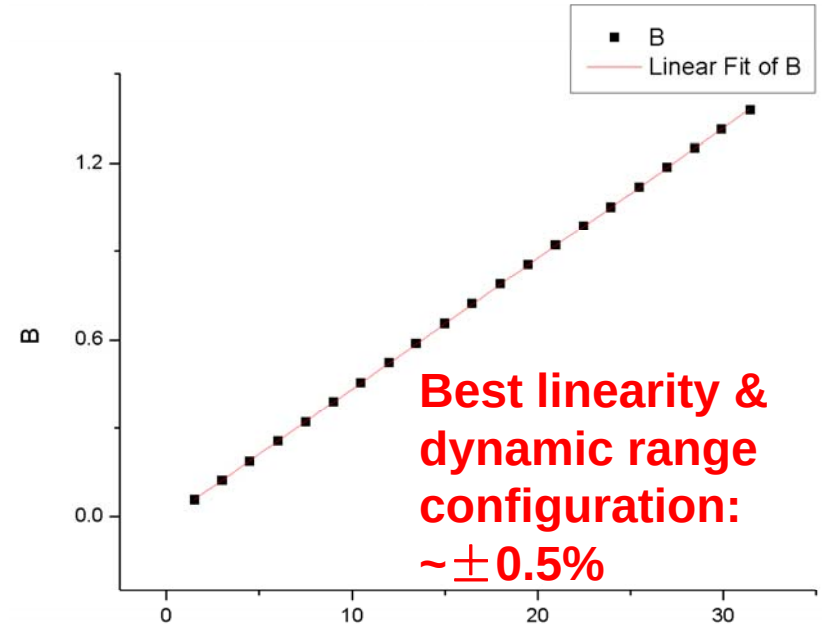


Best dynamic range case
Fastest rising edge <111>

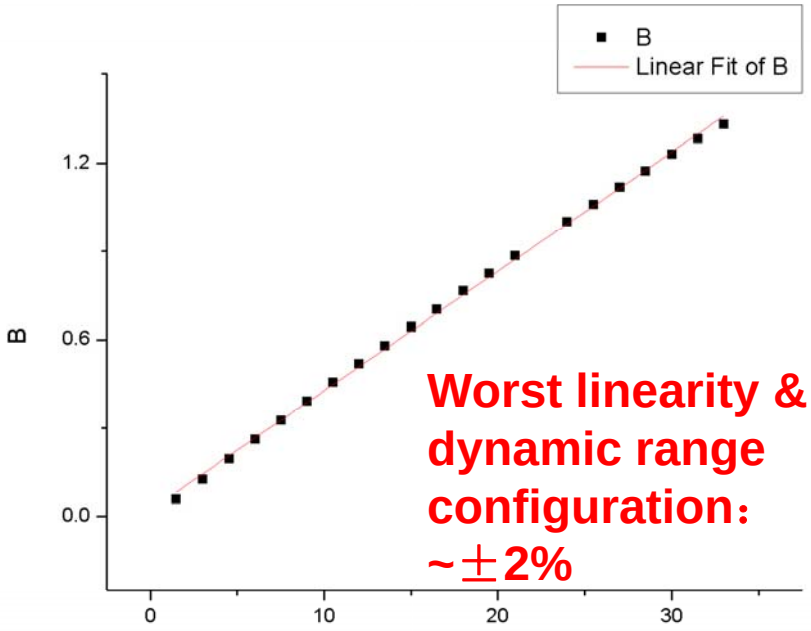


Worst dynamic range case
Slowest rising edge <000>

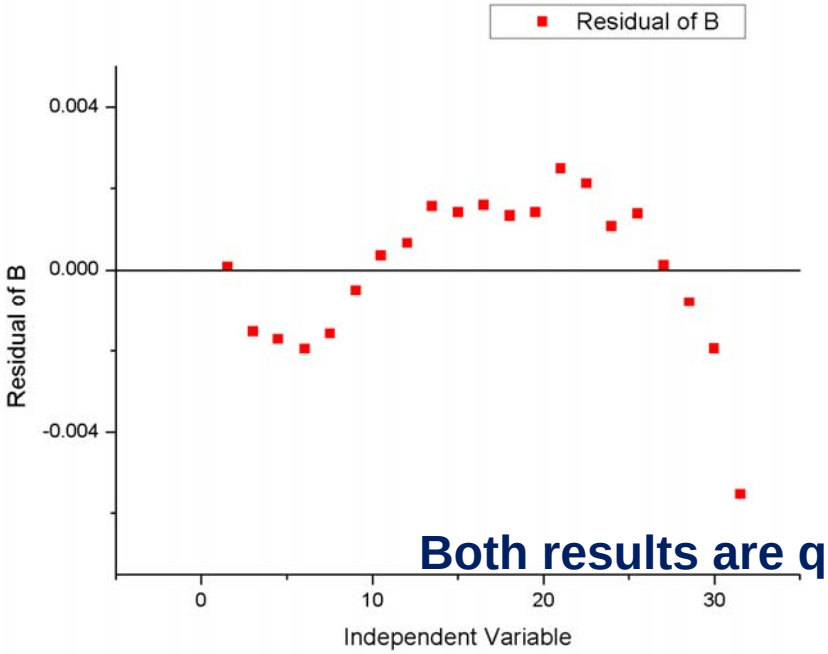
Linear fit result

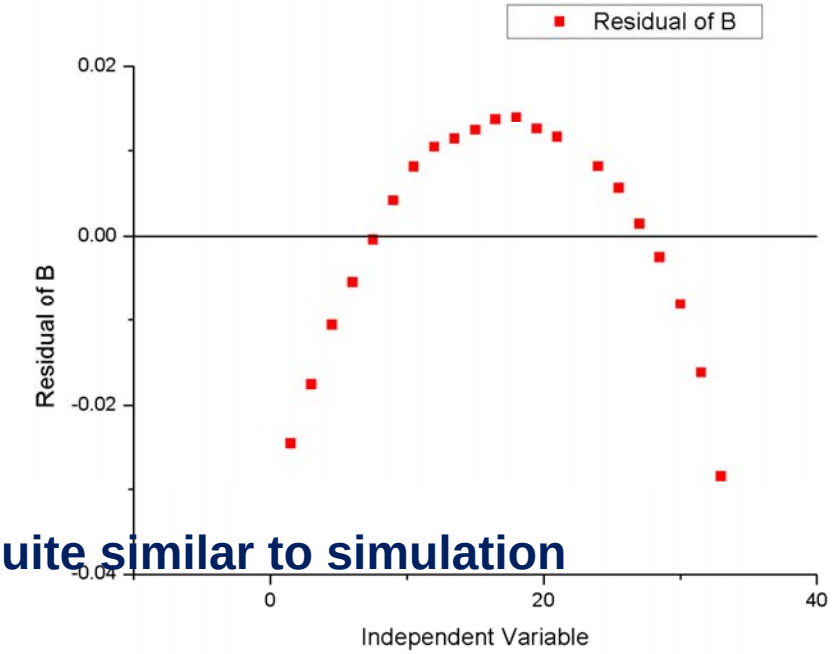


Best linearity & dynamic range configuration: ~±0.5%



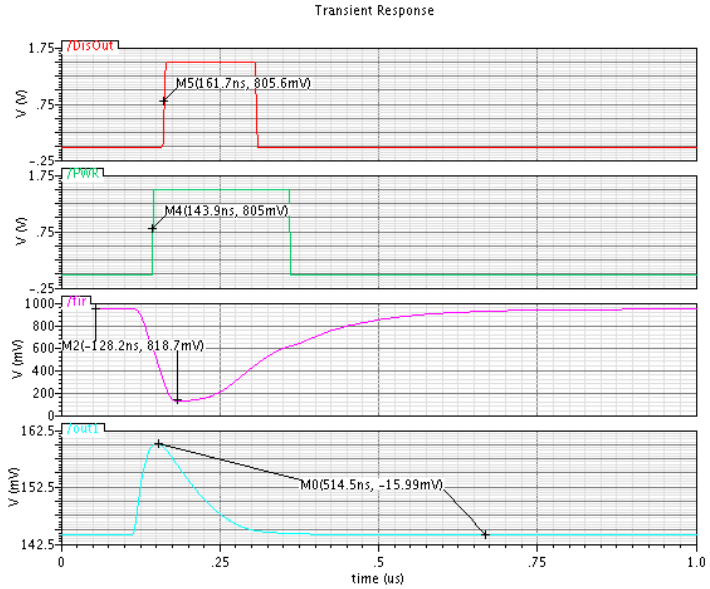
Worst linearity & dynamic range configuration: ~±2%





Both results are quite similar to simulation

Design and simulation



- Transimpedance
- Equivalent:
  - DC close loop (operating pt.)
  - AC open loop (large gain)
- Optimization: para. & corner
- Discriminator: modified for fast wakeup and settling
- M.C. sim: explore the full corner range