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# Simulation of the Tracker implementation in the electronic trigger at the super-LHC

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### Outline

#### Scenario for the luminosity upgrade

- Machine upgrade scenarios
- The CMS detector upgrade plans.
- Physics potential
- CMS Tracker Trigger for Phase II
  - Data rate reduction and requirements
  - Possible layouts
- First results with simulation and 7TeV Data
- Outlook and conclusion

### **Draft 10 year plans (Chamonix 2011)**

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Pixel	Upgrade	<ul> <li>CMS - New Pixel. New F</li> <li>Photodetectors. Compl</li> <li>FWD muons upgrade</li> </ul>			X-mai	-	
		LHCb - full trigger upgra vertexdetector etc.	ide, new				
Injectors					NI <b>K</b> NIKA		
	SPS - LINAC4 connection & PSB energy upgrade	x					

### **Physics potential**

- Improve Measurements of new phenomena 'seen' at the LHC for example:
  - Higgs coupling and self-coupling
  - Properties of SUSY particles (mass, decay branch ratios, etc.)
  - Coupling of new Z' or W' gauge bosons
- Detect/Search low-rate phenomena inaccessible at the LHC for example
  - $H_{SM} \rightarrow Z\gamma$  (BR ~ 10<sup>-3</sup>),  $H_{SM} \rightarrow \mu + \mu -$
  - Top decays via Flavour changing neutral currents (FCNCs)
- Push Sensitivity to new high-mass scales, for example
  - Quark substructure
  - New forces : Z', W'
- Extra dimensions
  - Reach 6TeV for 300fb<sup>-1</sup> (LHC) , ~7.7TeV for 3000 fb<sup>-1</sup> from direct observations

#### **REQUIRE FULL PERFORMANCE DETECTORS**

#### 2013 Shutdown:

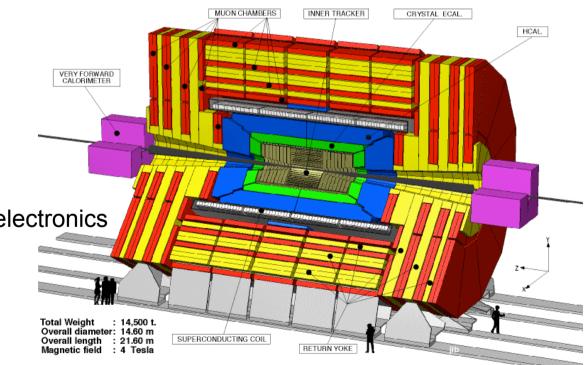
- Begin installing forward muon systems
- HO SiPMs (hadronic Calorimeter Tail Catcher)
- HF PMTs (Forward Hadron Calorimeter eta 3-5)
- Pixel Luminosity Telescope
- Install new beampipe

#### • 2017 Shutdown:

- Install new pixel detector
- Install HB/HE photo-detectors
- Install new trigger system

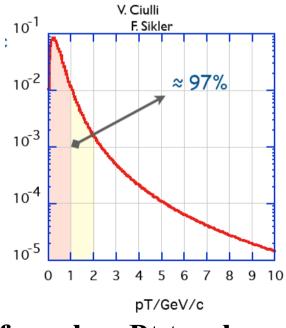
#### • 2021 Shutdown:

- Install new tracking system
- Trigger system upgrade
- Major consolidation/replacement of electronics systems
- Calorimeter Endcaps
- DAQ system upgrade

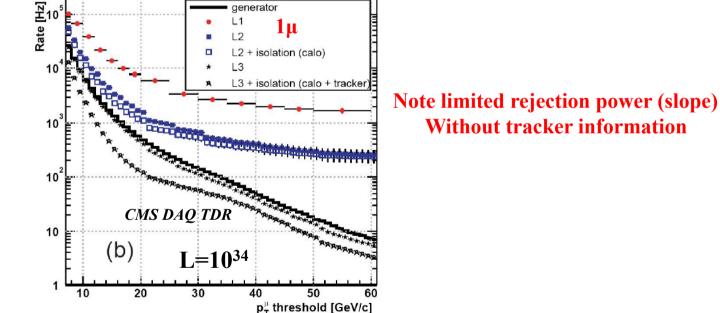


Current CMS detector

- At SLHC luminosities, the total L1 trigger rate, without use of Tracker data, is expected to exceed the nominal limit of 100kHz by a large factor, probably exceeding an order of magnitude.
  - Having tracking information available in trigger Level 1 (L1) would provide a new handle in the trigger to reduce the L1 rate
  - Without the Tracker it would be hard to maintain an open L1 trigger
- About 90% of the charged particles produced in minimumBias collisions have Pt<1GeV/c and ~97% have Pt < 2GeV/c</li>



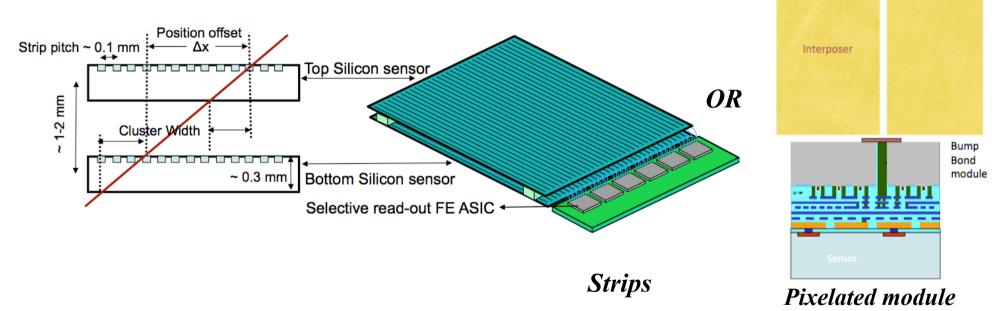
- At SLHC luminosities, the current L1 trigger for basically all trigger object (muons, electrons, taus) needs to be improved
- We need improved resolution for the Level1 itself by using the tracker data
  - Attach tracker hits to improve Pt assignment precision
  - The tracking trigger should provide a track matching and isolation for tau and electron identification



**Provide tracking info in L1 (trigger primitive up to eta=2.5)** 

### Tracker-trigger : How to reduce data volume

- Two possibilities to reduce data volume (based on the track deviation in the plan perpendicular to the CMS magnetic field):
  - Cluster width approach
    - Cluster width (number of contiguous strips) is proportional to the radial distance of the sensor from the IP and inversly proportional to the Pt
  - Stacked tracker: correlation between hits in nearby sensors
    - Exploit track direction of flight measurement to evaluate Pt

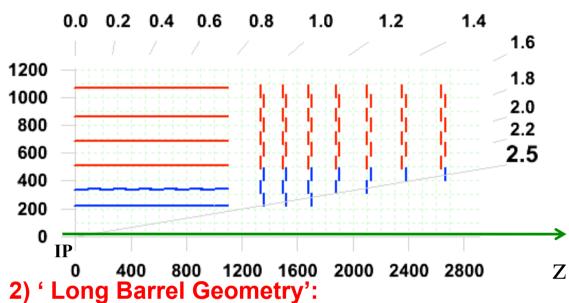


The location and geometry of the triggering layers have to be integrated into the layout of the 'outer' Tracker

- These layers are the most challenging
- Will require very dense services (power, cooling, readout)
- Note, triggerring layers should also contribute to 'regular' tracking

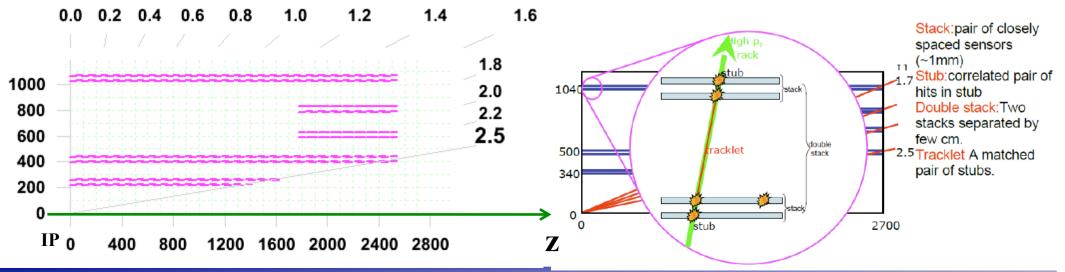
### Layouts under study

#### 1) Layout with Strip stacked modules ('Strip Pt Layout'):

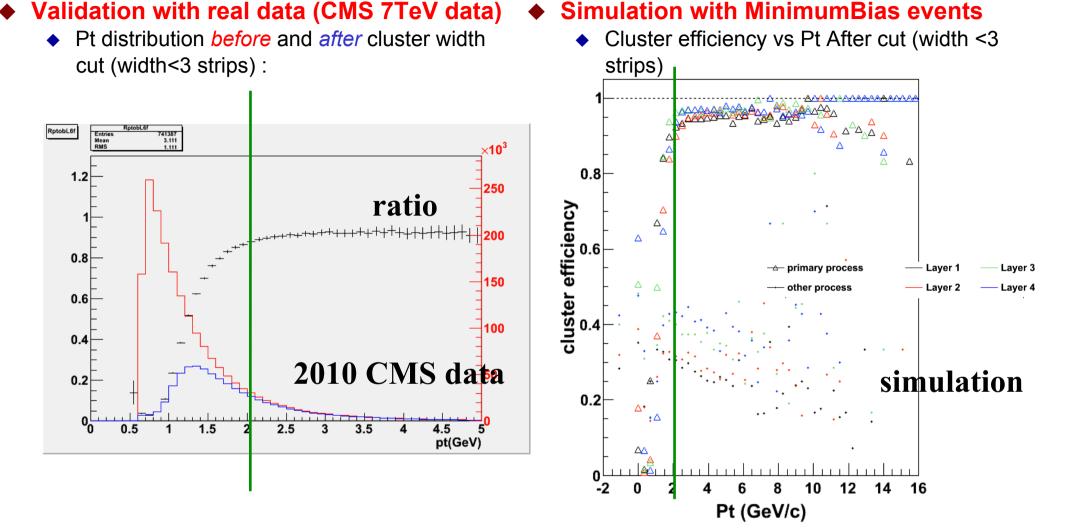


The outer part (red) is populated by Strip stacked Modules ('pt modules') The number of endcap disk is optimized for tracking performance. Possibility to improve z resolution under study.

Long closely spaced layers with coincidence beween layers allow a Pt cut to be applied (Full long Barrel outer tracker of stacked triggering layers) Cluster positions in z direction provided (pixelated modules).



### **Cluster width (CW) approach and Pt selection**



Two main parameters need to be optimized: -The cut on number of strips (cluster width) -The ratio between the layer radius and the pitch Generaly speaking, the typical cut value is at ~2 GeV

### **Occupancy and rejection factors**

- First results from Simulation based on the StripPt layout
  - 200pp interactions pile-up (5.10<sup>34</sup> cms<sup>-2</sup>s<sup>-1</sup> at 20MHz LHC Clock)
  - Silicon Sensors parameters:

Se	ensor thickness	Strip pitch	Strip length	
32	0 µm	90 µm	4.76 µm	
Layer radius (cm)	50	70	90	110
Strip occupancy(%)	1.6	0.8	0.5	0.26
Cluster occupancy (%)	0.4	0.2	0.12	0.06
CW reduction factor	· 2.3	2.5	2.3	2.1

Cluster Width method is a less demanding solution

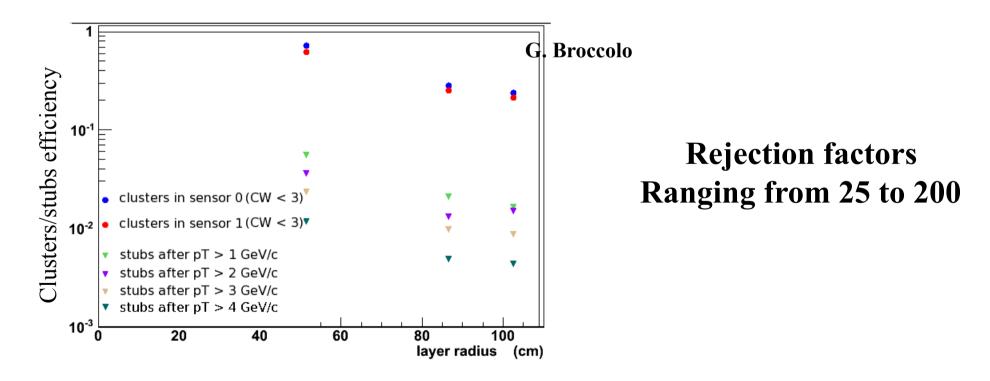
but the transverse momentum selection efficiency will be limited essentially by the sensor thickness (typically 300 microns) and by geometrical effects in the tracker end-cap regions where detectors are perpendicular to the beam axis

### **Cluster width approach and position correlation**

**7Tev Data** : Tracker outer barrel Layer 2 (stereo modules, offset 1 mm) to simulate <u>stacked</u> <u>modules.</u> Layer radius : 70mm



First results from simulation : Clusters and Stub (pair of associated clusters in the two sensors of Pt-modules) efficiency from simulations (offset 2mm):



Full simulation with strip Pt Layout geometry is needed.

### **Selective read-out electronic**

 Thanks to the simulation, one can estimate the needed bandwith (5.10<sup>34</sup> cm<sup>-2</sup>s<sup>-1</sup>, 20 MHz LHC Clock, X2 safety margin):

<sup>1</sup> / <sub>2</sub> modules (8 chips)	L1 (50 cm)	L2 (70 cm)	L3 (90 cm)	L4 (110cm)
Cluster Rate (MHz)	1.6	0.8	0.5	0.3
Stub Rate (MHz)	10.8	4.8	3.6	1.6

- IPNL is developing a full front end ASIC chip (128 channels) including the selective readout functionalities.
  - First version developed, tests in the coming months
- Thoughtputs can be estimated from simulations:

<sup>1</sup> / <sub>2</sub> modules (8 chips)	L1 (50 cm)	L2 (70 cm)	L3 (90 cm)	L4 (110cm)
Cluster flow (Mbps)	28	15	11	6.5
Stub flow (Mbps)	250	110	58	37

More simulation are needed to consolidate mean rates and margins

- Full simulation of the detector with the standard CMS software in needed in order to:
  - Evaluate the data reduction (cluster width study and position correlation),
  - Validate clustering features implemented in the front end readout chips,
  - Optimize configuration parameters (strip pitch length, sensor thickness and spacing between modules).
- Simulation of the track reconstruction from reduced data (Best algorithm and granularity to be implemented in tracking trigger electronic card)
  - Coupling tracker information to the other CMS sub-detectors (global acquisition trigger)
  - Such a step can be performed on the basis of a pattern comparison of cluster maps with a bank of pre-defined tracks or by construction of local track stubs propagated among tracker layers.
- Simulations of physics signals
  - Want to provide both Tracking Trigger and Optimal Tracking in future Tracker

### Conclusion

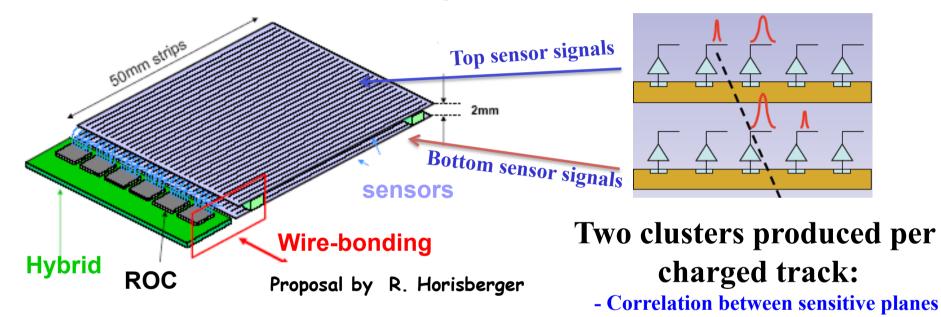
- SLHC would allow to extend significantly the LHC physics reach.
  - Inner/forward parts of the detector must be changed/hardened/upgraded
- Tracker in particular must maintain performances similar to present ones
  - New requirement for trigger functionality
  - Additional challenge of the operation environment
- Simulation activities are coupled with other R&D activities, in particular:
  - Electronic front-end development
  - Mechanics
  - Cooling
  - Data Acquisition system

in order to design a complete detection unit from sensor up to aquisition. The full readout chain could also be tested during dedicated beam tests

## BACKUP

### Strip Pt Modules

Two micro-strip stacked sensors assembled in a single readout unit Same basic concept as pixellated Pt modules For ull size modules, strip length limited to >=5cm



Two-in-one module design optimizes the common use of:

1) Assembly infrastructures: mechanical, material, ROC, cooling, cabling, ....

2) Read out electronics: simple logic to correlate hits, no need of high speed links or external

correlation circuits, saving power,....

➔ Maximize Benefit/Cost

### **Tracker Upgrade for Phase II : R&D activities**

#### **TK simulation and software**

•Layout modelling •Tracking trigger performances •Explore, study and validate trigger concept, compare different layouts •Noise, material, occupancy, cluster size, resolution, data rate •Tracking performance of conceptual Phase2 geometries •Development and maintenance of simulation codes (geometries, pile-up,...)

Electronics	Sensors	Mechanics	CO <sub>2</sub> cooling
<ul> <li>Front-End ASICS</li> <li>Hybrids and interconnects         <ul> <li>Data links</li> </ul> </li> <li>FE Driver and Controller Hardware         <ul> <li>Electronic System Architecture</li> <li>Test/commissioning hardware</li> </ul> </li> </ul>	<ul> <li>HPK sensors</li> <li>Irradiations</li> <li>3-d silicon</li> <li>Diamonds</li> <li></li> </ul>	Qualification of materials • 3d modelling • Thermal modelling / lab tests • Deformation analysis •	<ul> <li>Process qualification         <ul> <li>Modelling</li> <li>Components / system</li></ul></li></ul>
Power distribution	Beam tests		*
Activities/topics • ASICS evaluation • System development • Integration and system tests	Activities/topics <ul> <li>Hardware development and maintenance</li> <li>Planning/running tests</li> </ul>		