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Progress on TaichuPix chip

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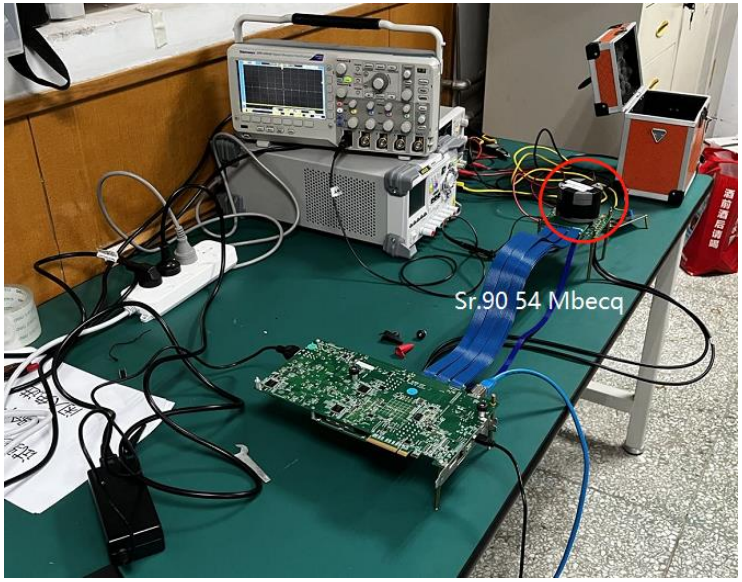
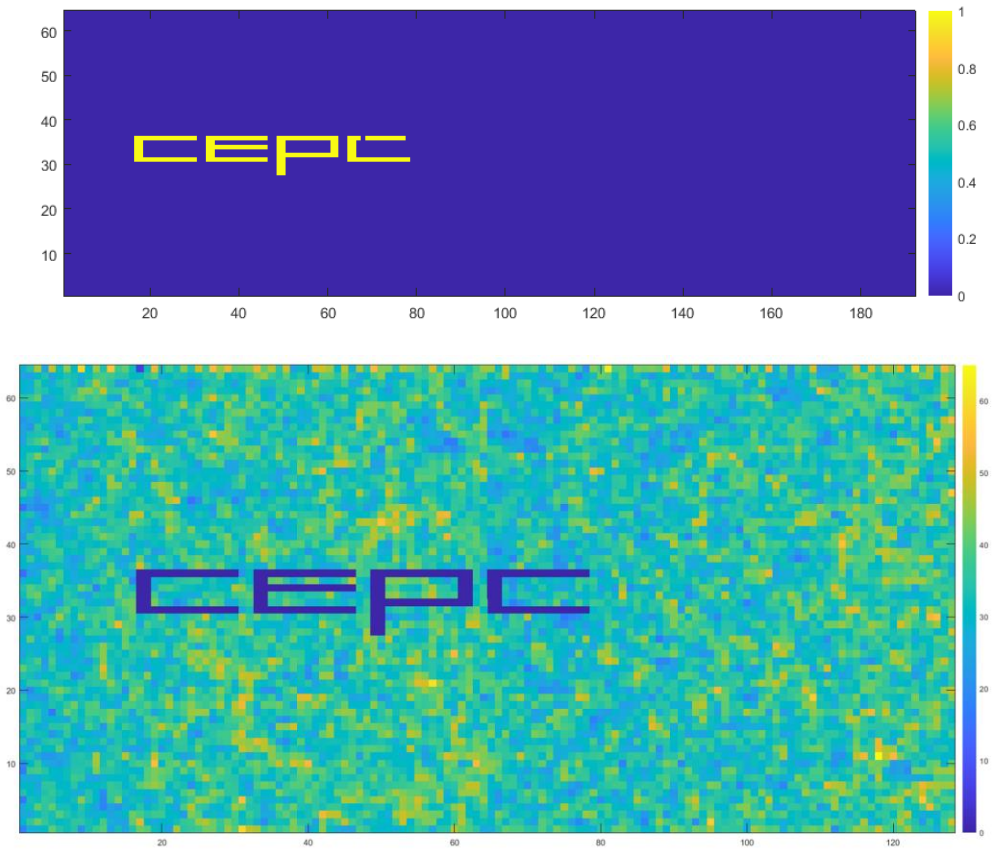
CEPC
Circular Electron Positron Collider

TaichuPix2 on new beta source

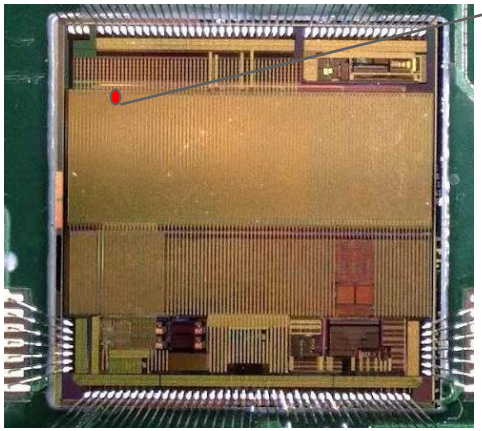




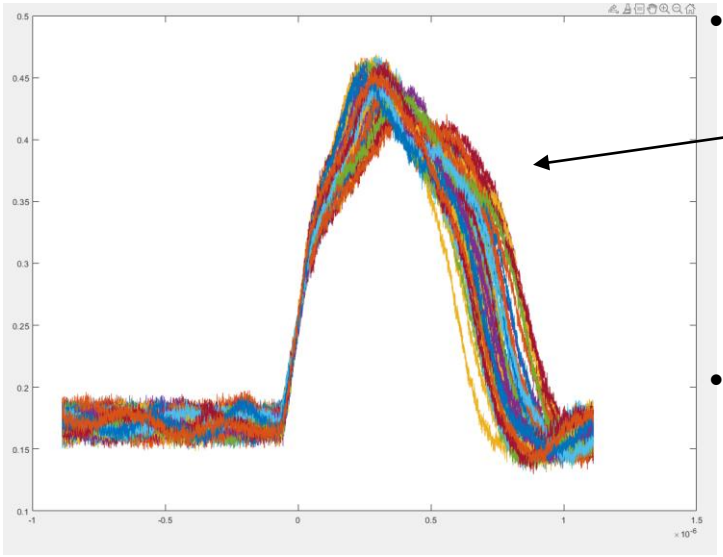
- Masking some pixels and writing a “CEPC” on the chip
- The beta ray injected into the masking field can be shielded

→*It indicates the noisy pixels can be shielded as well.*

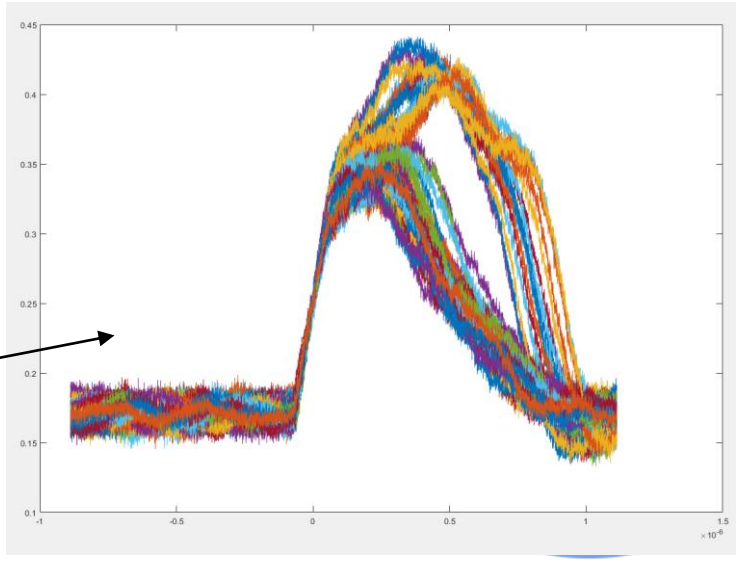
TaichuPix2 on new beta source



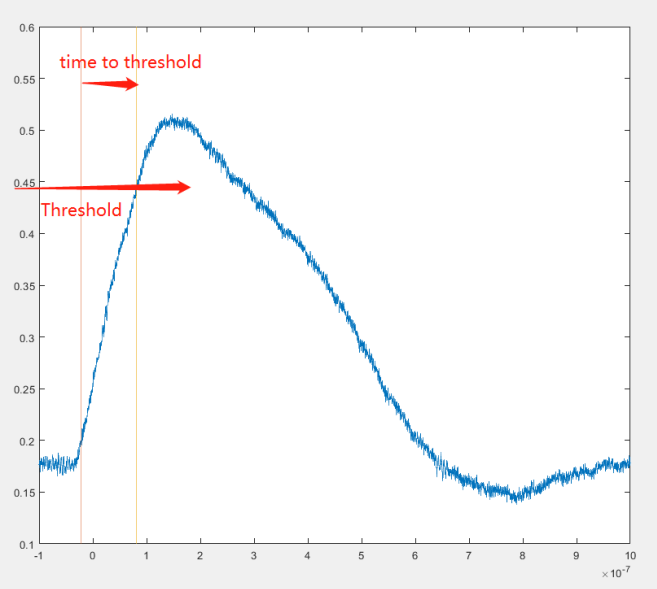
- *An OUTA0 prob is used to measure the waveforms (Pixel <7, 127>)*
- *ITHR is set to 1010, and VCASN is around 515 mV, with a measured threshold of 340mV apulse injected voltage.*
- *The response of OUTA0 at threshold injected voltage is shown below. (injected 340mV vs injected 300mV)*
- *It indicates a threshold waveform is a voltage level over 450 mV*

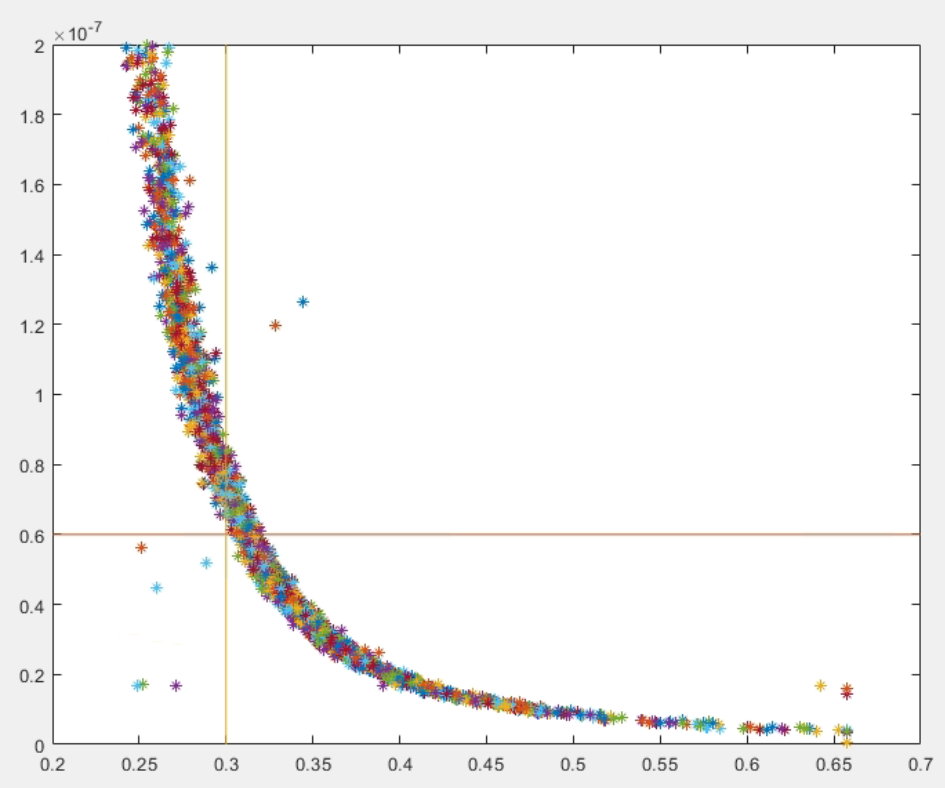


- **Many signals are over 450mV with 340mV injected voltages and 51 hits were recorded from the serializer.**
- **All of the signals are below 450mV and 18 hits were recorded.**



Timewalk scan by beta source

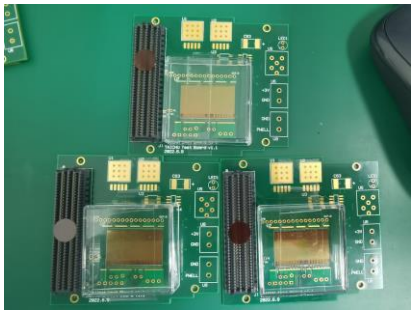


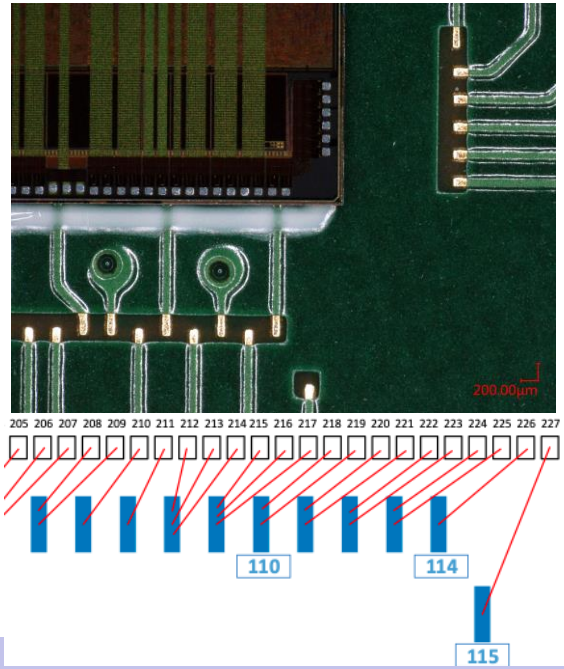


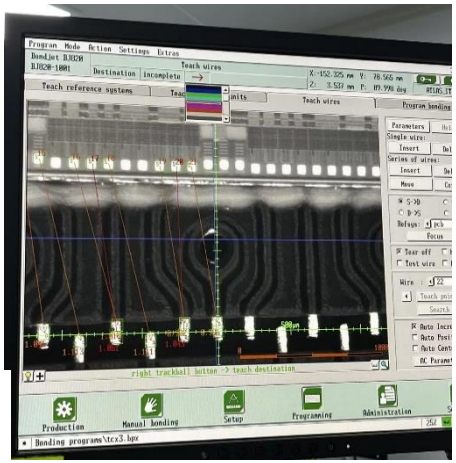
- Recording 3000 waveforms by oscilloscope.(from OUTA0)
- Calculate the time to the threshold to set the Y-axis, X-axis corresponds to the amplitude of each waveform.
- The average time walk obtained from distribution is around 70 ns.

Status of TaichuPix3

- Two strategies were carried out for test board wire bonding:
- 1) 5 test PCBs were sent to company (plan to do full wire bonding to every pad)
- 2) 1 test PCB was wired bonded at IHEP (only half pads can be done at this moment)



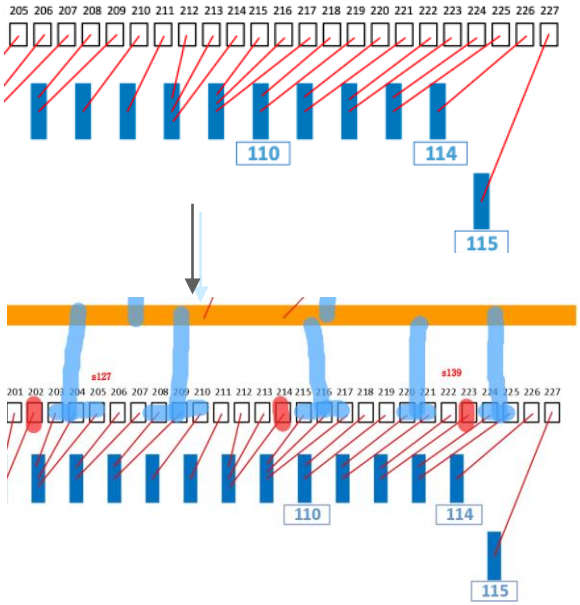


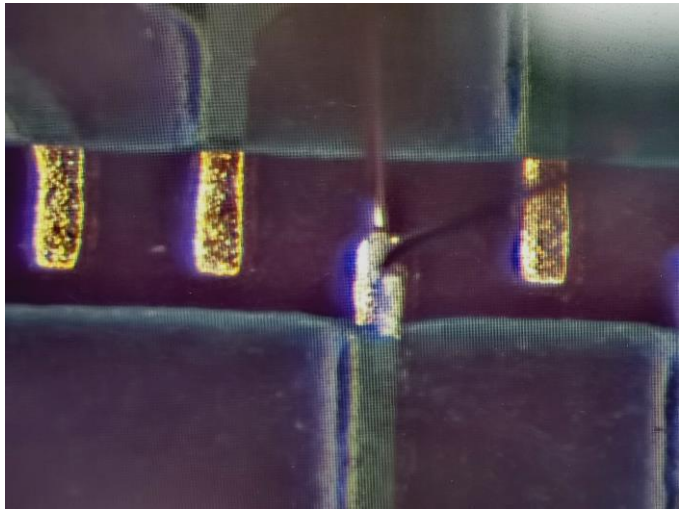


Challenges:

- 432 pads on TCX3 connect to 234 pins on PCB, it's easy to make mistakes on wire bonding, the rule is complicated to check wires one by one.
- For some pins on PCB maps to 3 wires, the dimension of pins is limited.

Status of TaichuPix3





- For wire bonding at IHEP

→disconnect one wire on the 3 wires-pins

→the GND is connected to the long GND bus

→ To flex board, only pads at the bottom will be connected, the half connected test board can compare the performance of the chip.

- For future test board

→Expecting a map that pads on TCX3 match pins on PCB(one by one), then it's easier for wire bonding and we could speed up the process at IHEP.

→Expecting a hole to the backside of PCB, more experiment can be carried out, like laser test?

Thanks for your attention!