Status of the JadePix telescope and the CPV chip development

Yunpeng Lu

Aug. 29, 2022

Outline

- JadePix-3 Telescope *
  - JadePix-3 CMOS chip
  - Prototype of beam telescope
  - Initial test with cosmic rays
- CPV-4 3D integration **
  - 3D-SOI and CPV-4 development
  - Visual inspection on 3D chips
  - Test plan

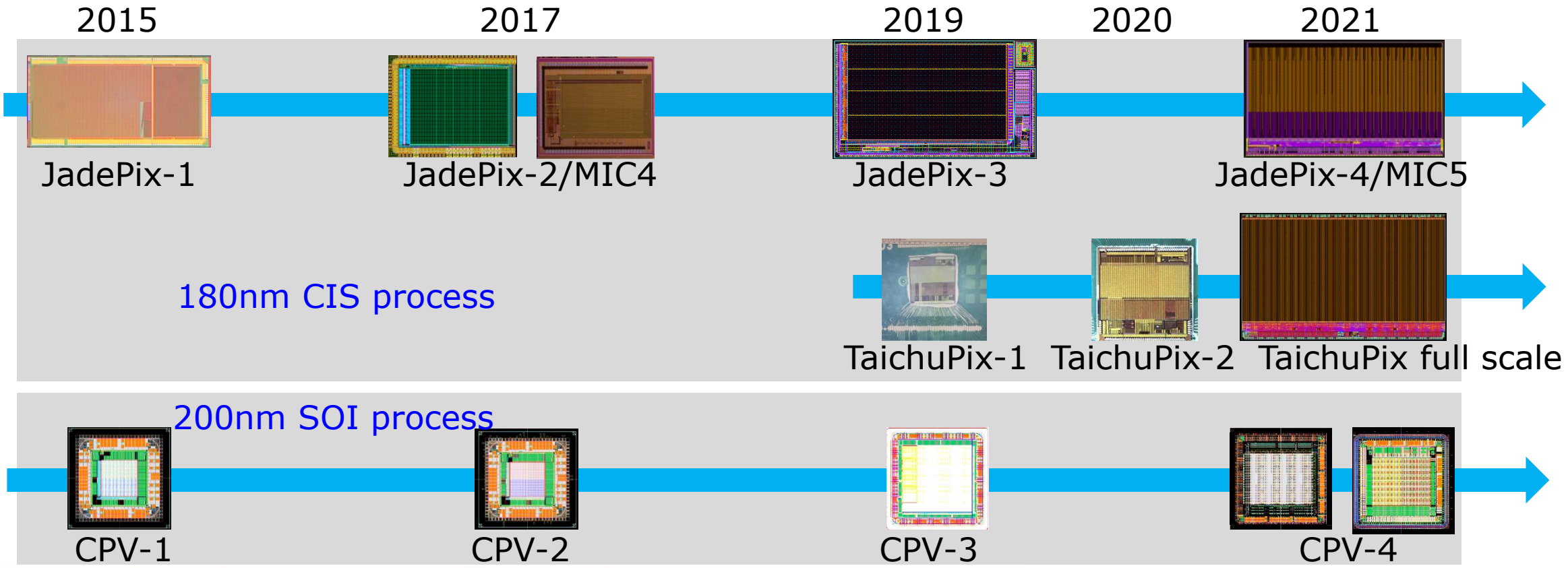
* Sheng Dong[1], Yunpeng Lu[1], Hulin Wang[2], Qun Ouyang[1]

** Yunpeng Lu[1], Yang Zhou[1], Jia Zhou[1], Hongyu Zhang[1], Jing Dong[1], Mingyi Dong[1], Qun Ouyang[1]

1 Institute of High Energy Physics, CAS
2 Central China Normal University

R&D of silicon pixel sensor for Vertex (in China)

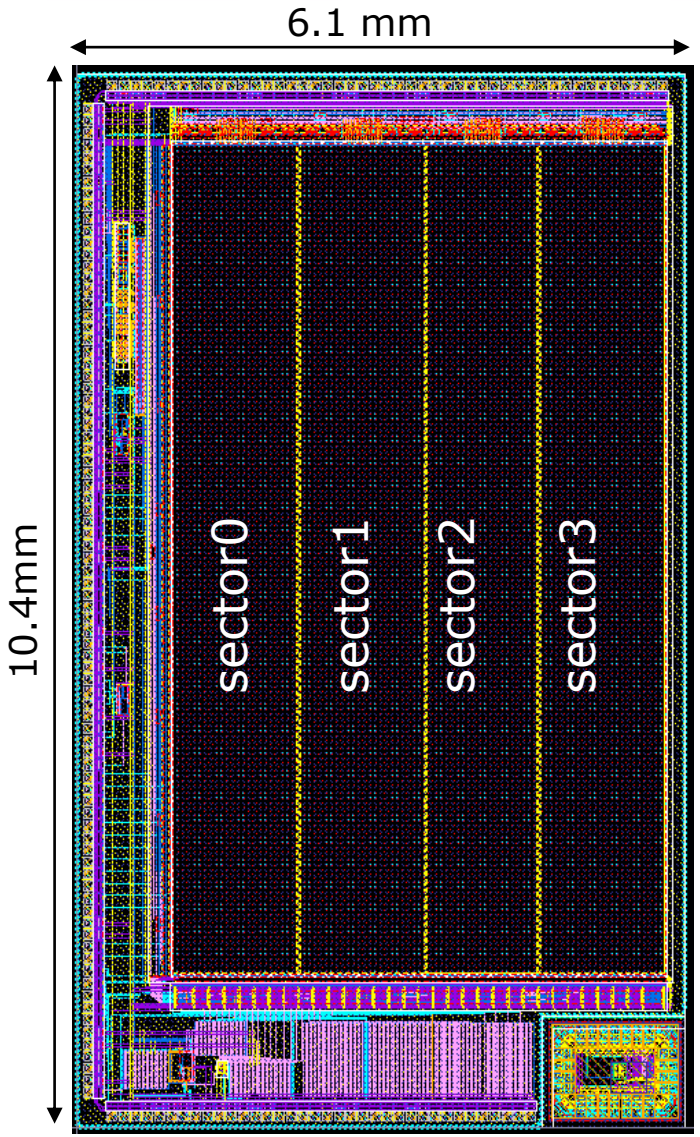
- Targeted on high resolution, low power and fast readout.
  - JadePix and TaichuPix on 180 nm CIS process
  - CPV on 200 nm SOI process



JadePix-3, a major effort on CMOS pixel sensor

- Technological preparation
  - JadePix-1 on the TowerJazz CIS process
  - JadePix-2 and MIC4 on the design schemes
- Collaborative design of a large team
  - Over 10 participants from IHEP, CCNU, SDU, Dalian Minzu U.
- Test work lasted for 1.5 years to fully characterize the chips
  - Highly required expertise on both sensor and electronics
- Highlighted as the achievements of MOST1 project

The pixel matrix of JadePix-3

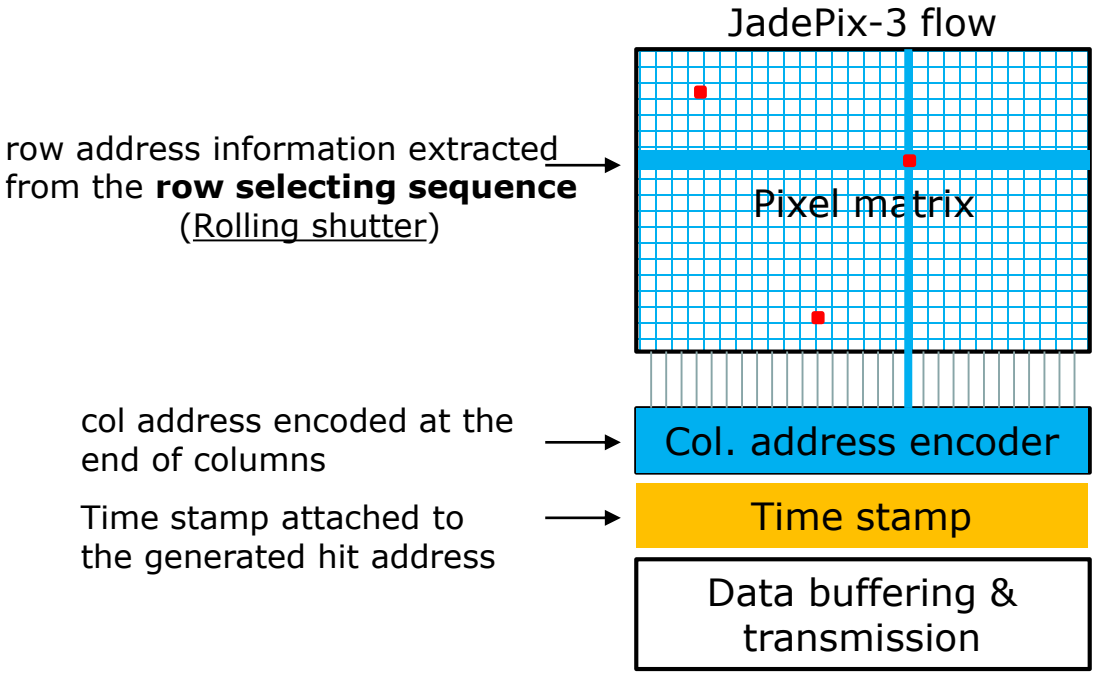


- **Full-sized** in the rφ direction of detector layout
  - Matrix coverage: 16 μm × 512 rows = 8.2 mm
- 4 parallel sectors, **scalable** in the z direction
  - 48 × 4 = 192 columns
- **Rolling shutter** to avoid heavy logic and routing in pixel matrix
  - Minimum pixel size: **16 μm × 23.11 μm**
  - Matrix readout time: **98.3 μs/frame**

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

Hit processing flow in JadePix-3

- Row address extracted from the **row selecting sequence** (Rolling shutter)
- Column address of HIT encoded at the bottom of matrix
  - Only HIT address recorded (zero suppression)
- Time stamp attached to the HIT address
  - In the form of frame number



<Example of data frame>

Head: Buffer status

Data: HIT address 1
Data: HIT address 2
Data: HIT address 3

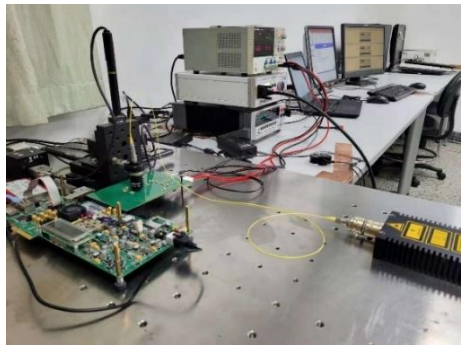
Tail: Frame number

Test system for single chip

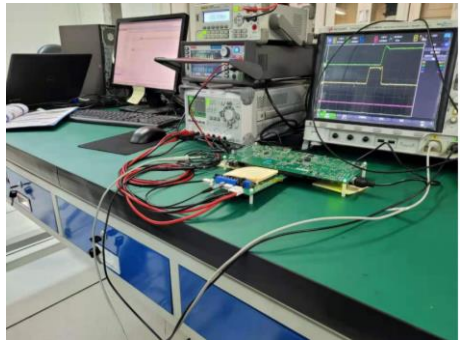
- 4 test setup deployed in IHEP, CCNU, USTC, JLU
  - Used to interact with single JadePix-3 chip
- General-purpose FPGA platform, KC705
  - Well-designed **FPGA firmware**

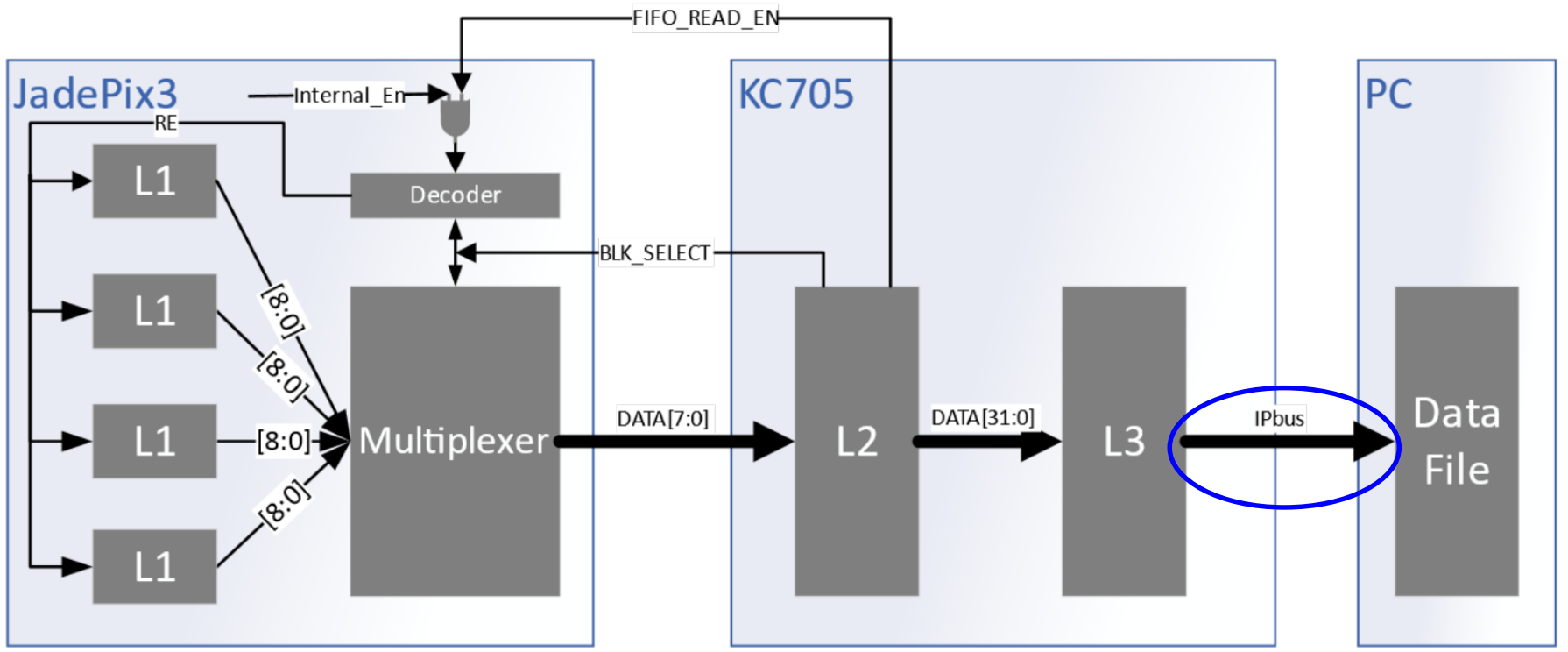
- **IPBUS protocol**
  - Reliable high-performance **control link** for particle physics electronics
  - **JUMBO PACKAGE feature** developed to boost the payload data rate up to 750 Mbps

In IHEP Lab

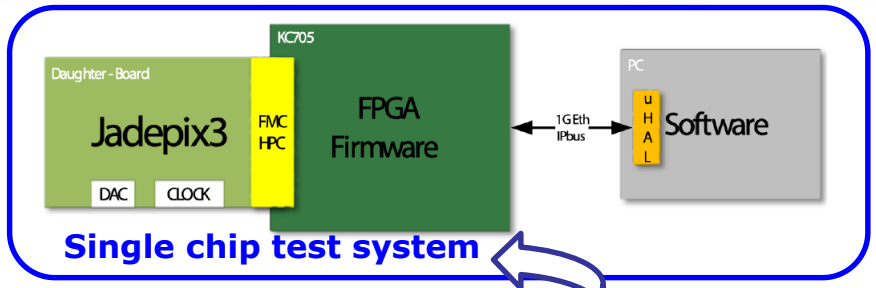


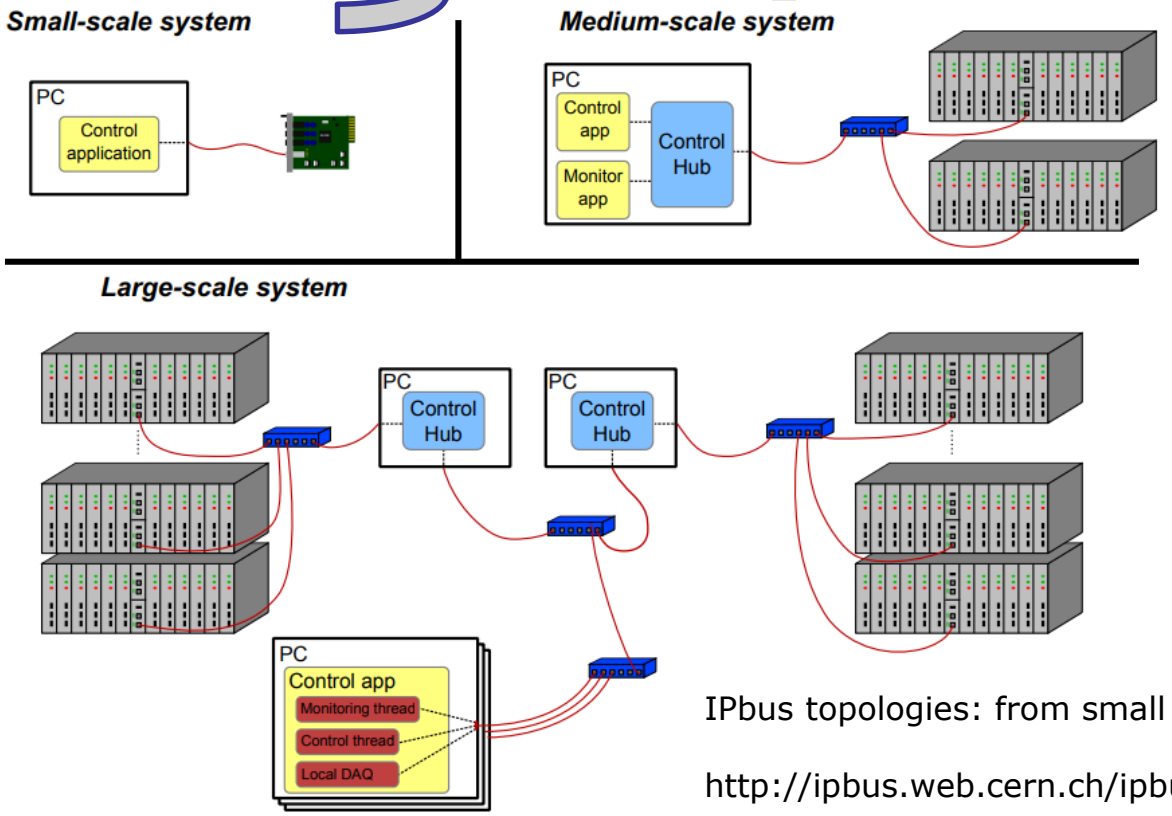
In CCNU Lab





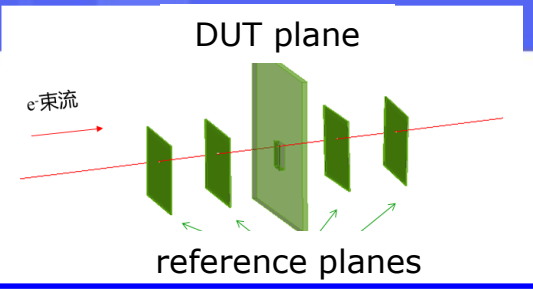
IPBUS: a flexible Ethernet-based control system

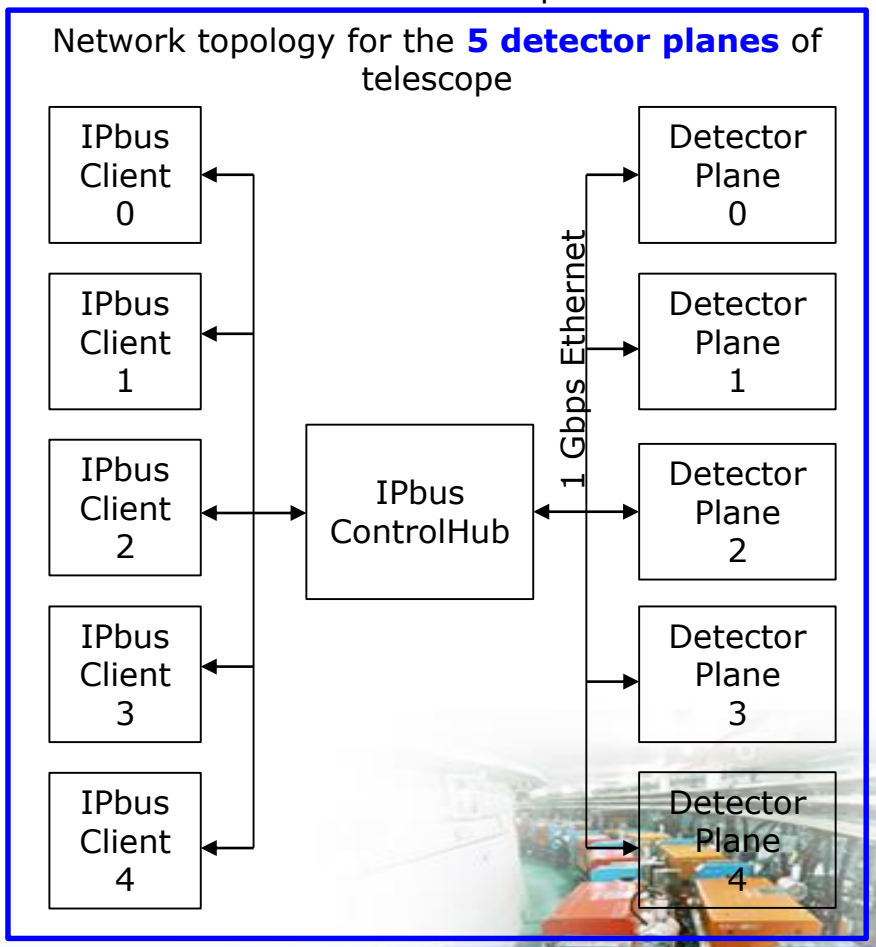




IPbus topologies: from small to large scale

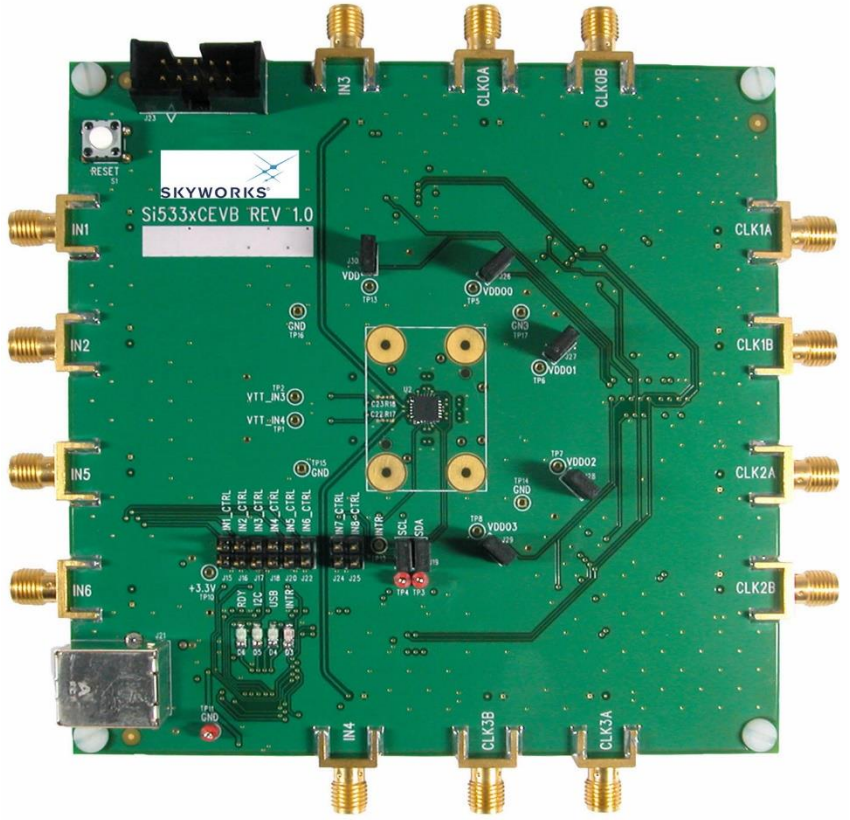
http://ipbus.web.cern.ch/ipbus/introduction/

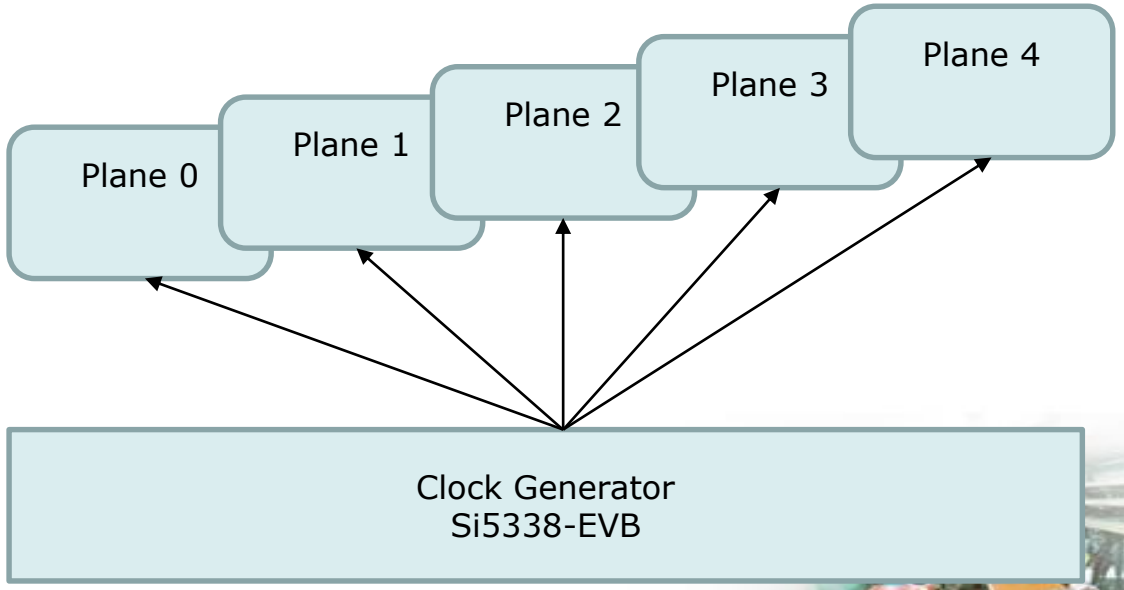




Distribution of System Clock

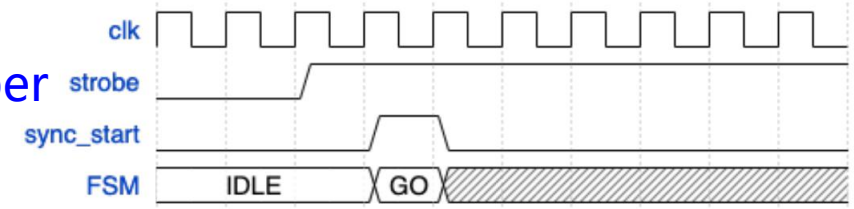
- System clock fanned out from a Si5338 board to all the detector planes
  - Each plane operated in the common clock domain
  - 200 MHz, differential pairs
  - Commercially available

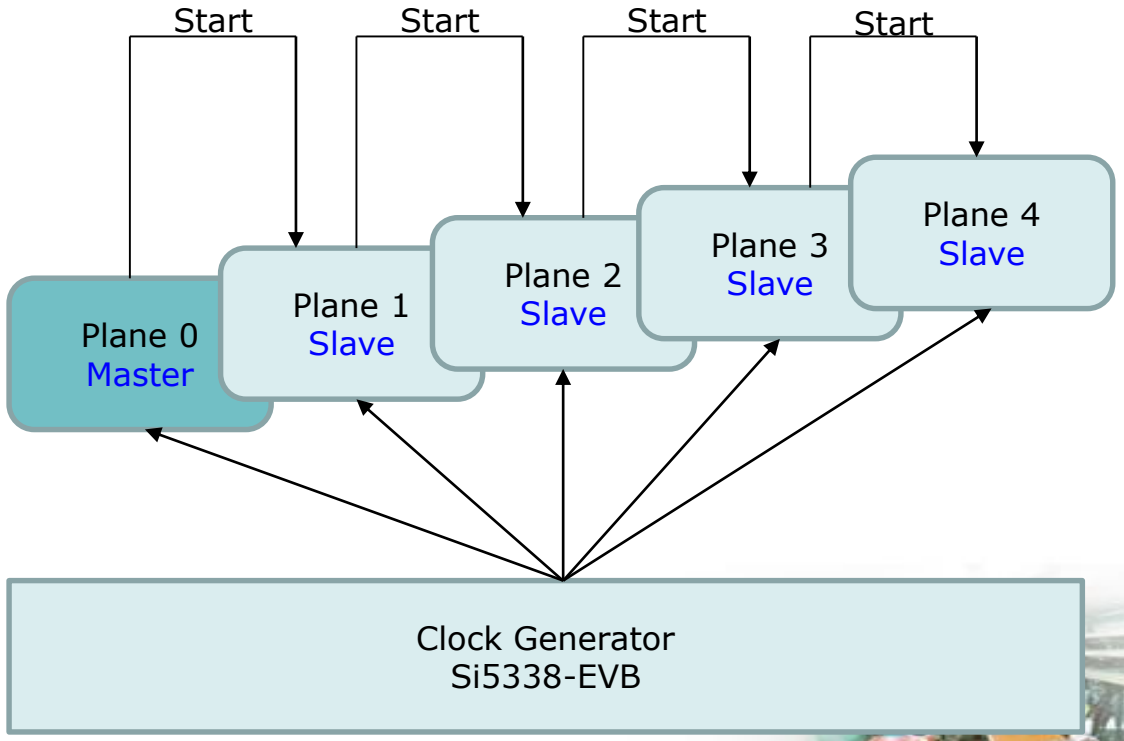




Synchronization of Start Up

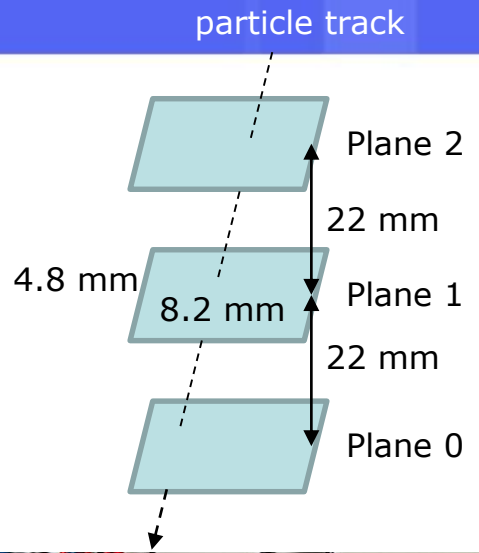
- Rolling shutter scan to start simultaneously
  - Coincidence of HITs recorded with same frame number
  - External trigger is not necessary
- Plane 0 configured as Master
  - To issue a hard-wired start signal
  - Start from plane 0 to plane 4 via a daisy chain

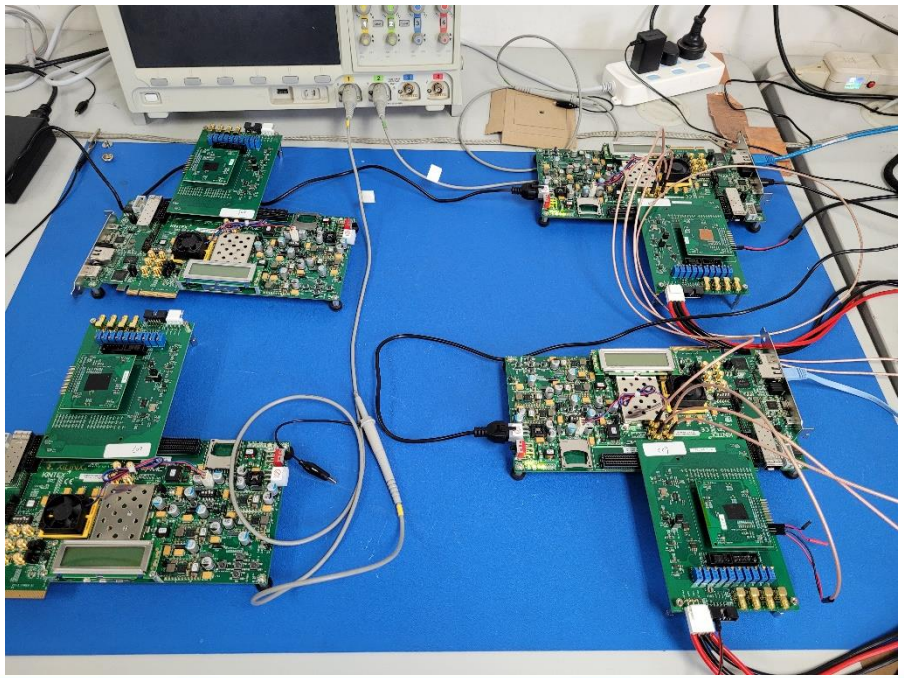


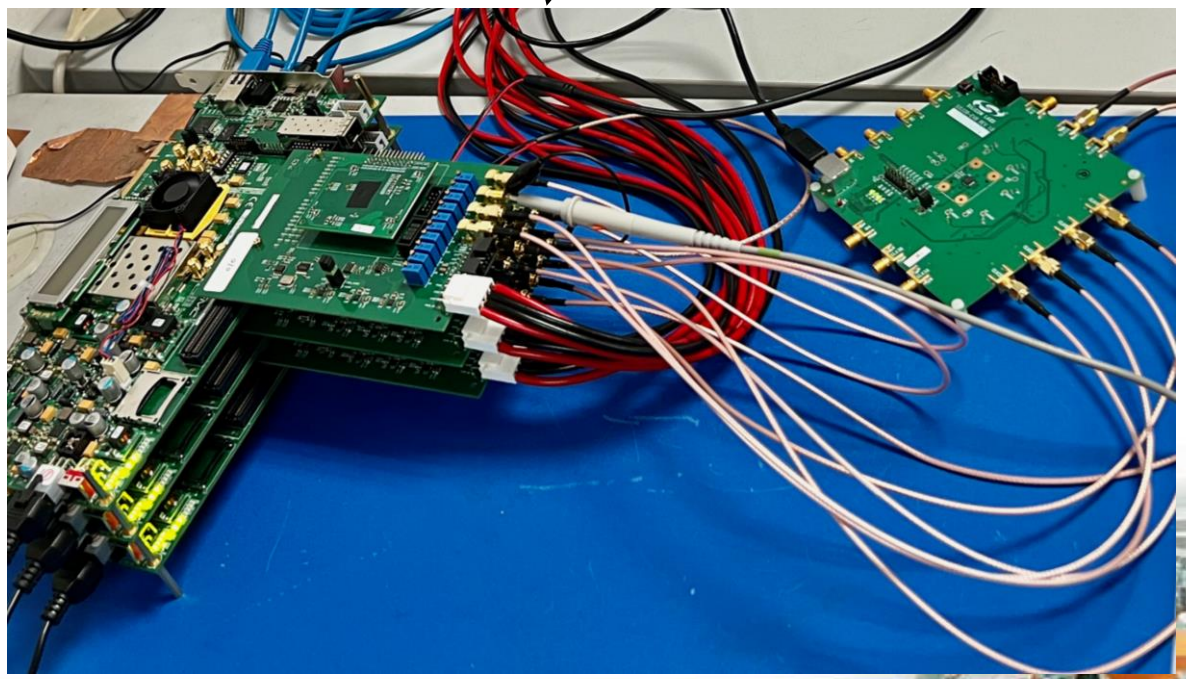


Hardware

- 5 detector planes prepared.
- 3 detector planes assembled for debugging
  - Sensitive area 8.2 mm * 4.8 mm
  - Detector plane distance 22 mm

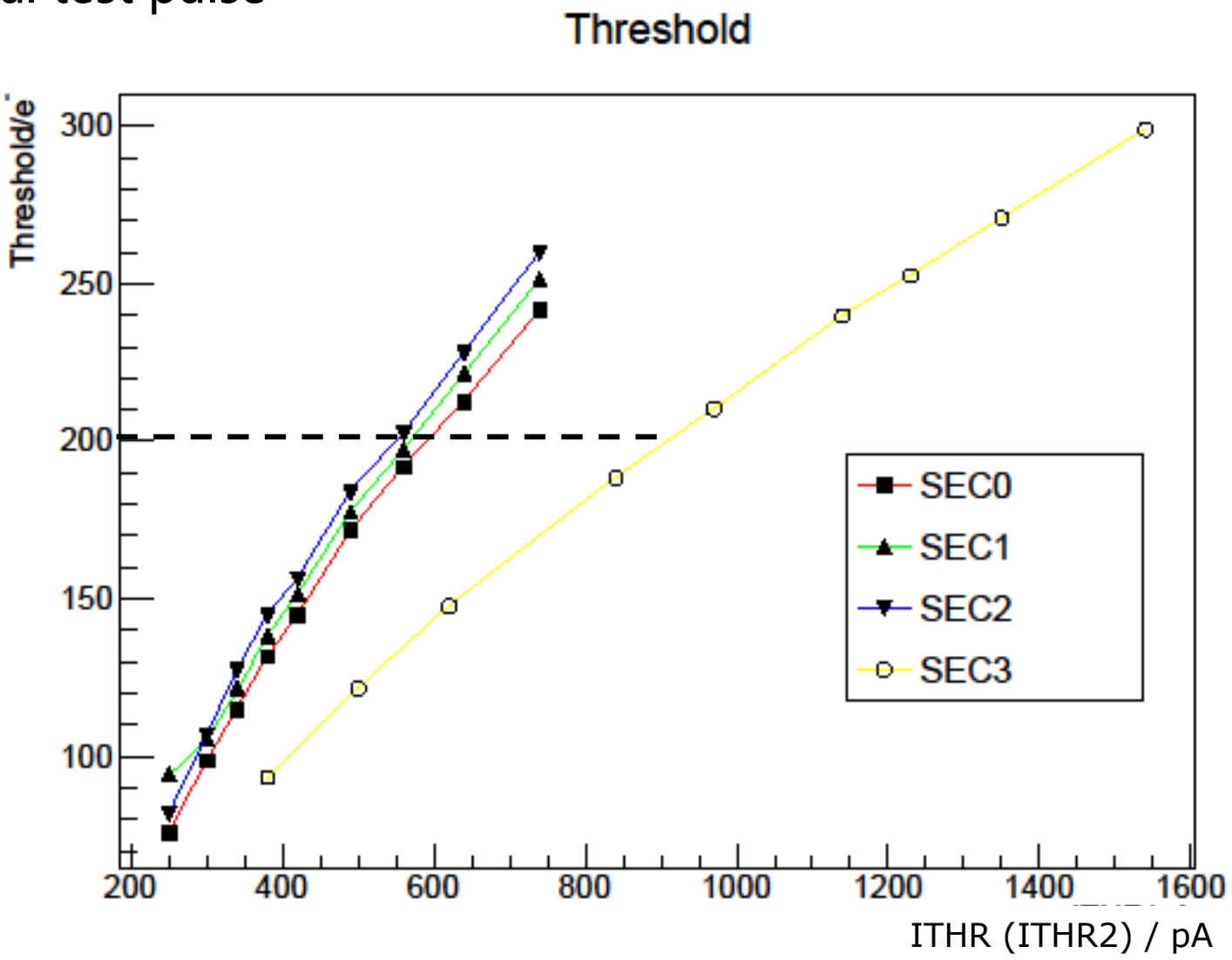






Threshold

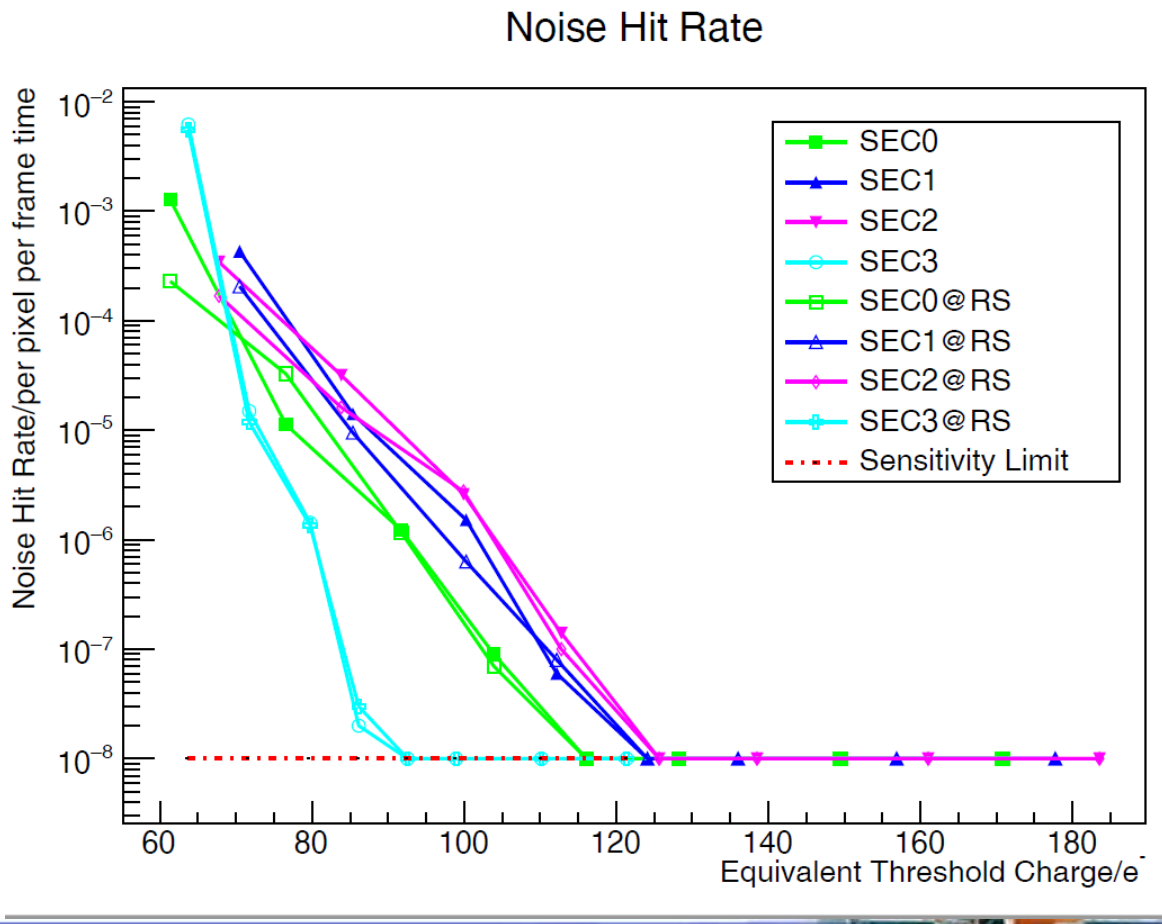
- Threshold calibrated with electrical test pulse
  - 200 e^- applied to the full matrix



Noise hit rate

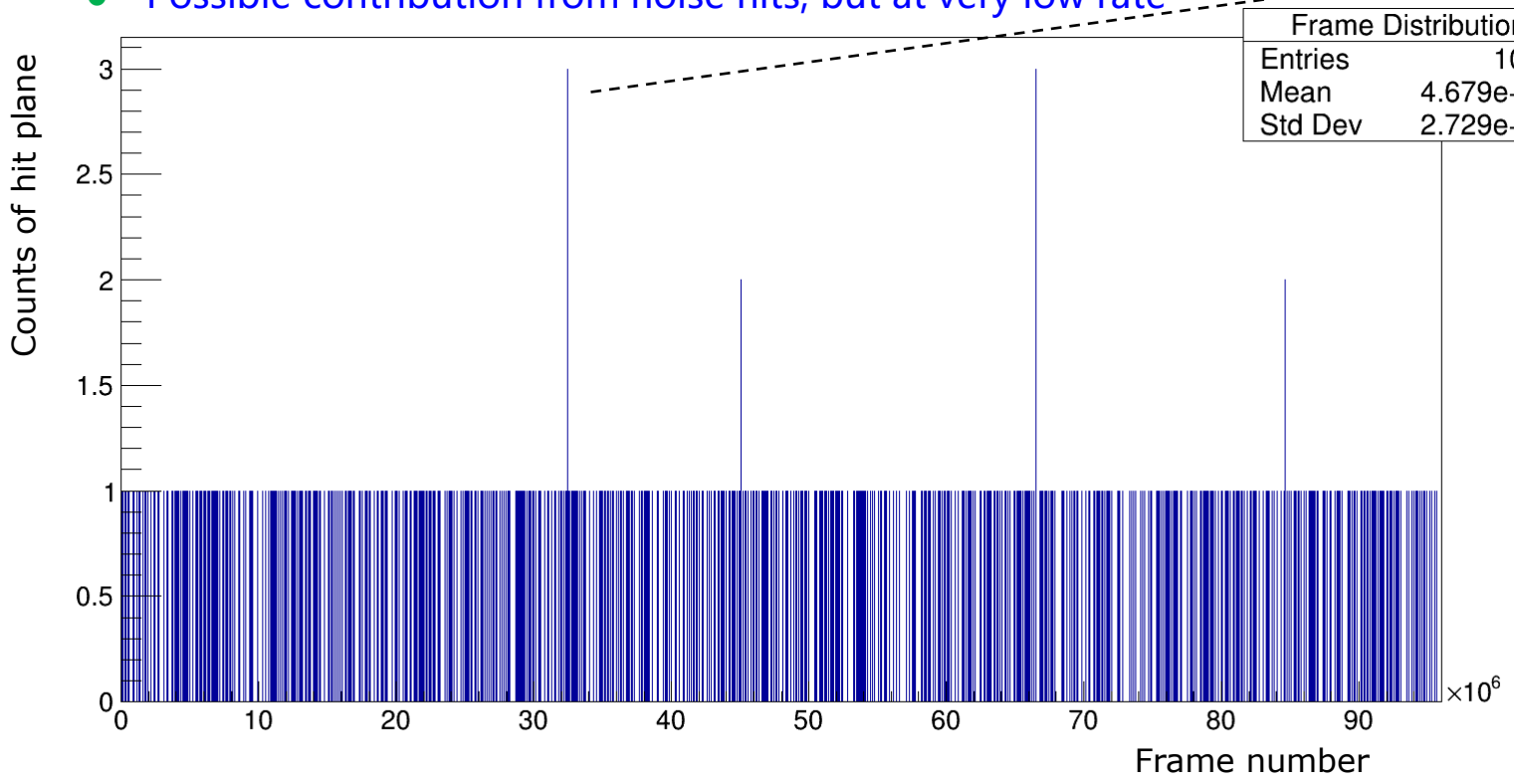
- Noise hit rate below 10^{-8} /frame/pixel
  - Low noise rate & Zero suppression resulted in ~100 Bytes / min @ threshold = 200 e^-

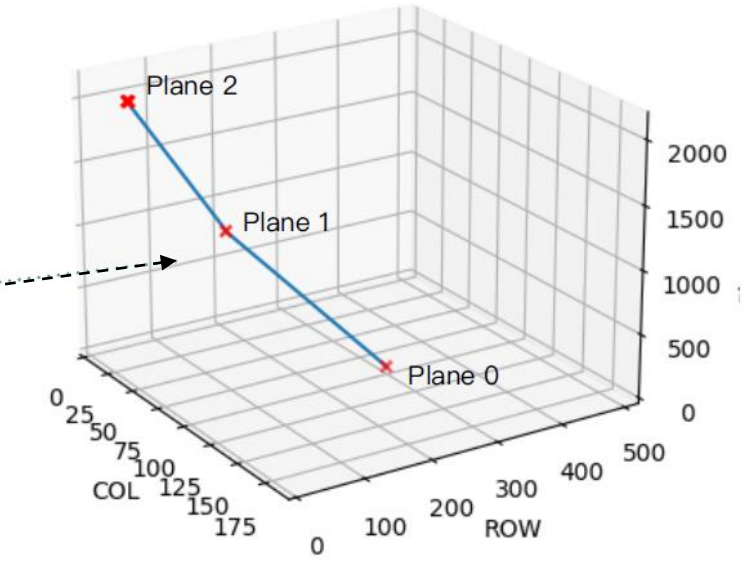
→ long time operation to collect cosmic ray events

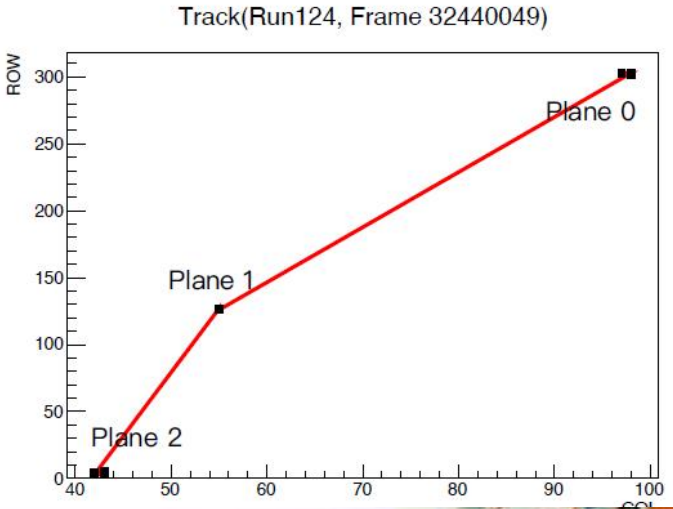


Initial test with cosmic ray

- 96 M frames scan in 160 minutes for a typical run
  - 1035 frames have hits on single plane
  - 2 frames have hits on 2 planes
  - 2 frames have hits on 3 planes
- Event rate 5.7/cm^2/min (assume one frame hits belong to one event)
  - Possible contribution from noise hits, but at very low rate

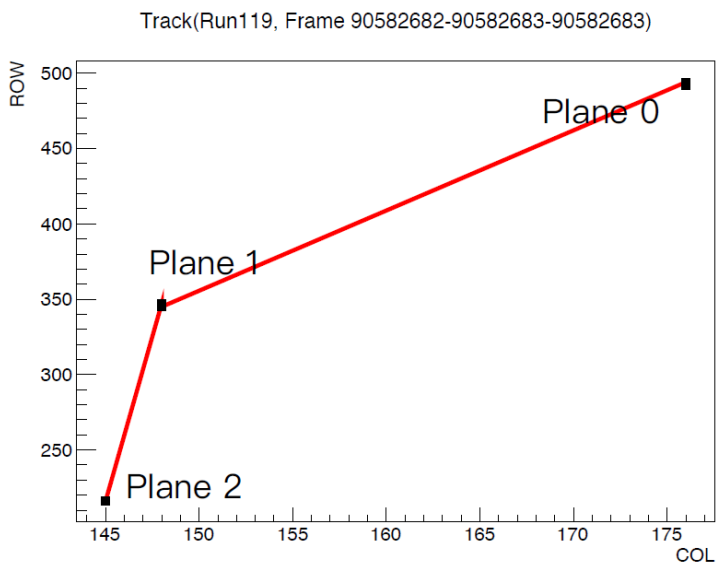


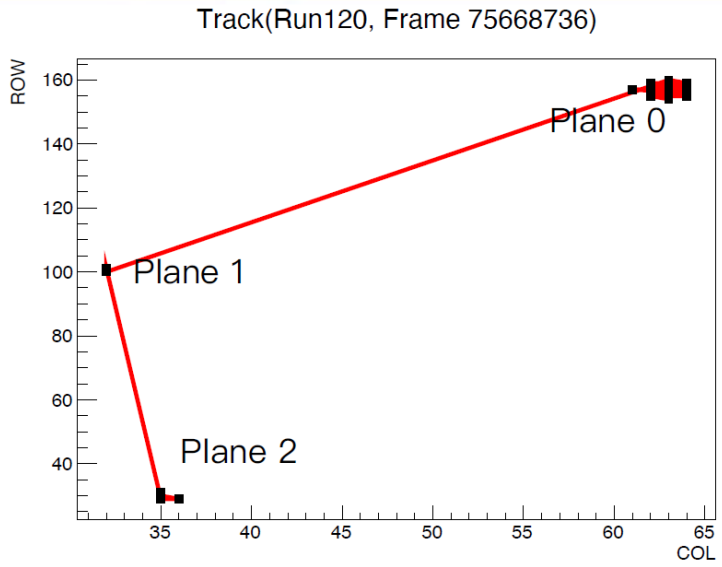


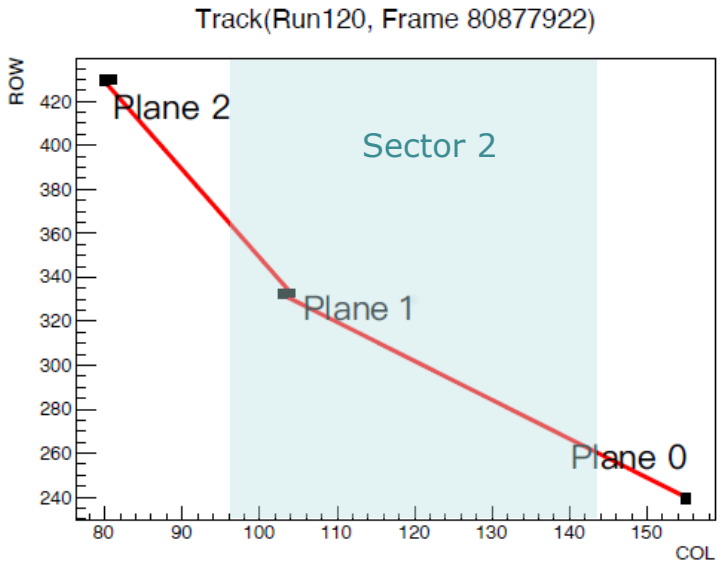


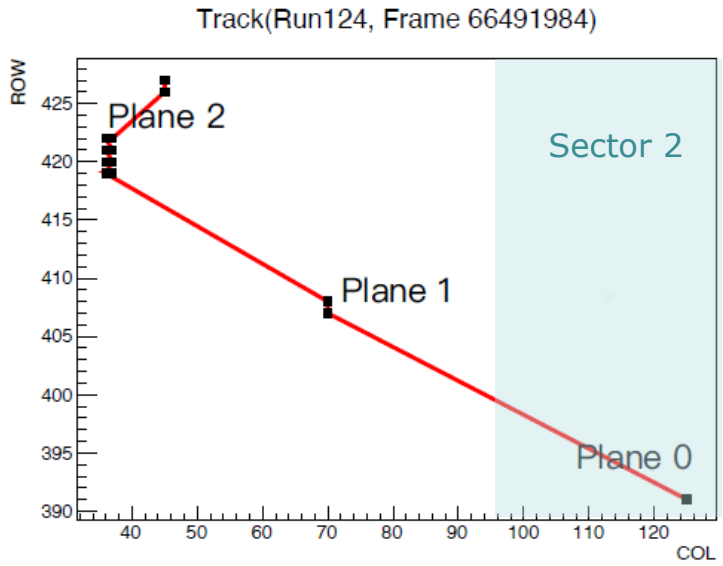
More 3-plane events displayed

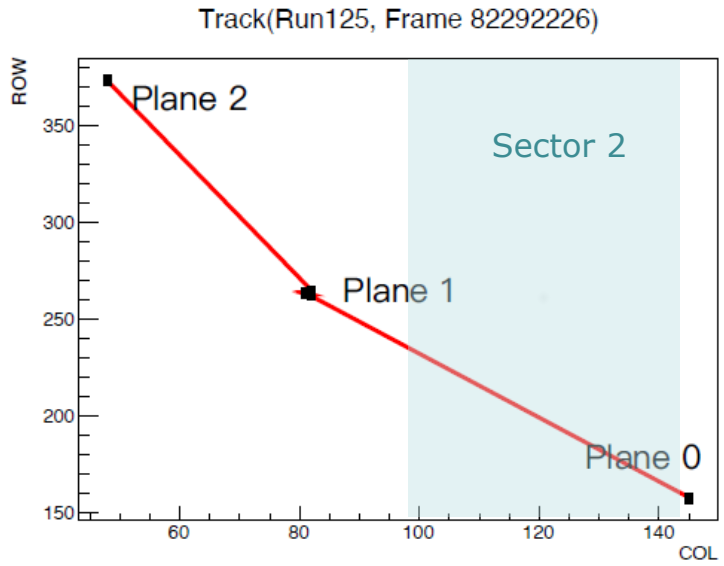
- Sources of position offset
  - Gluing of chips manually
  - Different pitch on sector 2







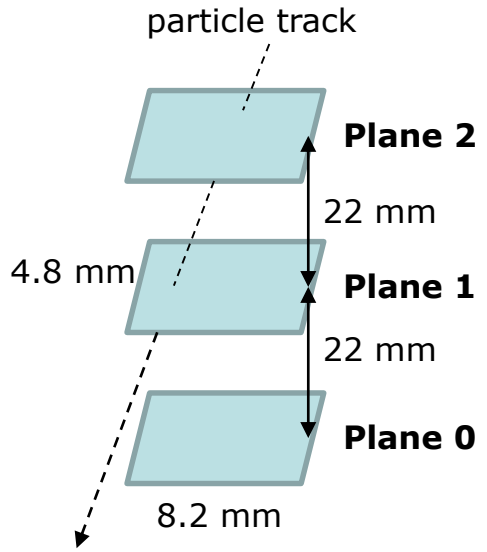




2-plane events checked

- Number of events sorted according to the combination of planes
  - No event falling in the category “plane 0&2”, consistent with the geometry constraints

	plane 0&1	plane 1&2	plane 0&2
Run 119	2	3	0
Run 120	3	1	0
Run 121	4	2	0
Run 122	5	2	0
Run 123	3	1	0
Run 124	0	2	0
Run 125	1	0	0
Sum	18	11	0



To do list

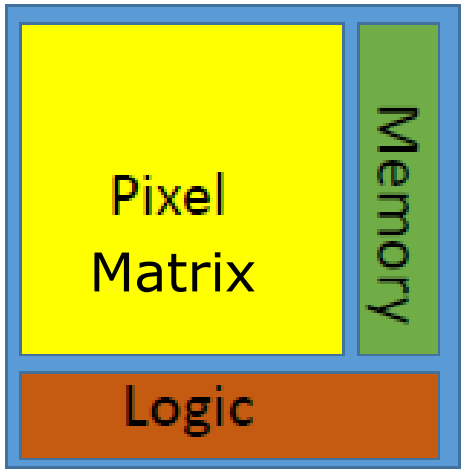
- To complete the integration of 5 detector planes
- EUTelescope software for track reconstruction and analysis
  - Need more experts in this area
- Time slot for test beam to be booked or shared
  - Not available yet

Motivation of 3D-SOI development

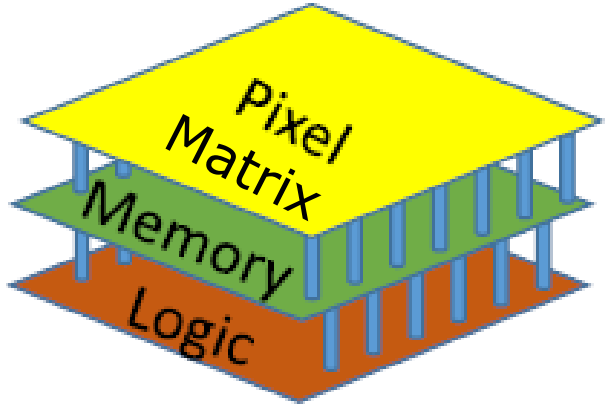
Vertex Detector — **Review report on the Vertex part of CDR in 2018**

Findings: there is active R&D and groups are making good progress, building on large effort by the international community. Compared to other efforts toward precise and transparent vertex detectors, CEPC (with its 100% duty cycle) should place stronger emphasis on power management. Advanced processes like 65 nm CMOS or 3D-integrated devices should be pursued actively and can have a big impact on the vertex detector performance.

- Pixel to pixel connection is needed to shrink the pixel size → spatial resolution — 3D-SOI
- IO to IO connection is used to shrink the peripheral area → 4-side abuttable



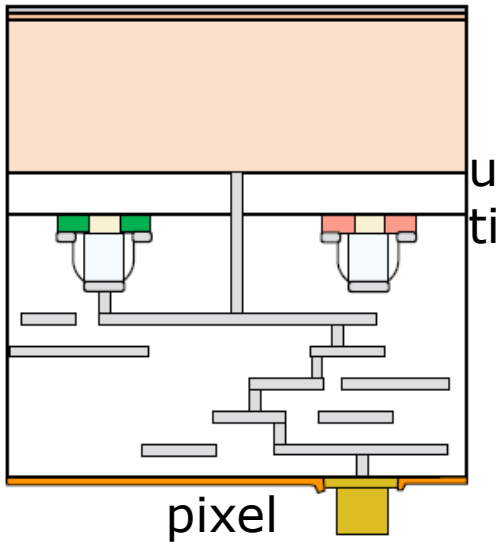
IO to IO connection

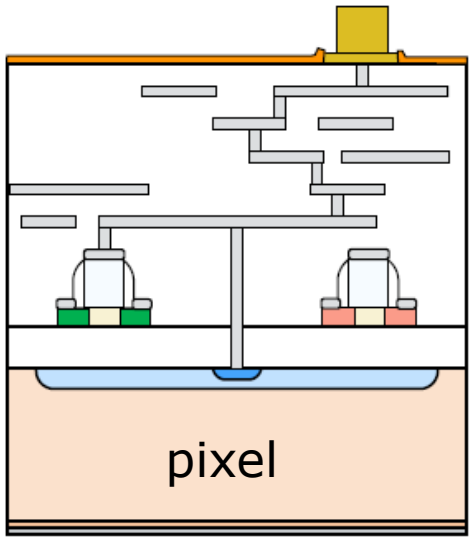


Applications of 3D in industry

3D connection	pixel to pixel	IO to IO
Industrial application	Imaging CMOS	ASIC circuit
Connection	u-Bump	TSV
Stacking	flip chip	top side up
# of layers	2 layers	≥ 2 layers

Design resource of 3D-SOI



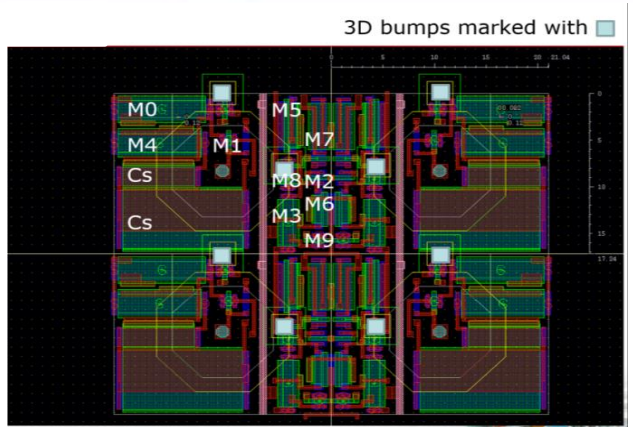


- 0.2um 3D-SOI process: ~100 transistors and 5 metal layers **in each tier**
  - lower tier: sensing diode and analog front-end
  - upper tier: digital logic and readout
  - Pixel size can be cut half without compromise of functionality
- Comparison to the CMOS process
  - 0.35um process: ~10 transistors and 6 metal layers, pixel size ~ 20*20 um^2
  - 0.18um process: ~100 transistors and 6 metal layers, pixel size ~ 26*28 um^2

*Credit of the conceptual drawing: Miho Yamada

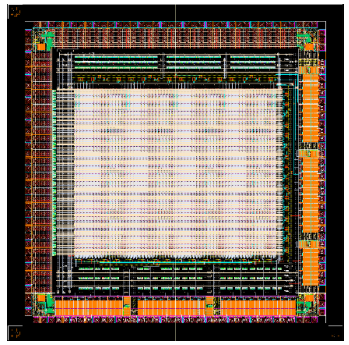
CPV-4 3D design

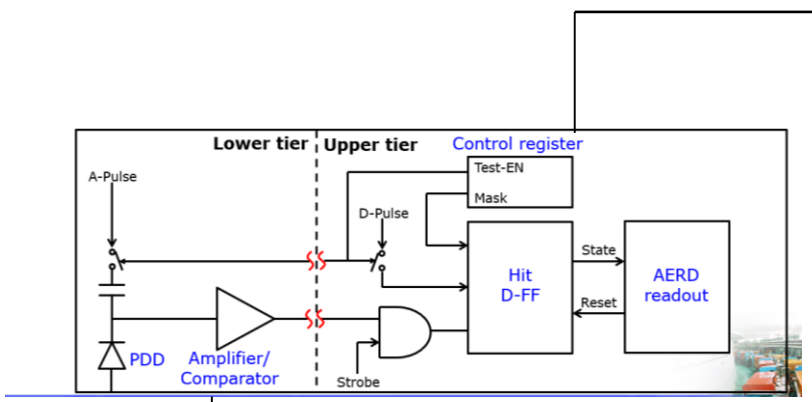
- Stacking of Sensor + Analog + digital to pursue
  - Pixel size 17um * 21um
  - Data-driven readout ~ 1us of time stamp
  - Power consumption ~ 50mW/cm^2

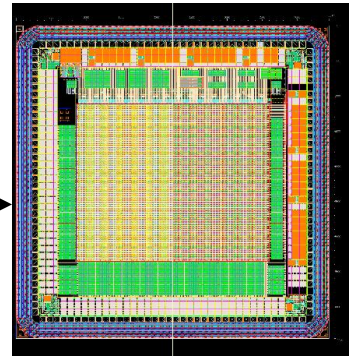


4 pixels arranged in 2 columns

CPV4_Upper

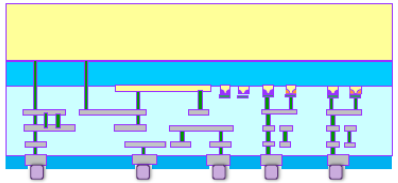


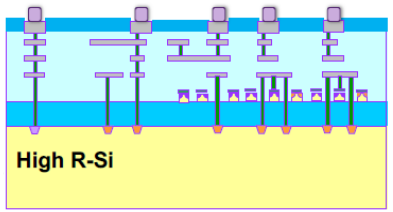




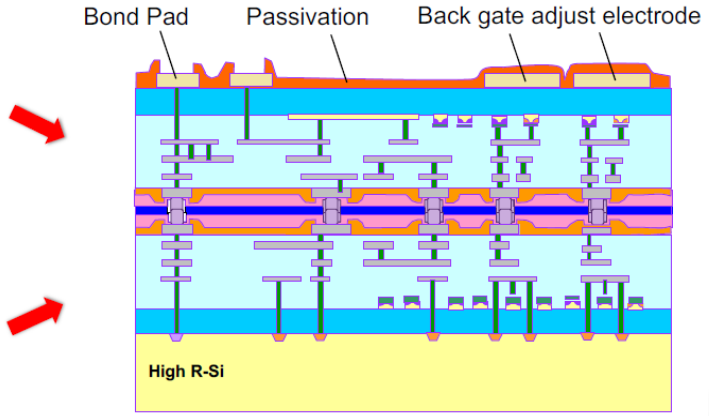
CPV4_Lower

Upper Chip



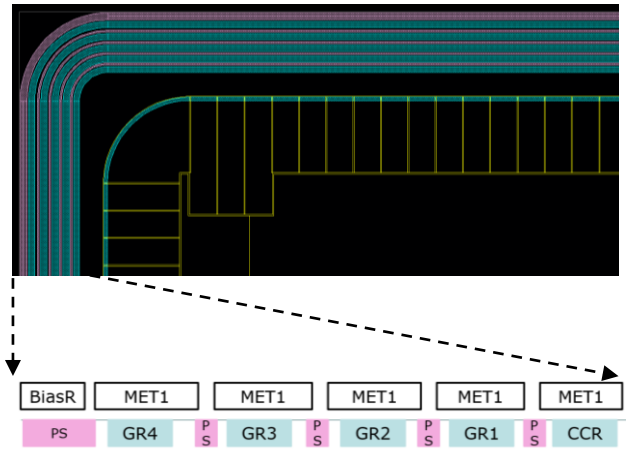


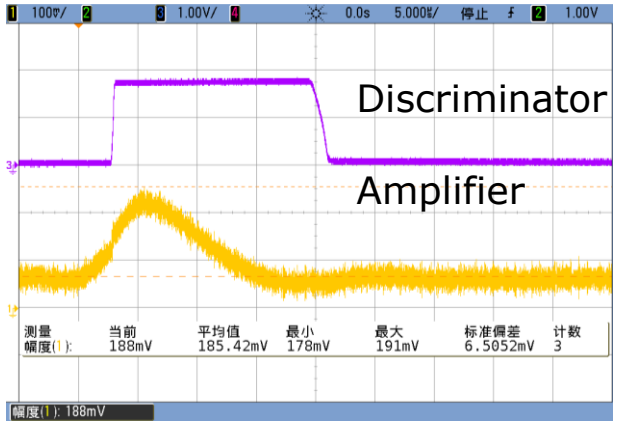
Lower Chip



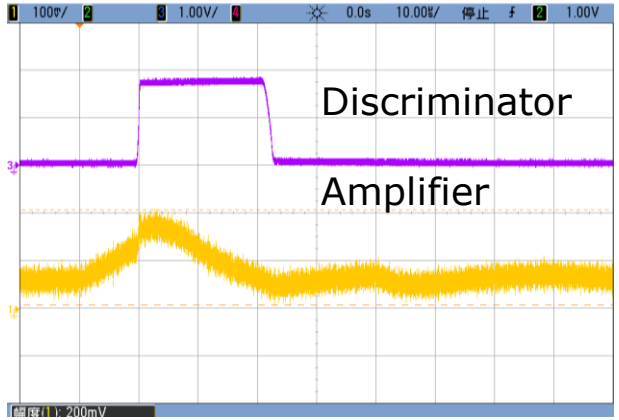
Before 3D integration

- Test on lower and upper tier independently
  - ✓ Low leakage current on **sensor** (Diode + Guard Ring)
  - ✓ Signal waveform observed on **analog** front-end
  - ✓ Response from the **digital** logic and readout
- Test system developed and debugged interactively with the upper tier chip

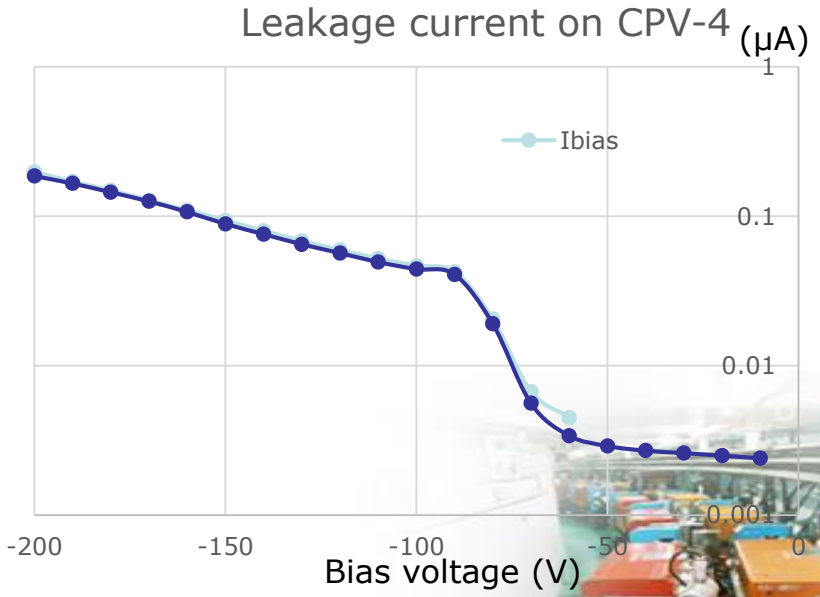




Analog frontend w/o PDD
Test charge injected ~ 100 e-

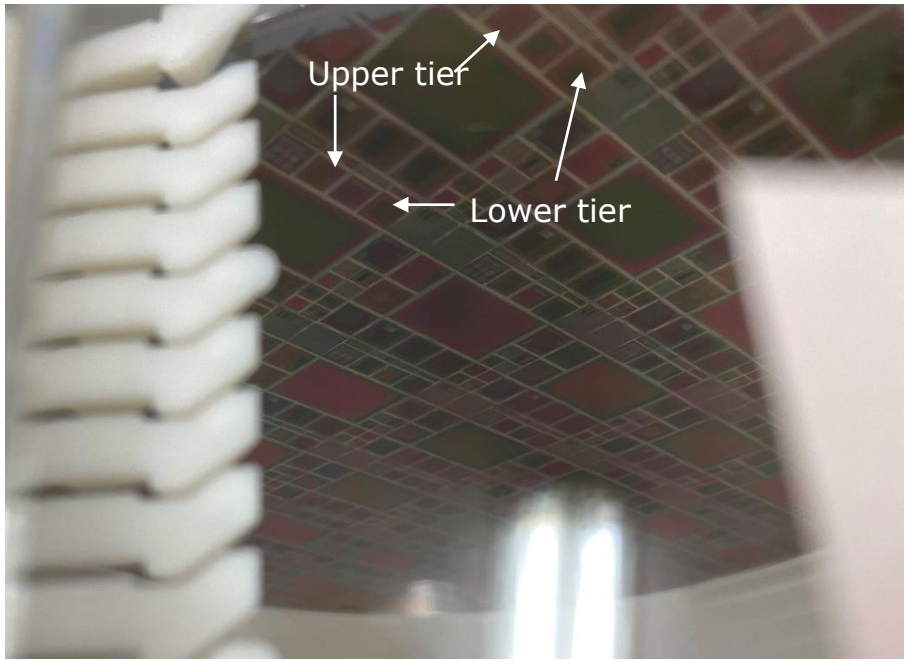


Analog frontend with PDD
Test charge injected ~ 750 e-

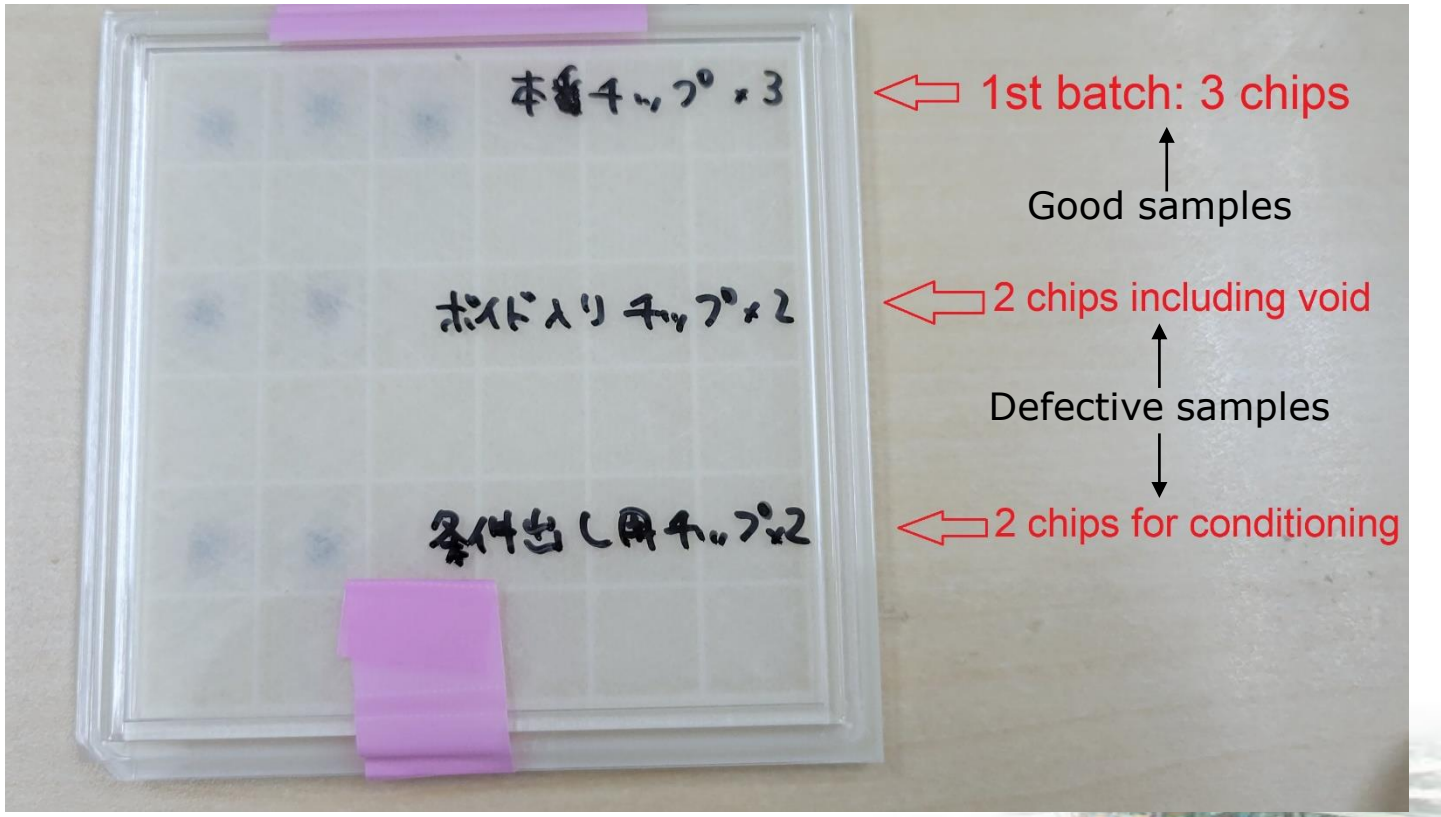


Delivery of 3D chips

- First batch arrived in Aug.
  - Second batch of 17 chips in a couple months



Upper and low tier chips on the wafer

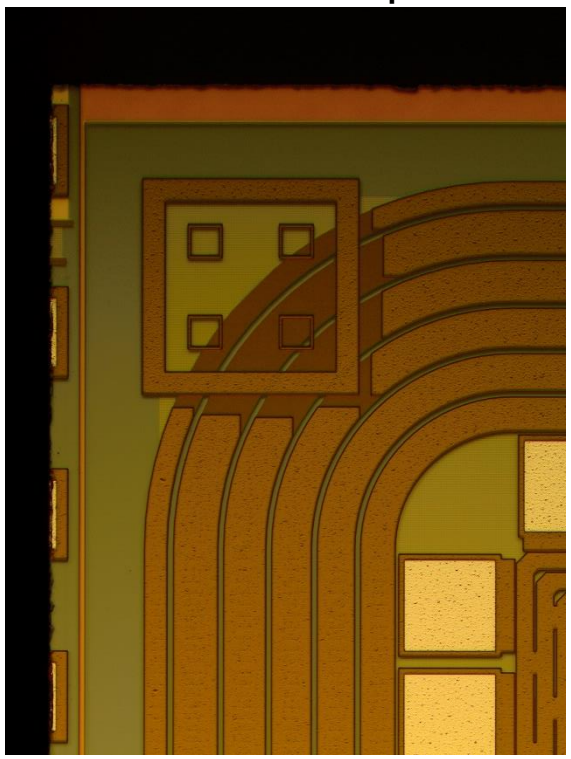


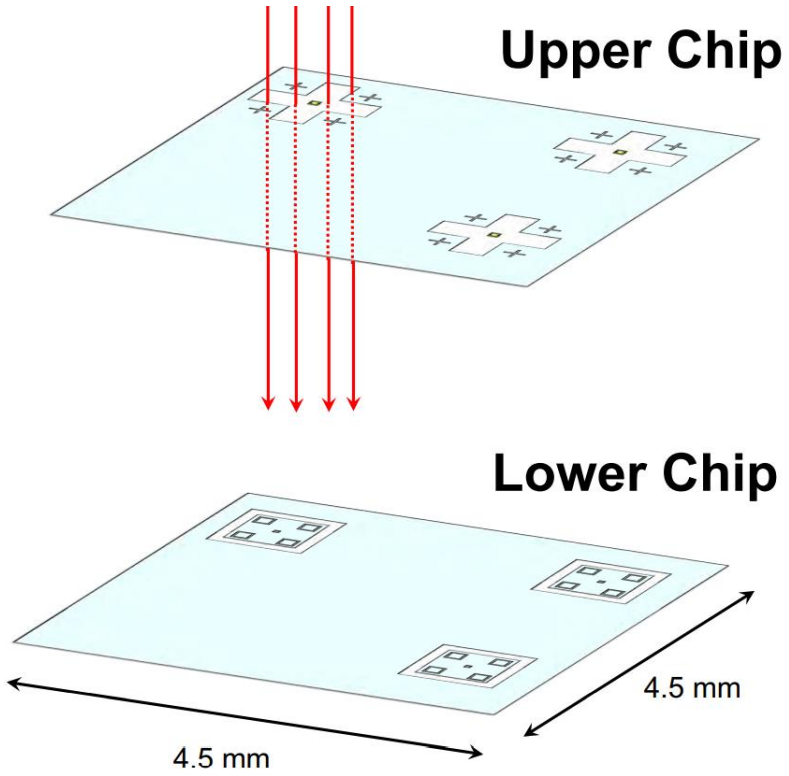
Chips delivered after 3D integration

Visual inspection on 3D chips

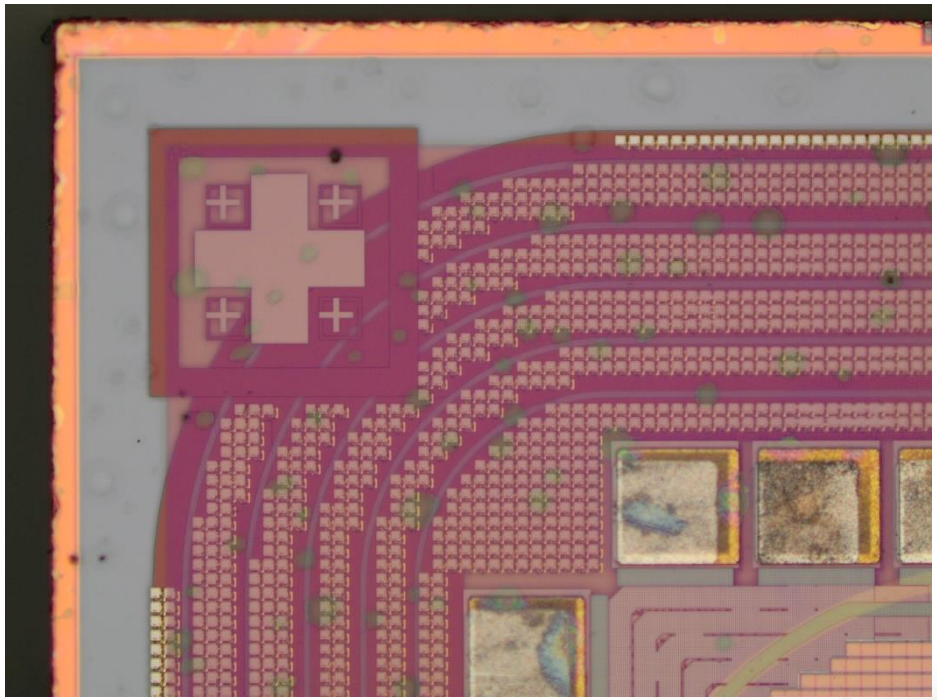
- Alignment of marks

Lower chip



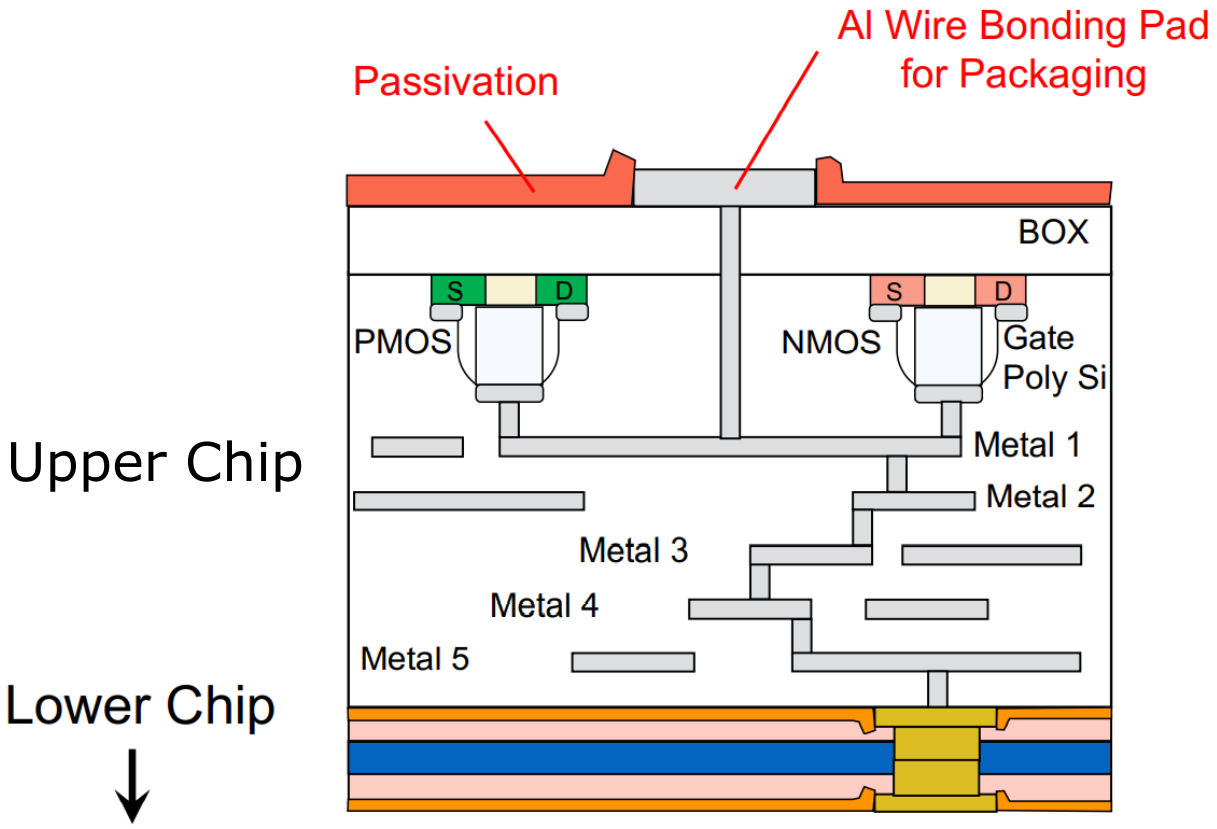


3D chip

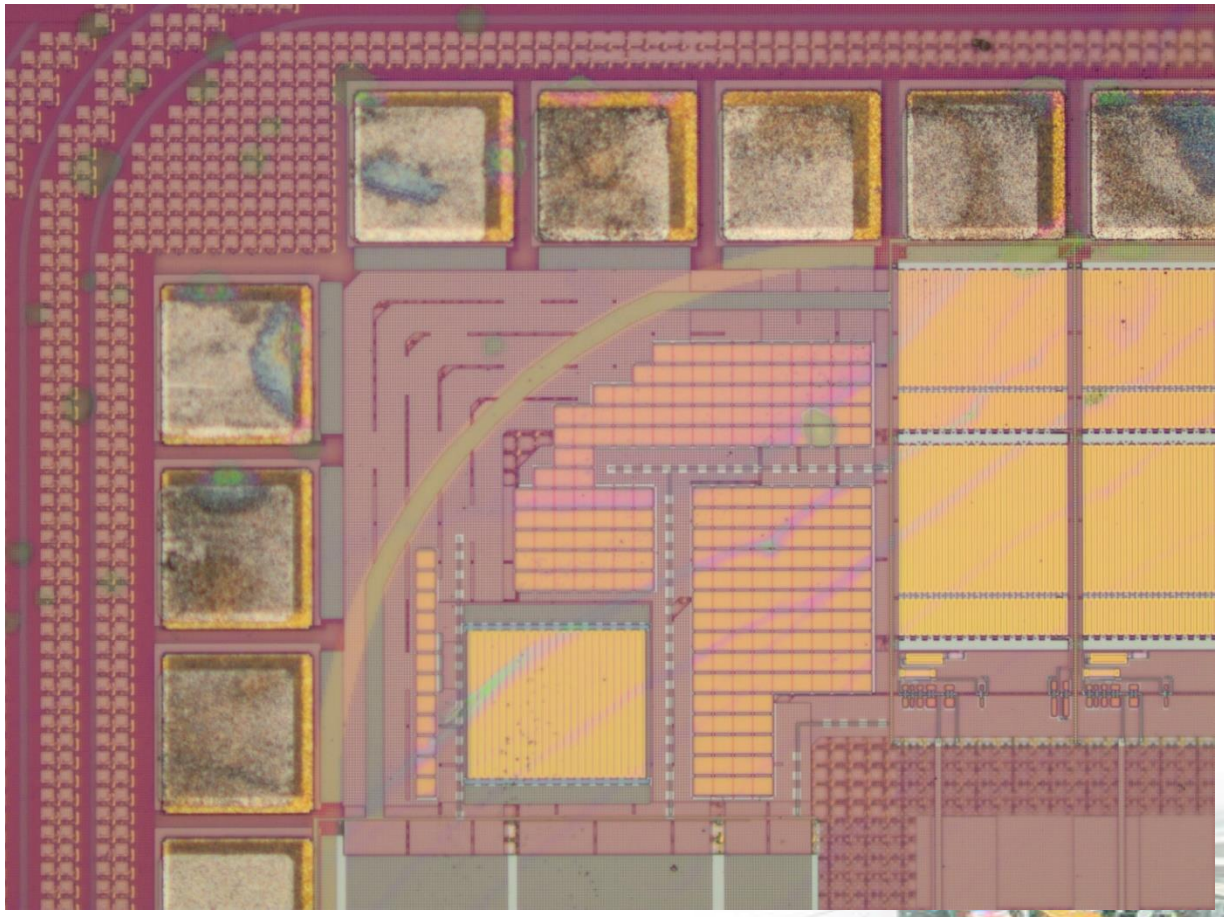


Visual inspection on 3D chips

- Bonding pad rebuilt on top

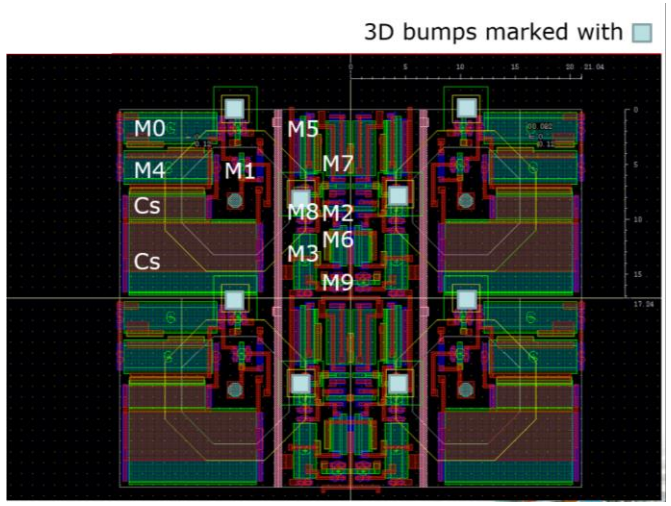


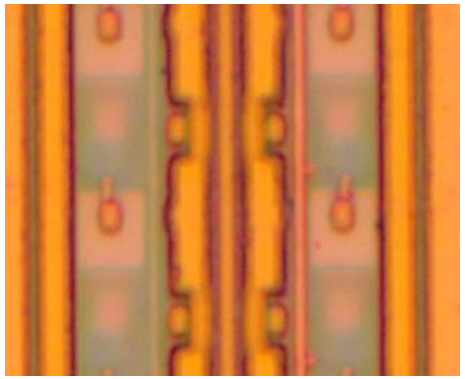
3D chip



Visual inspection on 3D chips

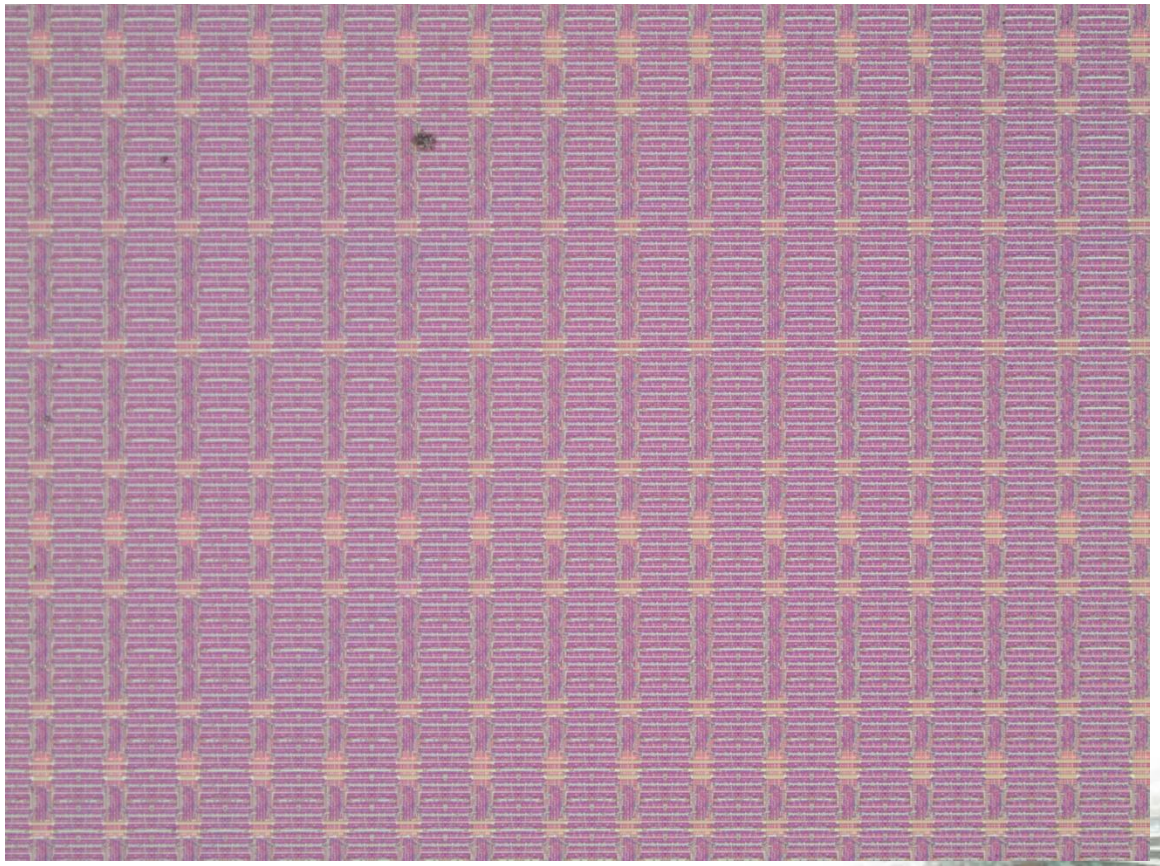
- Pixel matrix





Lower chip
(2*2 pixels)

3D chip (Pattern of upper chip)



Test plan

- Glue and wire bonding on the 3D chips
  - Trial and test with defective samples firstly
- Repeat and compare the tests on lower and upper tier respectively
  - To check possible change on the 3D chips
- Debug and operate the 3D chips as a whole
  - Yield of pixel to pixel connection
  - Electrical calibration
  - Radiative source test
  - Laser test
  - Particle beam test if available

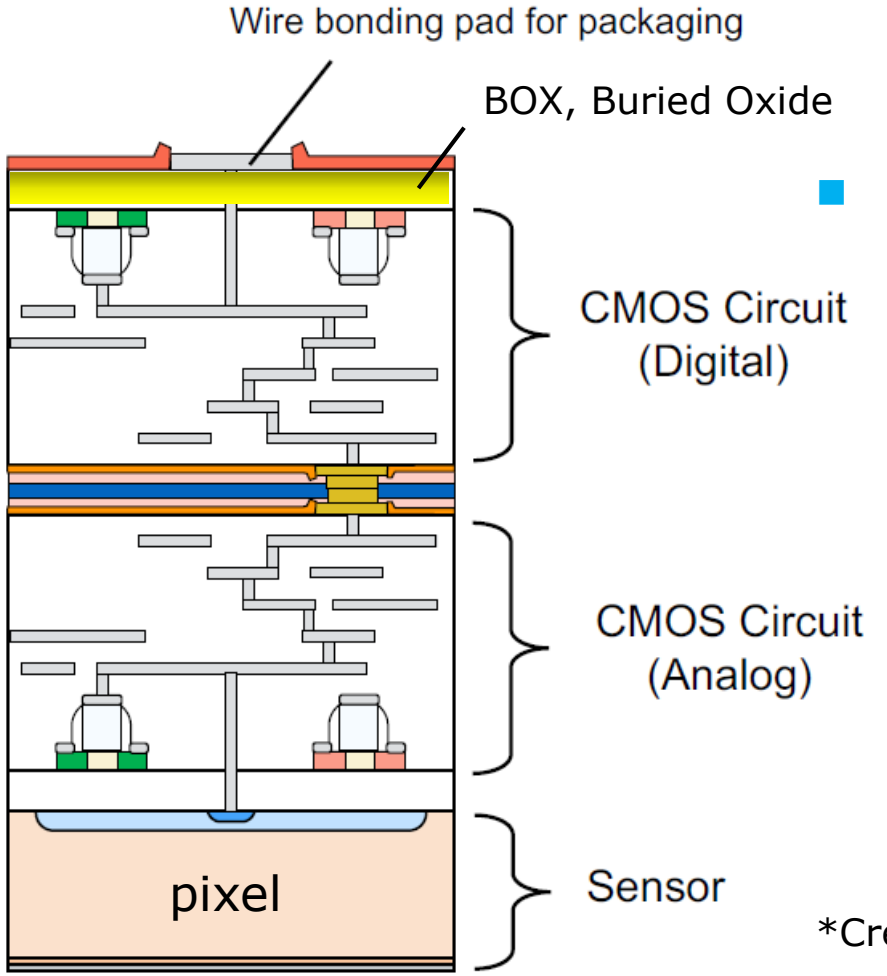
Summary

- JadePix-3 telescope prototype of 3 planes tested with cosmic ray
  - Very low event rate due to the small active area and narrow acceptance angle
  - 3-plane and 2-plane events seemed reasonable
  - Ready to proceed for a 5-plane configuration
- 3D chips for the CPV-4 design were ready for test
  - The essential elements were checked visually
  - Conclusion of test are expected before the end of this year

Thanks for your time

- Backup slides

Features of 3D-SOI: low material



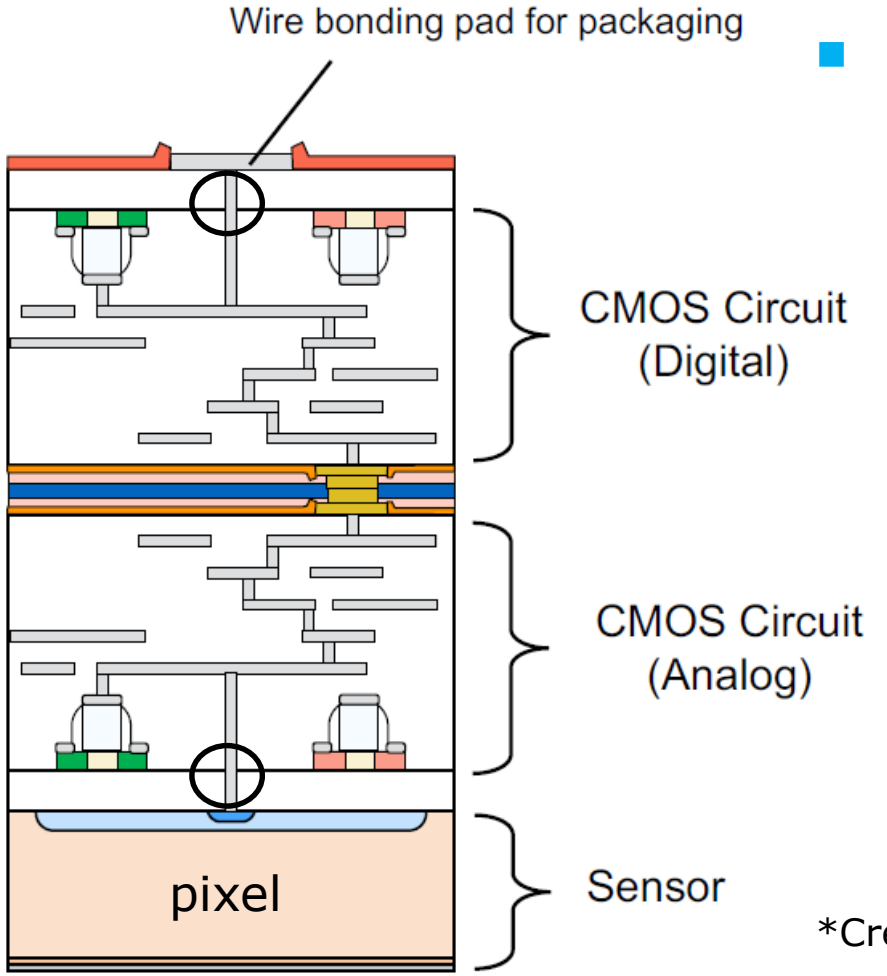
- The bulk of upper tier is **removed by wet-etching**
  - 260 um → 10 um thick
  - Wet-etching stopped by the BOX oxide layer automatically → makes SOI quite **compatible with 3D integration**
- Thinning of the lower tier is also possible
  - 75 um in conventional SOI and 50 um in CMOS (lower tier not necessarily an SOI sensor)

* Currently 3D-SOI demonstrated on a lower tier of 260 um thick

*Credit of the conceptual drawing: Miho Yamada

Features of 3D-SOI: TBV

- Backside connection is Through Box Via (TBV)
  - Already established in the SOI process
- Additional metal layer formed for wire bonding
  - Post-process after 3D integration



*Credit of the conceptual drawing: Miho Yamada