R&D status for CEPC vertex detector prototype

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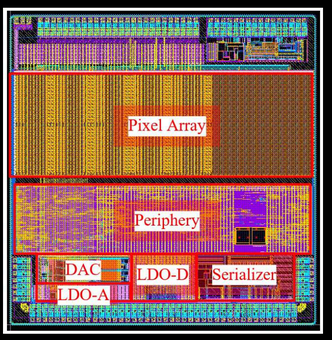
On behalf of CEPC vertex detector MOST2 team

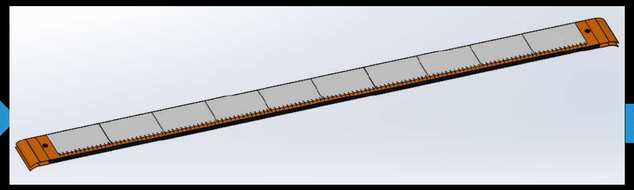

Overview of task2： vertex detector R & D

- Can break down into sub-tasks:
  - CMOS imaging sensor chip R & D
  - Detector layout optimization, Ladder and vertex detector support structure R & D
  - Detector assembly
  - Data acquisition system R & D

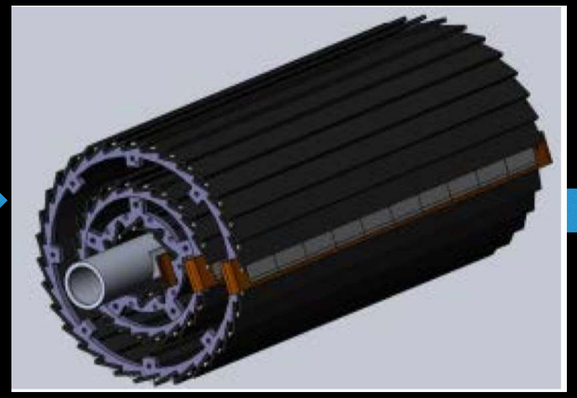
CMOS imaging sensor prototyping



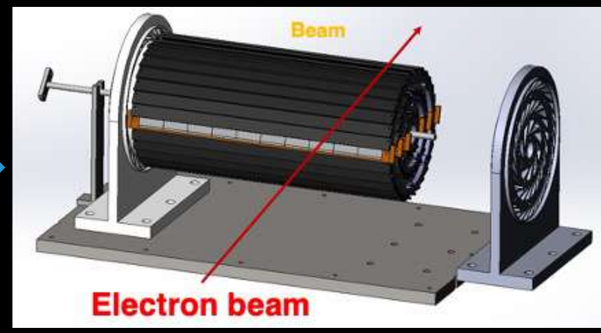
Detector module (ladder) Prototyping



Full vertex detector Prototype

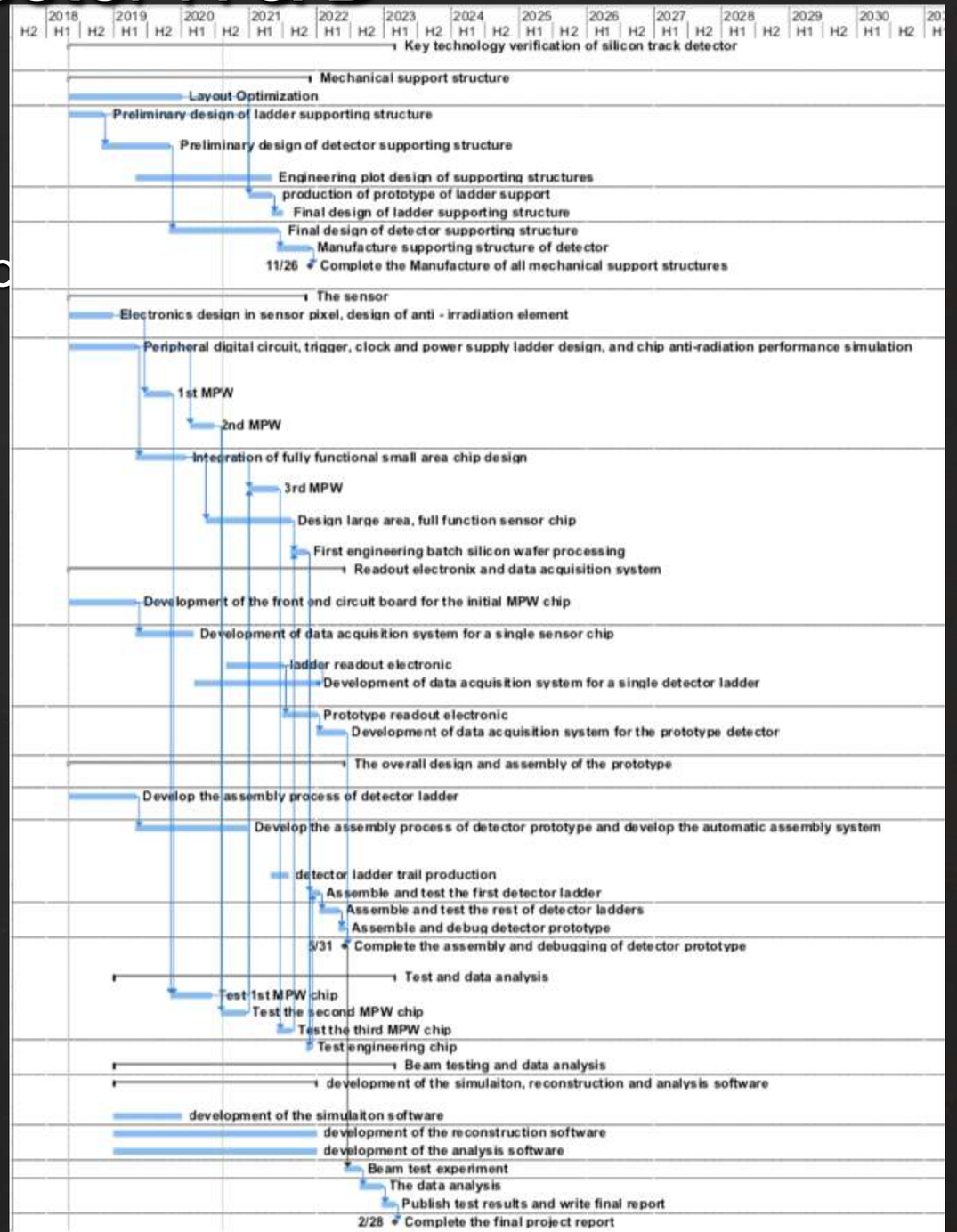


Beam test to verify its spatial resolution



Overall plan of task2： Vertex detector R & D

- 4th Year (2021.7 –2022.6) :
  - Competed R & D full-size TaichuPix sensor
  - Manufactured the support structure for whole detecto
  - Assembling and installing the detector prototype
  - Completed DAQ system for whole detector
- 5th Year(2022.7 –2023.6) :
  - Completed detector assembly and commissioning
  - Test beam and data analysis
  - Finish assembling of prototype



CMOS Sensor chip R & D

- The existing CMOS monolithic pixel sensors can't fully satisfy the requirement
- Major Challenges for the CMOS sensor
  - Small pixel size -> high resolution (3-5 μm)
  - High readout speed (<500ns dead time @40MHz at Z pole) -> for CEPC Z pole
  - Radiation tolerance **(per year):** 1 MRad

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

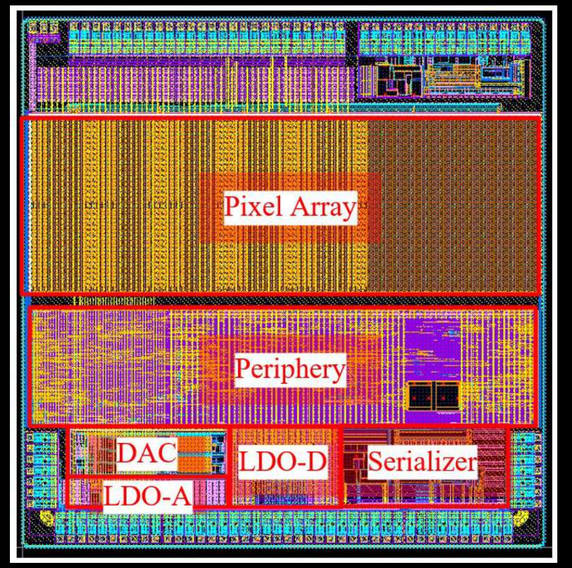
Sensor prototyping

- Completed 3 round of sensor prototyping
  - 1st Multi-wafer project chip (Taichupix1)
    - Submitted in June 2019, received in November 2019
  - 2nd Multi-wafer project chip(Taichupix2)
    - Submitted in Feb 2020, received in July 2020
    - A full functional pixel array (64×192 pixels)
  - 1st engineering run (Taichupix3)
    - Submitted in Q4 2021, received in Q2 2022
    - Full-size chip (1024× 512 pixels)

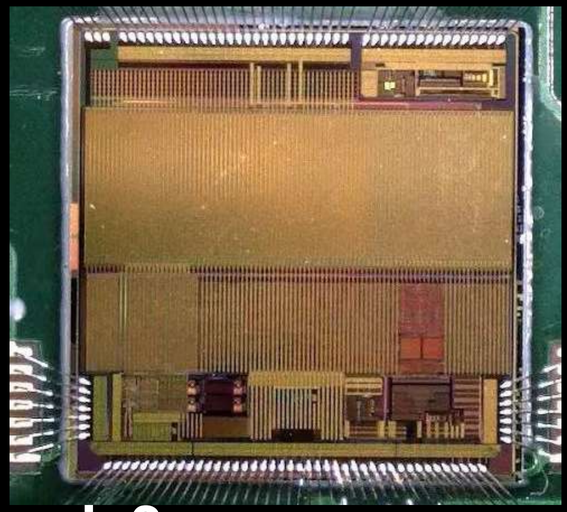
Taichupix2

Chip size：5mm × 5mm

Pixel size：25μm × 25μm



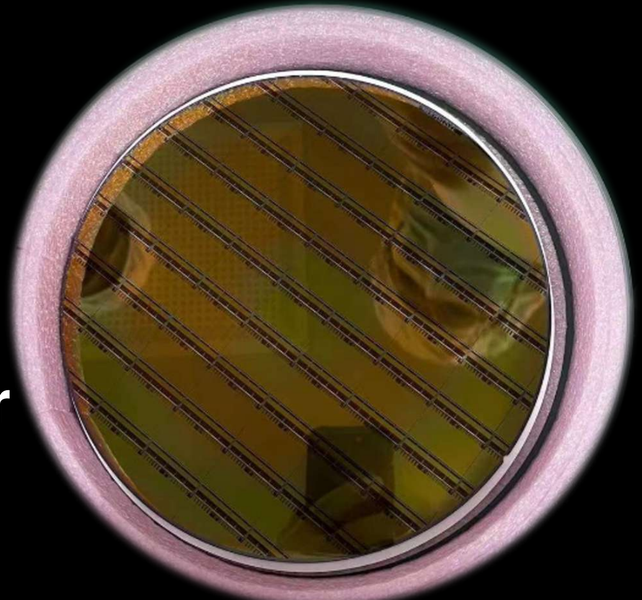
Taichupix2 on test board



Taichupix3

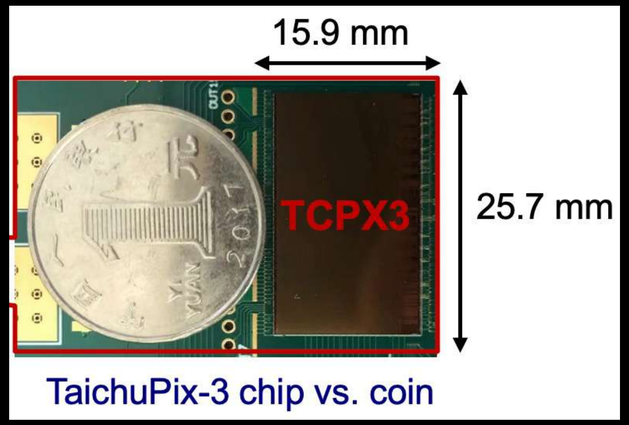
Chip size：26 ×16 mm

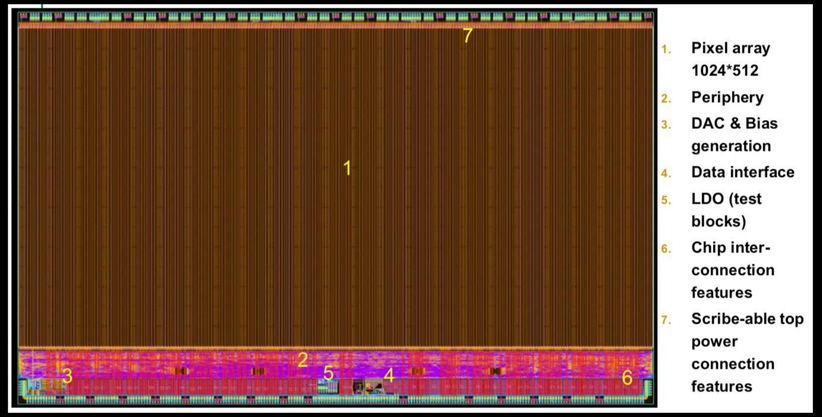
Pixel size：25μm × 25μm



TaichuPix3
8-inch wafer

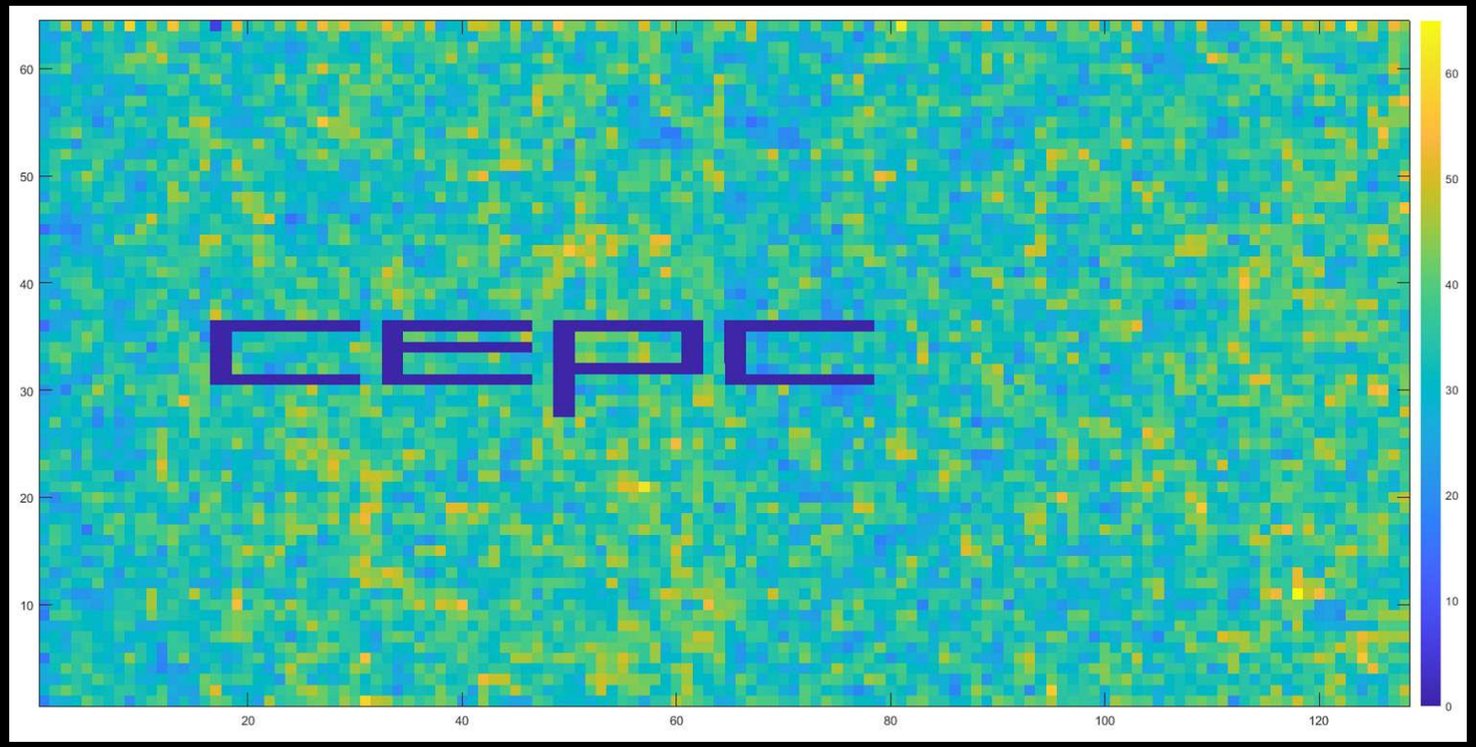
Taichupix3 photo





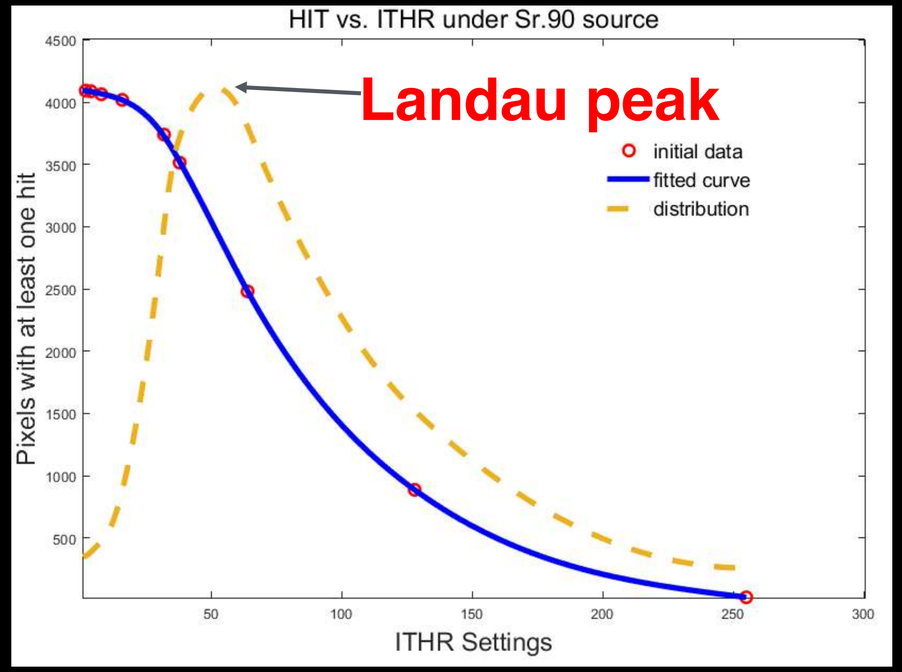
TaichuPix2 test with ^{90}Sr source

- Exposure to ^{90}Sr at different threshold (ITHR)
- **Mean cluster size around 2.2**

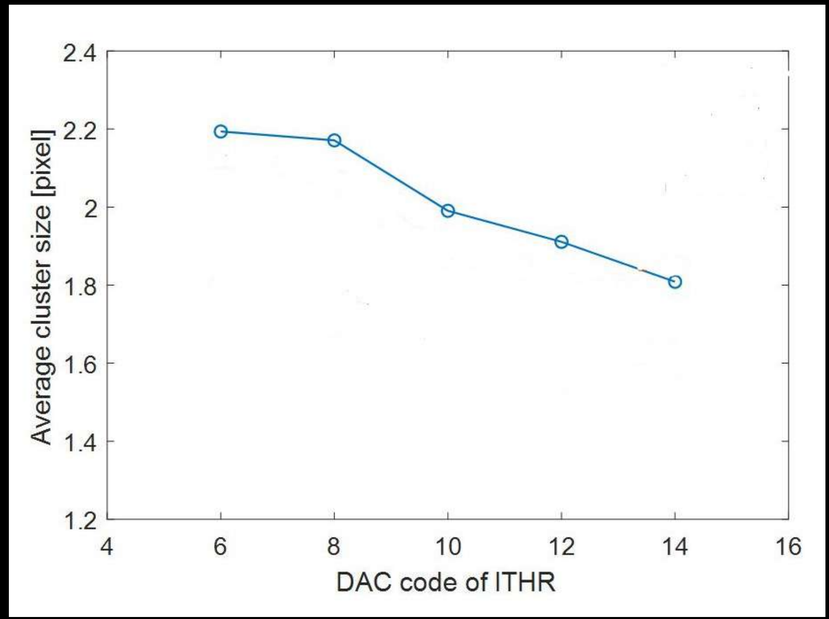


Hit map of TC2 exposure to ^{90}Sr
With CEPC maskoff pattern

Threshold scan in beta tests



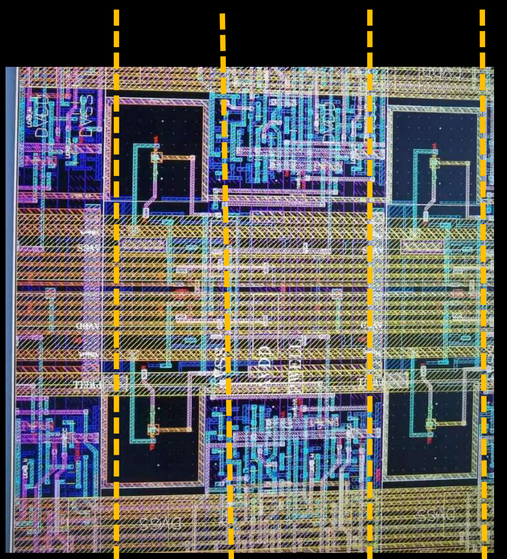
Mean cluster sizes Vs threshold



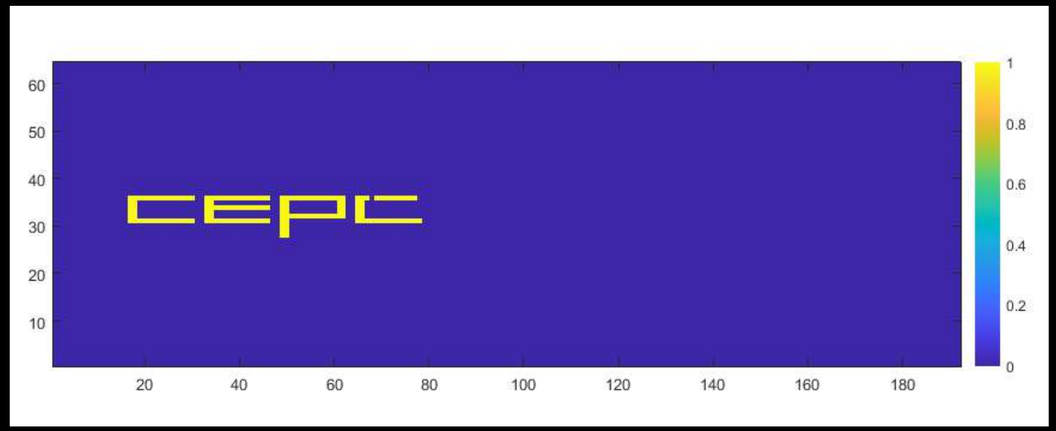
TaichuPix2 Laser test （fine scan)

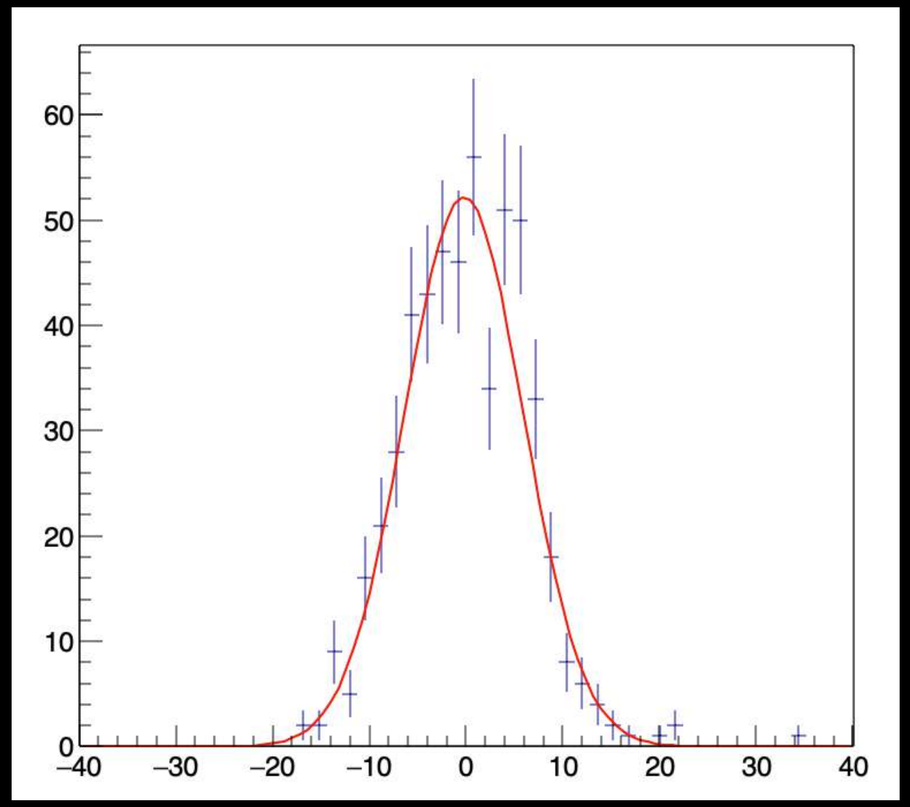
- Resolution in laser tests
  - 5~6 um (depending on thresholds)

Designed diode window width : 9 um

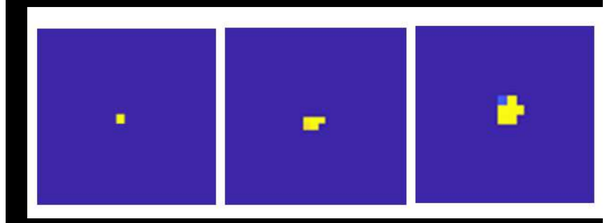


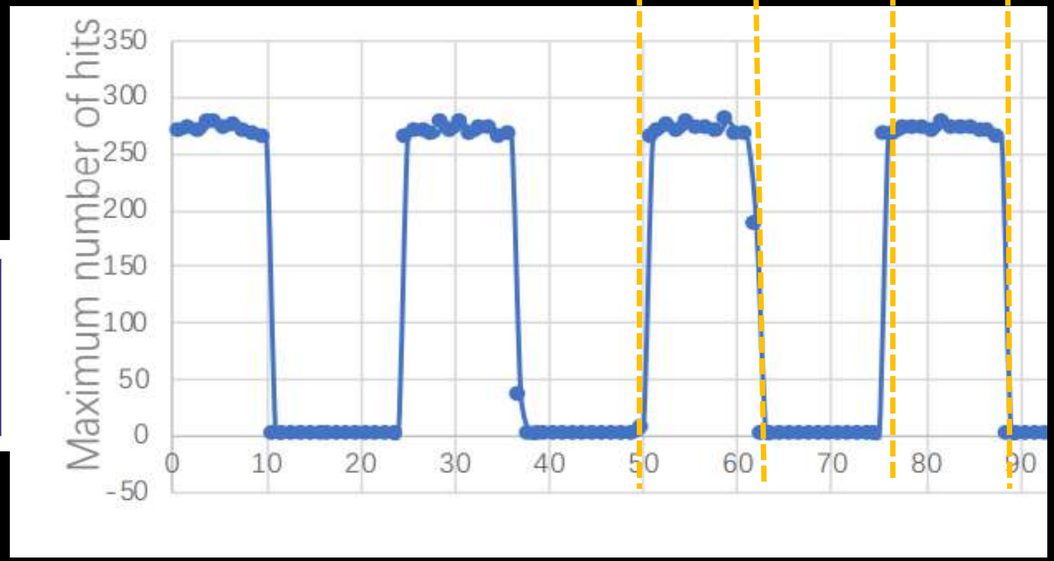
CEPC letter scan using laser





Laser focusing

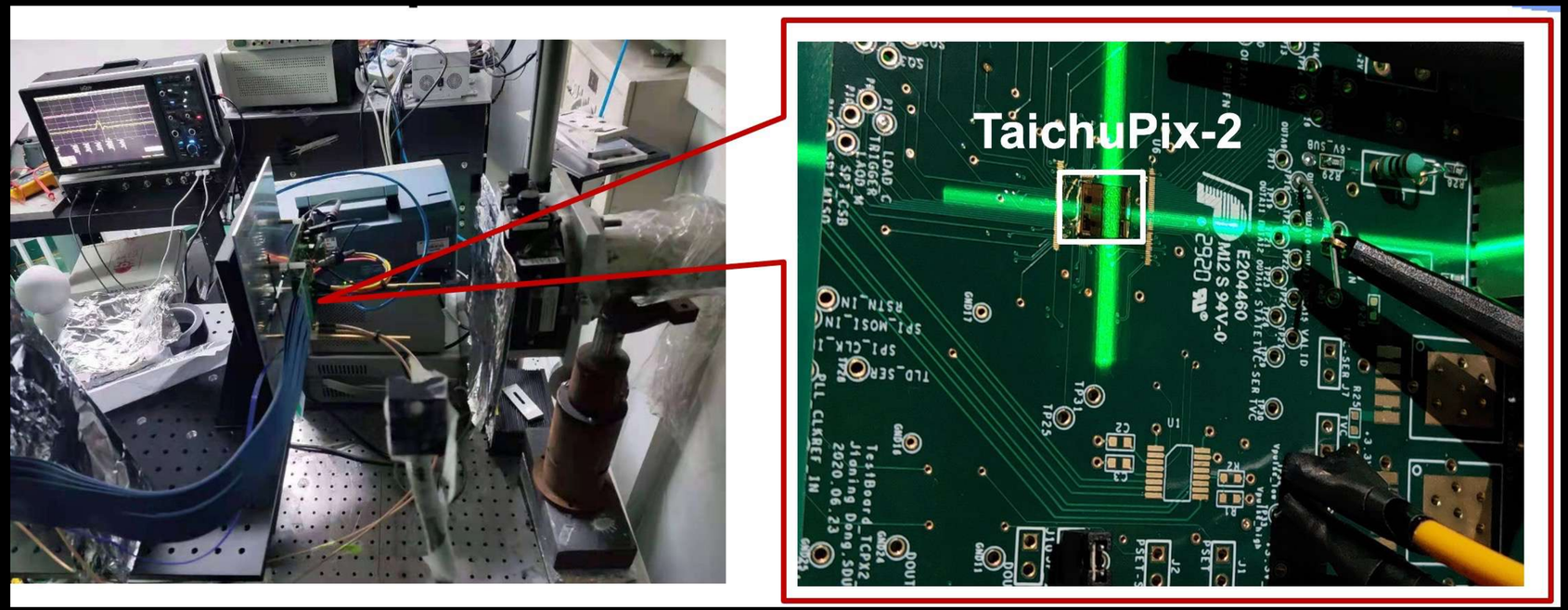


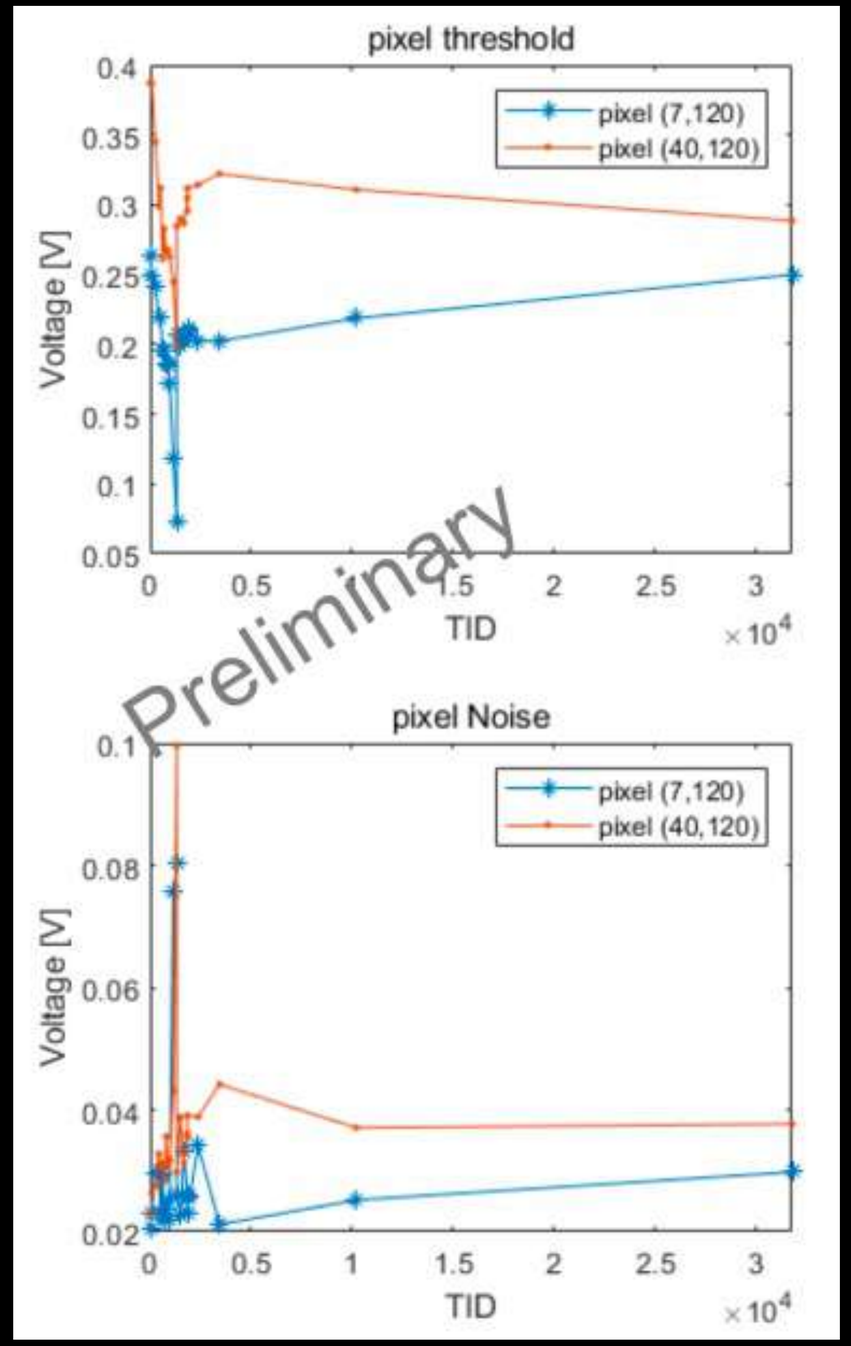


TaichuPix radiation test

- Completed two round of CMOS sensor prototyping
  - Radiation to 30Mrad at BSRF ,TaichuPix2 is still functional
  - TaichuPix-2 irradiated at BSRF 1W2B beamline (6 keV X-ray)
    - Dose rate ~17.63 krad/min for the first 2.5 Mrad
    - then 211.56 krad/min for 51 min, then 1.24 Mrad/min for 15 min
    - Dose rates were calibrated with an ion chamber before test

Radiation test at BSRF for 2nd MPW chip

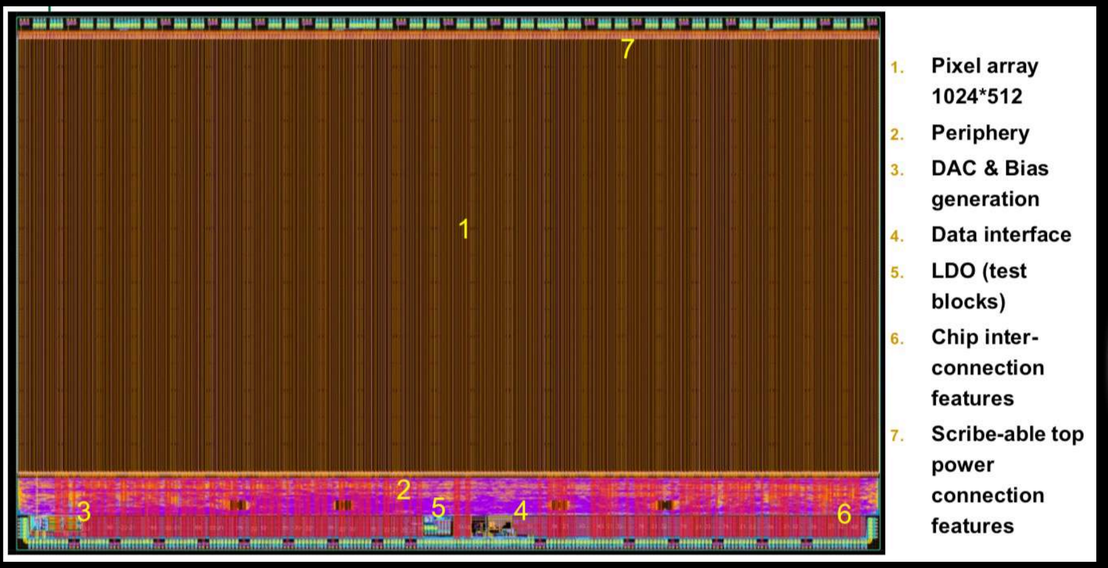




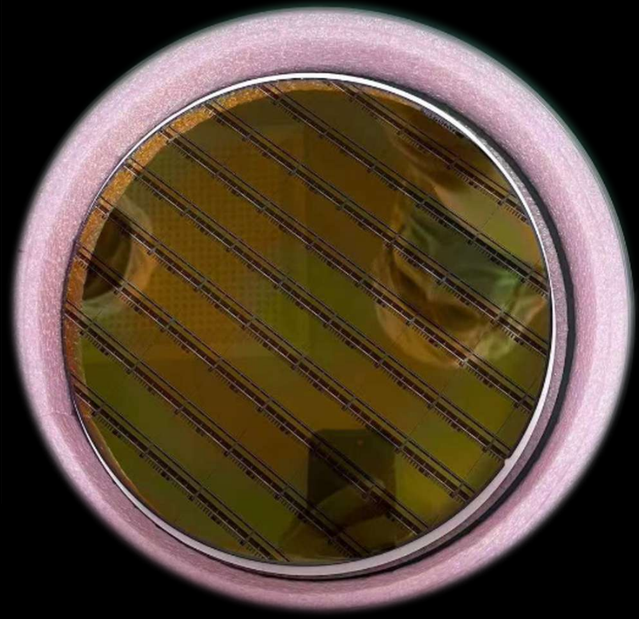
Full-size TaichuPix3 (engineering run)

- **Full-size Taichu pixel received**
  - **6 wafers of TaichuPix3 (3 wafer with standard CIS process, 3 wafer using modified process)**
    - **Sent 1 wafers for thinning (150um) and dicing**
    - **Other wafers will do wafer-level testings**
  - **1024×512 Pixel array (25μm×25μm pixel size), Process: Towerjazz 180nm**
  - **FE-I3 like Periphery digital readout , high speed data interface**
    - **Time stamp precision: 25ns (modified process）-50ns (standard process)**

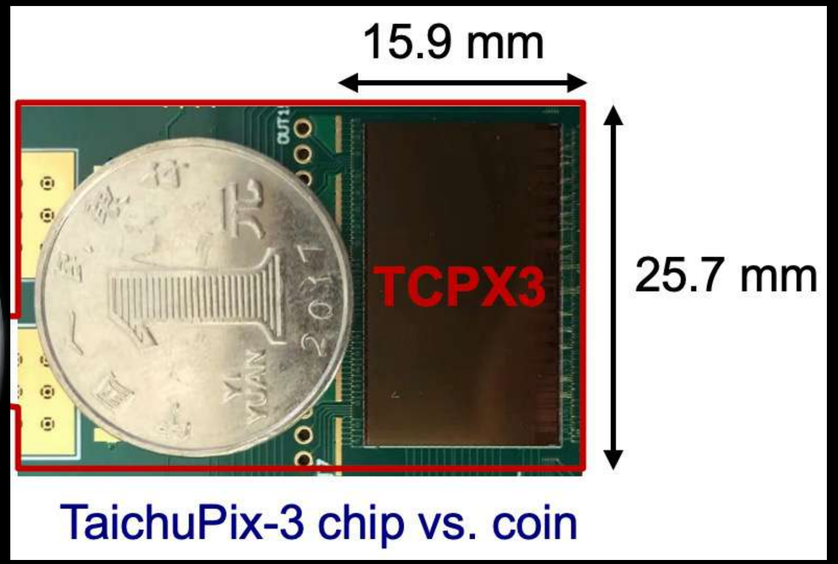
Taichupix3 design



Taichupix3 Wafer

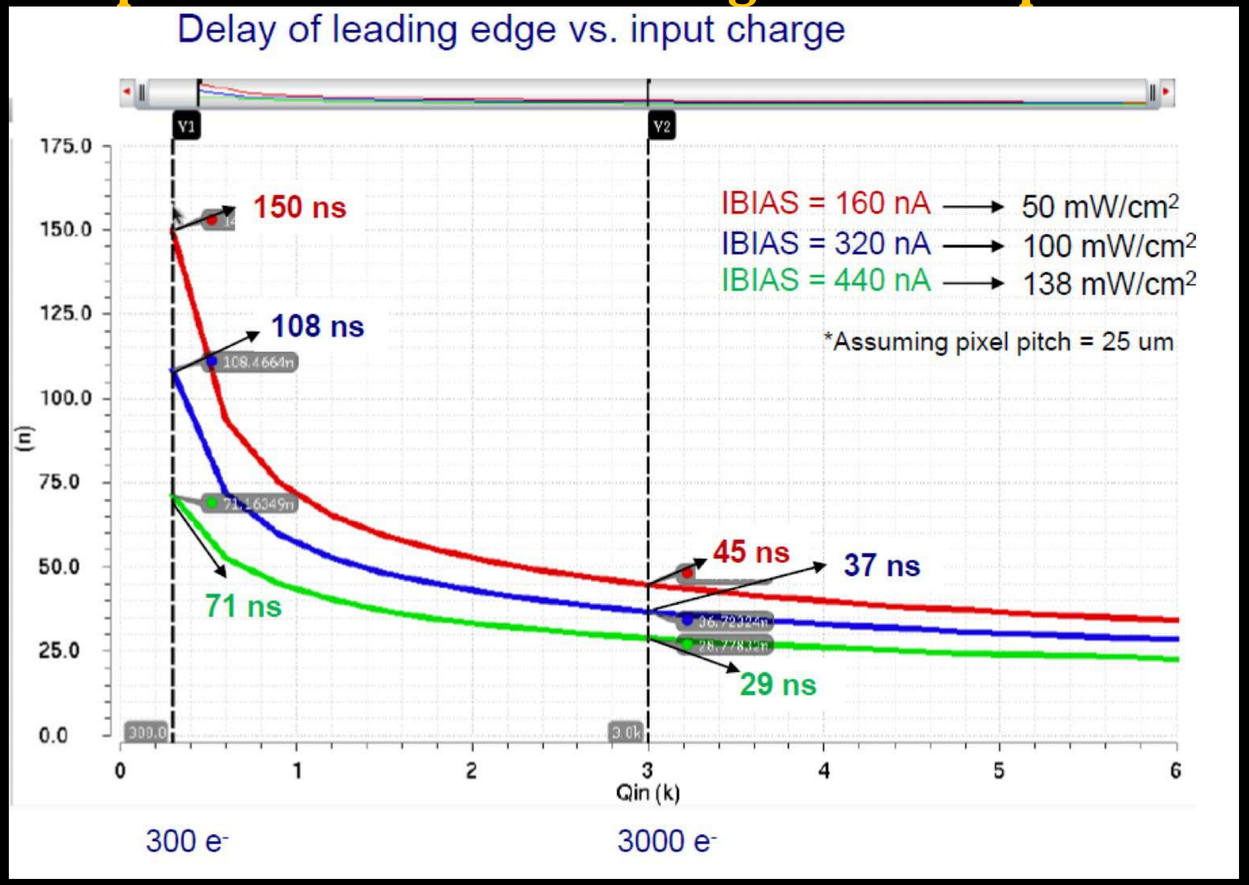


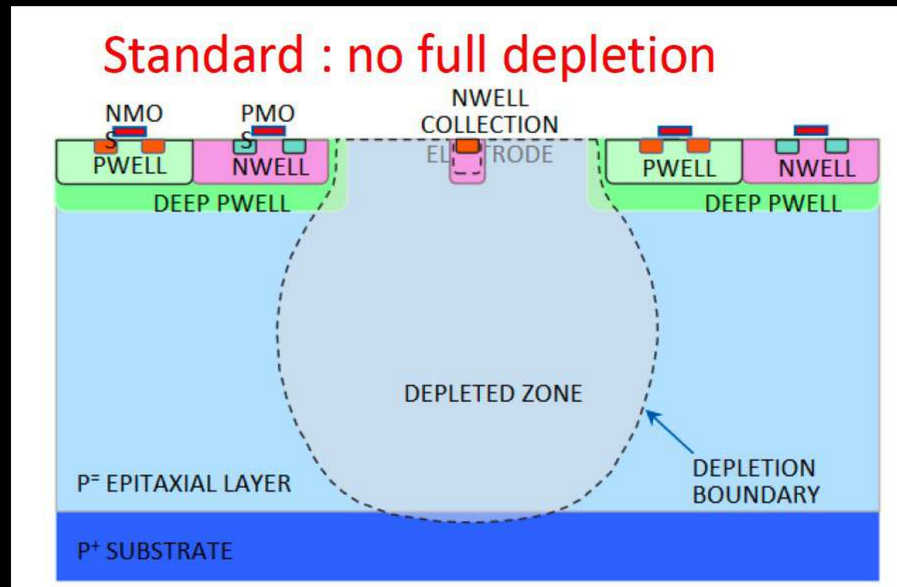
Taichupix3 chip

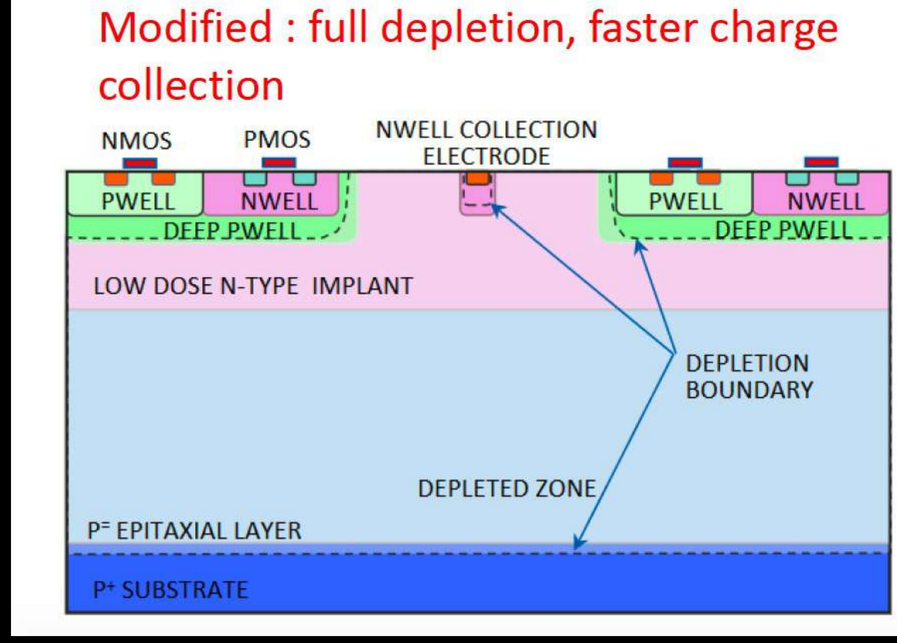


Pixel Analog design

- CEPC time stamping precision requirement:
  - 25-50ns time stamp presition , stamping collisions at Z pole
  - <500ns dead time
- Taichu pixel analog design:
  - ~50ns~150ns time stamp (standard CMOS MAPS tech.)
  - Expect to read ~25ns using Modified process:





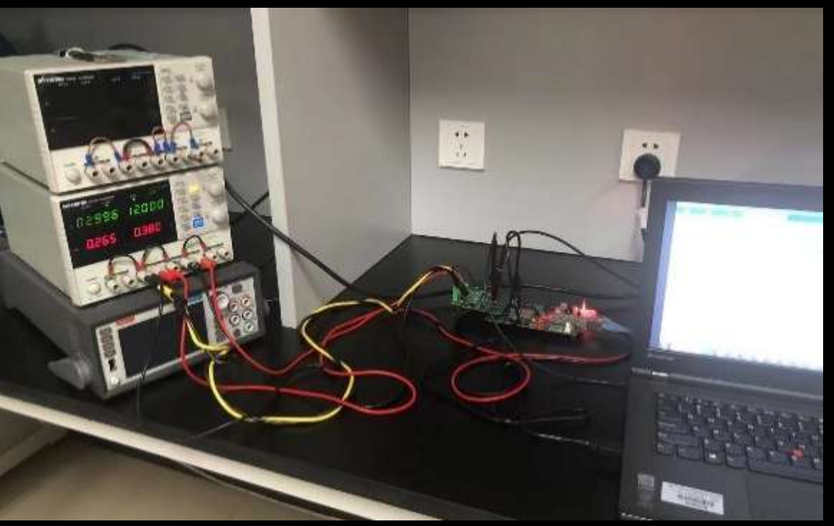


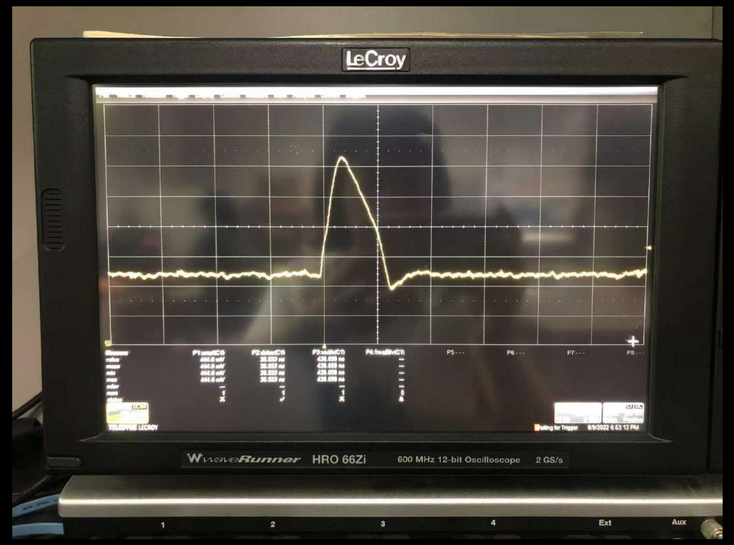
Preliminary TaichuPix-3 test

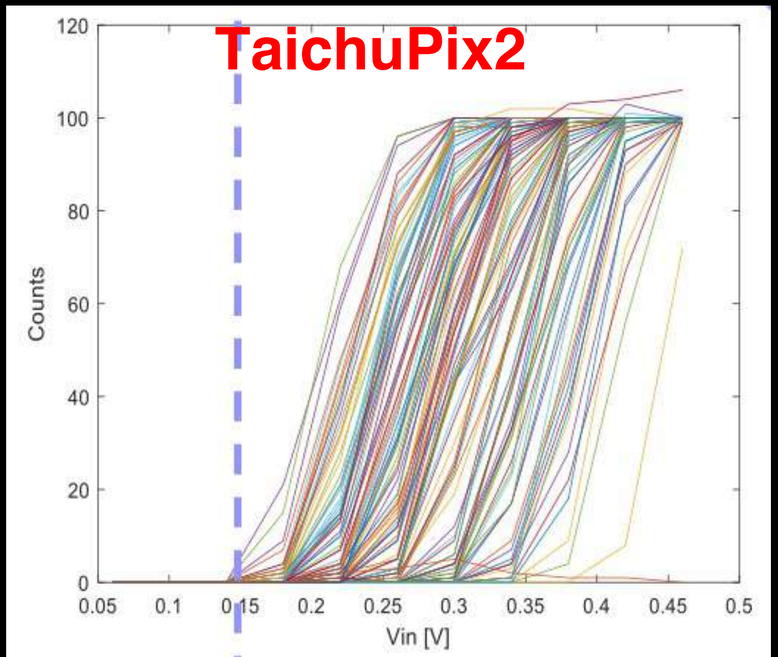
- Single chip test system built
- Taichipix3 can reach ~100 e- lower threshold than Taichu2

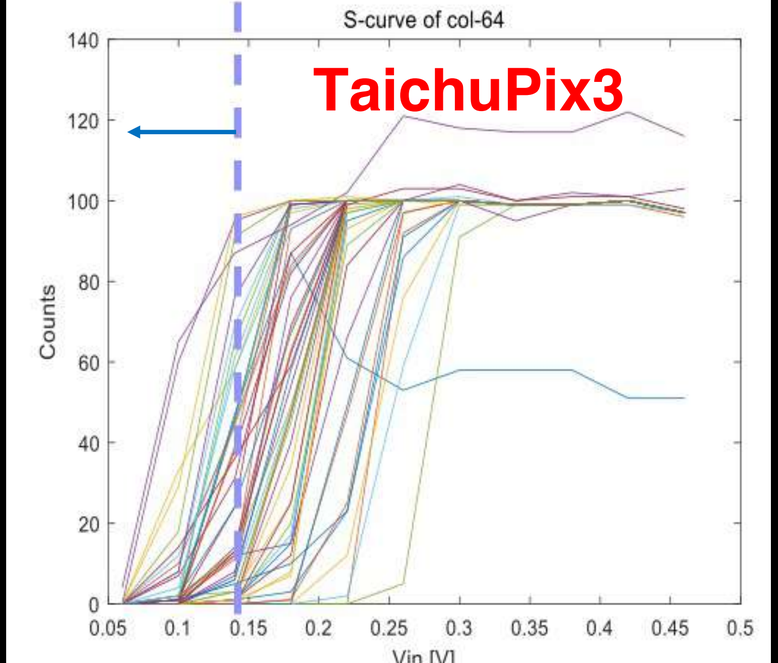
➢Improvement of DAC design in TC3 verified

Taichu2 mean threshold	Taichu3 mean threshold
267 e-	~169 e-



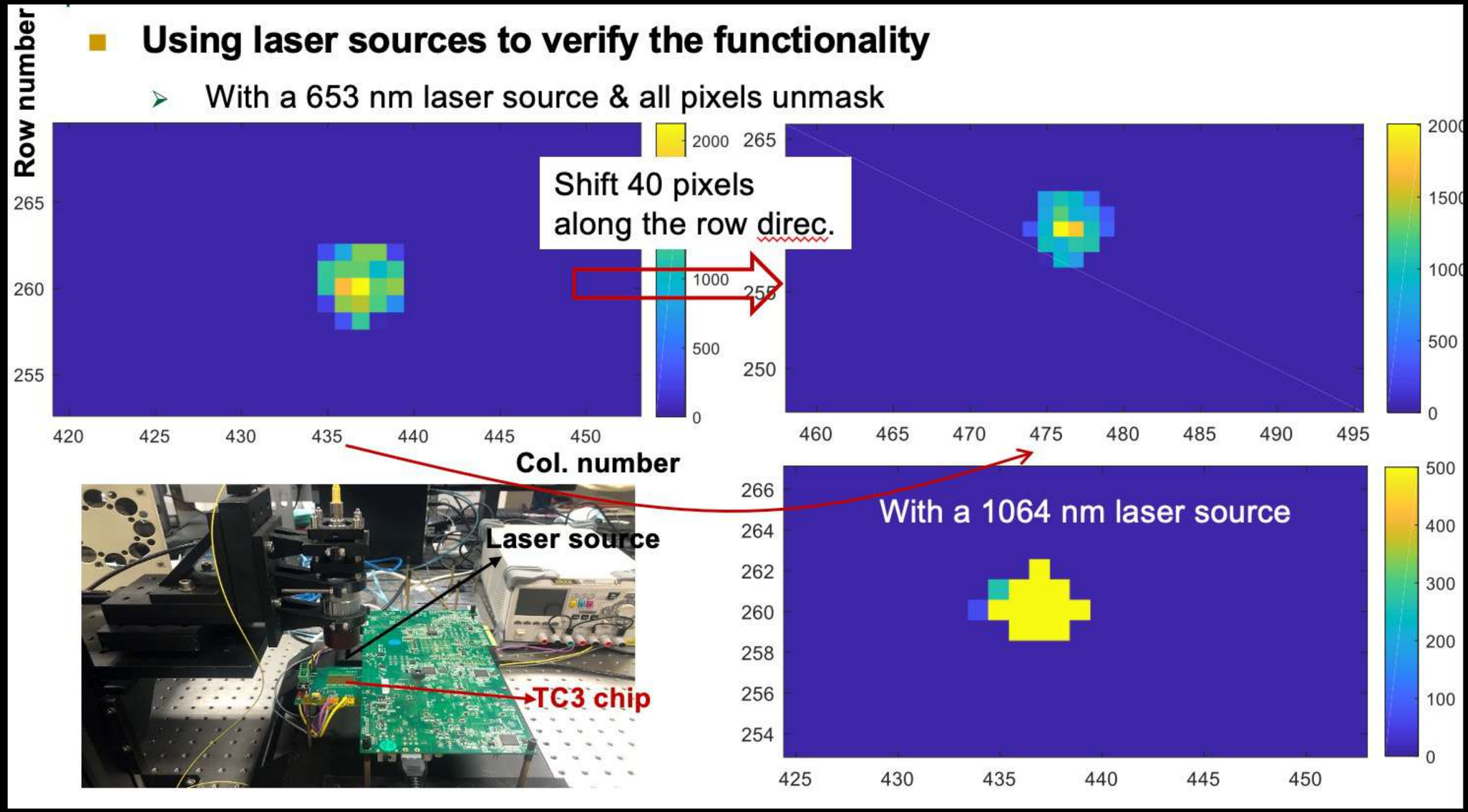






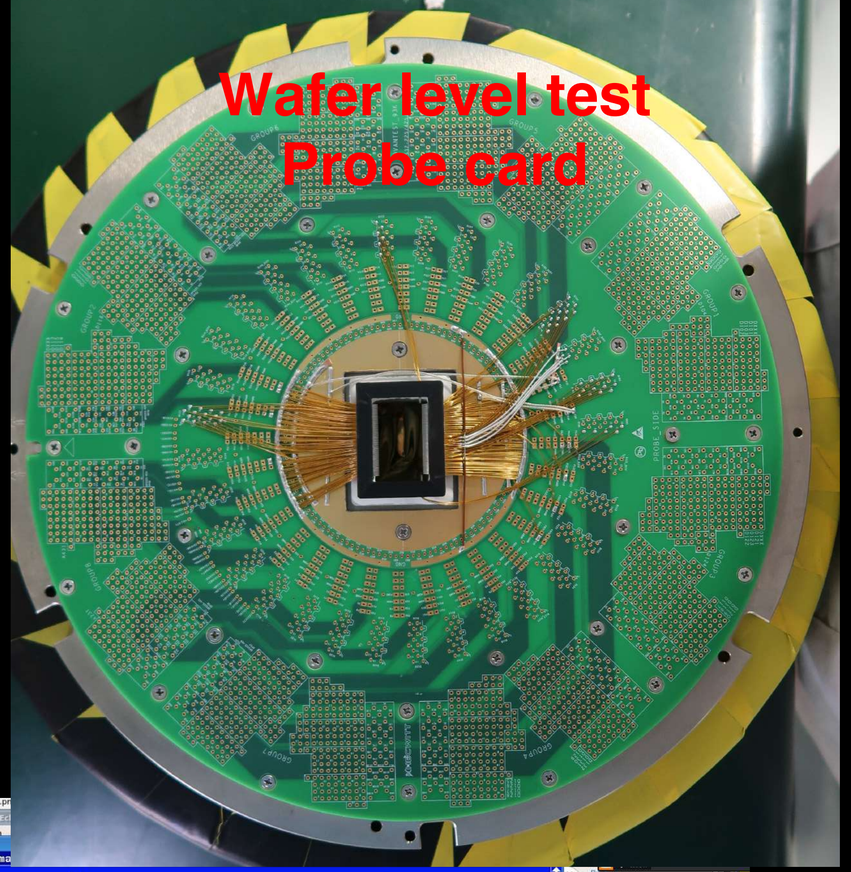
TaichuPix3 laser tests

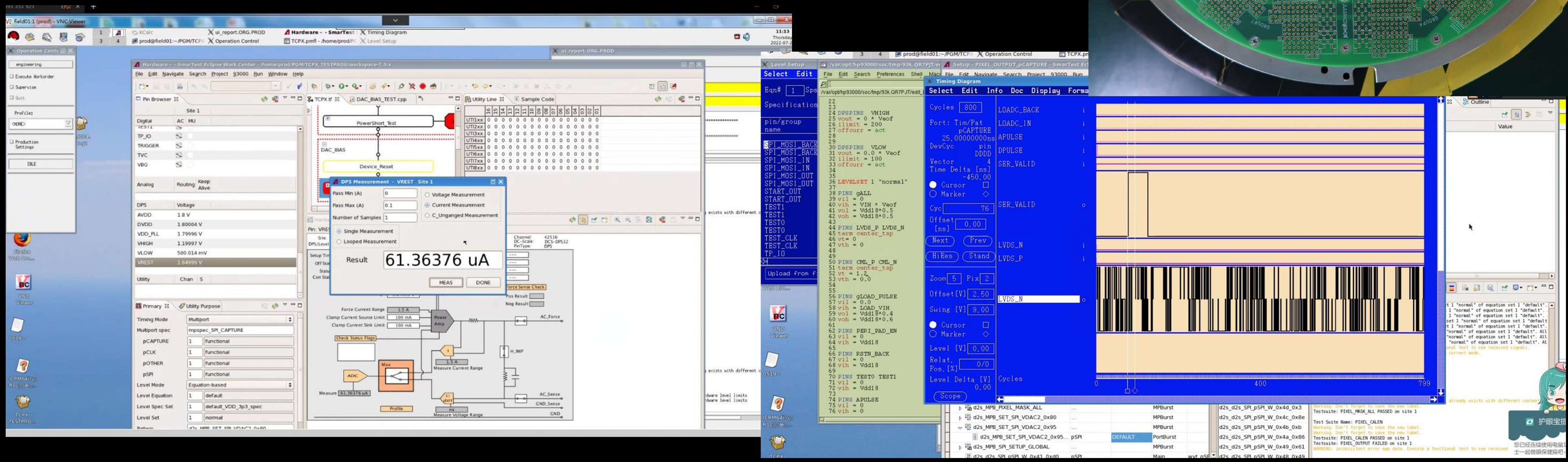
- Functionality of the full signal chain proved with laser tests



Taichupix3 wafer-level testing

- Wafer level testing in NCAP (on-going)
  - Remote commissioning of testing program
  - probe cards ready
  - Plan to measure the yield and select good sensors for aseembly

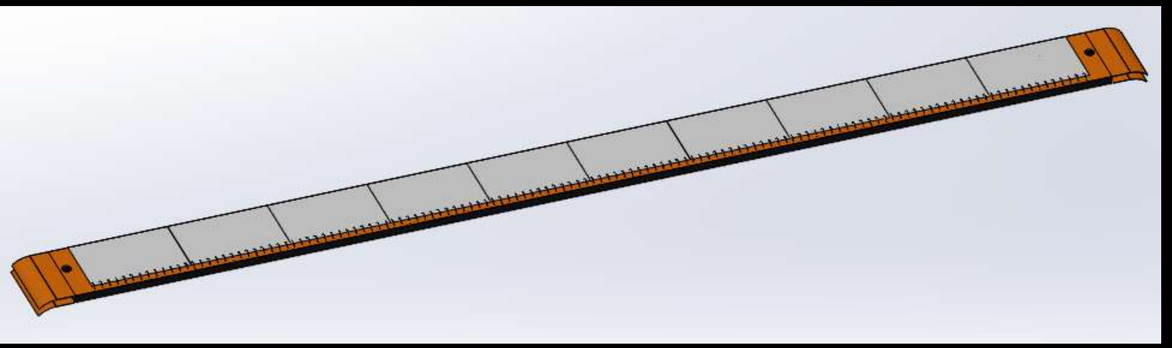




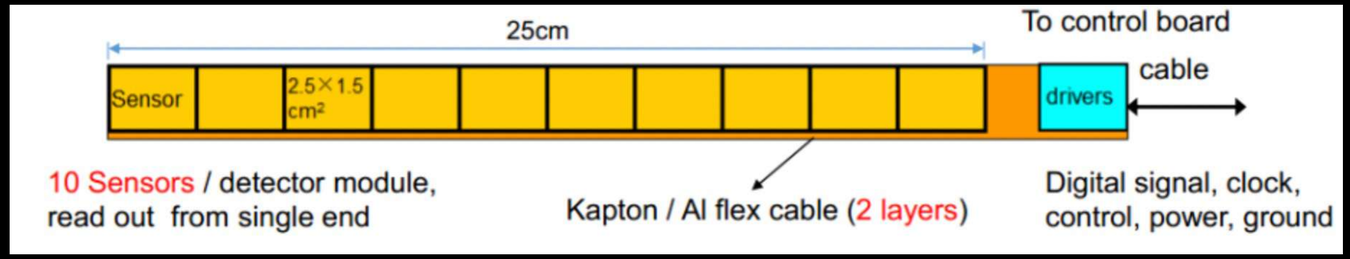
Detector module (ladder) R & D

- Completed preliminary version of detector module (ladder) design
  - Detector module (ladder)= 10 sensors + support structure+ flexible PCB+ control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control , power, ground will be handled by control board through flexible PCB

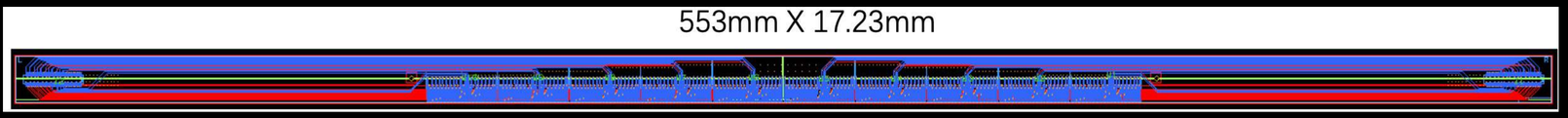
3D model of the ladder



Schematic of ladder electronics



flexible PCB design

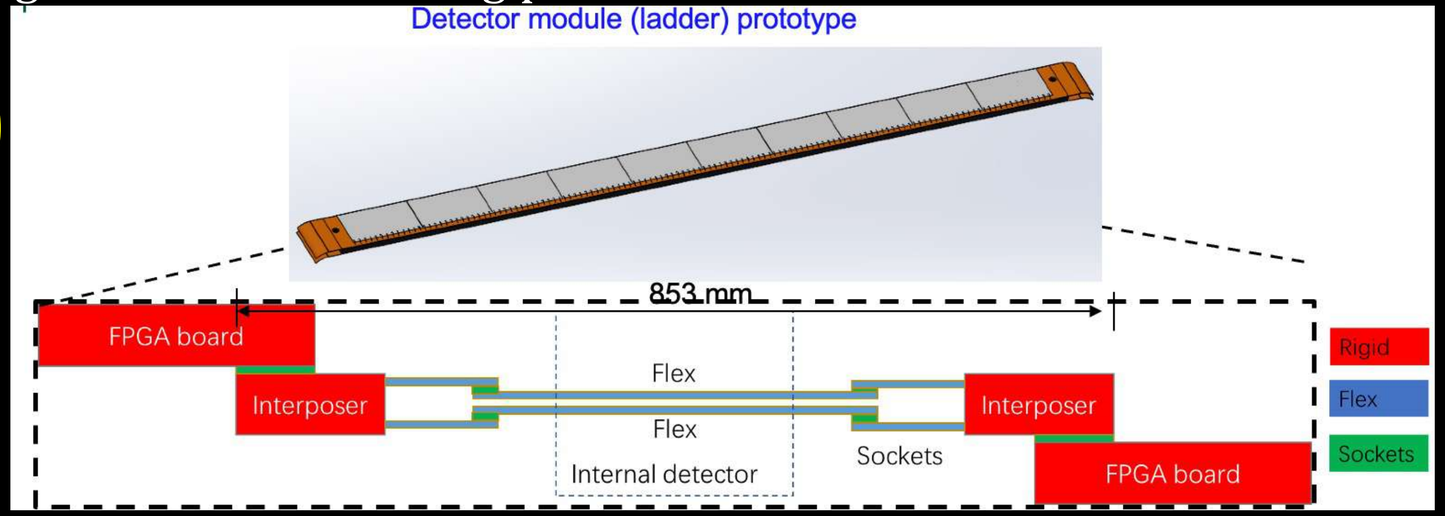


Profile of flexible PCB

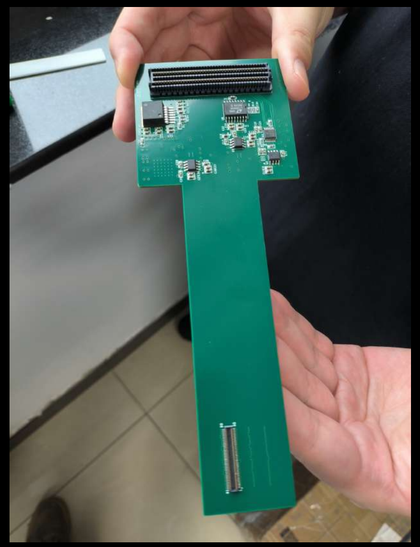
	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

ladder readout design

- Flexible PCB board
  - First version of the flex board produced, glue and wire bonding performed in IHEP with TaichuPix3
  - 2nd version submitted last week
    - 2 metal layer (lower material budget)
- Interface board
  - First version ready (Hard PCB)
  - Connecting flex to FPGA boards

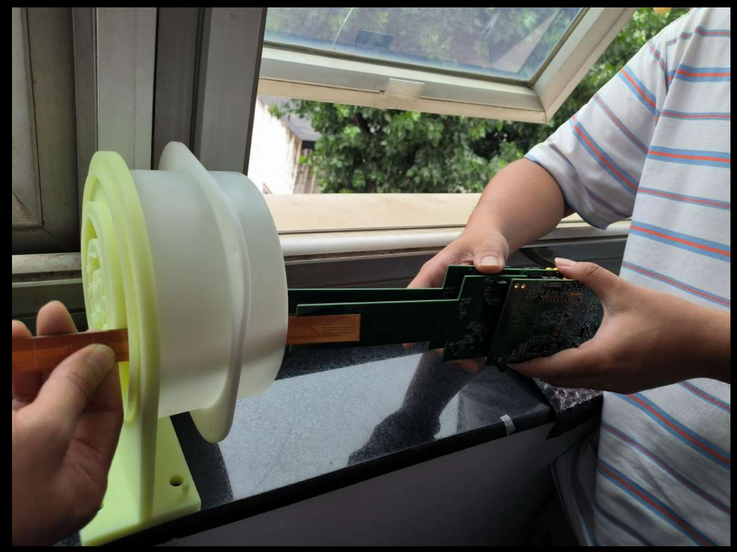


Interface board



Taichupix3 chip bonded to the flex board

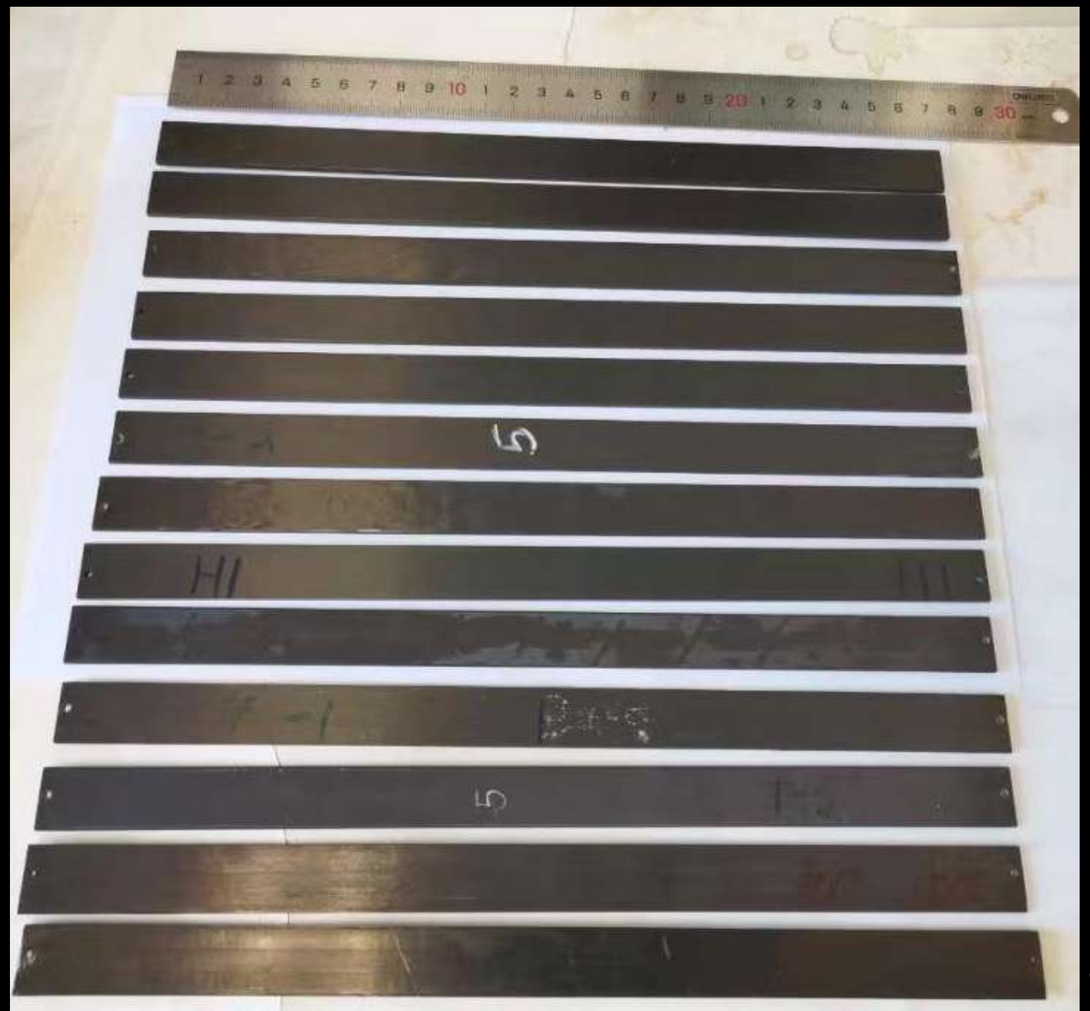
Ladder readout in vertex detector mockup



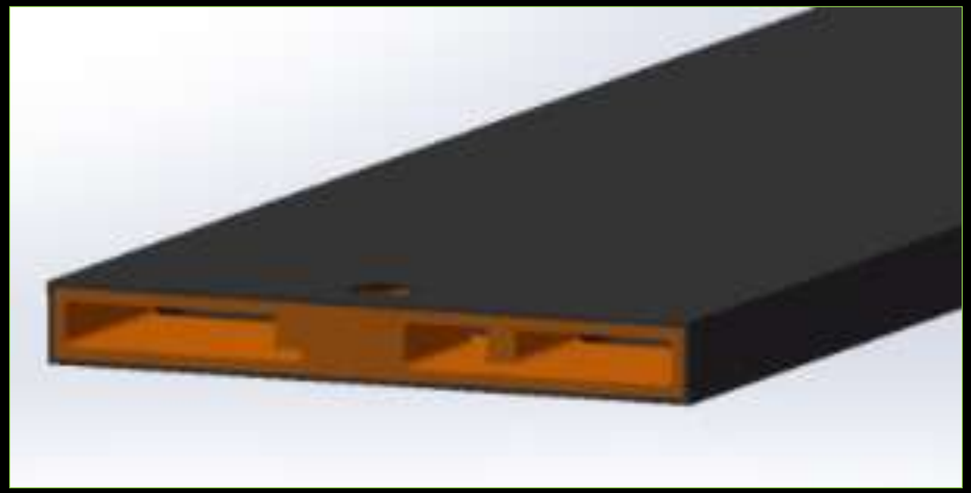
Support structure of the ladder

- Production of ladder support with carbon fiber is in good progress
  - Half of the ladder support has been produced.
  - The yield of first batch of production is a bit low (~10%)
  - New batch of production has higher yield
  - Expected 120 good ladder support in this production

Ladder support production



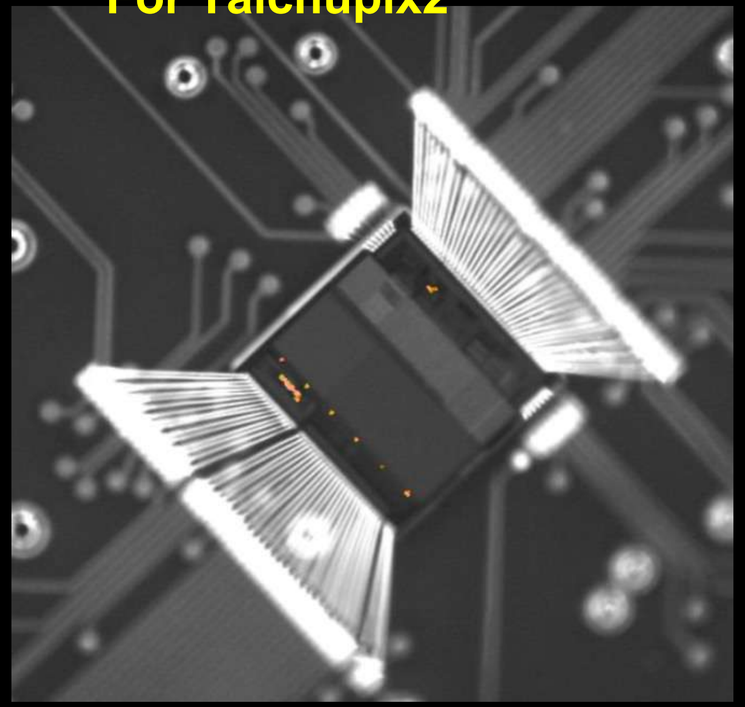
Ladder support structure 3D model



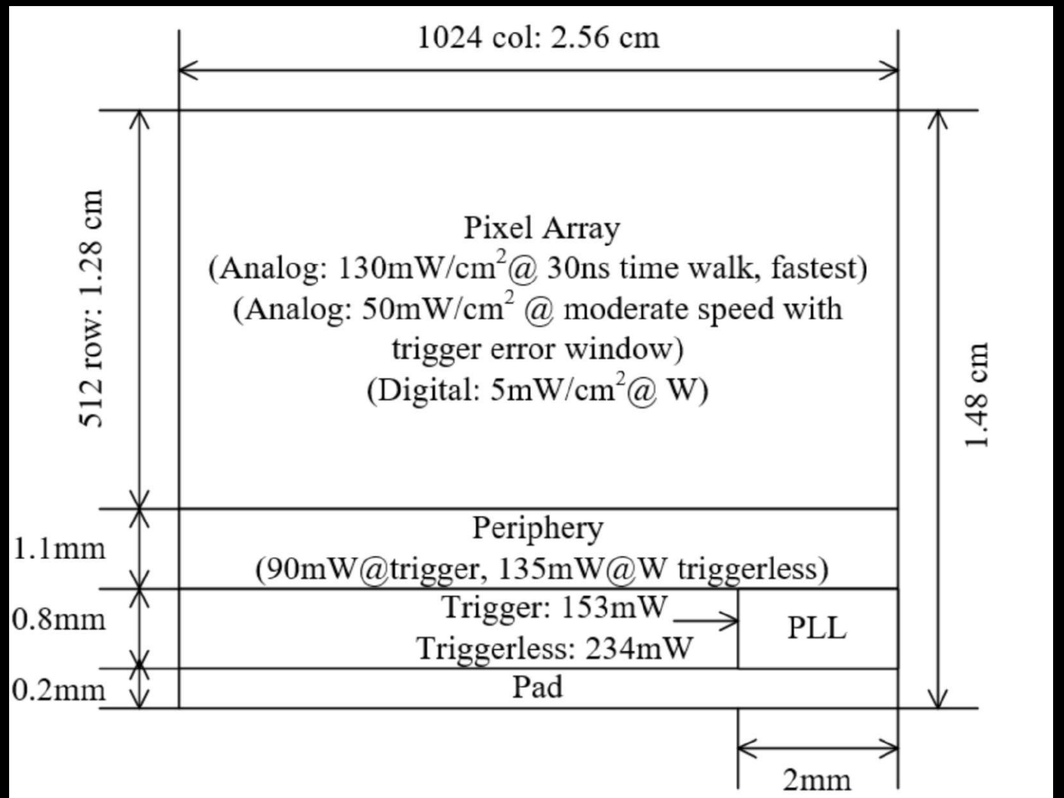
Cooling design

- **Air cooling is baseline design for CEPC vertex detector**
- **Sensor Power dissipation:**
  - Taichupix : $\leq 100\ mW/cm^2$. (trigger mode) ; CEPC final goal : $\leq 50\ mW/cm^2$
- Cooling simulations of a single complete ladder
  - Testbench setup has been designed and built for air cooling , vibration tests

The EMMI (Emission Microscope) For Taichupix2



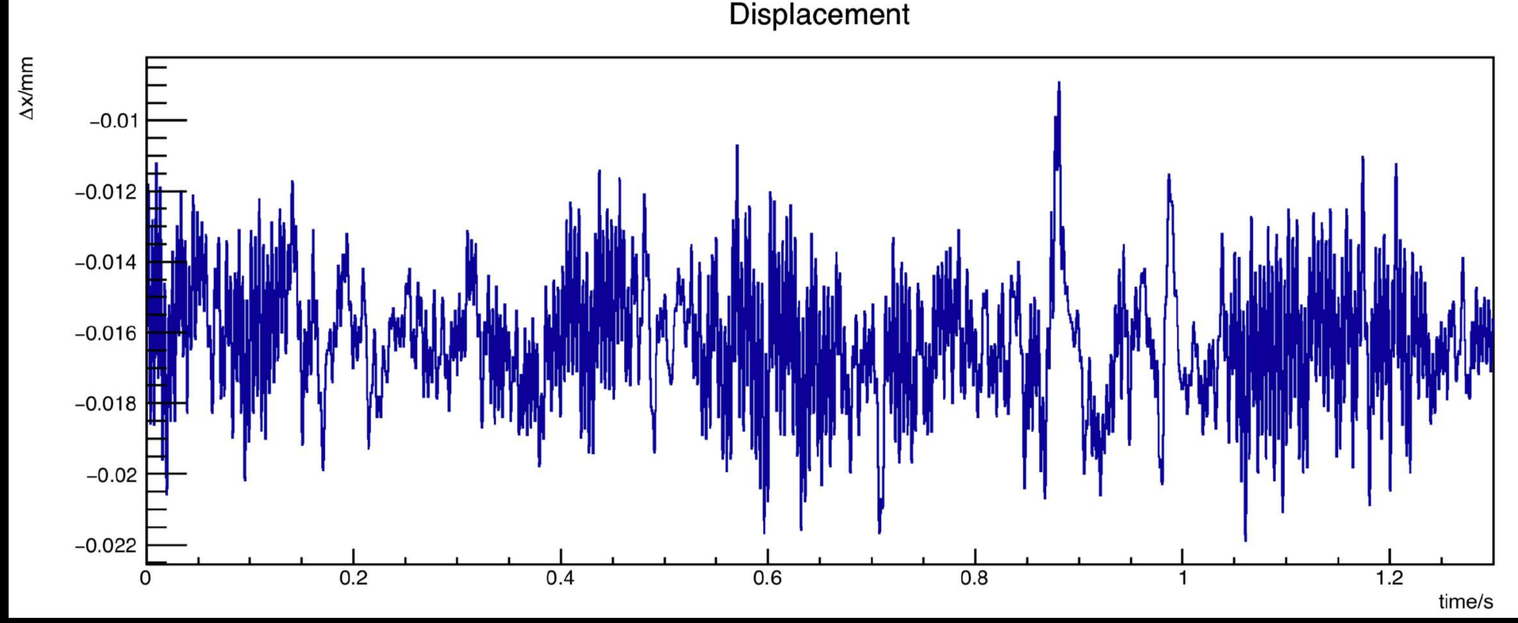
Power consumption



Air Cooling test

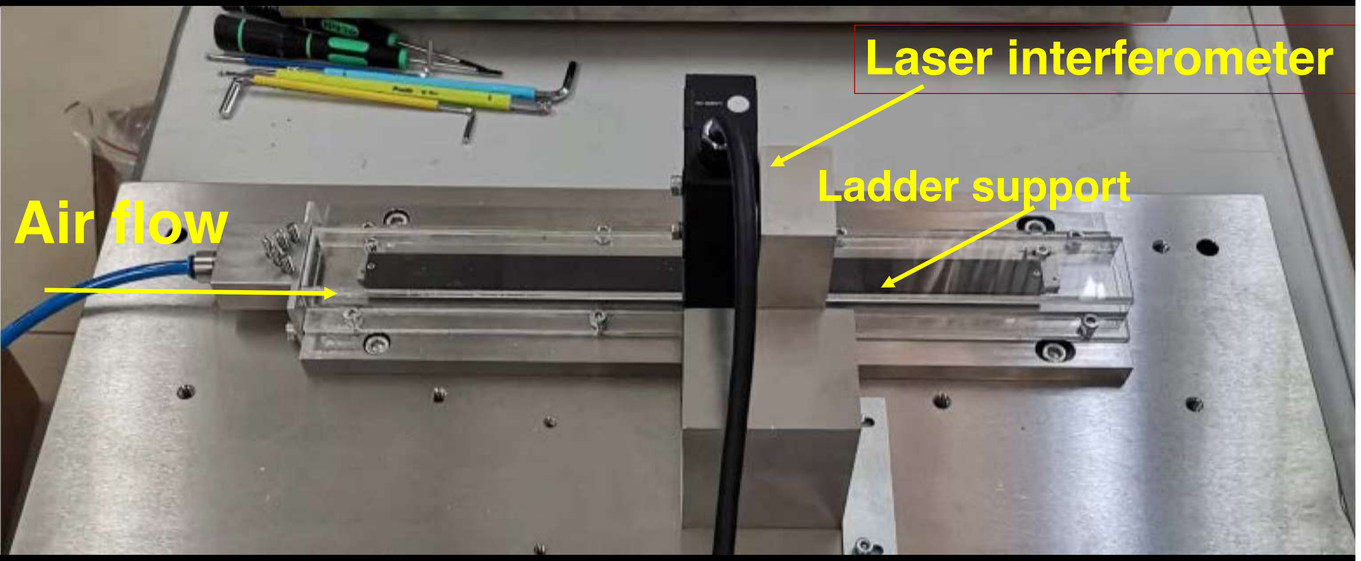
- Test bench setup for air-cooling
- Vibration follows Gaussian distribution
  - Displacement below (σ~2μm)

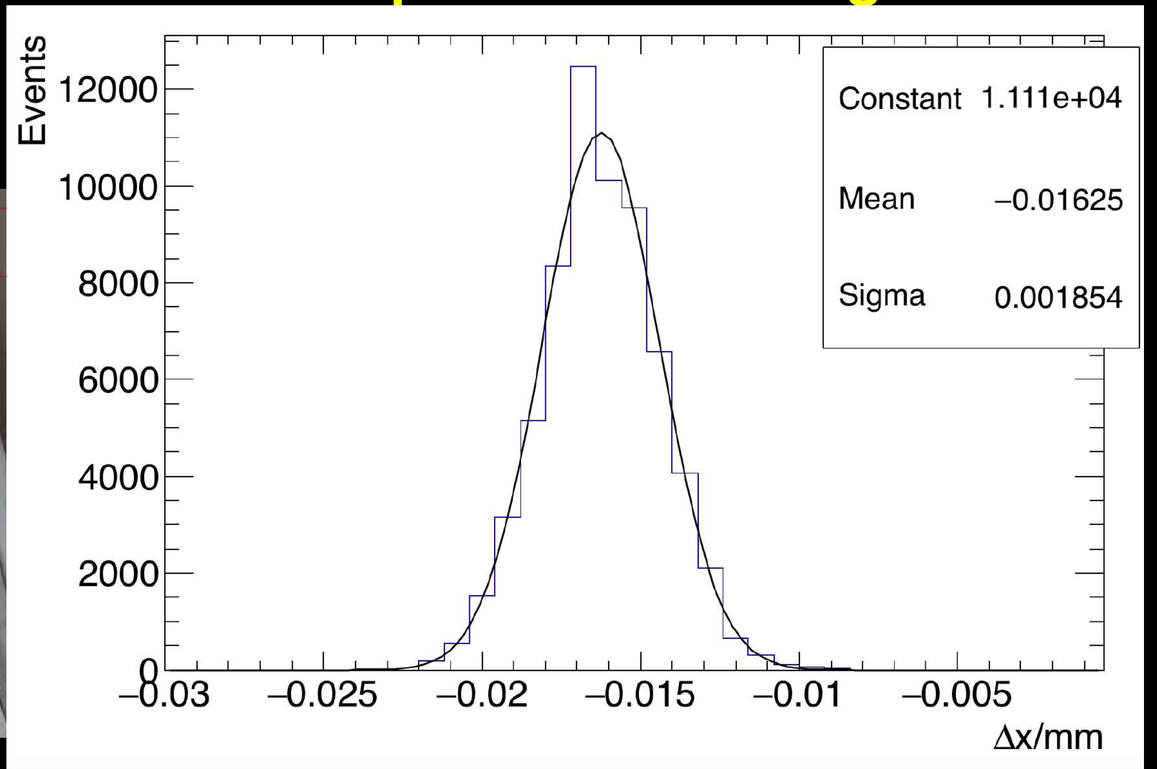
Core of Gaussian is still under control



Typical Vibration displacement during air cooling

Test setup prototype for ladder cooling
Use compressed air for cooling

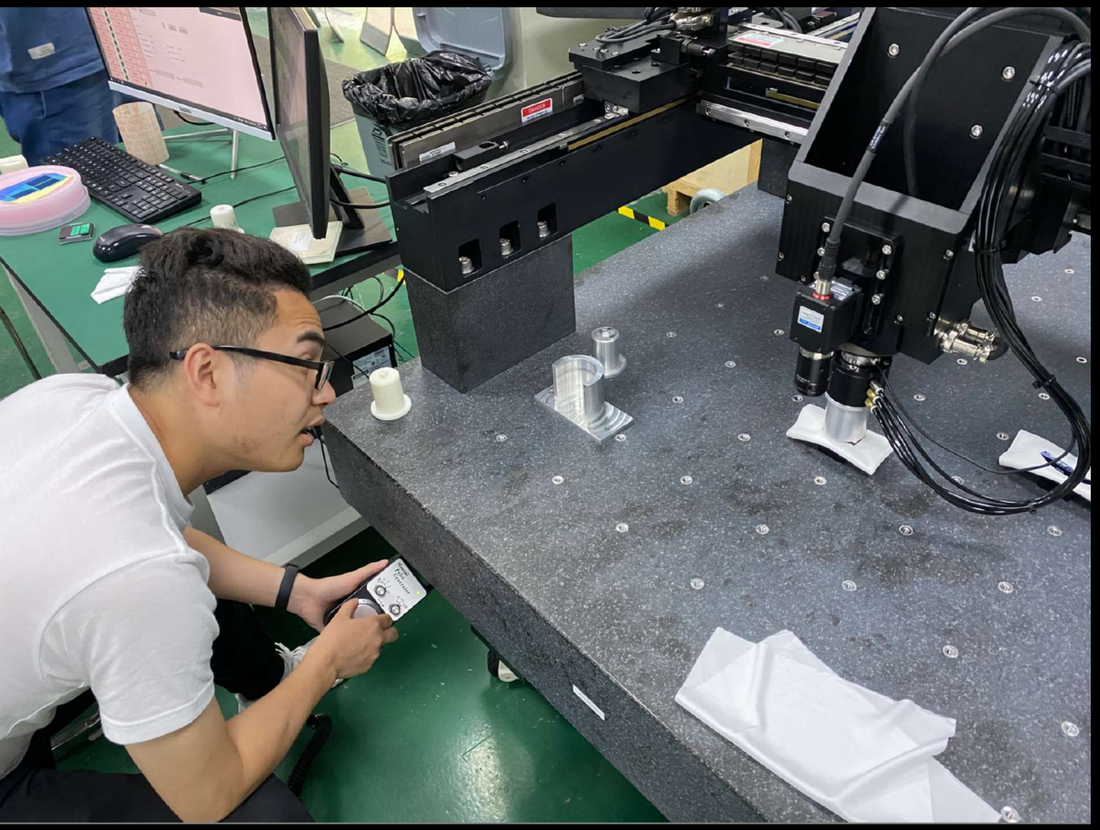




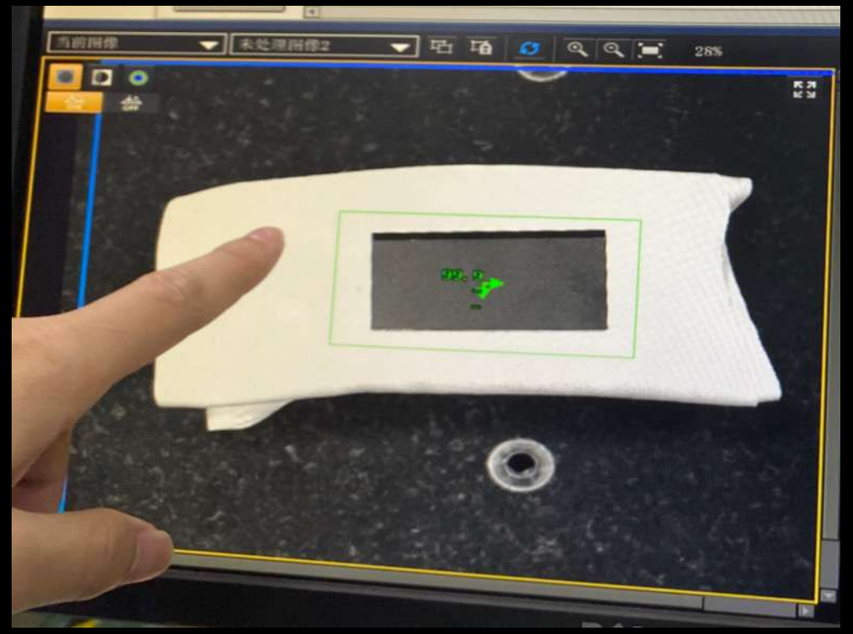
Gantry for vertex detector prototype assembly

- **3~5um good position resolution require high assembly precision**
- **Cooperate with domestic company on R & D Gantry automatic module assembly.**
  - **Pattern recognition with high resolution camera**
  - **Automatic chip pick-up and positioning**
  - **Automatic Glue dispending**

Gantry system



Pattern recognition



automatic glue dispending

Ladder assembly

- Ladder (double side)= 20 ASIC chips + two flexible PCB + carbon fiber support
- Ladder assembly procedure verified with dummy ASIC (glass) using gantry robot

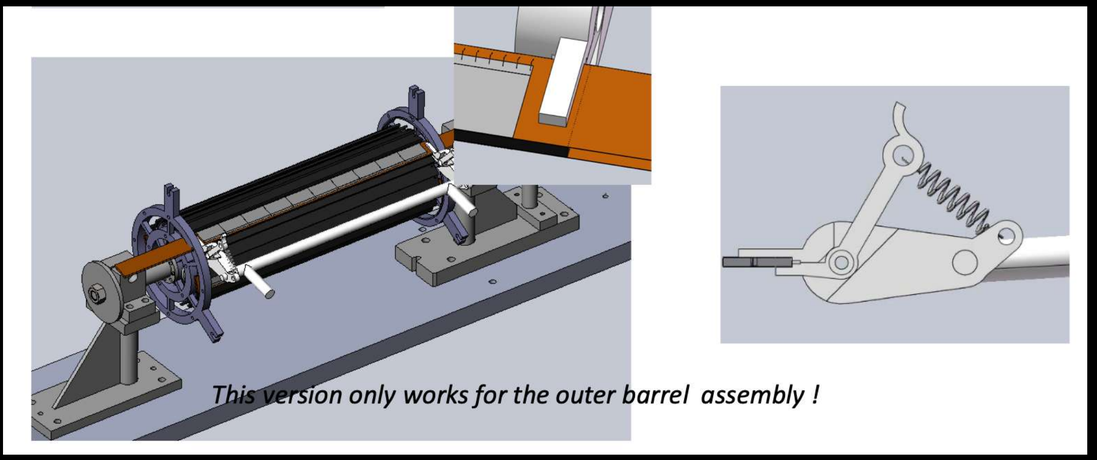
ladder on wire bonding machine

Dummy ladder glue dispensing using gantry

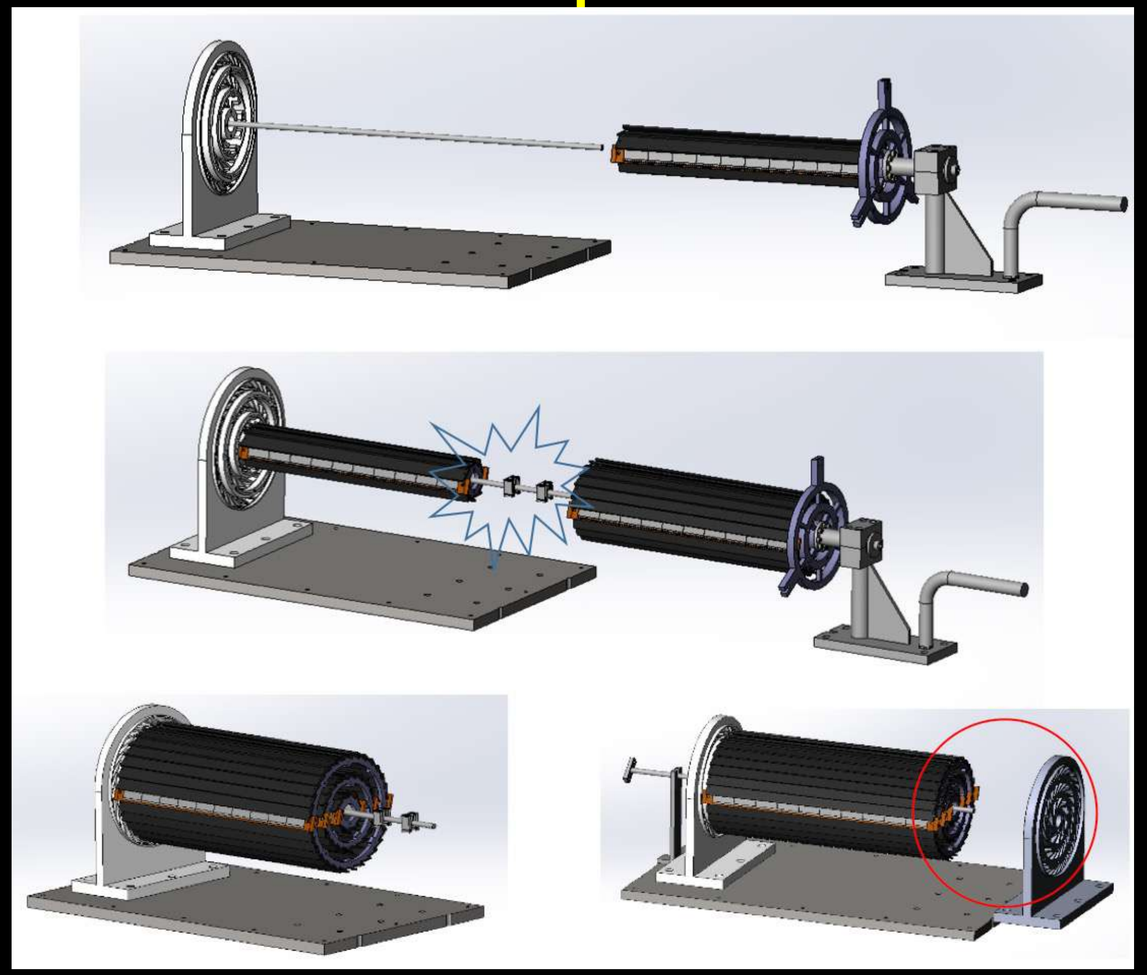
Tooling Design for Barrels Assembling

- Ladder installation procedure designed
- 3 sets of tooling for 3 layer of barrel assembling.
- Tooling and special tool for inner and middle barrels assembling.

Tooling for installation

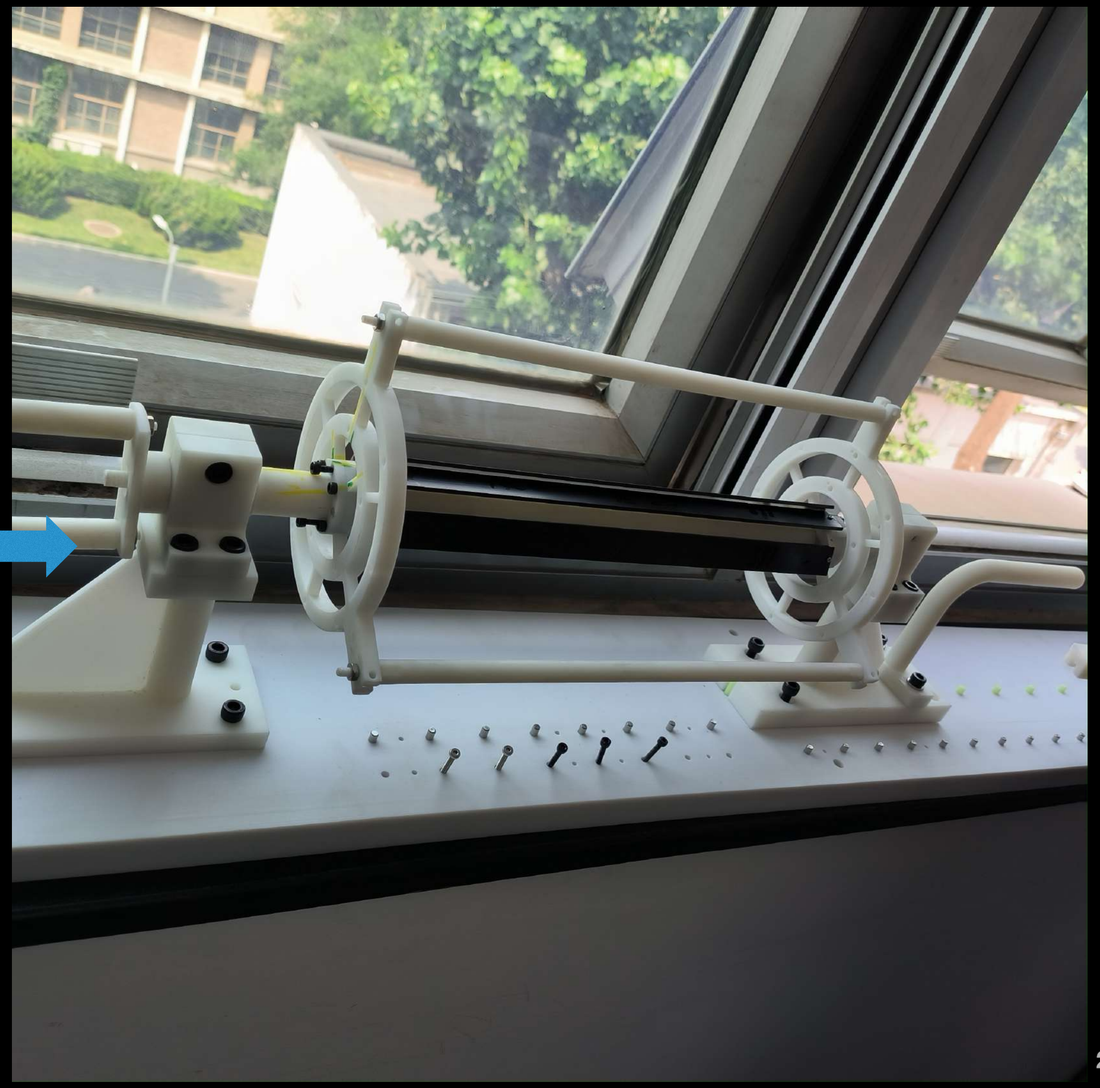


Installation procedure



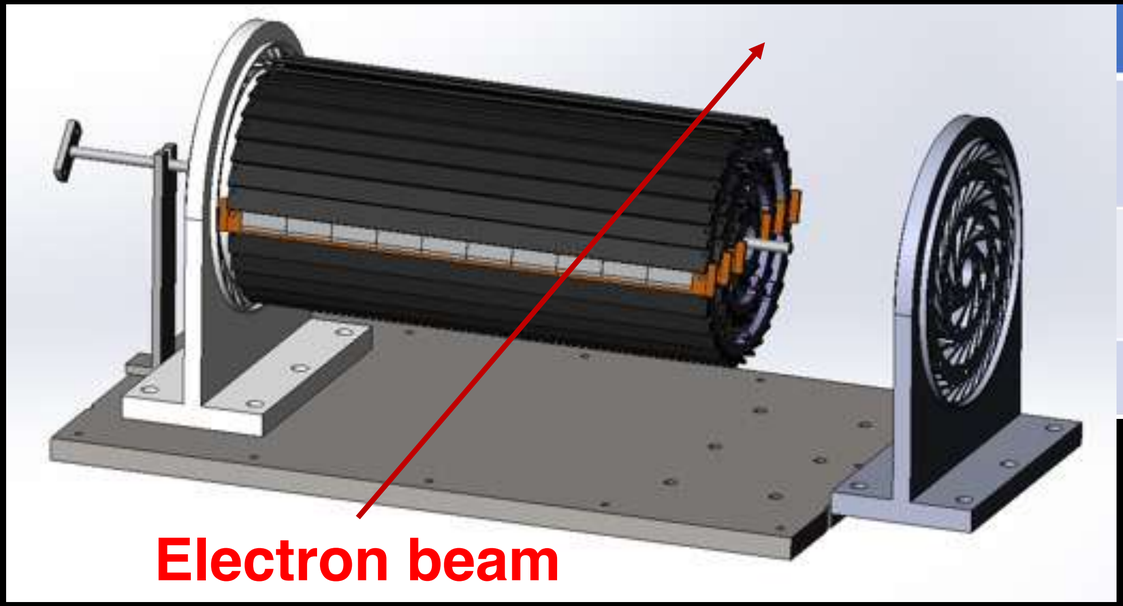
Vertex detector prototype assembly procedure

- Mockup with 3D printing production done
  - Assembly with 3D mockup model verified the installation procedure
- Production with precise machining started
  - Expected finished at middle of September



Plan for test beam

- Expect to perform beam test in DESY(3 - 7GeV electron beams)
  - Rehearsal testbeam at Beijing Synchrotron Radiation Facility(BSRF) (1-2 GeV electrons)
  - **Plan to Installed 6 real ladders on prototype**
  - **Plan to install all the carbon fiber support structure for full vertex detector**
  - Beam is shooting at one section of vertex detectors



	DESY	IHEP E3 beam	BSRF
Momentum	1-6 GeV	<1 GeV secondary beam	1~2.5 GeV
Particles	electrons	Protons/ Pions/ /Electrons	electrons
Trigger rate	4000 Hz/cm^2	0.6 Hz/cm^2	~50 Hz/cm^2

Schedule

- 2022
  - September: mounting readout ladders
  - October: finished mounting the ladders, and readout tests
  - Earlier November: Finish assembly of prototype
  - November: Cosmic ray testing or BEPC beam test
  - December 12-22: DESY test beam (test beam time slot reserved for two weeks)
- 2023
  - Q1: testbeam data analysis, paper publication
  - Q2: MOST review meeting

5-Dec-22	49		CMS-InnerTracker	X			
12-Dec-22	50		CEPC Vertex	X	HVMAPS	X	
19-Dec-22	51	Beam till 22/12 0800	CEPC Vertex	X	HVMAPS	X	
26-Dec-22	52		Shutdown				

Summary

- Large-scale full-size sensor chip (Taichupix3) from engineering run ready
  - Promising test results obtained in single-chip testing
  - Can reach lower threshold in Taichupix3 → expect to have higher efficiency than Taichupix2
- Detector module (ladder) assembly in progress
  - Assembly tools and procedure verified with dummy chips
  - 1st version of electronics board ready
- Full vertex detector prototype assembly in process
  - Assembly procedure are validated with 3D printing mockups
- Next major milestone:
  - Test beam at DESY at December 2022
  - MOST2 project review meeting at Q2 2023

	Final goal	Status
Spatial resolution	3~5 μm	Will measure in DESY test beam
Radiation hardness	>1MRad In radiation test	First test up to 30 Mrad. Chip is still functional

Research Team in task 2

4 institutes

课题2：**IHEP - 中国科学院高能物理研究所**
SDU - 山东大学
NJU - 南京大学
NWU - 西北工业大学

Institutes	Tasks
IHEP	Full CMOS chip modeling, Pixel Analog, PLL block Detector module (ladder) prototyping Data acquisition system R & D Vertex detector assembly and commissioning
CCNU/IFAE	CMOS sensor chip: Pixel Digital
NWPU	CMOS sensor chip: Periphery Logic, LDO
SDU	CMOS sensor chip: Bias generation, TCAD simulation Sensor test board design
NJU	Irradiation, test beam organization

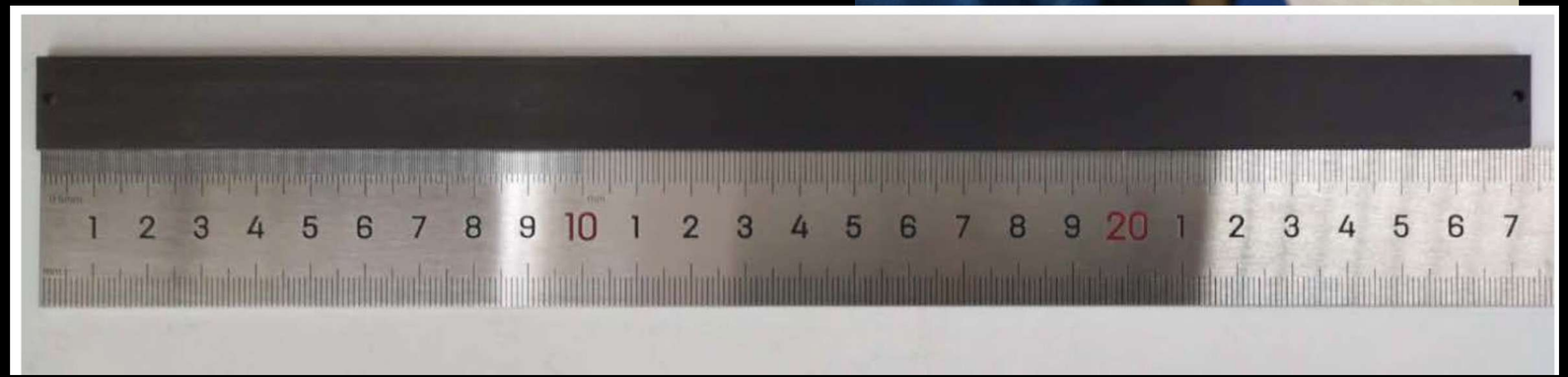
Backup: International collaboration

- **IFAE(Spain): very active in CMOS Sensor design and testing**
- Liverpool (UK): Tracker mechanical design,
- Oxford(UK): CMOS sensor design validation, thermal design
- RAL(UK): Pixel module design
- Queen Mary(UK): module mechanical design (Zero mass concept)
- Strasbourg (FR): CMOS sensor design, Tracker mechanical design
- University of Massachusetts (US): Tracker mechanical design, thermal design

In 2019, we have one engineer visited Oxford and Liverpool for 4 weeks, learned a lots about silicon.

Carbon fiber Support structure of the ladder

- Fabricated first support structure prototype of the ladder (IHEP designed)
  - **4 layer of carbon fiber, 0.12mm thick**
  - **Thinner than conventional carbon fiber**

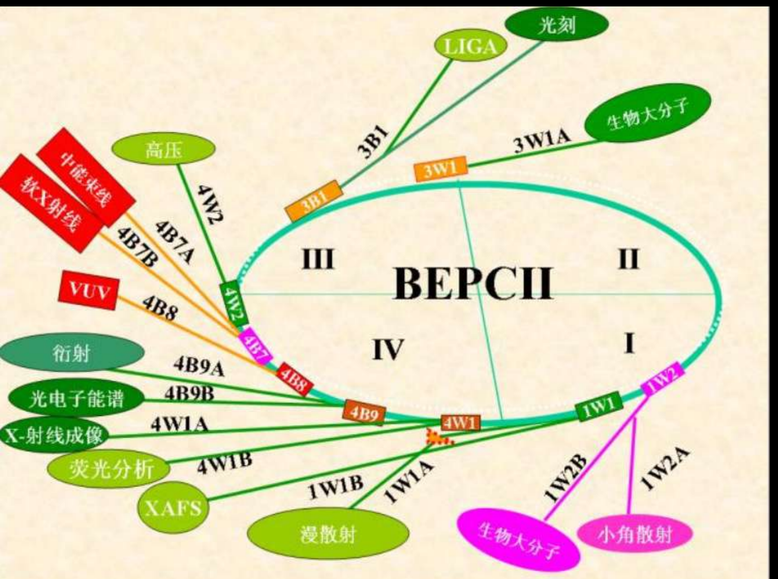


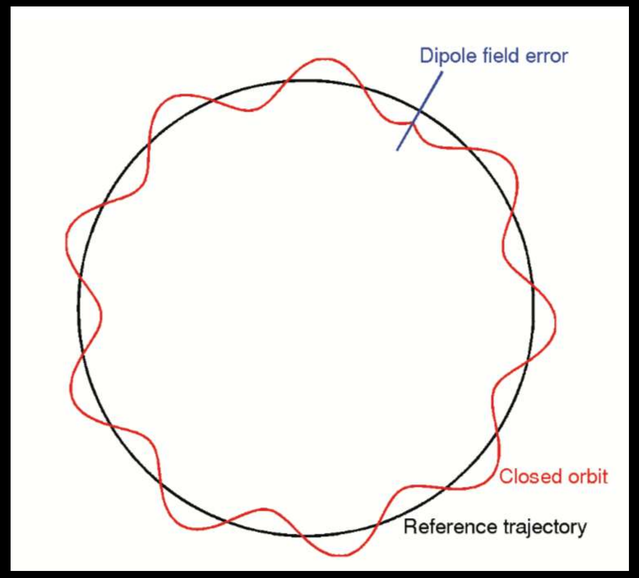
Plan for test beam (2)

New opportunity in Beijing Synchrotron Radiation Facility (BSRF)

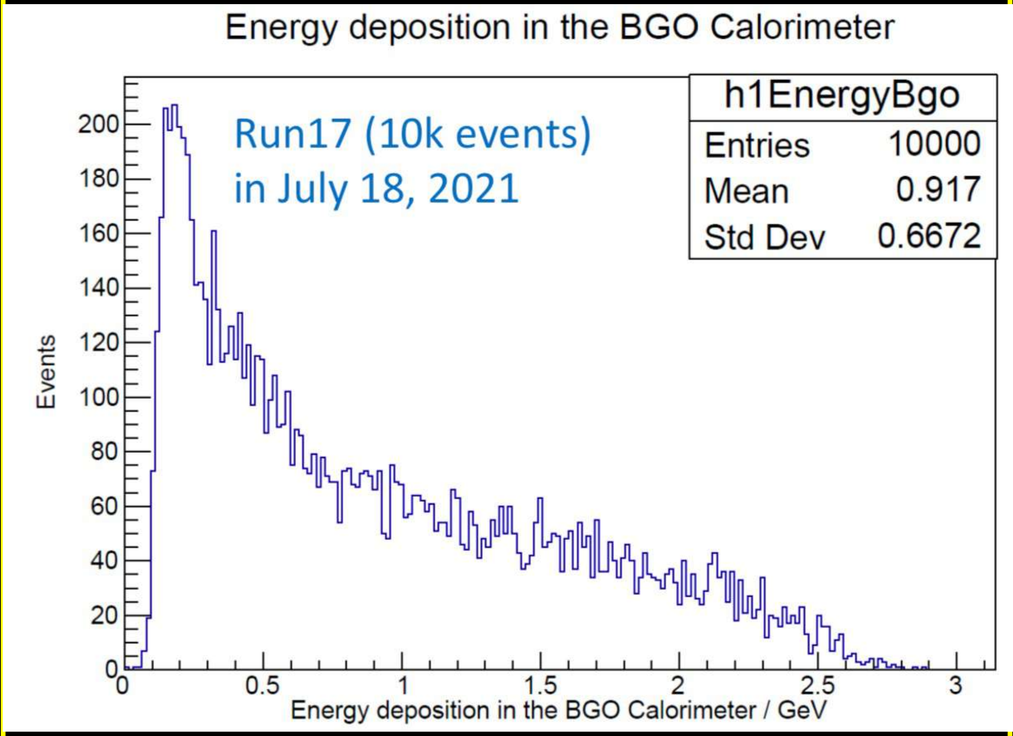
- **High energy electron (0.2~2.5 GeV) leakage from BEPC**
- **High trigger rate (up to 50Hz/cm^2)**
- **Need to filter low energy particles for vertex test beam**

	DESY	IHEP E3 beam	BSRF
Momentum	1-6 GeV	<1 GeV secondary beam	1~2.5 GeV
Particles	electrons	Protons/ Pions/ /Electrons	electrons
Trigger rate	4000 Hz/cm^2	0.6 Hz/cm^2	~50 Hz/cm^2



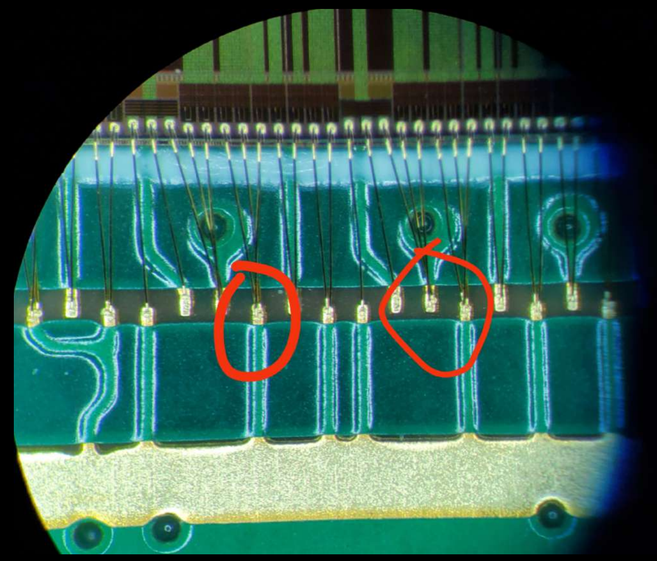


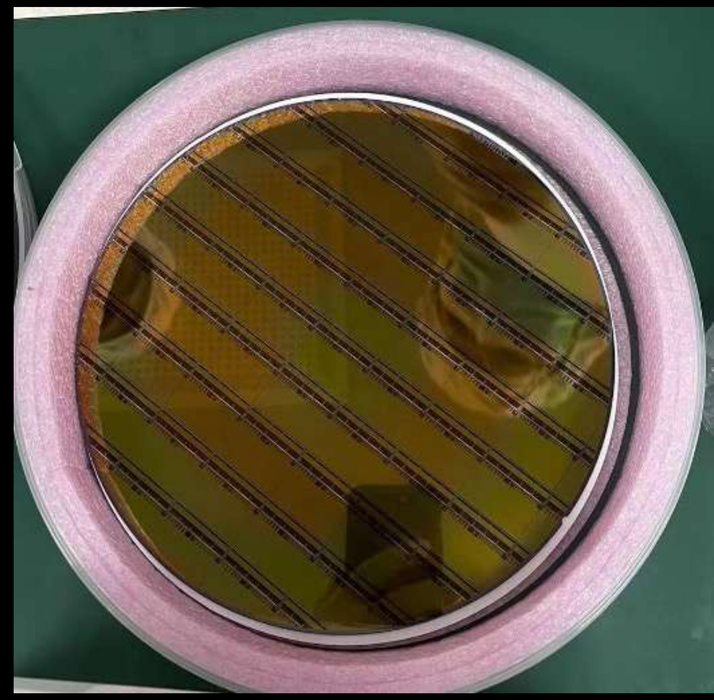
Energy spectrum measured by calorimeter (by Yong Liu)



News about Taichupix3 production

- 6 Taichu3 wafers are ready.
  - wafer arrival at IHEP in 5th July
  - 3 wafers (standard process) + 3 wafers (modified process)
    - After irradiation, modified process will give better resolution
    - Will modified process sensors into the detector assembly
- Send 1 wafers for thinning (150um) and dicing
  - Test single chip performance
  - Send 5 chips with PCB boards to company for wired bonding
    - 5 board bonded.
  - Wire bonding one PCB board at IHEP
  - Try to wire bonding one chip on flex at IHEP next week
- Send 3 wafers to NCAP for wafer testing , thinning and dicing

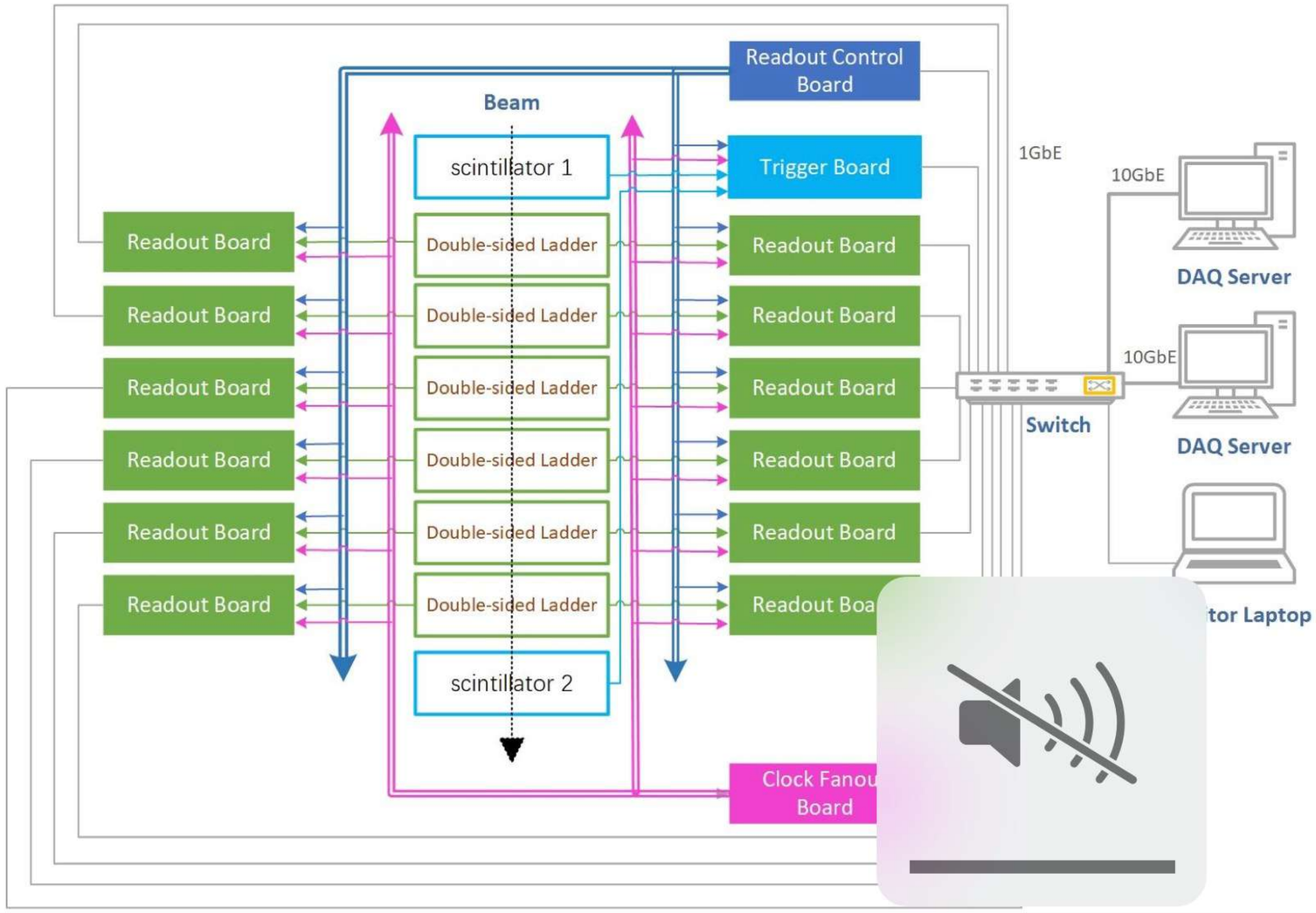




Backup: DAQ status

Design of DAQ

Hongyu Zhang



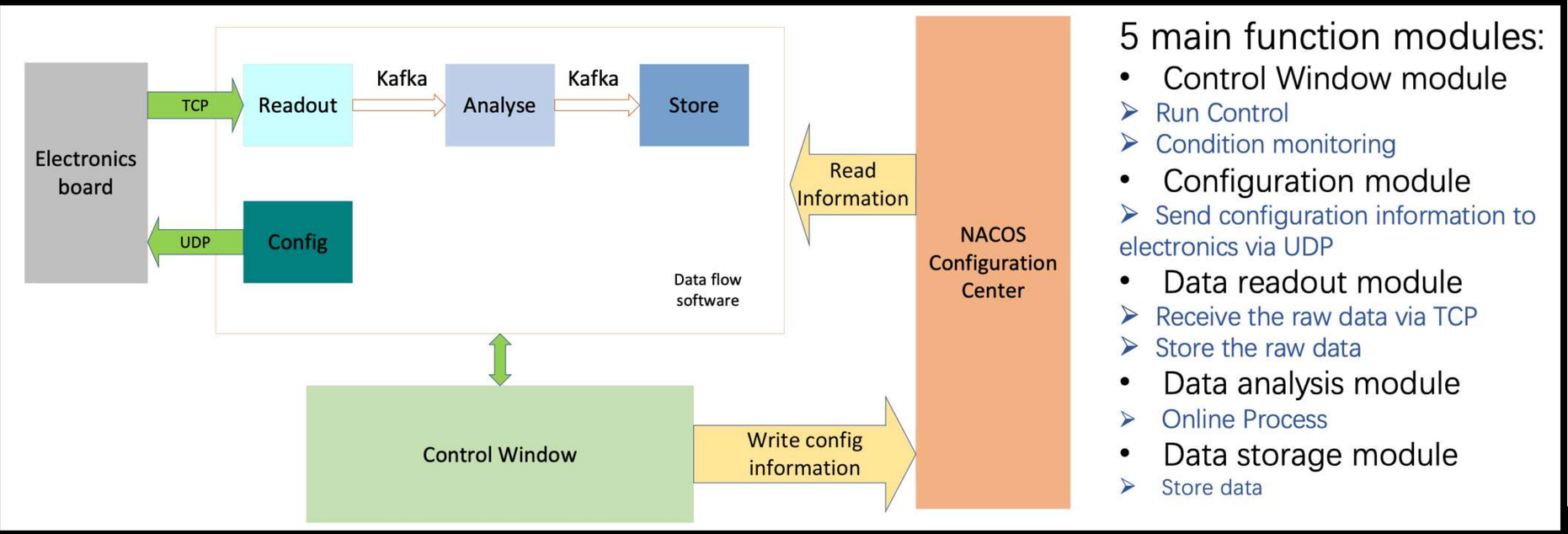
Front End Electronics:

- Readout Board: x12
  - Readout Ladder electronics data
- Clock Fan-out Board: x1
  - Fan-out common clock signal to each readout board
- Readout Control Board: x1
  - Fan-out common reset / common start / common stop signals to each readout board
  - Synchronize global timestamps of each readout board
- Trigger Board: x1
  - Provide timestamp of Scintillator trigger signal

DAQ Architecture development

- Try to config single chip test board and data handling with DAQ software (next step)
- Purchase 3 DAQ PC for data taking (next step)
- Parallel processing for each FPGA board
- Hit maps on-line monitoring

DAQ Architecture



5 main function modules:

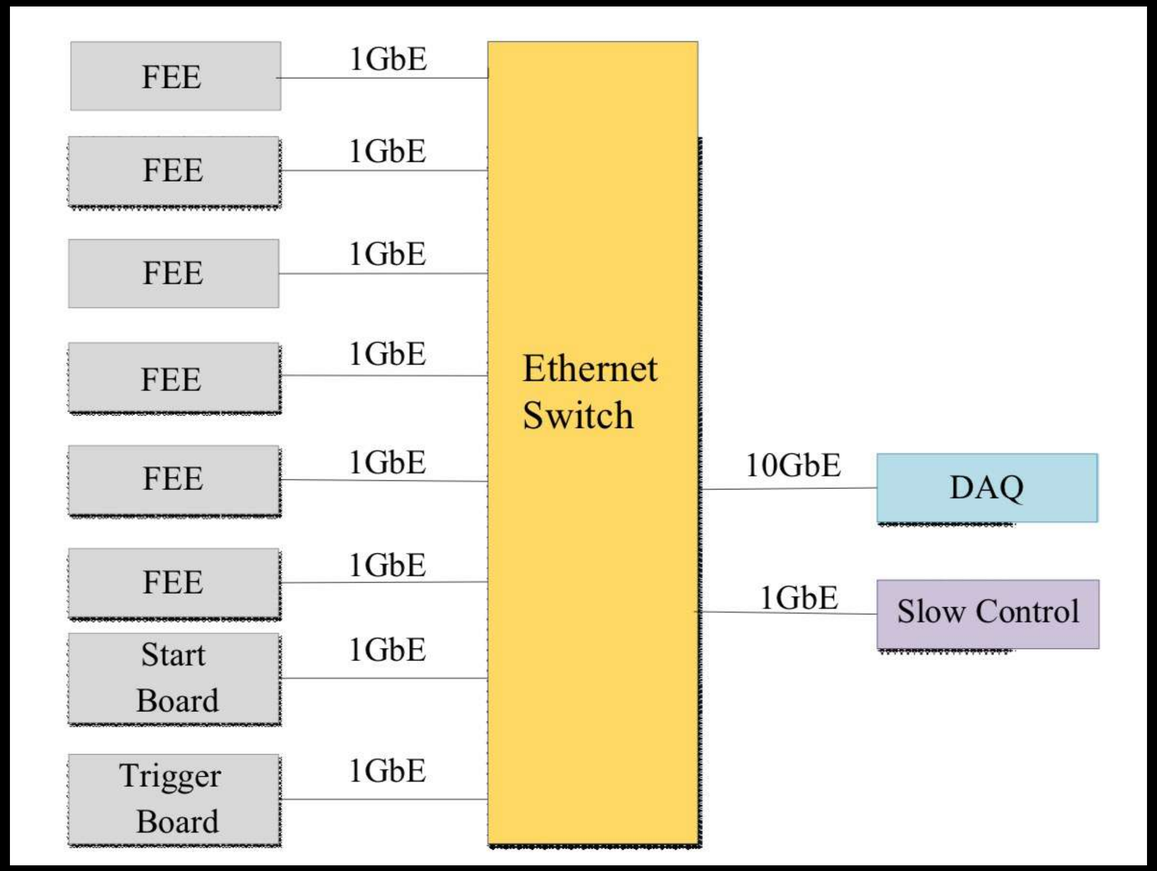
- Control Window module
  - Run Control
  - Condition monitoring
- Configuration module
  - Send configuration information to electronics via UDP
- Data readout module
  - Receive the raw data via TCP
  - Store the raw data
- Data analysis module
  - Online Process
- Data storage module
  - Store data

data structure

7 0
Package Header (0xaa)
Package Header (0xbb)
Hit_Num per package (0x10 or 0x40)
Header_id (8 or 16 bits)
...
Trigger_num (8 bits)
Chip Timestamp (8 bits)
FPGA Timestamp (Low 8 bits)
FPGA Timestamp (Middle 8 bits)
FPGA Timestamp (High 8 bits)
Addr_Dcol + Addr_row + Chip_id + Valid_flag (9 bits + 10 bits + 4 bits + 1 bit = 24 bits)
...
Package Trailer (0xcc)
Package Trailer (0xdd)
Byte count
Error coding
...

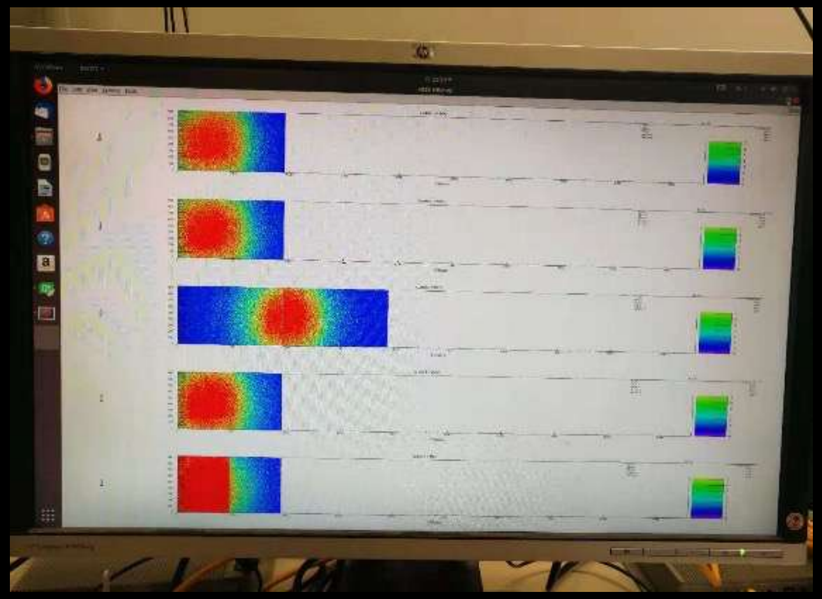
Data acquisition system

- Preliminary design of data acquisition system(DAQ)
  - Ladders are reader by readout boards
  - All readout boards connected to computer through a switch
  - User interface developed
  - DAQ tested in five modules equipped with MIMOSA sensors

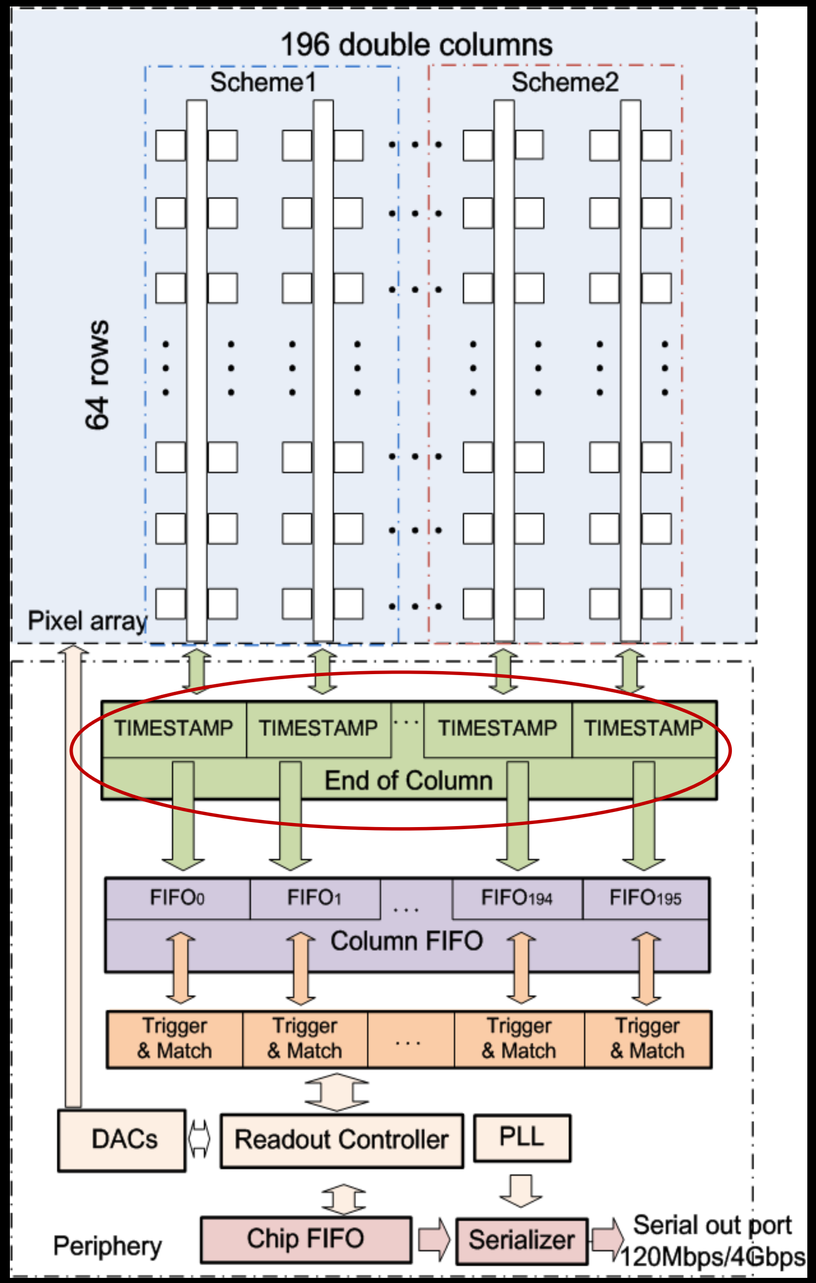


DAQ Tests with 5 MIMOSA chips

DAQ system data display
Tested with MIMOSA modules



New proposed readout architecture in TaichuPix

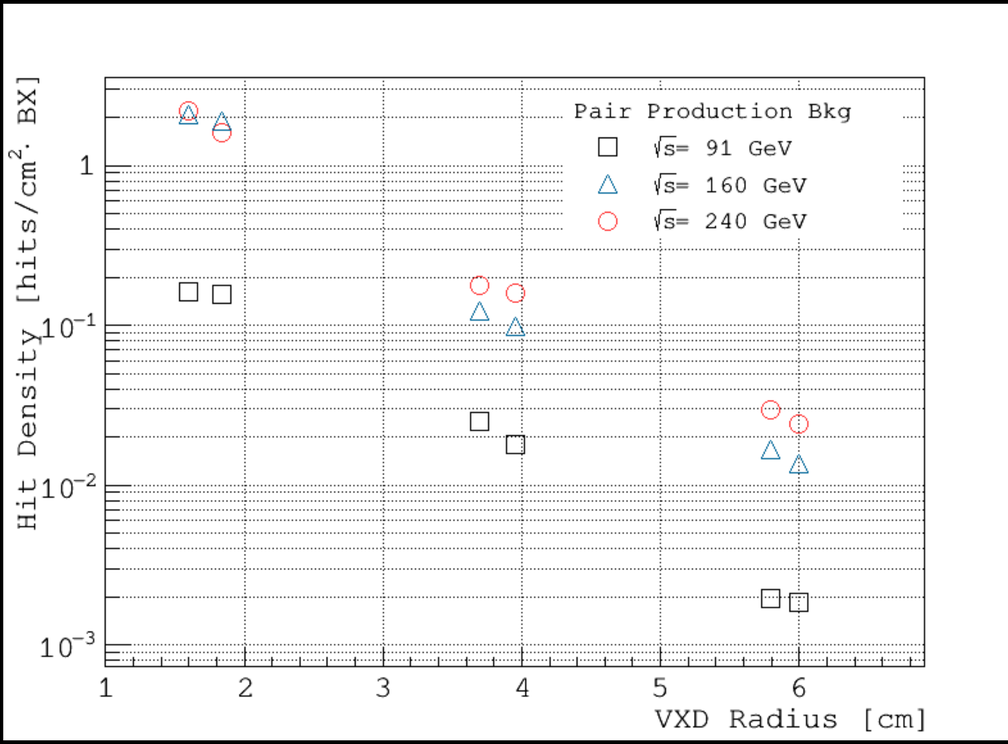


- New readout architecture
- → reduce power consumption and reduce pixel size
- CEPC readout time requirement:
  - <500ns deadtime @40MHZ(Z pole)

- Taichu-1 Column-drain readout
  - Priority based data driven readout; time stamp at EOC
  - Dead time: 2 CLK for each pixel (50ns @40MHz CLK)
  - Two digital pixel designs: FEI3-like and ALPIDE-like design
- 2-level FIFO architecture
  - L1: column level, to de-randomize injecting charge
  - L2: chip level, to match in/out data rate between core and interface
- Trigger readout:
  - Coincidence by time stamp, matched event read out

Main specs of the full size chip for high rate vertex detector

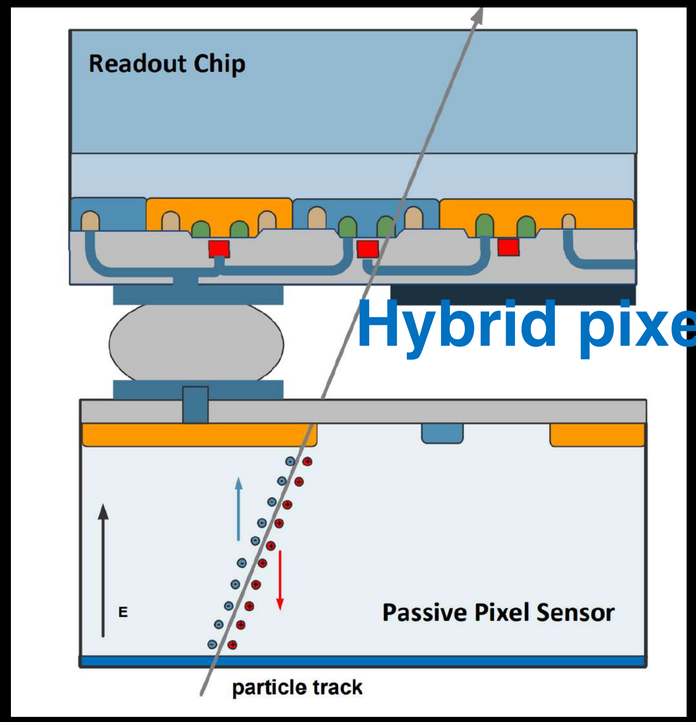
- Bunch spacing
  - CEPC Z+Higgs (240GeV): 680ns;
  - WW threshold scan (160GeV): 210ns;
  - CEPC Z pole runing (90GeV) Z: 25ns
- High Hit density
  - 2.5hits/bunch/cm^2 for Higgs/WW runs
  - 0.2hits/bunch/cm^2 for Z pole running

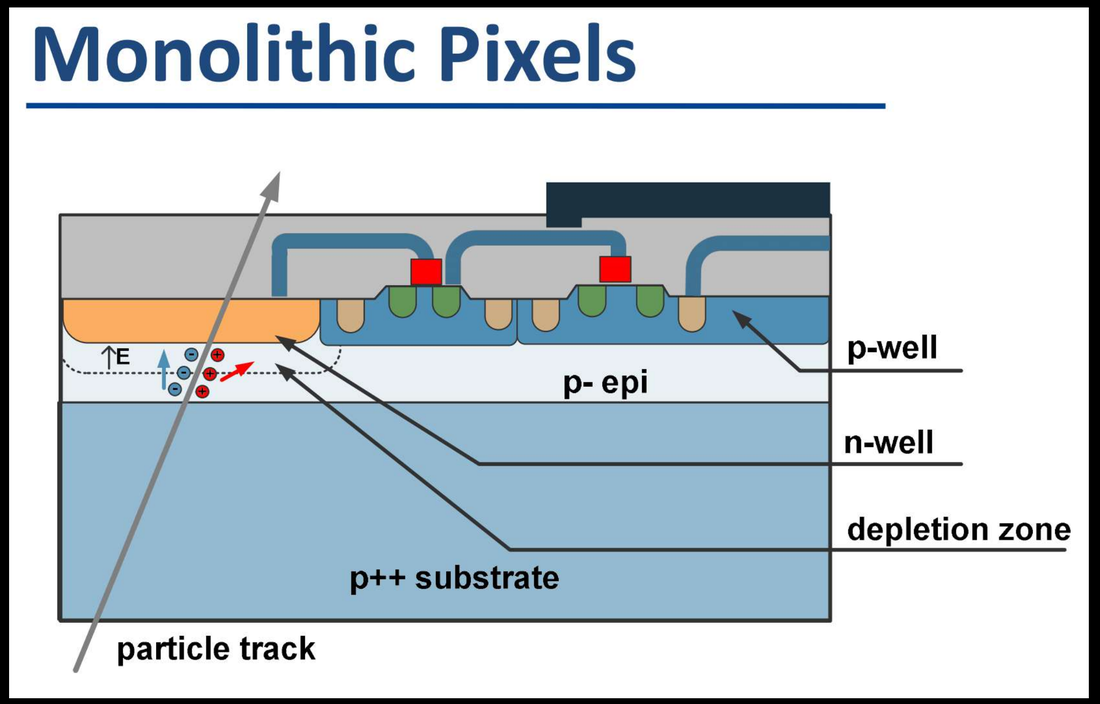


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

CMOS Monolithic pixel sensor

- CMOS Monolithic pixel (CIS process) is ideal for CEPC application
  - low material budget (can be thin down to 50μm)
  - This project use TowerJazz CIS 180nm technology
- Hybrid pixel technology developed by ATLAS and CMS
  - Thickness of sensor is about 200~300 μm
  - Need to bump bonding with readout ASIC (ASIC thickness is about 300μm)
  - Material budget about silicon sensor is about 10 times larger than CIS process

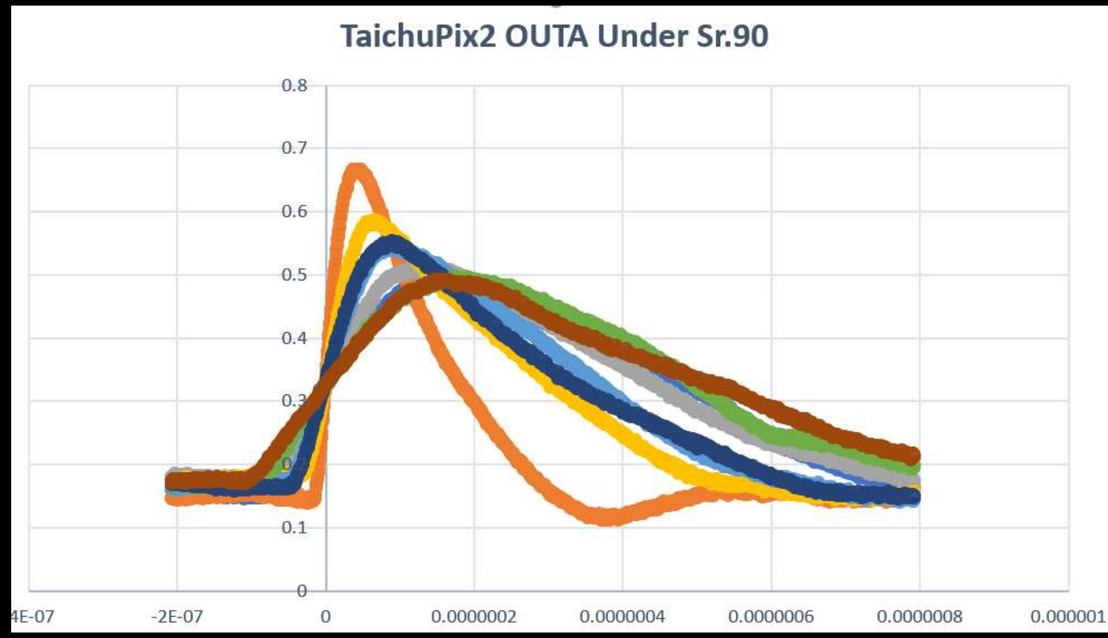


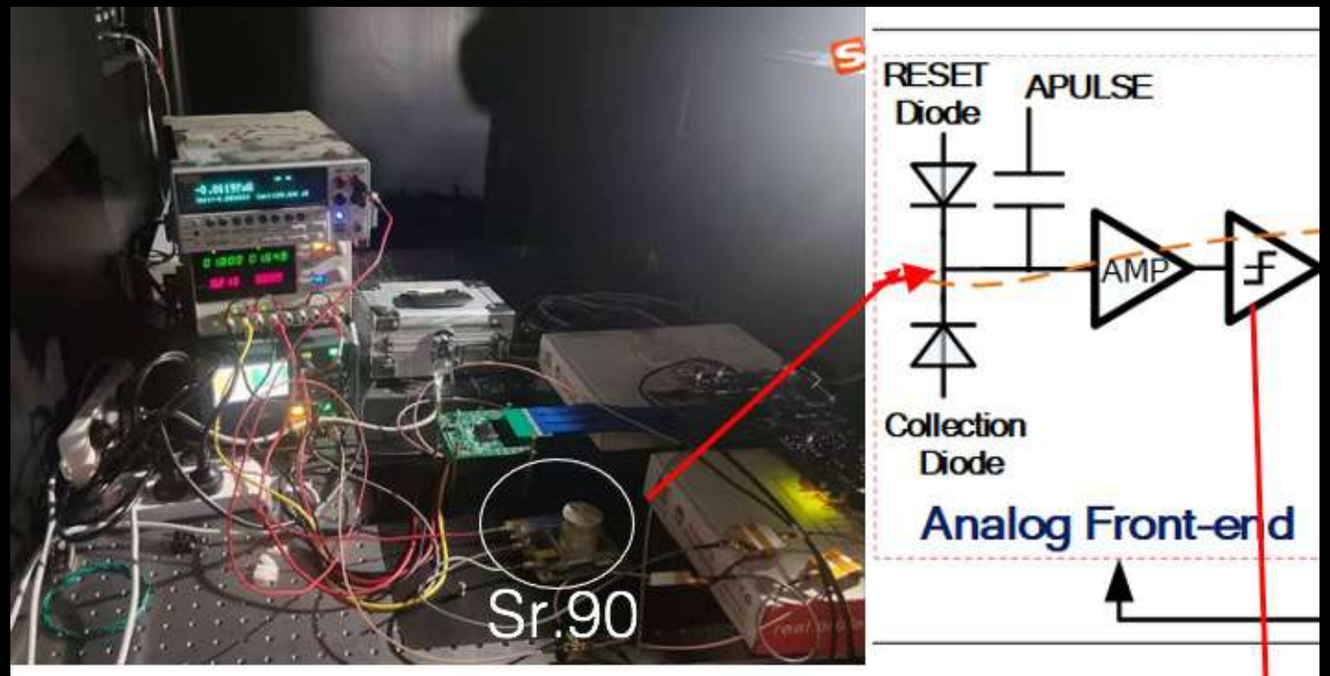


TaichuPix2 test with ^{90}Sr source

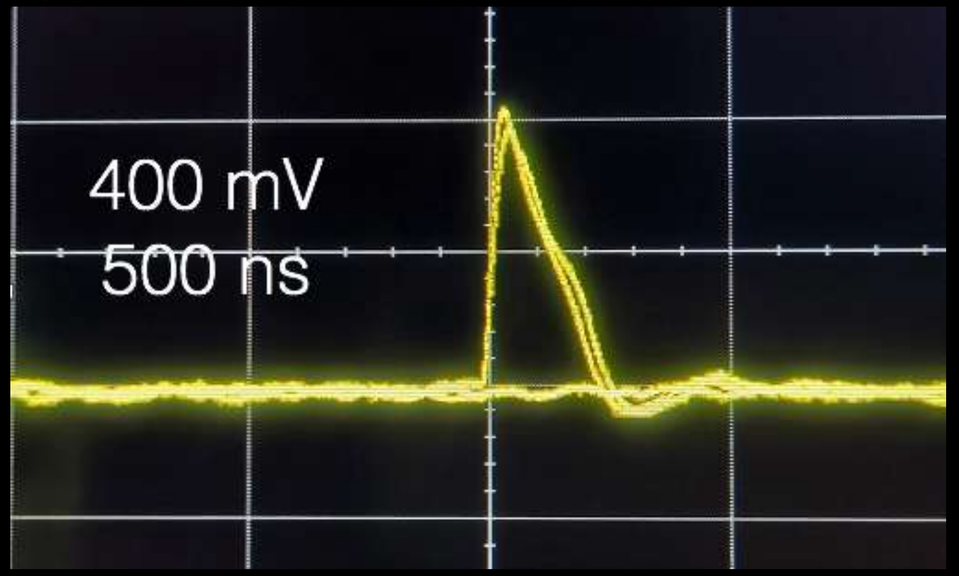
- Digital readout (full chip)
- Analog readout (debug mode for one row of pixel)
  - High signal to noise ratio found in analog readout
- More studies are on-going

Analog waveform in beta tests





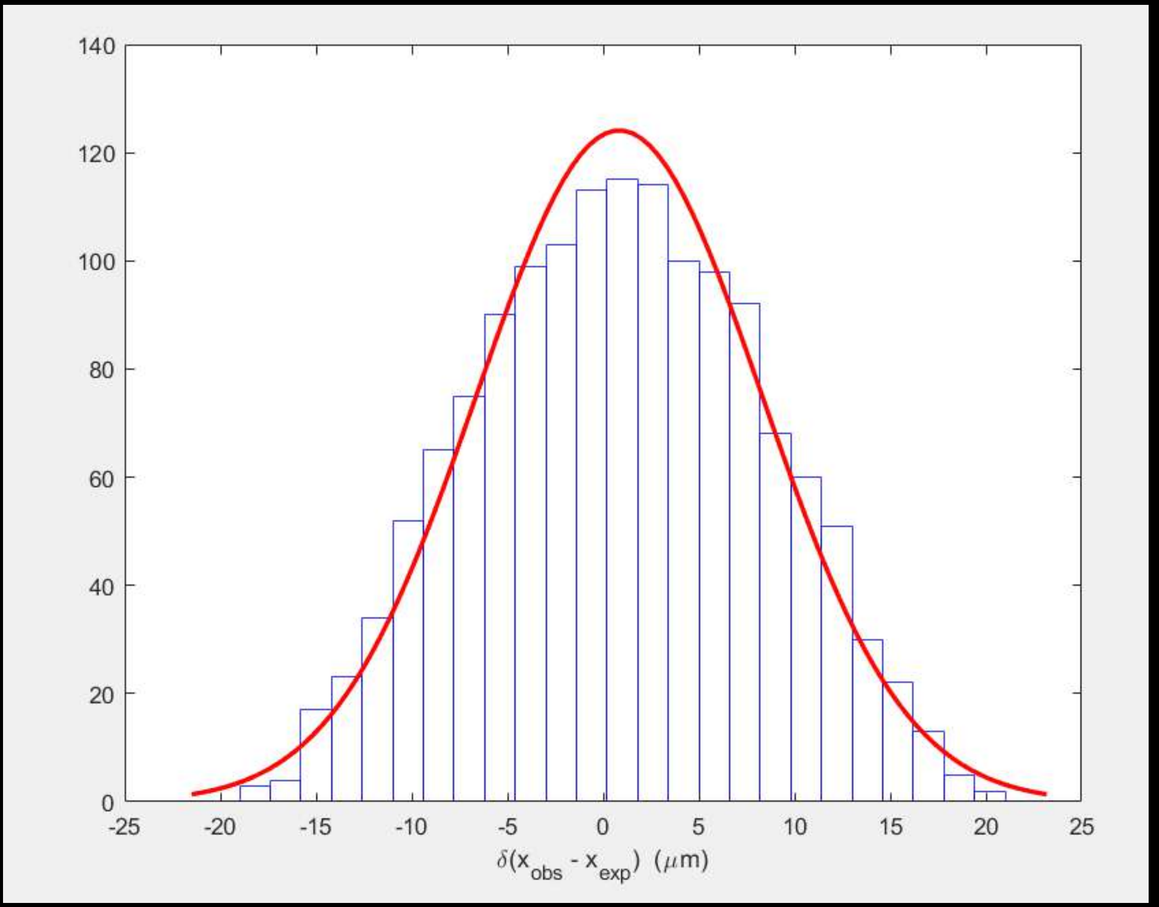
typical waveform in beta tests



Spatial resolution study with laser

- Spatial resolution is measured with laser scan with X-Y-Z stage.
  - Consistent with expected resolution : pixel size (25μm) divided by $\sqrt{12}$~ 7 μm
  - Plan to lower the threshold, increase charge sharing to reach 5 μm resolution

TaichuPix Spatial resolution with high threshold: σ~5-7μm



Alice ALPIDE chip: resolution vs threshold

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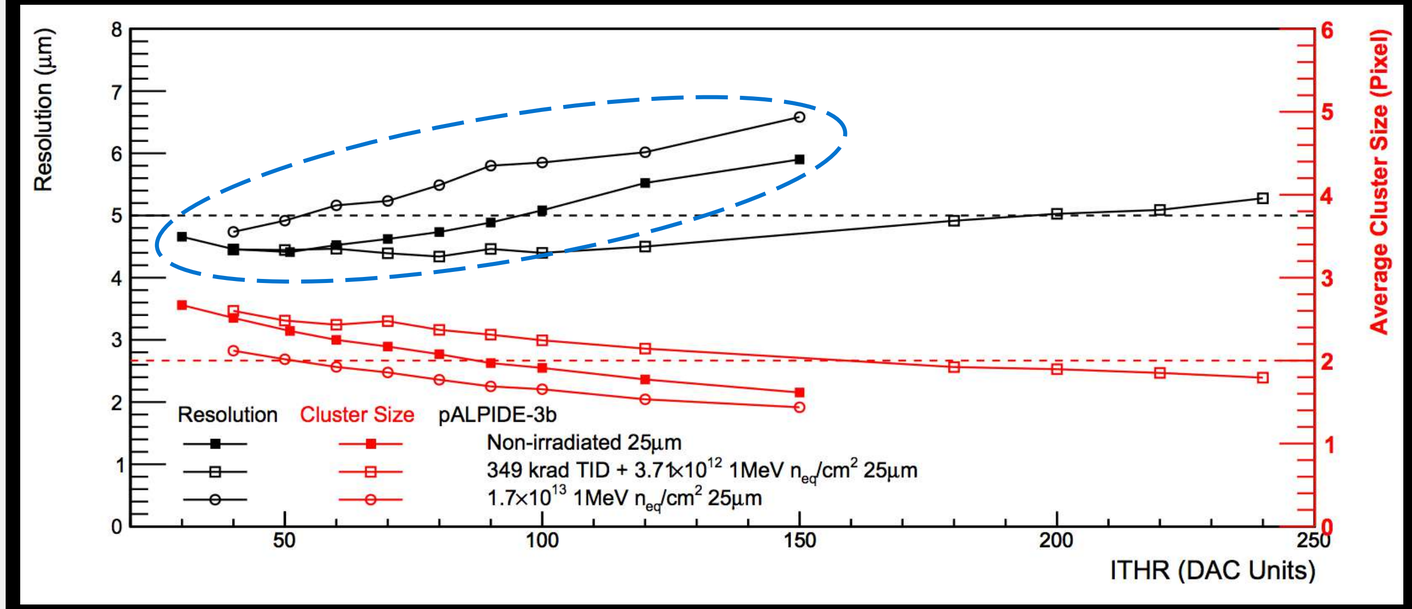
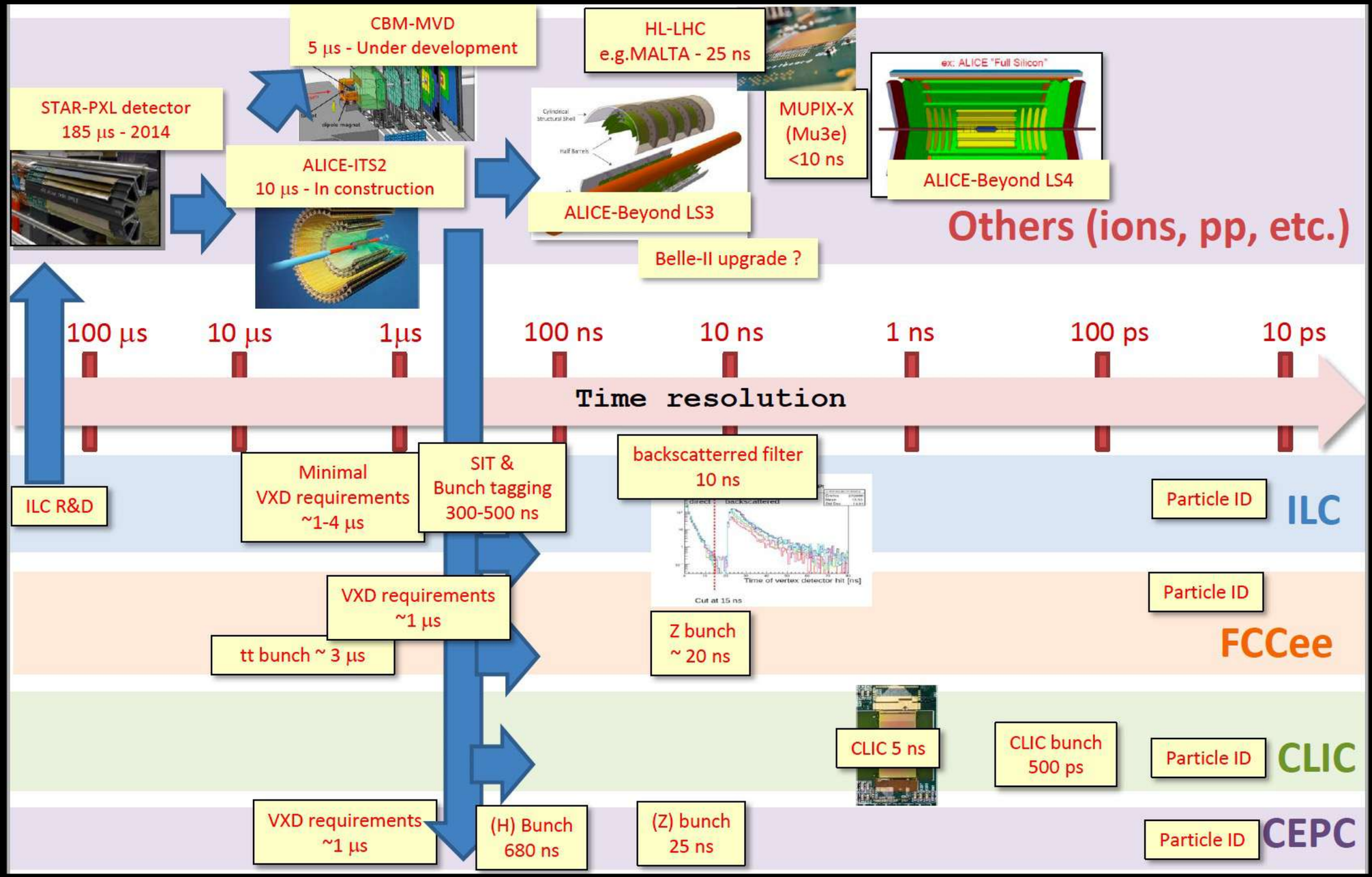


Timing for lepton collider detector



Tooling Design for Barrels Assembling

- 3 sets of tooling for 3 layer of barrel assembling.
- Tooling and special tool for inner and middle barrels assembling.