Development of JadePix-3 telescope for beam test

Sheng Dong[1], Yunpeng Lu[1], Hulin Wang[2], Qun Ouyang[1]

1 Institute of High Energy Physics, CAS

2 Central Normal University of China

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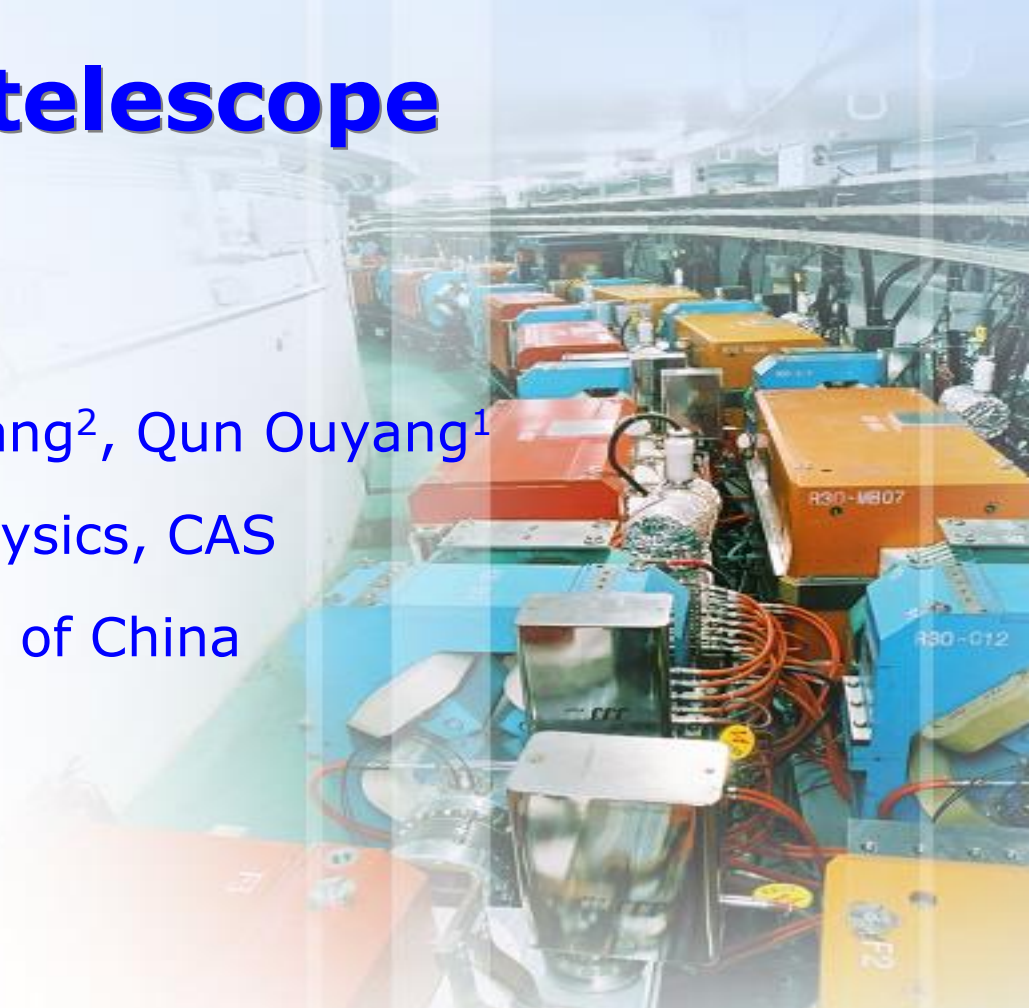
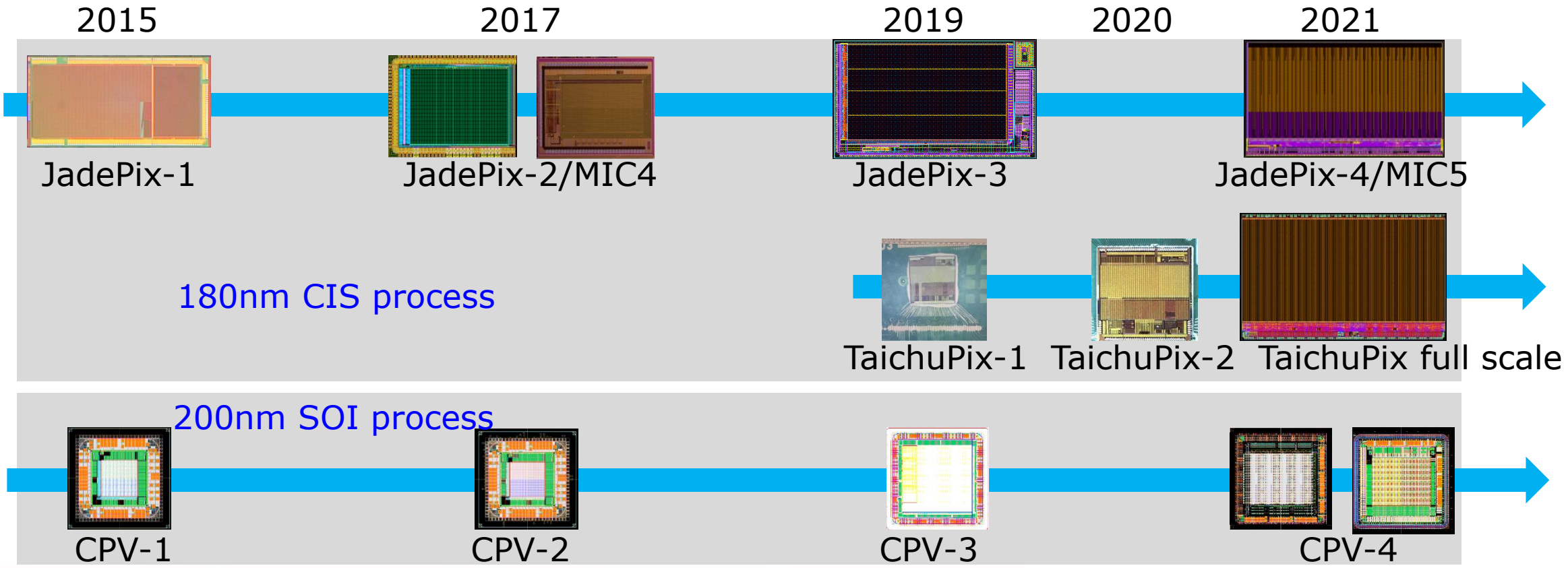


Outline

- Review on JadePix-3 CMOS Pixel Sensor
- Prototype of beam test telescope
- Initial test with cosmic rays
- Next plan

R&D of silicon pixel sensor for Vertex (in China)

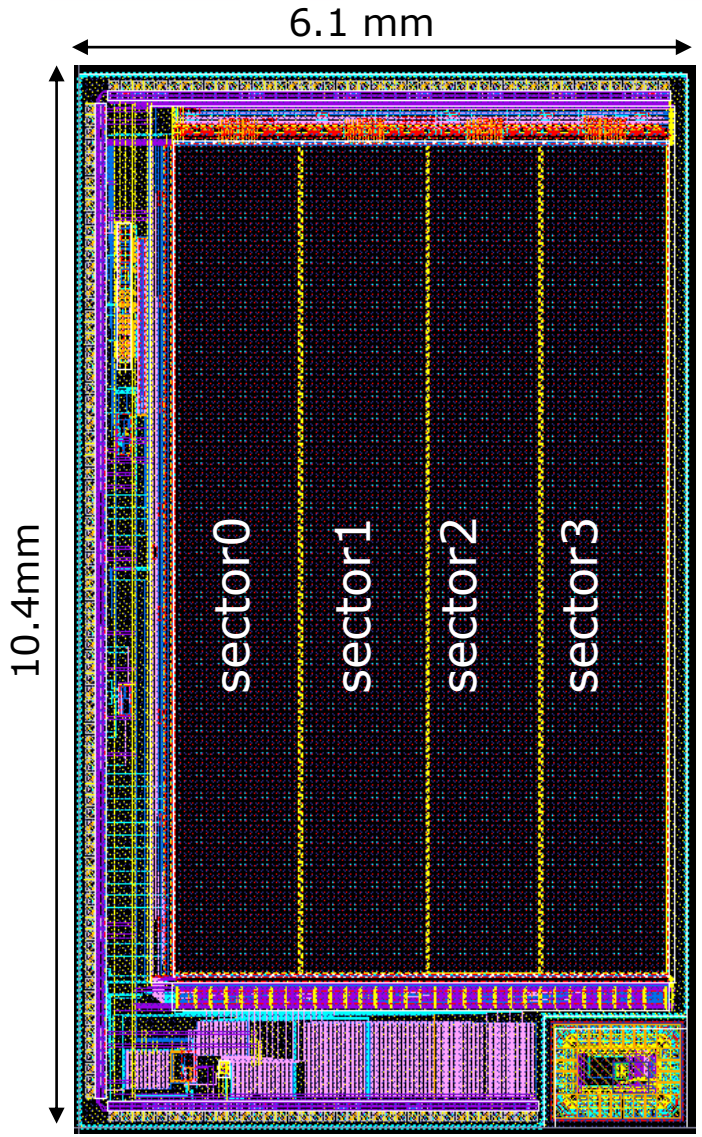
- Targeted on high resolution, low power and fast readout.
  - JadePix and TaichuPix on 180 nm CIS process
  - CPV on 200 nm SOI process



JadePix-3, a major effort on CMOS pixel sensor

- Technological preparation
  - JadePix-1 on the TowerJazz CIS process
  - JadePix-2 and MIC4 on the design schemes
- Collaborative design of a large team
  - Over 10 participants from IHEP, CCNU, SDU, Dalian Minzu U.
- Test work lasted for 1.5 years to fully characterize the chips
  - Highly required expertise on both sensor and electronics
- Highlighted as the achievements of MOST1 project

The pixel matrix of JadePix-3

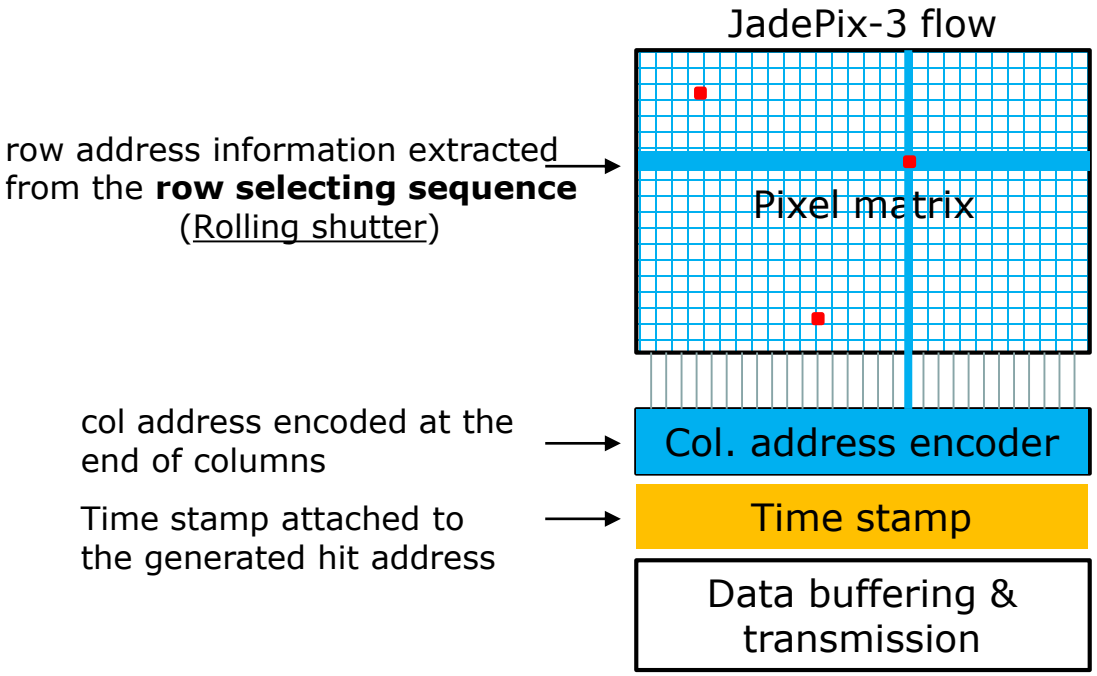


- **Full-sized** in the φ direction
  - Matrix coverage: 16 μm × 512 rows = 8.2 mm
- **Rolling shutter** to avoid heavy logic and routing in the column-wise
  - Minimum pixel size: **16 μm × 23.11 μm**
  - Matrix readout time: 512 rows × 192ns/row = **98.3 μs/frame**
- 4 parallel sectors, **scalable**
  - 48 columns/sector × 4 = 192 columns

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

Hit processing flow in JadePix-3

- Row address extracted from the **row selecting sequence** (Rolling shutter)
- Column address with HIT encoded at the bottom of matrix
- Time stamp attached to the HIT address
  - In the form of frame number



<Format of data frame>

Head: Buffer status

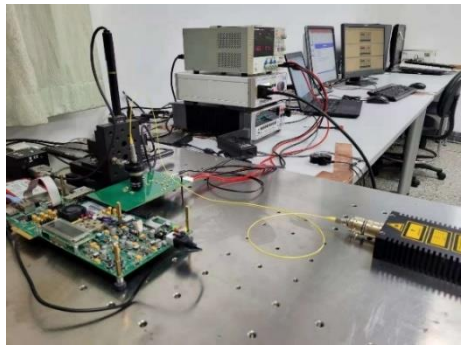
Data: HIT address 1
Data: HIT address 2
Data: HIT address 3

Tail: Frame number

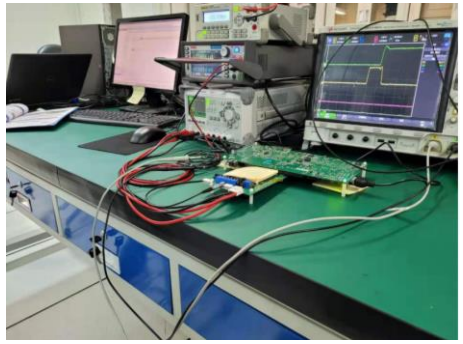
Test system for single chip

- General-purpose FPGA platform, KC705
  - Well-defined **FPGA firmware**
  - Debugged **Interactively** with the JadePix3 chips
- 4 test setup deployed in IHEP, CCNU, USTC, JLU

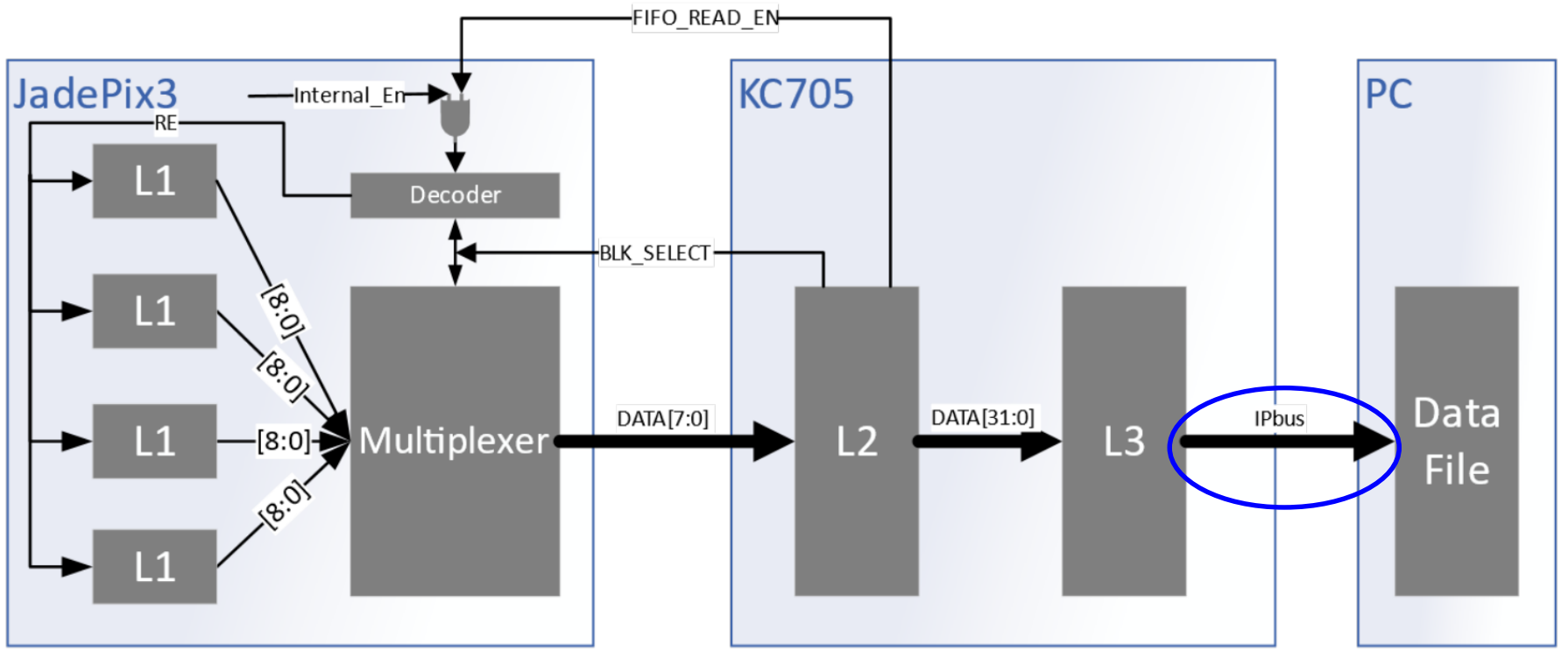
In IHEP Lab



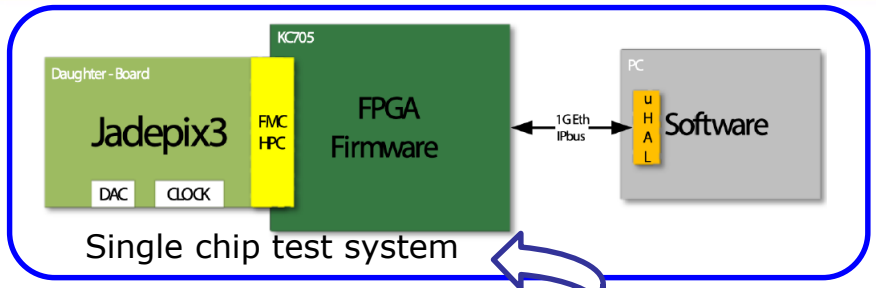
In CCNU Lab



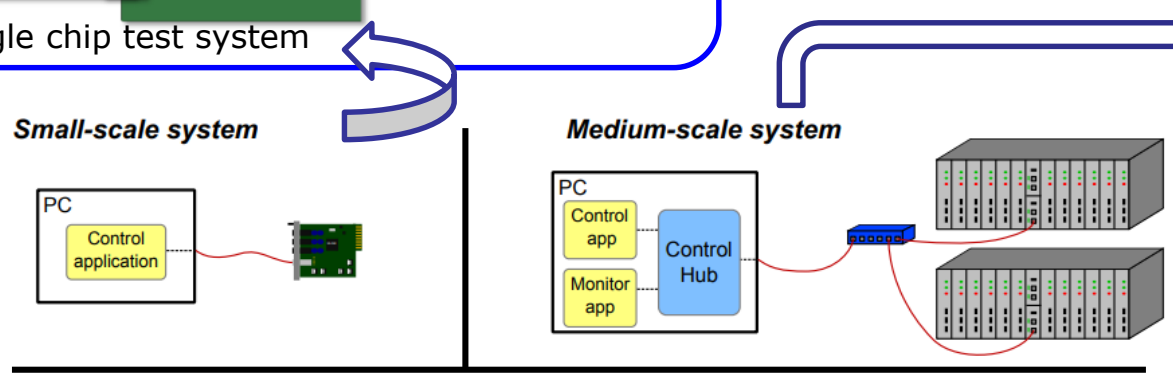
- **IPBUS protocol**
  - Reliable high-performance **control link** for particle physics electronics
  - **JUMBO PACKAGE feature** developed to boost the payload data rate up to 750 Mbps

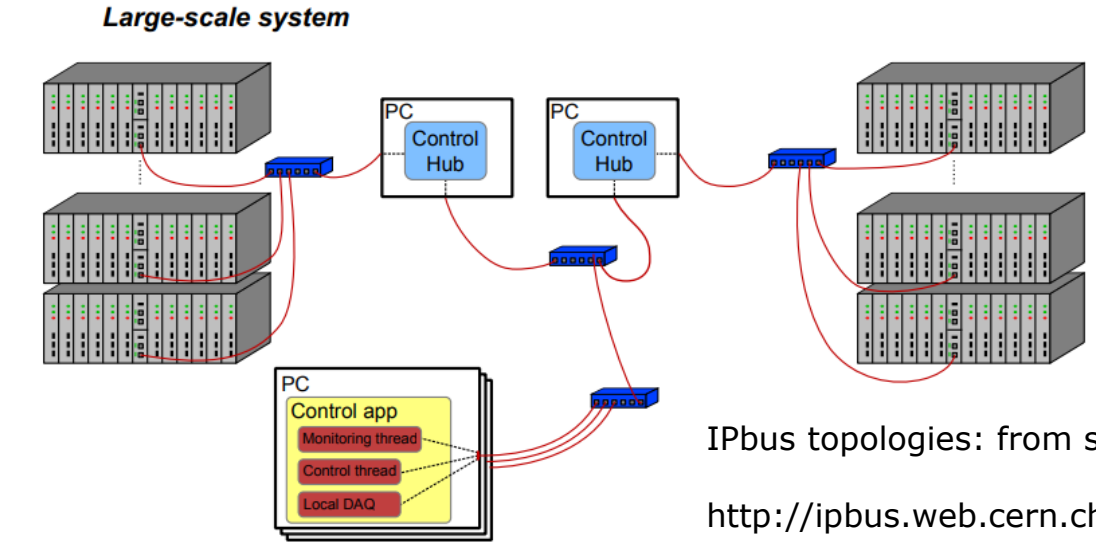


IPBUS: a flexible Ethernet-based control system



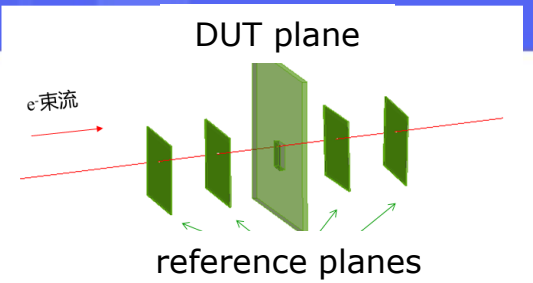
Single chip test system

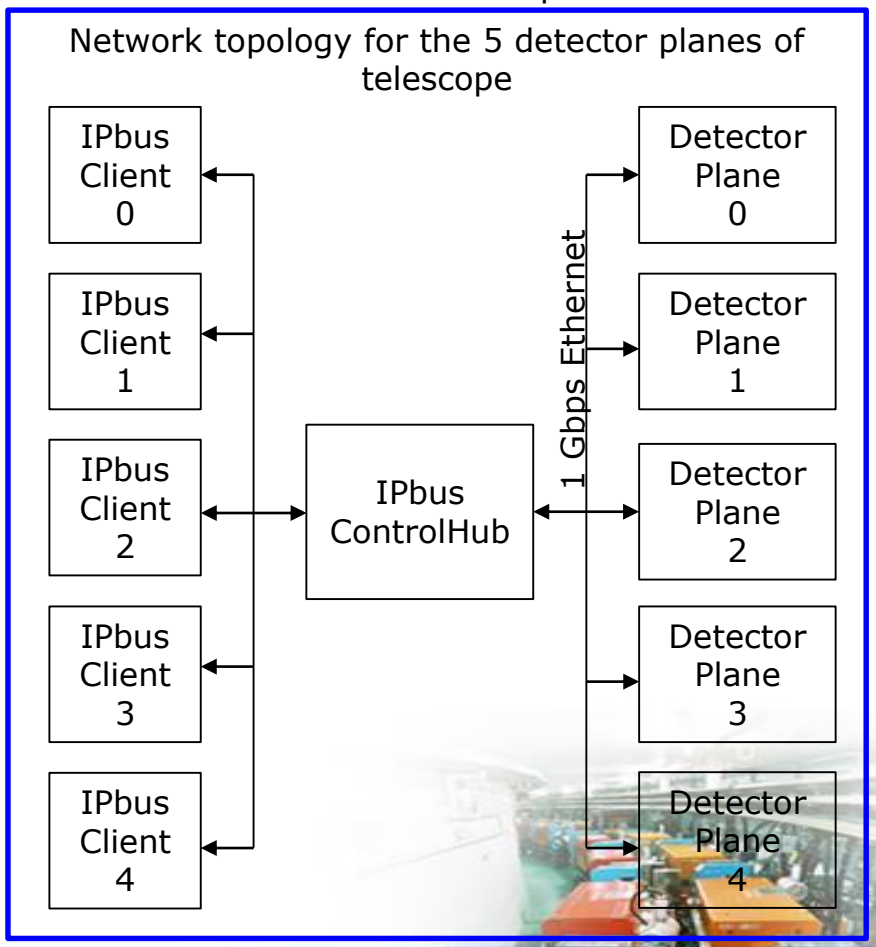




IPbus topologies: from small to large scale

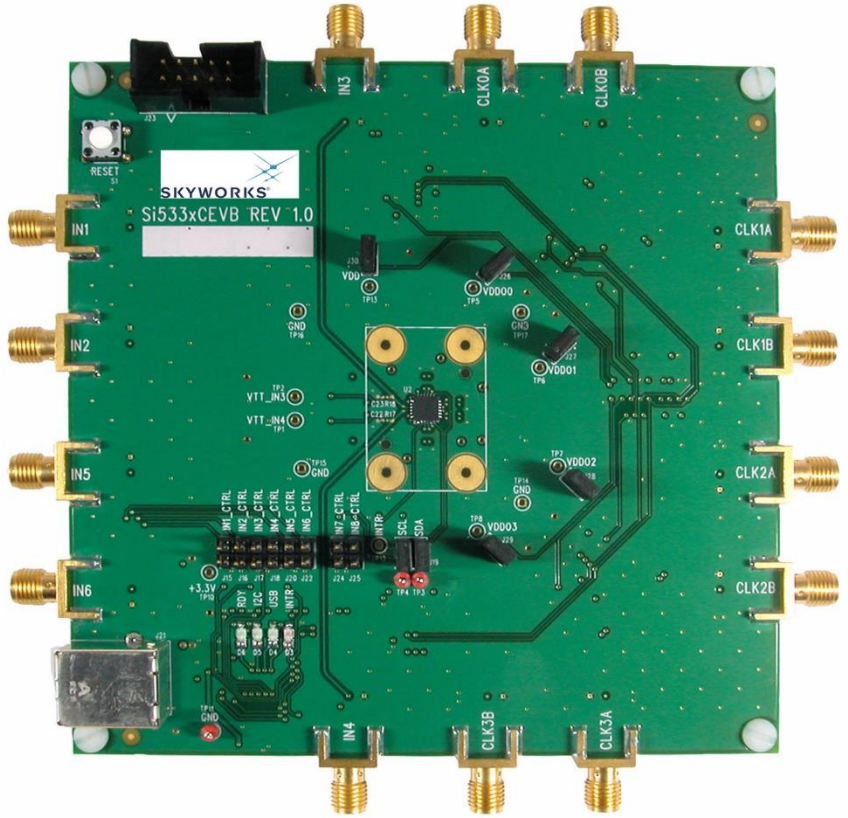
http://ipbus.web.cern.ch/ipbus/introduction/

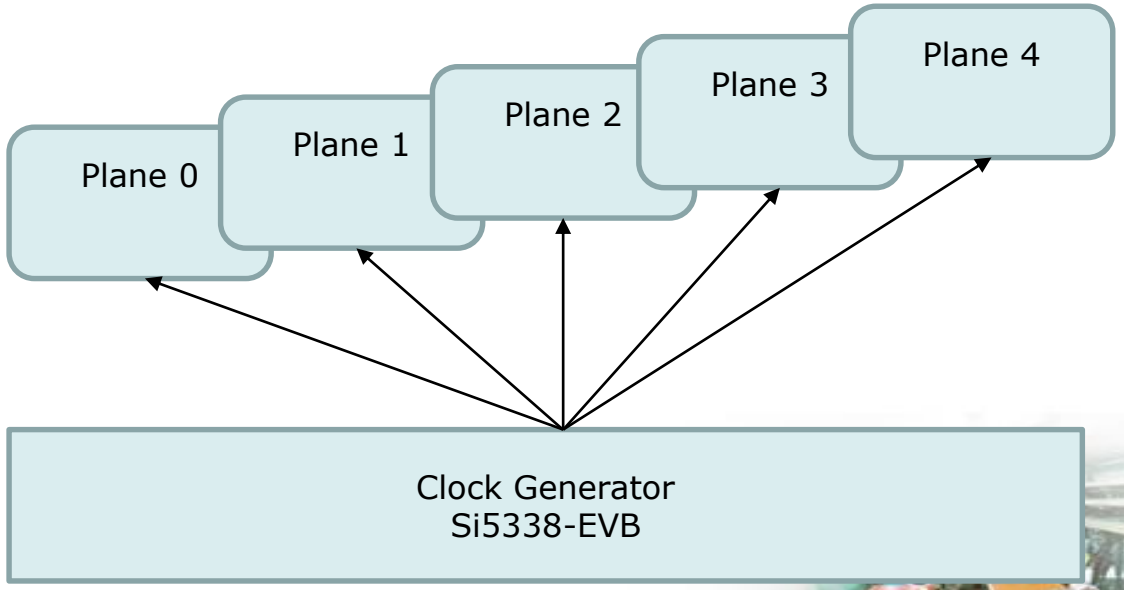




Distribution of System Clock

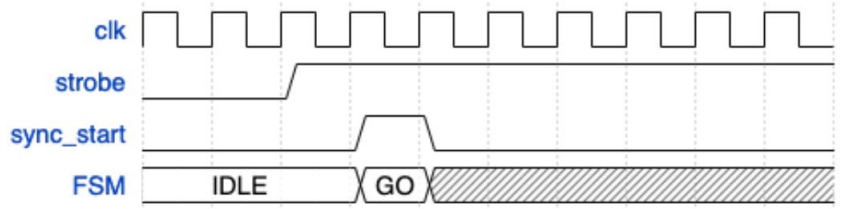
- System clock fanned out from a Si5338 board to all the detector planes
  - 200 MHz, differential pairs
  - Clock source for the rolling shutter scan
  - Commercially available

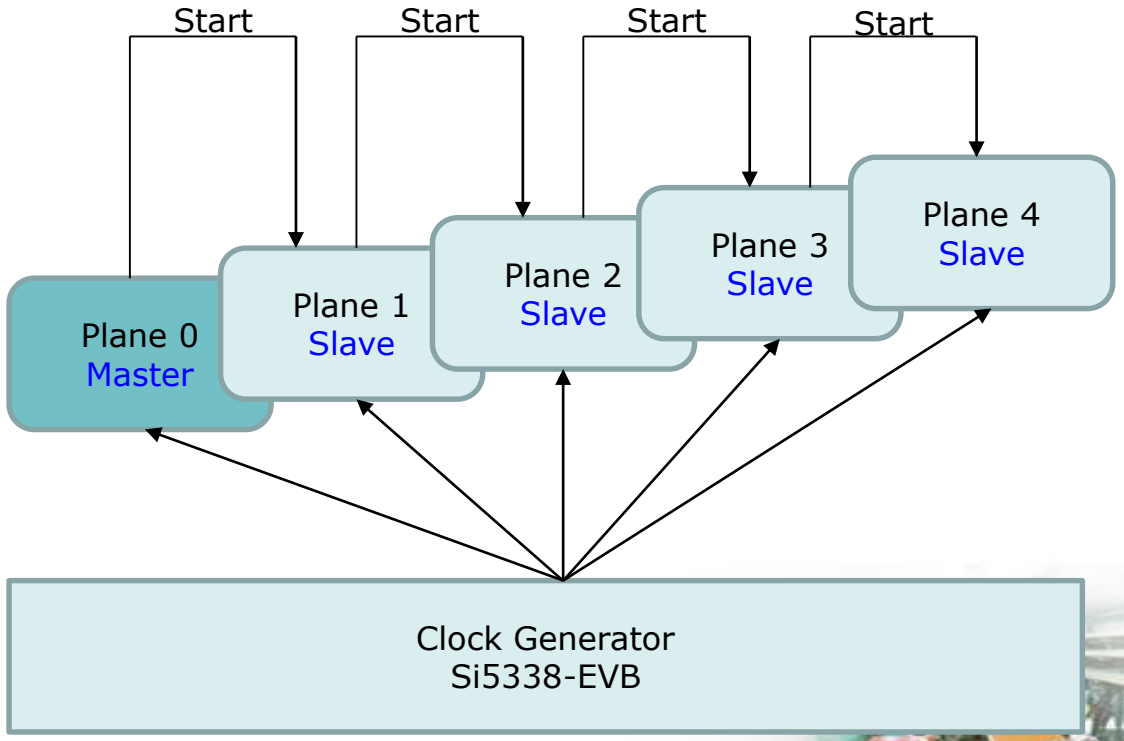




Synchronization of Start Up

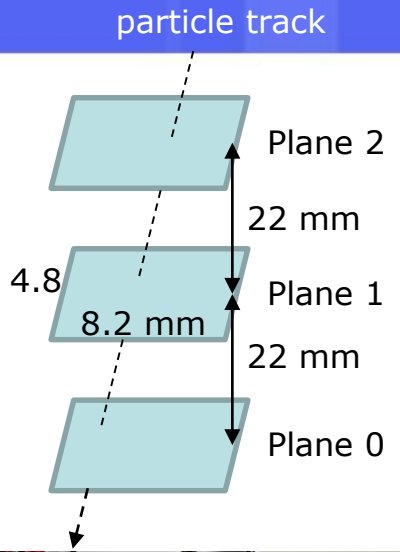
- Plane 0 configured as Master
  - Convert a software start to a hard-wired signal
- Start from plane 0 to plane 4 via a daisy chain
  - Rolling shutter scan synchronized
  - **Data from different planes correlated by their frame number**

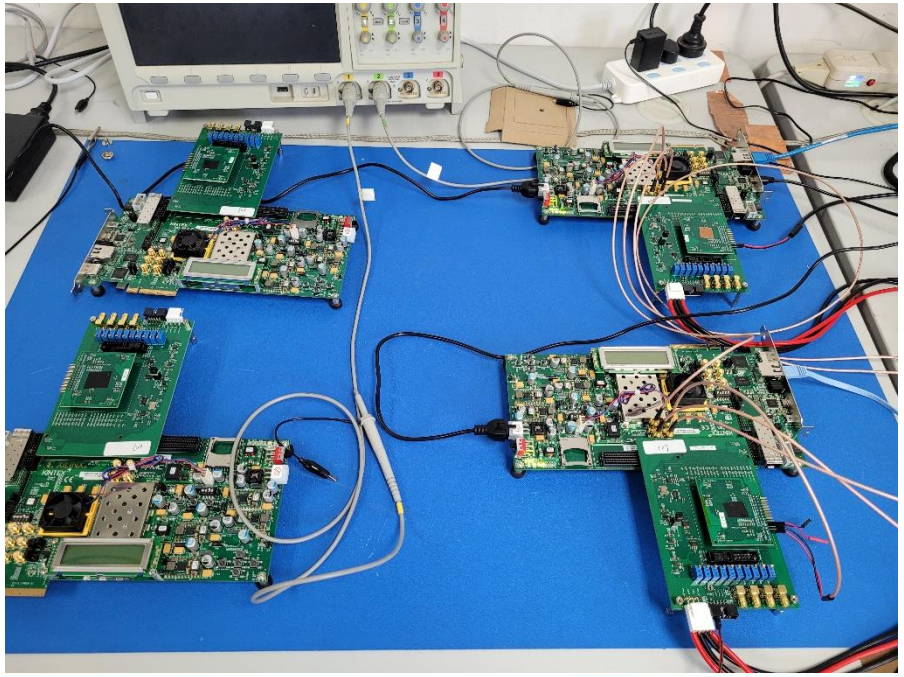


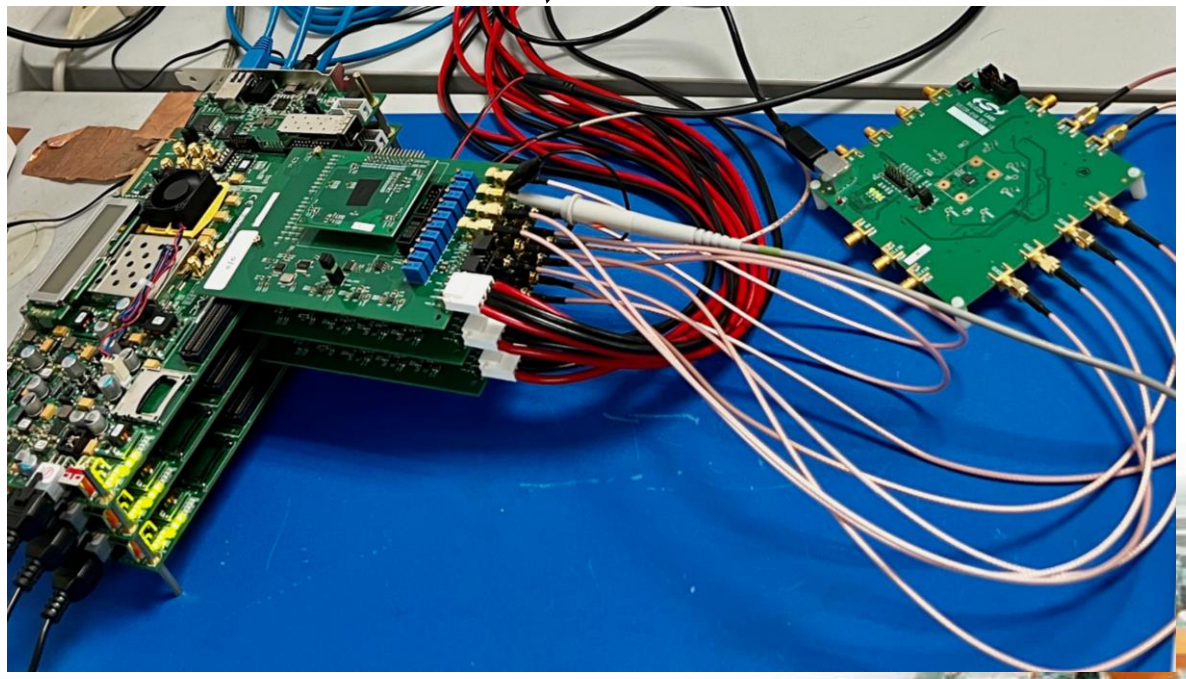


Hardware

- 5 detector planes prepared.
- 3 detector planes assembled for debugging
  - Sensitive area 8.2 mm * 4.8 mm
  - Detector plane spaced 22 mm

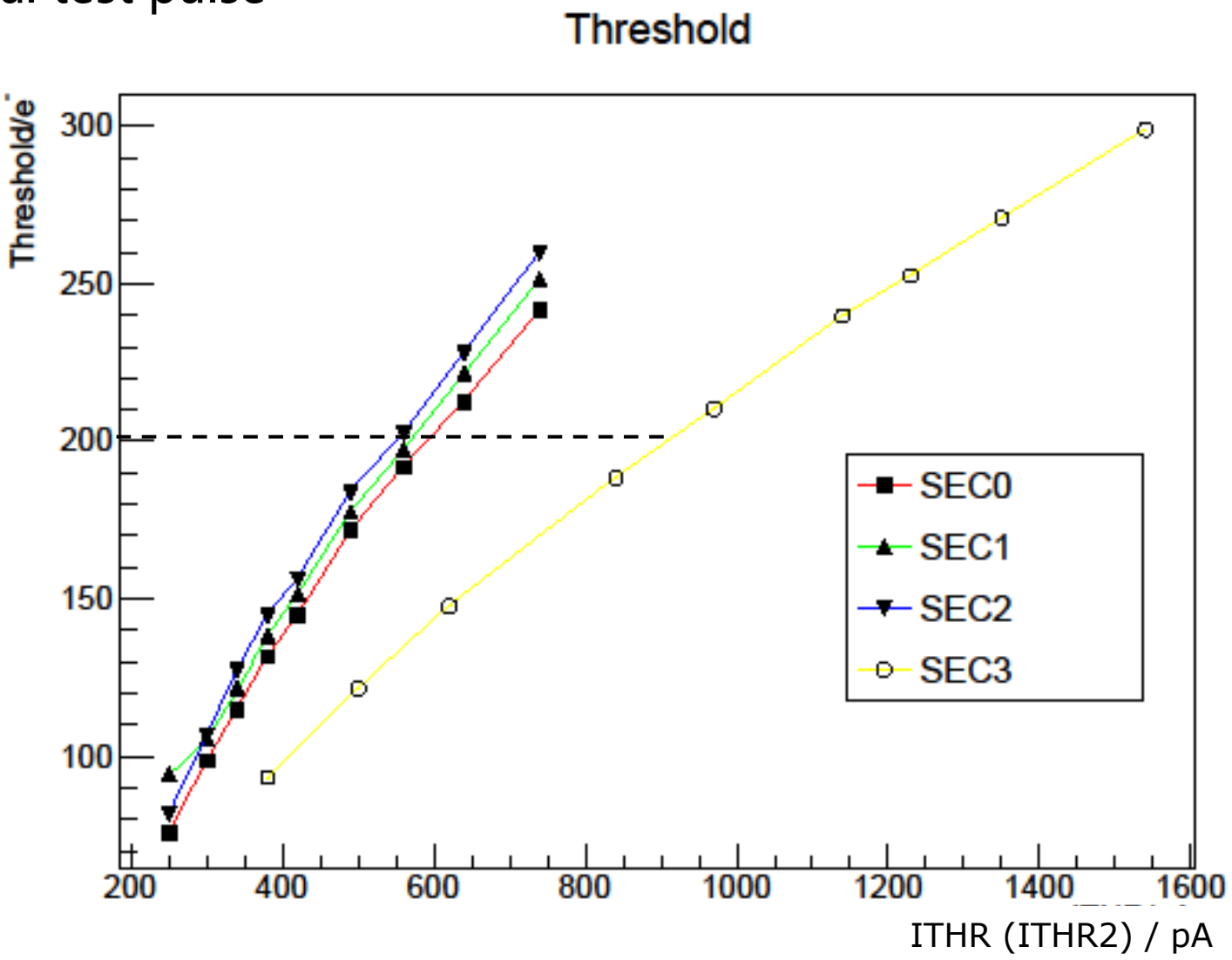






Threshold

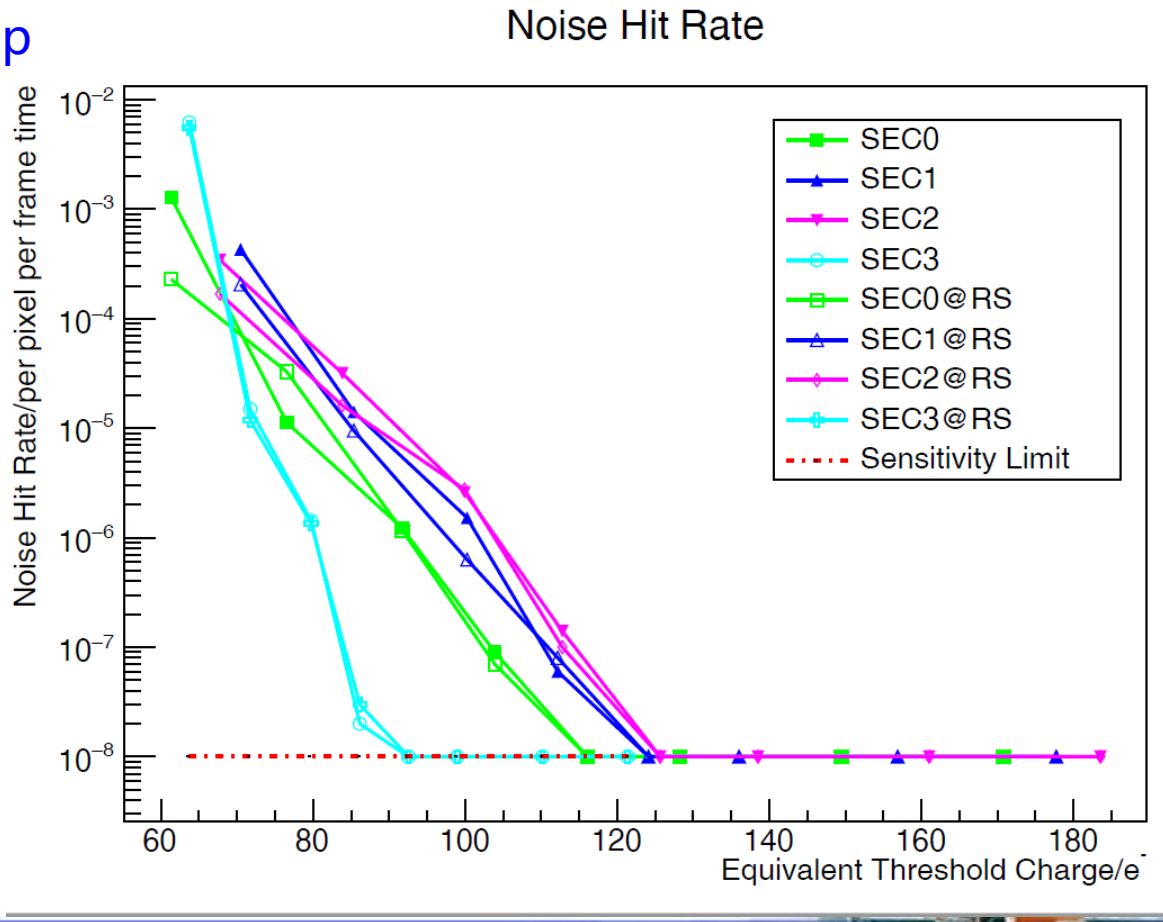
- Threshold calibrated with electrical test pulse
  - 200 e^- applied to the full matrix



Noise hit rate

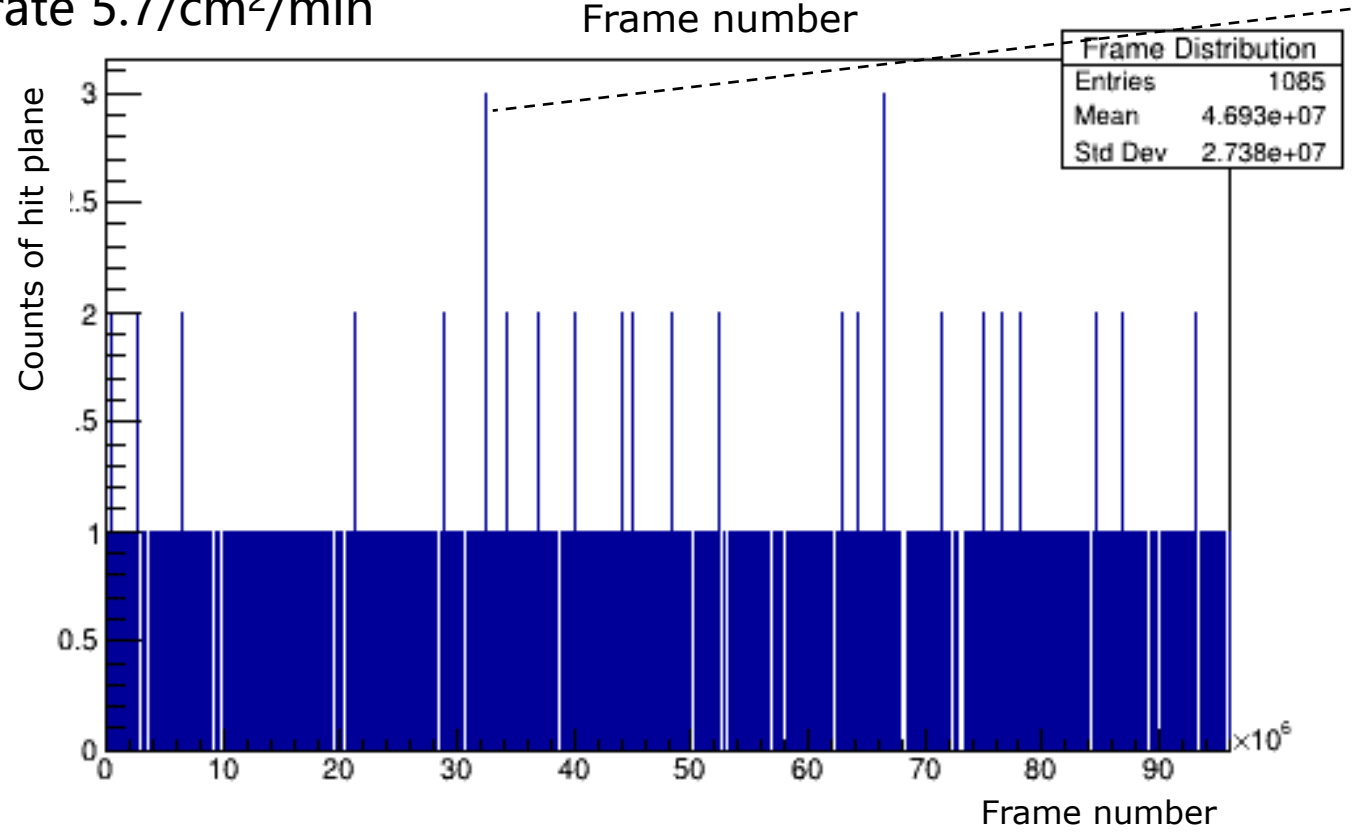
- Noise hit rate below 10^{-8} /frame/pixel
  - Sensitivity of measurement limited by the test time and environmental radiation
  - Data size proportional to the number of hits, a few bytes / hit

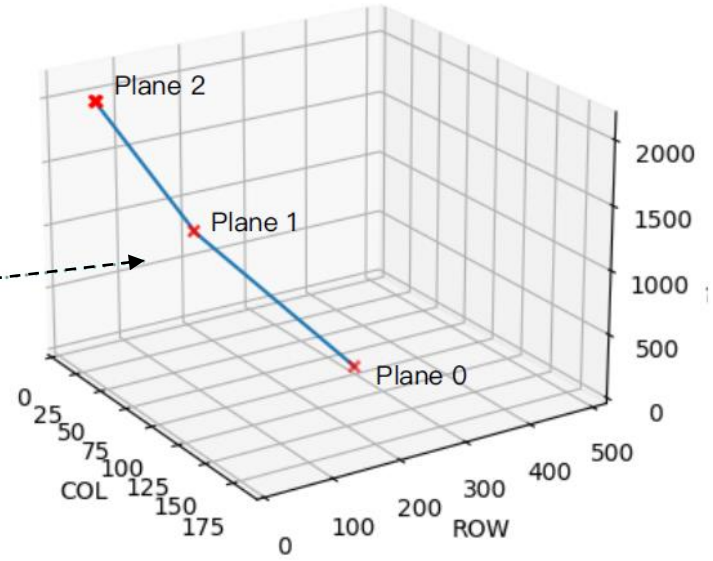
→ long time operation and data analysis on a laptop

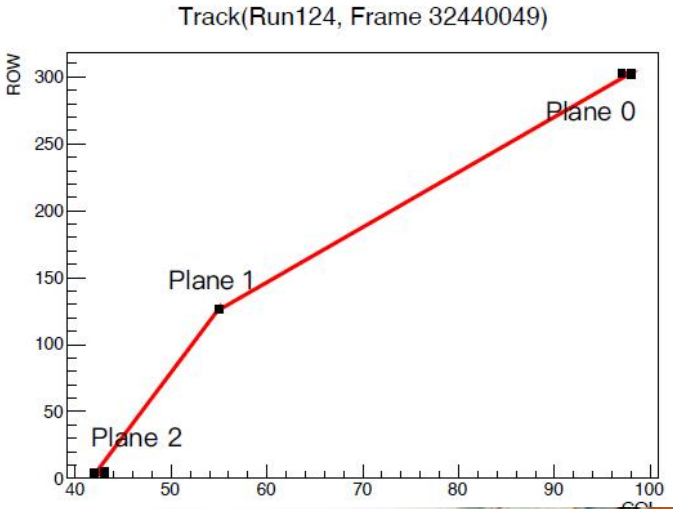


Initial test with cosmic ray

- 96 M frames scan in 160 minutes for a typical run
  - 1063 frames recorded with single plane hit
  - 20 frames recorded with 2 planes hit
  - 2 frames recorded with 3 planes hit
- Hit rate 5.7/cm^2/min

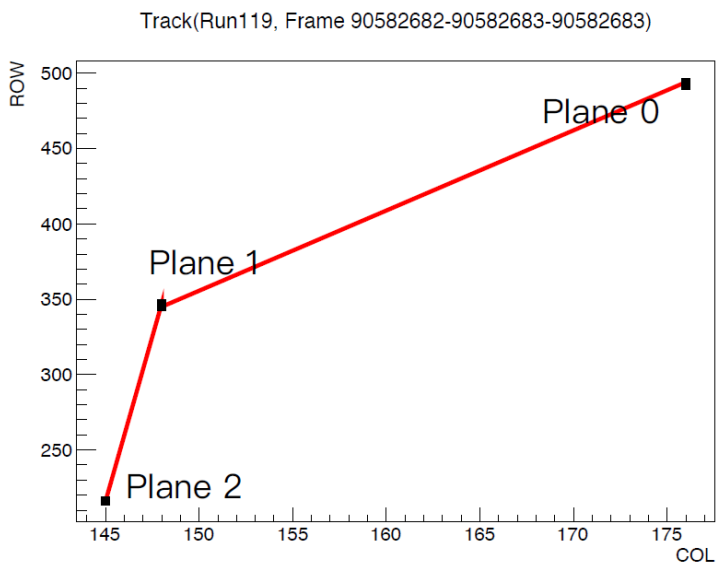


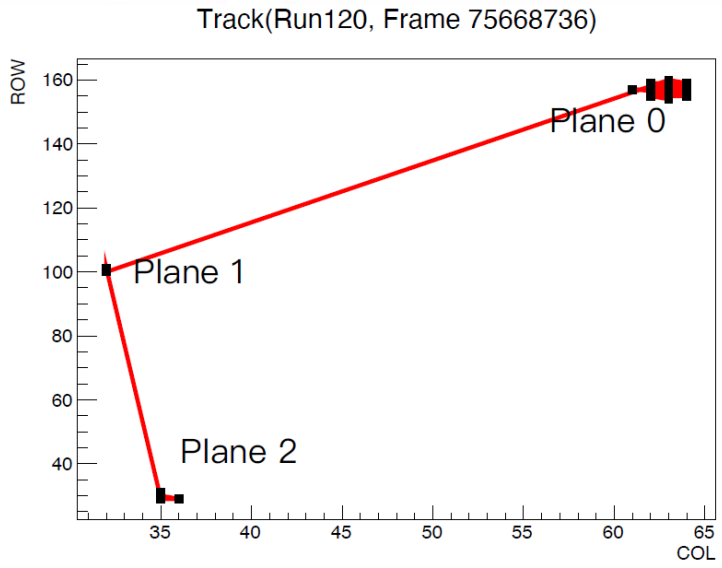


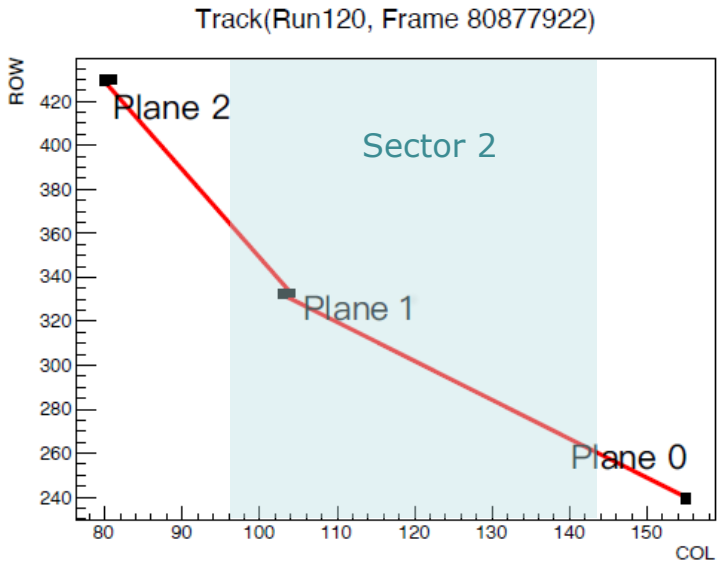


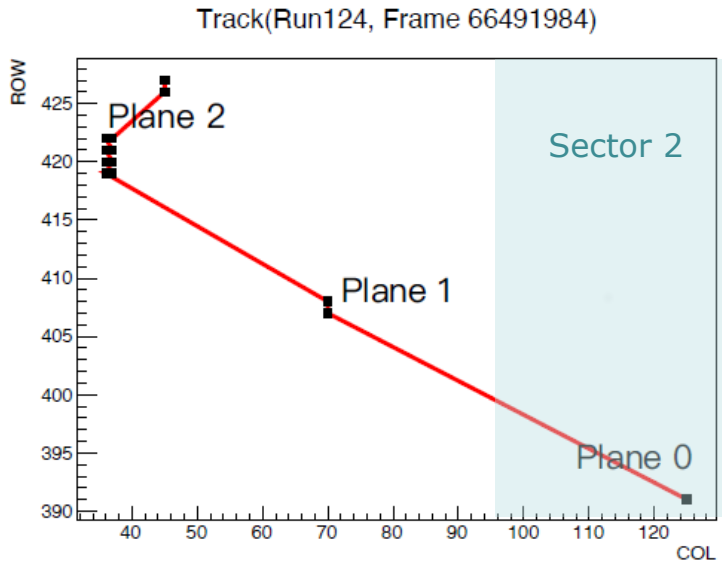
More cosmic ray event

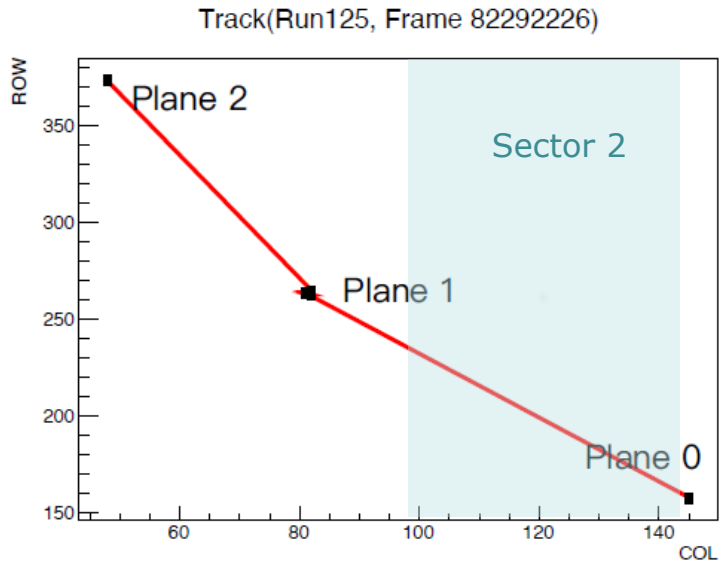
- Tracks hit 3 planes displayed
  - 2.5 hours / run
- Sources of position offset
  - Gluing of chips manually
  - Different pitch on sector 2











Next Plan

- To complete the integration of 5 detector planes
- Trigger detector
  - Plastic scintillator + SiPM
  - To provide a “gate” signal for the HIT register (short trigger window ~ a few us)
- EUTelescope software for track reconstruction and analysis
  - Need more experts in this area
- Time slot for test beam to be booked or shared
  - Not available yet