



The LHCb Upgrade Programme and the VELO

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Image credit: Arthur Hennequin Hadronic Interactions in VELO, Early Data, October 2022



First sighting of the VELO in situ

Image credit: Arthur Hennequin Hadronic Interactions in VELO, Early Data, October 2022

LHCD THCD

LHC Page1 Fil	II: 8288 E: 450 GeV 19-10-22 08:09:02			8:09:02		
PROTON PHYSICS: CYCLING						
Energ y :	450 GeV					
Post Mortem Information PM event ID: PM event category: PM event classification: PM BIS Analysis result: PM comment:	Wed Oct 19 03:04:00 C PROTECTION_DUMP MULTIPLE_SYSTEM_DU	IMP	> F on CIB.UA47.R4.B1			
		BIS status and	SMP flags	B1	B2	
Comments (19-Oct-2022 08:06:20)		Link Stat	us of Beam Permits	false	false	
	g for precycle first VELO full closure	Glob	Global Beam Permit		false	
			Setup Beam		true	
Next: 500b fill for		Be	Beam Presence		false	
		Moveable	Moveable Devices Allowed In		false	
	Stable Beams false				false	
AFS: Single_42b_0_0_0_nd	oHOnoLR	PM Status B1	ENABLED PM Status	B2 EI	NABLED	

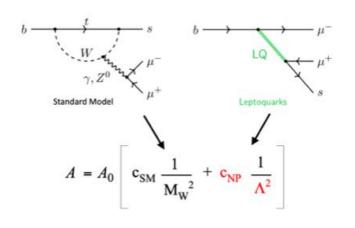
Contents

- LHCb Upgrade I
 - Overview
 - Tracking
 - PID
 - Fixed Target
- Focus on the VELO
 - Cooling
 - ASIC
 - Commissioning
- VELO at LHCb Upgrade II

Flavour Physics at LHCb

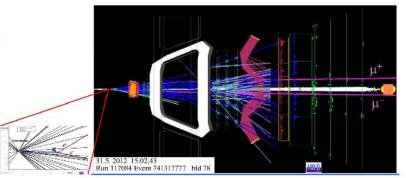
New physics searches with flavour look for the indirect effects on low energy processes, for instance rare b-hadron decays, probing mass scales not directly accessible at the LHC

The LHC provides huge statistics and access to all cand b-hadrons - but **event topology is challenging**; need low material, ability to trigger on low p_T , and particle identification to flavour tag and distinguish topologically similar decays e.g. $B \rightarrow \pi\pi$, $B \rightarrow K\pi$



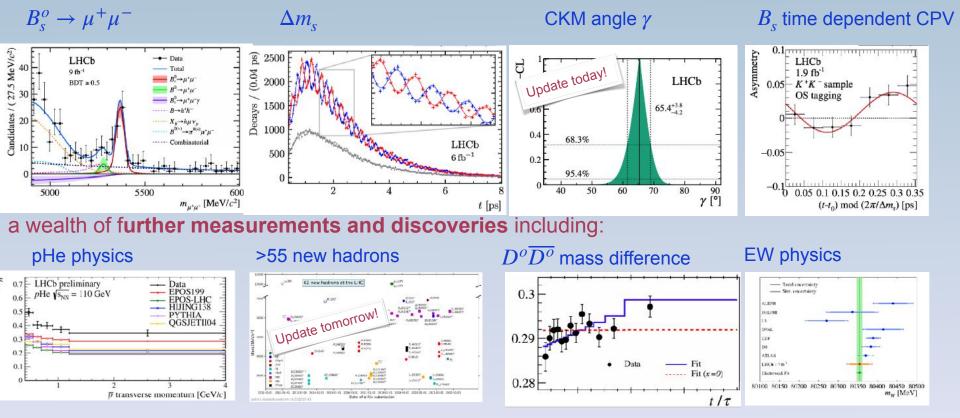
LHCb is a **general-purpose forward detector** at the LHC which is **particularly suited** to precision measurements in the beauty and charm sectors

- ✓ Δp / p = 0.5% at < 20 GeV/c, 1.0% at 200 GeV/c
- ✓ IP resolution = 15 + 29/ p_T [GeV/c] µm
- \checkmark decay time resolution 45 fs for $B_s
 ightarrow J/\psi \phi$ and $B_s
 ightarrow D_s$
- ✓ Kaon ID \sim 95% for 5% π → K mis-id probability
- $\checkmark\,$ full real time reconstruction in the high level trigger



LHCb Detector Performance

LHCb accumulated 9 fb^{-1} of integrated luminosity during LHC Runs 1 & 2 yielding **precision measurements including**:



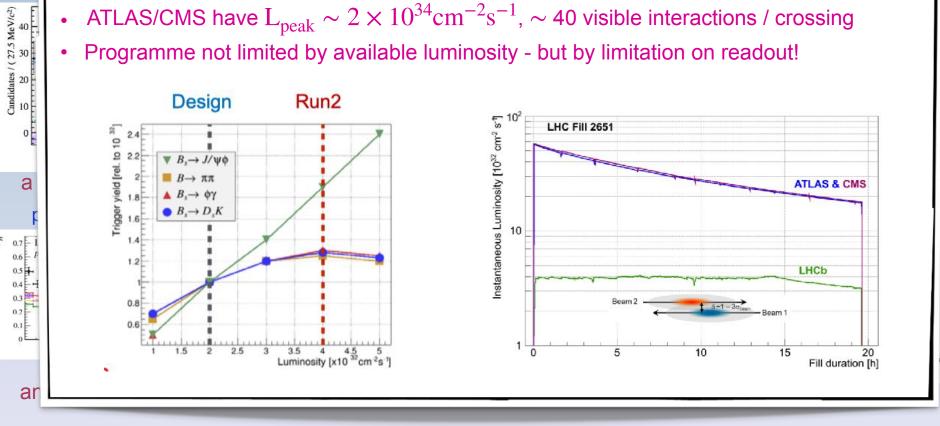
and also **intriguing anomalies**: R(D*), R(K), R(K*), angular analysis of $K^*\mu^+\mu^-$...

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LHCb Detector Performance

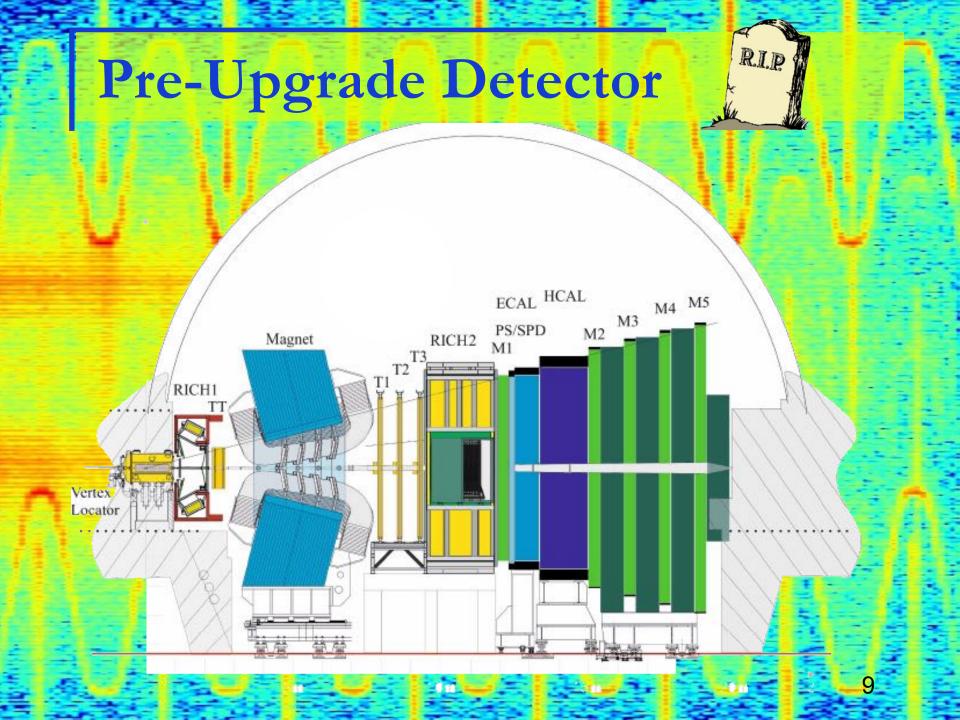
This was all achieved running at lower luminosity than LHC could provide

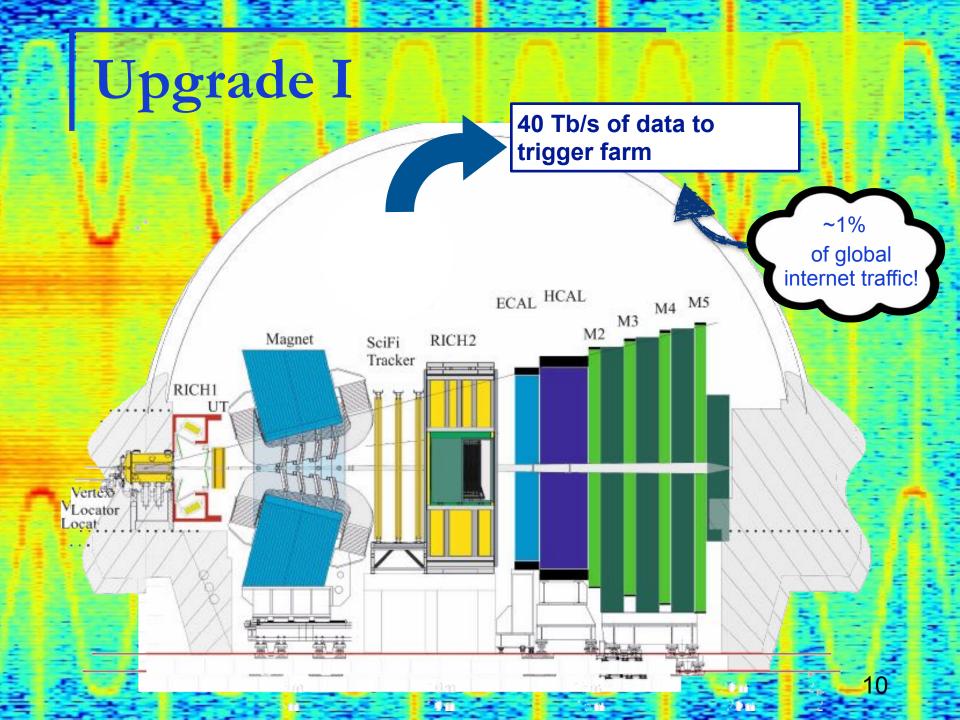
- $L_{peak} \sim 4 \times 10^{32} cm^{-2} s^{-1}$ levelled, \sim 1 visible interaction / crossing
- ATLAS/CMS have $L_{peak} \sim 2 \times 10^{34} cm^{-2} s^{-1}$, \sim 40 visible interactions / crossing
- Programme not limited by available luminosity but by limitation on readout!

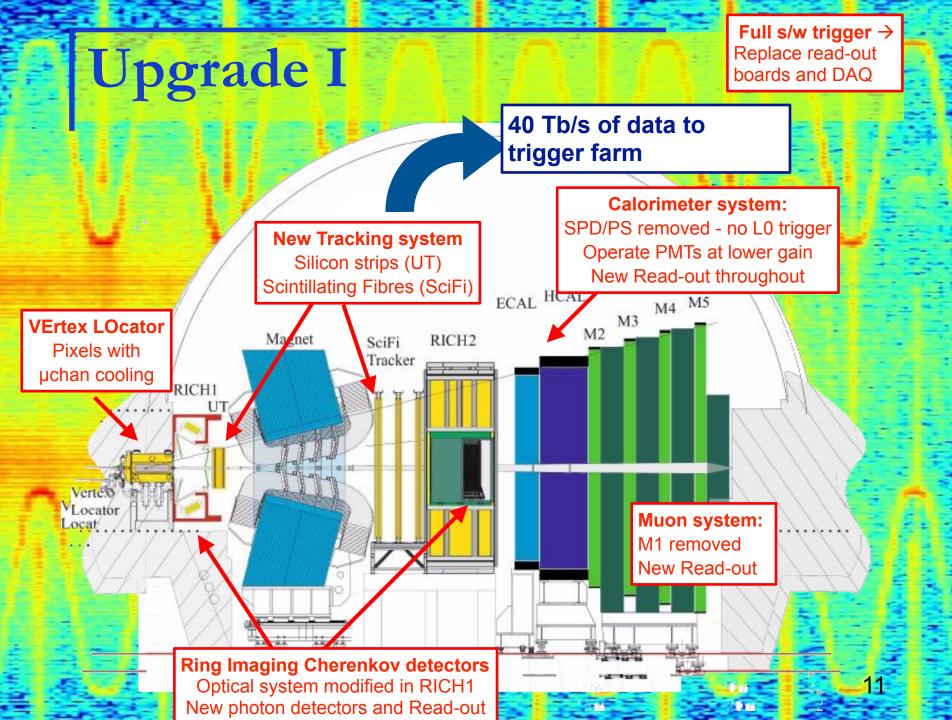


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LHCb Upgrade I in a nutshell **Upgrade** I **Upgrade II Original LHCb** Max Luminosity [10³³ / cm² / s] 1 1 1 1 1 1 8 Run 5 Run 6 350 Move to full software trigger -uminosity Allows effective operation at higher luminosity 300 • Improved efficiency in hadronic modes LS4 Raise luminosity to 2×10^{33} cm⁻² s⁻¹ (5x Run 2) 250 value) ntegrated Redesign of several sub-detectors & ambitious readout upgrade LS2 5 LS3 100 Run 3 Run 4 4 50 2 Run 2 Run 1 0 0 2010 2015 2020 2025 2030 2035 2040 Year

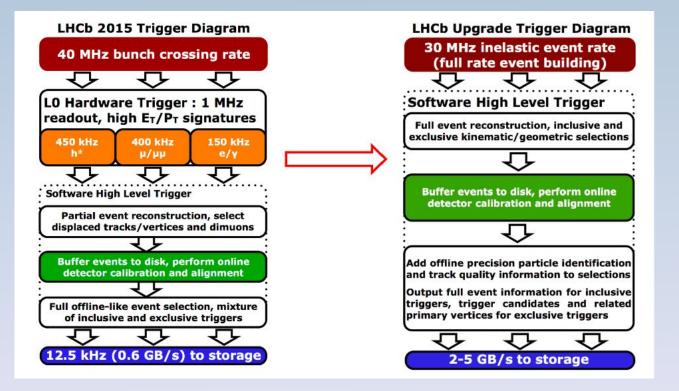






Trigger Transformation

Goal: Achieve same reconstruction performance in harsher environment Record all bunch crossings with full software trigger



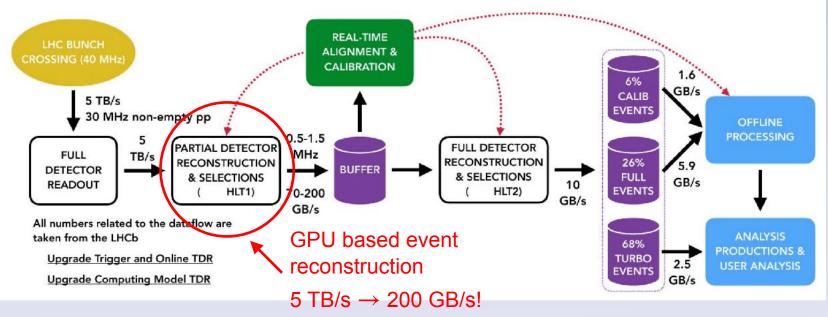
Pioneering Use of GPUs

Backend electronics on surface in data center ~19000 long distance optical fibres (99.75% yield)

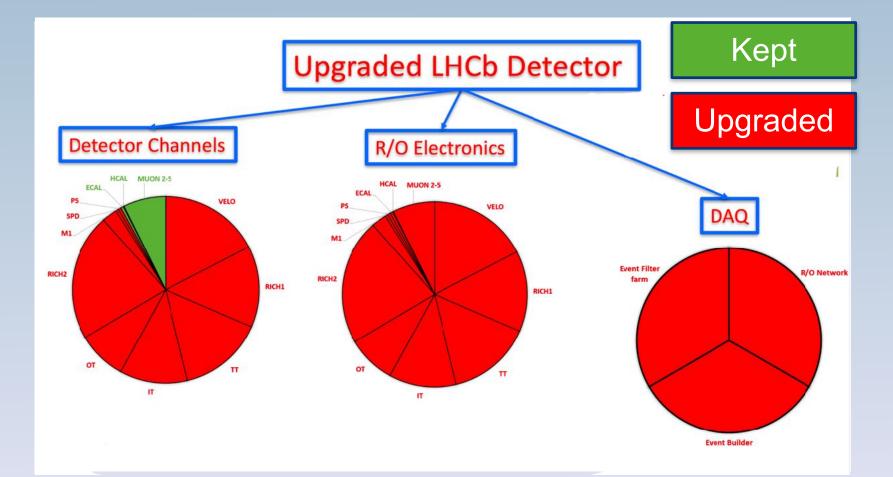
- Common backend boards (PCIe40) housing large FPGAs and optical links (48 x 10 Gbps)
- Flavour of firmware defines functionality

Total effective bandwitdh of up to 40 Tbps



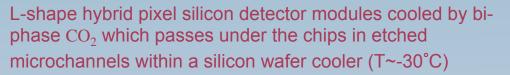


Putting it all together



Major Upgrade \rightarrow it's an all together new detector!

New VErtex LOcator



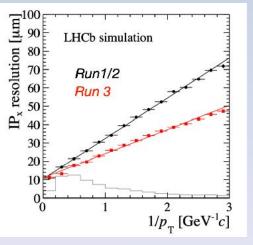
- ~ 3 % X_0 radiation length before second measured point on track

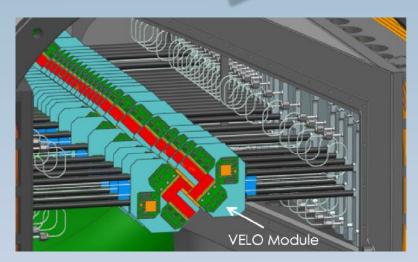
Two moveable halves: closer to beam line (R = 8.2mm \rightarrow R = 5.1 mm) for improved IP resolution

• 52 modules, 41M pixels, 208 x 200 µm sensor tiles

New ASIC: VeloPix ~ 20 Gb/s in hottest ASIC for a total of 3 Tb/s for whole VELO

Improved impact parameter and decay time resolution





CERN-LHCC-2013-013

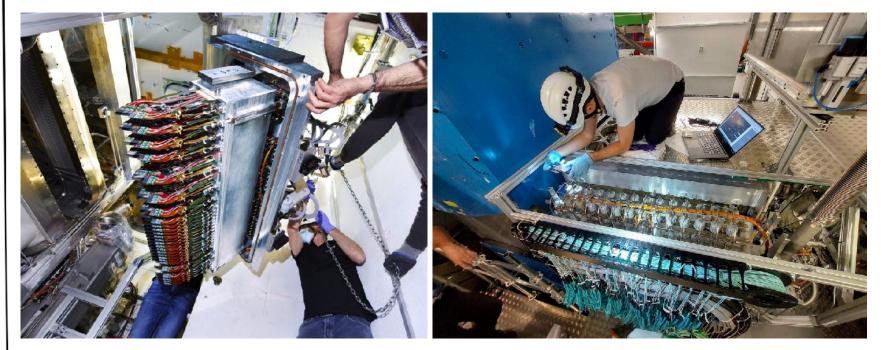


VELO half being installed

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New VErtex LOcator

Second half of VELO installed in May 2022



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LHCb VELO Upgrade Programme, IHEP Seminar

 $1/p_{\pi}$ [GeV⁻c]

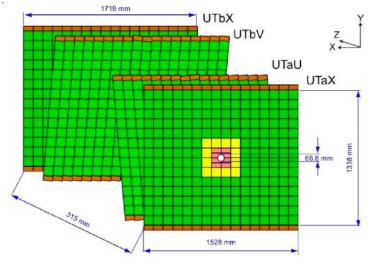
Tracking Detectors

Upstream Tracker (UT) : 4 planes made of silicon strips, with finer segmentation and improved acceptance

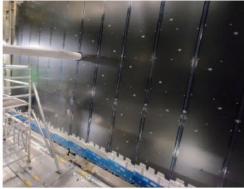
- fast p_T determination for track extrapolation reduce ghost tracks and improved trigger bandwidth
- Long lived particles decaying after VELO (K_s , Λ)

SciFi : downstream tracker made of 12 planes of scintillating fibres read out by SiPMs, to cope with increased occupancy

- each plane, with dimensions 6 x 5 m2, is made of scintillating fibres with 2.5 m length and 250 µm diameter
- Spatial resolution is better than 80 µm and hit efficiency better than 99%
- Readout with linear arrays of SiPMs cooled to -40°C



CERN-LHCC-2014-001



SciFi plane fully installed and aligned

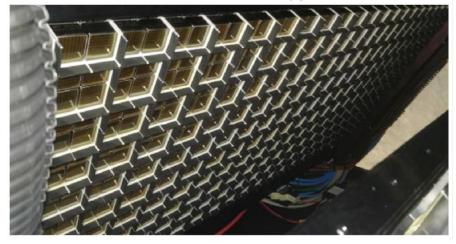
PID detectors: RICH

Goal is to maintain the excellent Run 1/2 performance with the increased occupancy foreseen at Run 3

RICH1 (closer to the IP); new mirrors with $\times \sqrt{2}$ focal length, to halve the occupancy

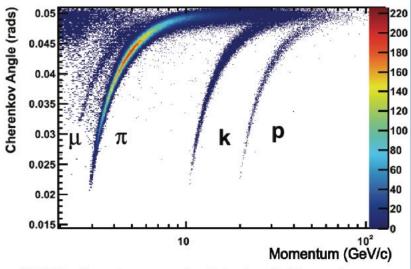
RICH 1 & 2; new photodetectors; MaPMTs with increased granularity and 40 MHz readout

RICH1: MaPMTs installed upper side

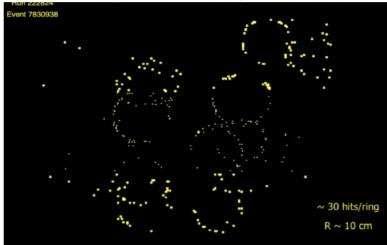


Run 1/2 performance of the RICH system

CERN-LHCC-2013-022



RICH2: first rings acquired during LHC october test



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PID Detectors: CALO and MUON

Present calorimetry system can withstand the increased luminosity of Run 3/4

Shashlik calorimeters

ECAL = Pb+Sci ~25X₀, HCAL = Fe+Sci ~ $5\lambda_I$

PMT gain reduced to stand the higher occupancy new front-end electronics with improved S/N and 40 MHz readout

Muon stations

- 4 walls equipped with MWPCs, and interleaved with iron filters front-end electronics upgraded for 40 MHz readout, granularity increased on first station to reduce occupancy
- Large improvements expected from software trigger
- reduced p_{T} threshold on electrons after removal of hardware L0
- improved muon software selection will allow to reject a factor of ~2 more bkg at trigger level

more improvements in high-level electron and muon PID selections will allow to compensate the occupancy increase



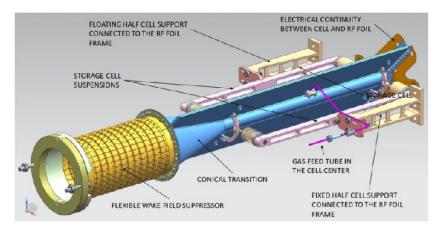


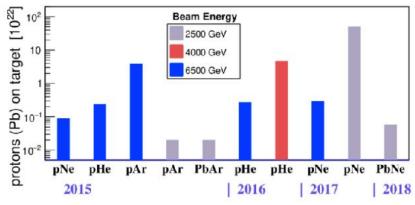
CERN-LHCC-2019-005

SMOG2 and Fixed Target Physics

New SMOG2 system installed to inject various gas species in the LHCb IP

- Fixed Target physics at the LHC collider: in // with pp data taking
- Gas cell attached to VELO, displaced p-gas IP for easy distinction from pp data



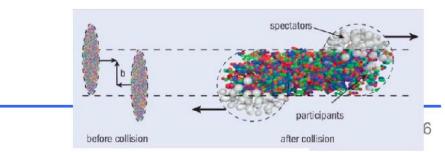


Physics program spans over:

- o anti-proton production
- o Central exclusive production
- o X(3872)/ψ(2S)
- ο ψ(2S) / J/ψ
- o Strangeness production
- Λc → pKπ

+ LHCb participation in Heavy lon runs (PbPb and pPb data taking)

✓ Down to 30% centrality in LHCb in Run3!

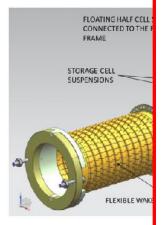


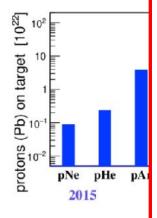
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SMOG2 and Fixed Target Physics

New SMOG2 system installed to inject various gas species in the LHCb IP

- Fixed Ta
- Gas cell



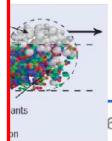


Last view of the cavern before commissioning started, upgrade is almost complete! The final subdetector, the UT, will be installed in the upcoming shutdown ata

pn



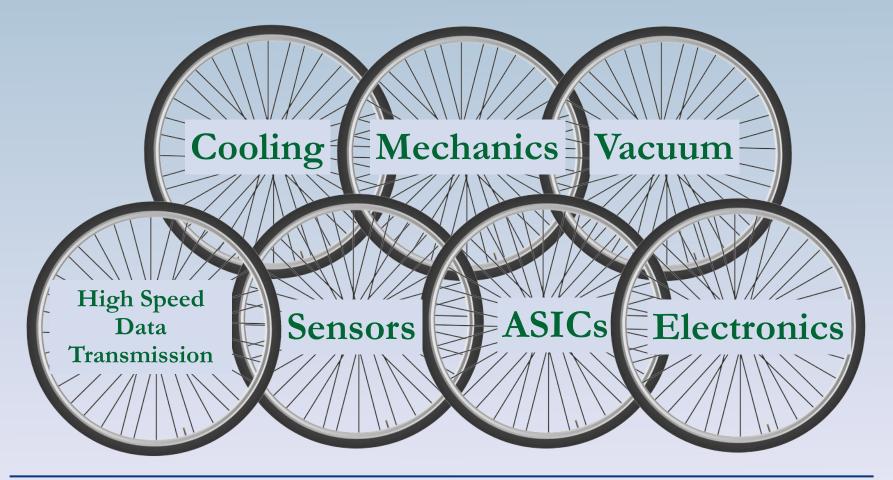
in Run3!



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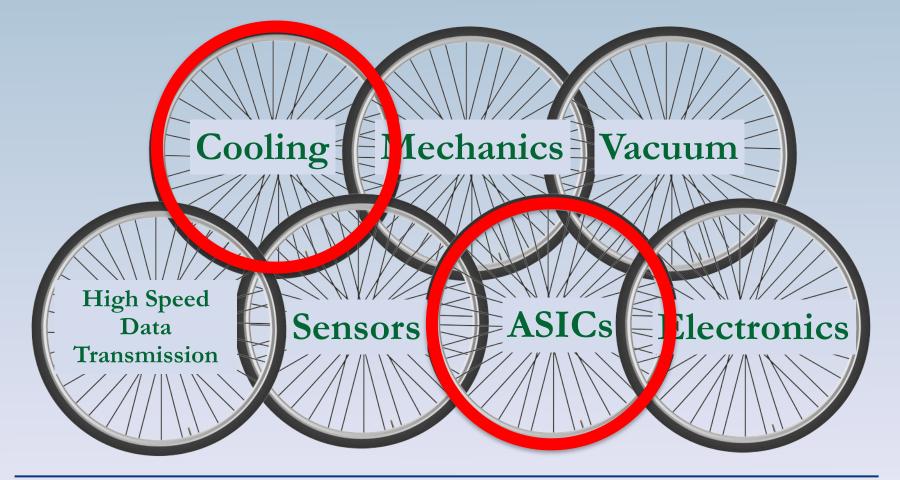
Focus on the VELO

VELO runs on many technologies

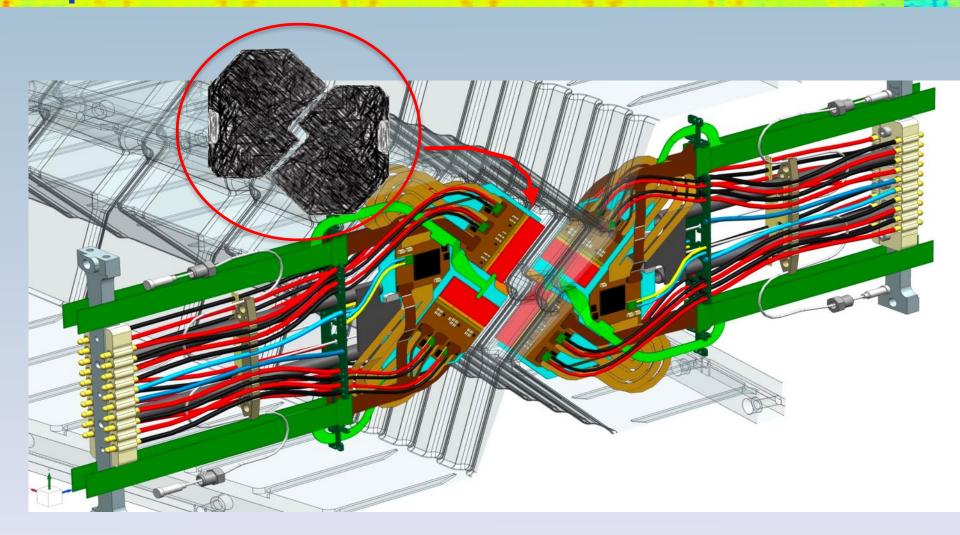


Focus on the VELO

Today will take a deep dive into two of these



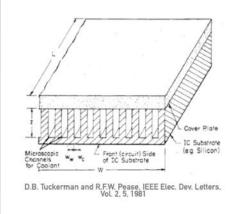
Microchannel Cooling



What is "microchannel cooling"?

TFM = (Δ T fluid - sensor)

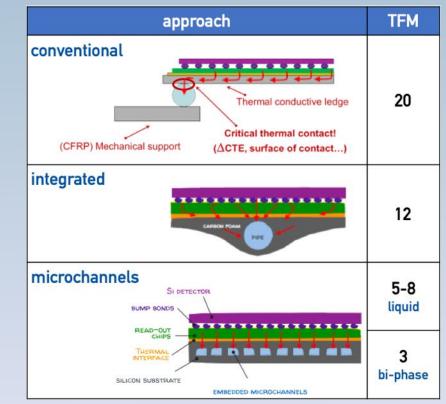
Original idea (liquid H₂O)



D.B. Tuckerman, R.F.W.Pease,: High performance heat sinking for VLSI, IEEE Electron Device Letters Vol. 2, Issue 5, pages 126-129,1981

- No CTE mismatch
- Low Material budget
- Active/distributed cooling
- Radiation resistance
- Great integration potential
- Great Thermal Figure of Merit

power density



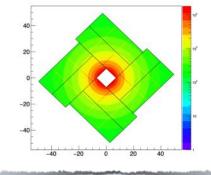
see P.Petagna, presentation, EIC tracking Workshop, Jul 24th 2018, A. Mapelli, presentation, 3rd FCC Physics and Experiments Workshop

VELO Pixel Cooling Requirements

Silicon pixel modules will accumulate ~ 50 fb⁻¹ at a closest distance of 5.1 mm from the beam

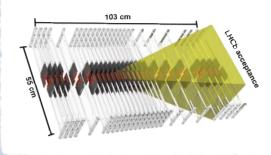
non-uniform Irradiation up to $8 \times 10^{15} \text{ MeV} n_{eq} \text{ / } \text{cm}^2$

Sensor tips must be kept < -20°C (almost) permanently while bump bonded directly to heat source



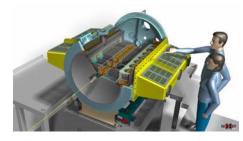
Cooling partially in acceptance for physics tracks

Vital to minimise material over entire cooling plate



Modules dissipate 30W <u>in vacuum</u> Total power:1.5 kW silicon tip: 1W/cm² after irradiation

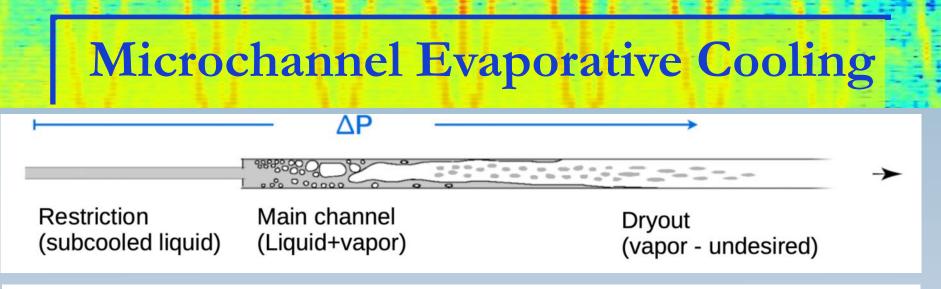
High thermal efficiency mandatory



ASICs cooling cookies

Ideal to find a solution which uses the CO_2 evaporative cooling already developed for LHCb (-35°C)

However the previous solution of cooling pipes embedded in aluminium "cookie" heat spreaders does not satisfy the pixel upgrade requirements



- CO₂ has high latent heat capacity, low viscosity and is radiation hard
- The heat from the electronics is absorbed by the liquid CO₂, that evaporates
- Structures of the orders of 10s of µm are accessible
- The coolant temperature decreases from the input to the output
- The restriction dominates the fluidic resistance and so provides excellent control
 - · Instabilities are avoided and the channels have even flow
- The system must withstand operational pressures
 - · normal operation at -30°C \rightarrow 20 bar
 - \cdot at room temperature \rightarrow 65 bar
 - entire system must be validated to > 186 bar for safety reasons

LHCb Implementation

Channels integrated in silicon substrate under hybrid pixel tiles

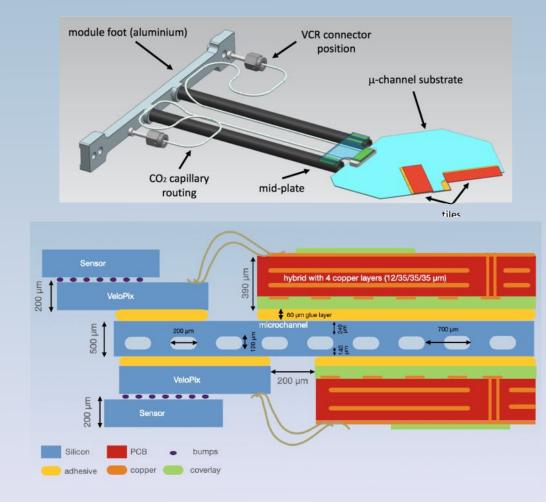
Material budget: 500 µm Si + coolant Very homogenous material distribution Cooling delivered directly under heat sources Thermal contact over flat area No CTE mismatch wrt ASICs and sensor Very efficient cooling performance

- 60 µm glue interface only
- 120/240 µm Si between coolant and electronics
- Very high thermal conductivity (Si 150 W/m.K)
- Very low temperature gradients over substrate

Evaporative cooling \rightarrow fast response to changes in power dissipation

Cooling is so effective that the microchannel can be withdrawn 5 mm from module tip

Challenges: Production (large size of device), Mastery of full silicon process (DRIE, Direct Wafer Bonding), Fluidic connector attachment, QA for proven long term mechanical stability



Bonding Layer Options



Scanning Acoustic Microscope image of bonded wafers with test structures

See A. Mapelli: Microfabricated silicon substrates for pixel detectors assembly and thermal management, presentation at 15th Vienna Conference on Instrumentation

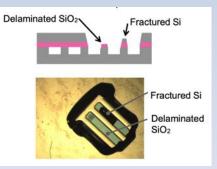
Hydrophilic bonding

- water molecules coat the surface
- T_{anneal} = 1050^oC, P_{max} 400 bar
- Gives a good quality, even bond





When tested to very high pressure: Tendency to delamination + rupture



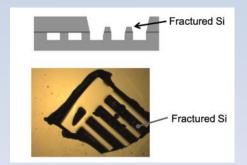
Hydrophobic bonding

- · Highest quality bond with no oxide layer
- T_{anneal} = 1050°C, P_{max} 700 bar
- but more sensitive surface preparation



- Sue

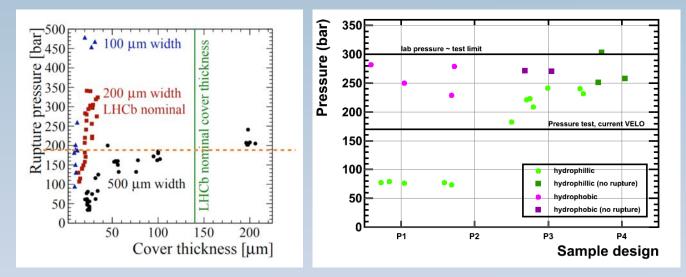
When tested to very high pressure: Tendency to rupture without delamination



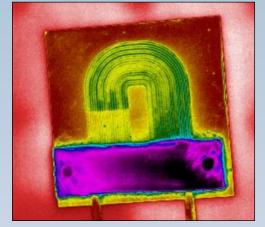
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Test Results I

At room temperature, saturation pressure of CO_2 is around 65 bar For safety reasons, the system must be validated to 186 bar



Layout test



Cooling test (with different prototype)

Even with a silicon cover << nominal, the safety requirements are surpassed

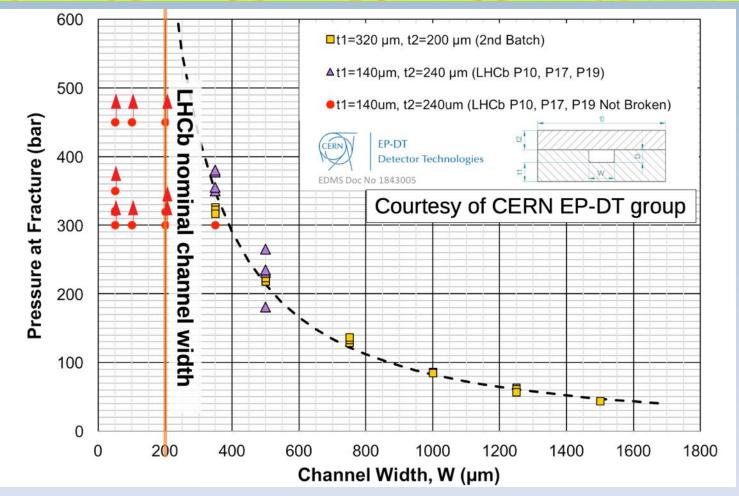
Cover test

As long as the large manifolds are avoided, the samples surpass the safety test for both hydrophilic and hydrophobic bonding

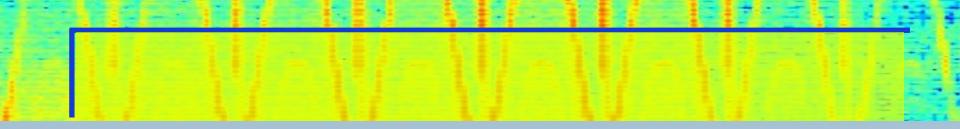
Qualitative results show expected behaviour

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Test Results II



Measurements made in collaboration with NA62 and fitted to a theoretical curve, demonstrating role of the channel width No LHCb sample with nominal geometry broke, up to maximum test pressures of 400 bar

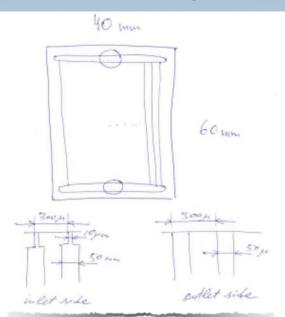


Microchannels are proven to be small, but very strong!



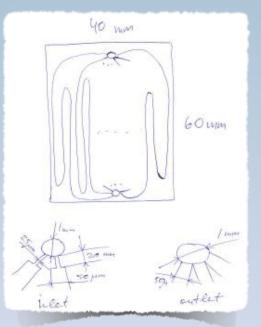
Initial Designs

'Simple Design'



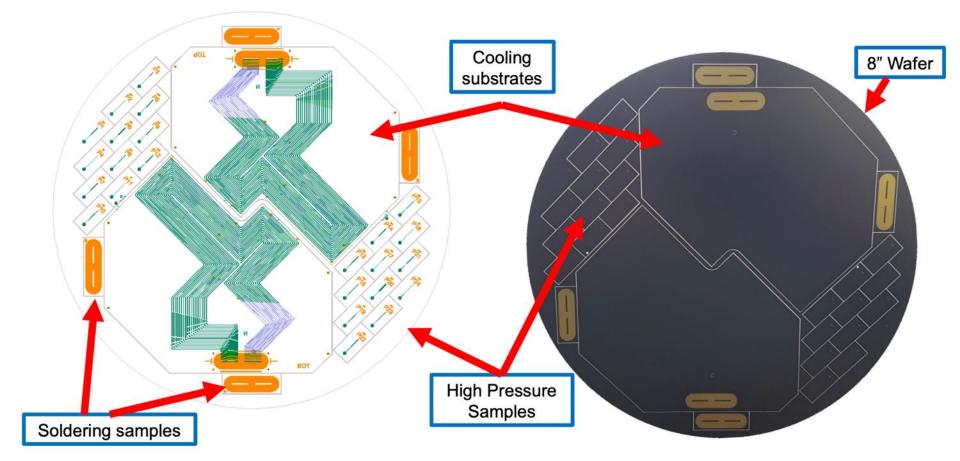
- 75 parallel channels on 300 µm pitch
- 10 μm x 5 mm inlet
- 50 µm x 45 µm boiling channel
- 100 µm etching depth (channels and manifold)
- 1 mm wide manifold

'Spider Design'

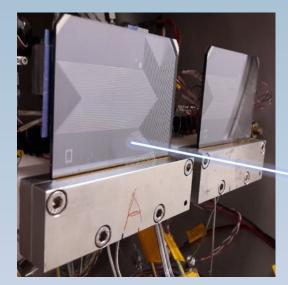


- using microchannels etched in silicon for the future LHCb vertex detector" ink see A. Nomerotski et al, "Evaporative CO2 cooling
- 15 parallel channels on 200 µm pitch
- 25 µm x 20 mm inlet
- 200 µm x 135 µm boiling channel
- 100 µm etching depth (channels and manifold)
- manifold is small and can be located anywhere

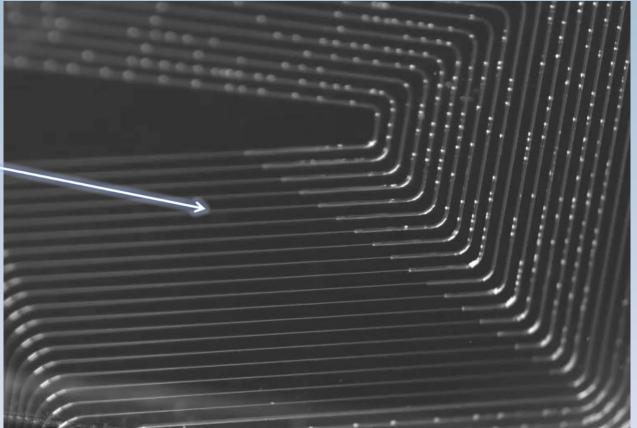




Demonstrator



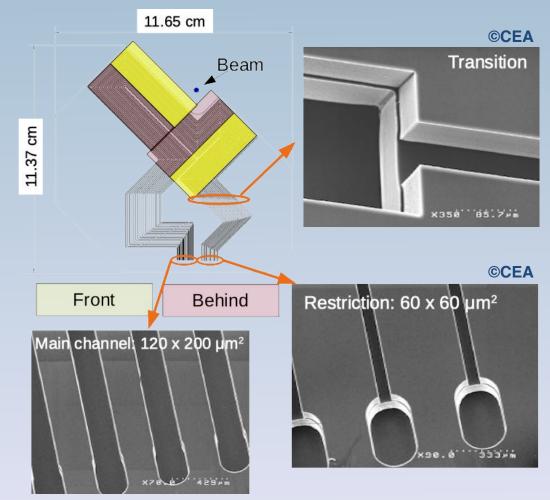
Single CO₂ bubble speed up to 1 m/s

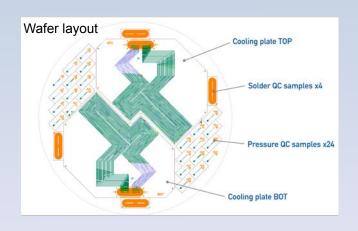


Final Design

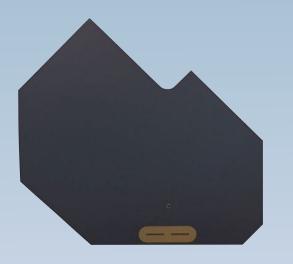
Race track like layout Restrictions: 60 x 60 µm² Main channels: 120 x 200 µm² 19 channels with approximately the same total length (~ 30 cm)

Each channel has its own inlet and outlet hole (200 x 600 μ m²) CO₂ distribution among channels done by connector









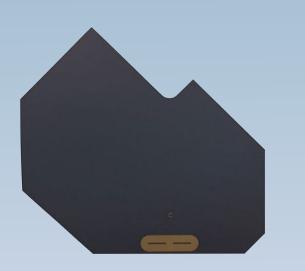
Grade A: no defects

- Grade B: defects close to input/output
- Grade C: defect near channels
- Grade P: dicing defects

See <u>presentation</u> of C. Bertella, 28th International Conference on Vertex Detectors, October 2019 Major part of grading based on high resolution scanning acoustic microscope images (resolution < 50 μ m) taken at wafer level after bonding, and again after thermal annealing



Guiding principle, limiting channel width (see slide 13) Additional grading added for surface quality, planarity etc.

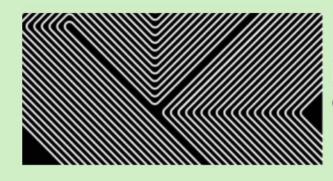




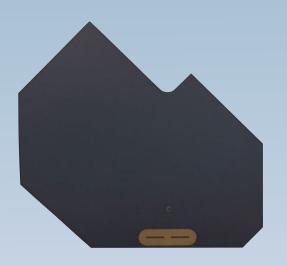
N In m

No defects: Input manifold

Grade A: no defects Grade B: defects close to input/output Grade C: defect near channels Grade P: dicing defects



No defects: Channels

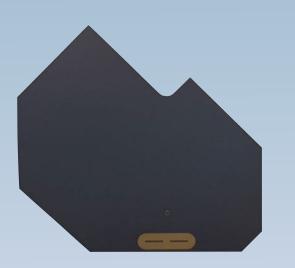


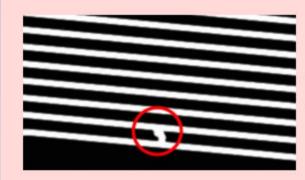
Connected channels, output manifold

Defect close to the input manifold

Grade A: no defects Grade B: defects close to input/output Grade C: defect near channels Grade P: dicing defects

See <u>presentation</u> of C. Bertella, 28th International Conference on Vertex Detectors, October 2019

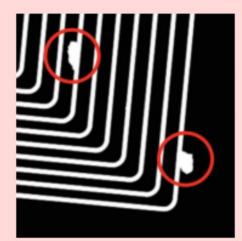




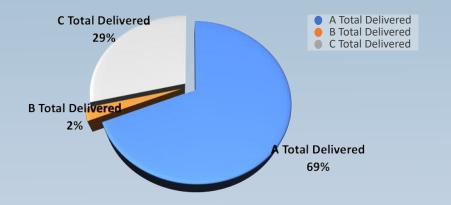
Connected channels

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See <u>presentation</u> of C. Bertella, 28th International Conference on Vertex Detectors, October 2019



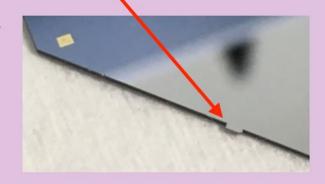
Defects connected to the channels



Grade A: no defects Grade B: defects close to input/output Grade C: defect near channels Grade P: dicing defects

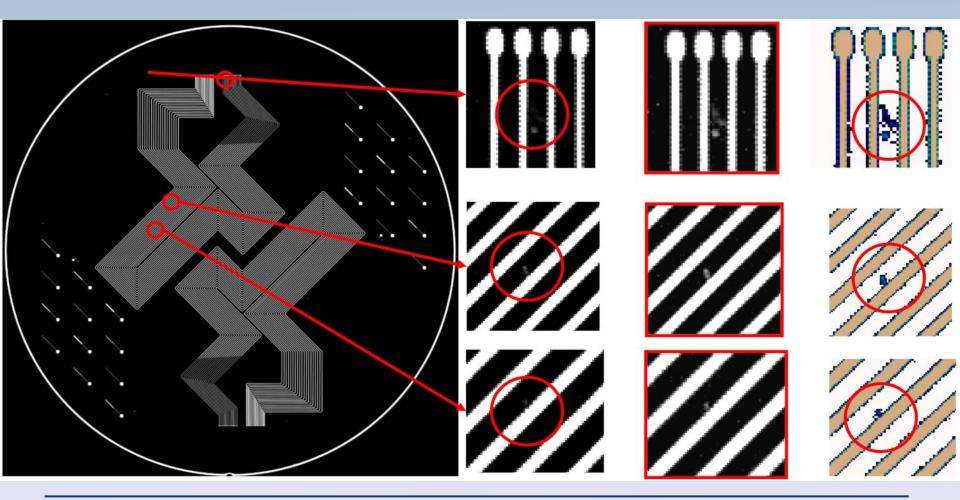
Bonding grading most challenging component of overall yield

"Pont"

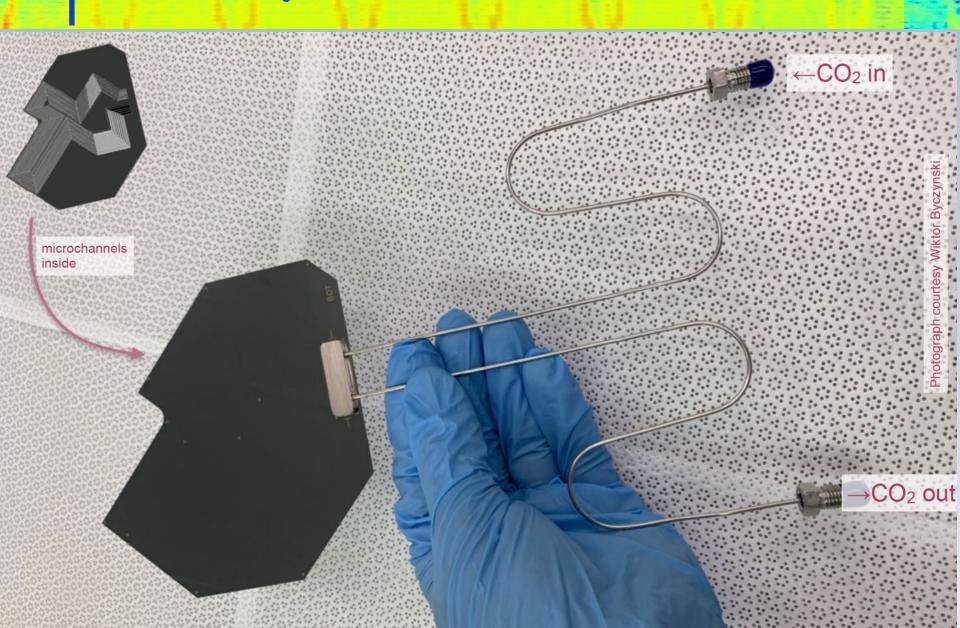


Analysis of images very time consuming and tiring: new technique developed to process the images

- Grey scale transformed to colour map with background suppression
- Algorithm useful to assist visual inspection all features found verified in original SAM



Assembly of Connector and Susbstrate

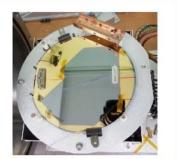


Fluxless Connector Soldering

Fluxless process to avoid long term corrosive effects in the cooling system

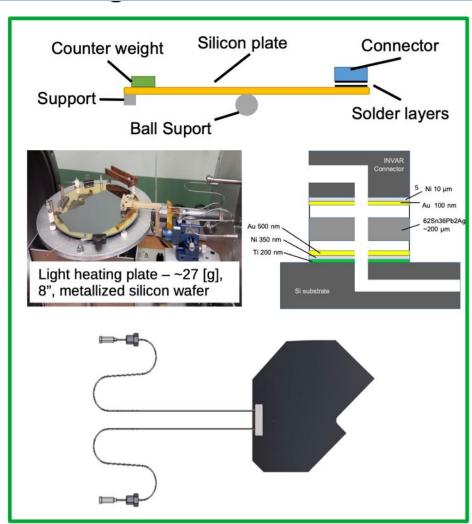
Silicon pretinning





Connector pretinning

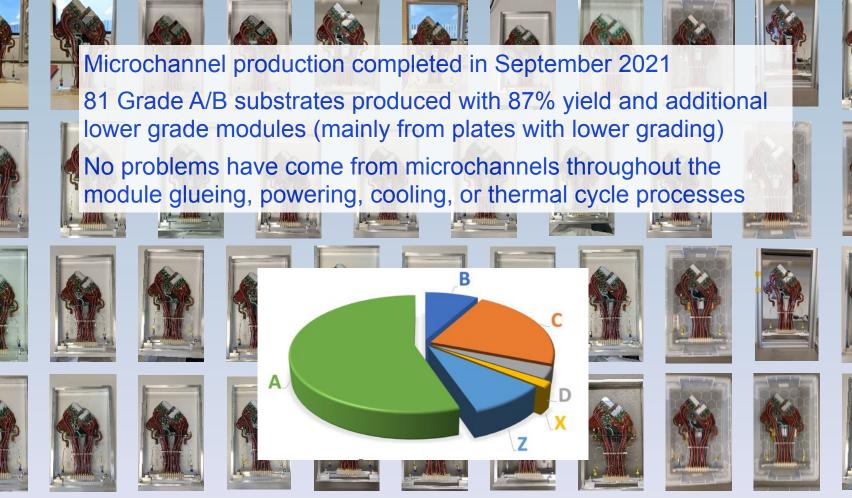




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Production Yield



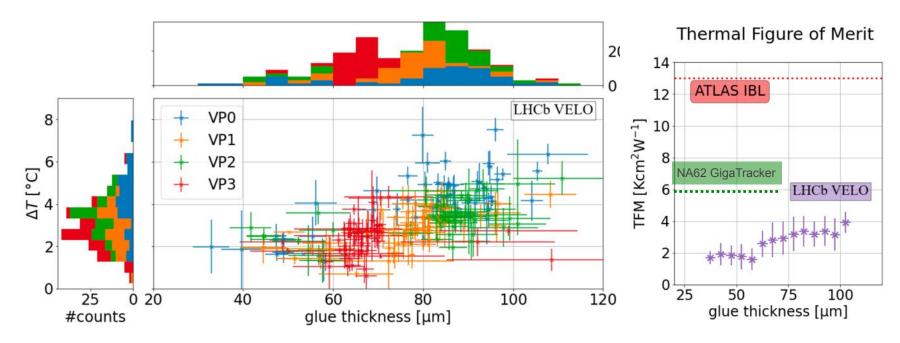


Cooling Performance

The performance of a cooling system can be characterised by the Thermal Figure of Merit;

TFM = Difference in temperature between coolant and power dissipating element Power Density

Expected values: ~ 20 for classical systems, ~12-13 for integrated pipe systems, ~5-6 for single phase microchannels

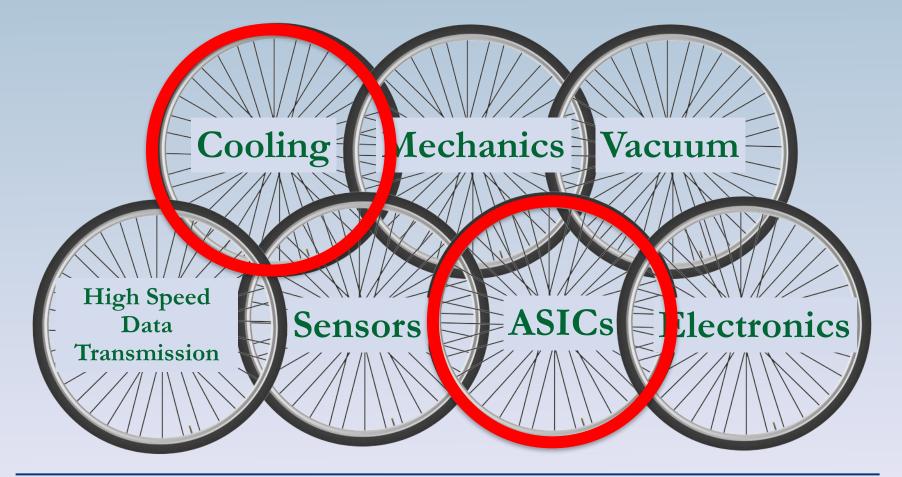


TFM measured value for all produced VELO modules between 2 and 3 (dependent on glue thickness)

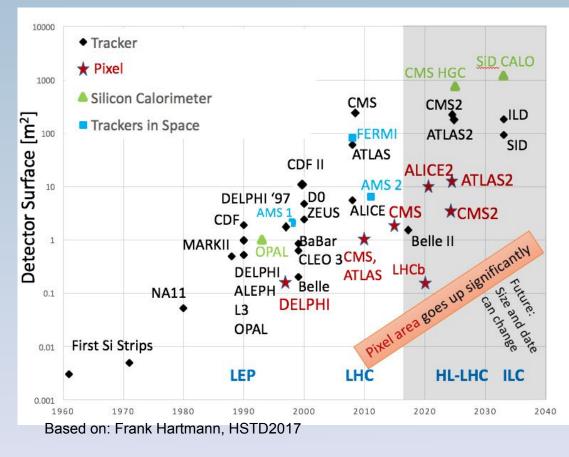
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Focus on the VELO

Today will take a deep dive into two of these



VELO in line with rise of hybrid pixels



In general global tracker sizes are saturating

However cell sizes and data rates are evolving significantly

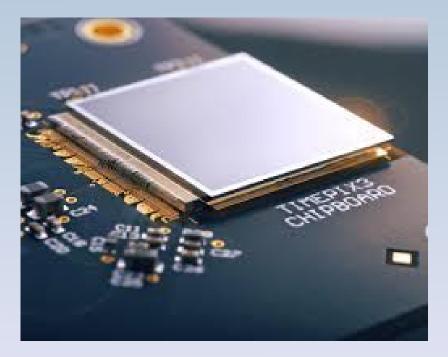
Detector	Current	Upgrade
CMS strips	9.8M	42M + 172M
CMS Pixels	127M	2GP
ATLAS strips	6.3M	60M
ATLAS pixels	92M	5GP
VELO	171k	41M
ALICE	12.5M	12.5G

Cell granularity, the weapon against high-PU keeping occupancy at a reasonable level

Hybrid Pixels: Medipix/Timepix

Hybrid pixels used in tracking detectors, gaseous detector readouts, RICH, biomedical applications and photon science, space applications etc...

In the case of the VELO close integration with Medipix/Timepix family.

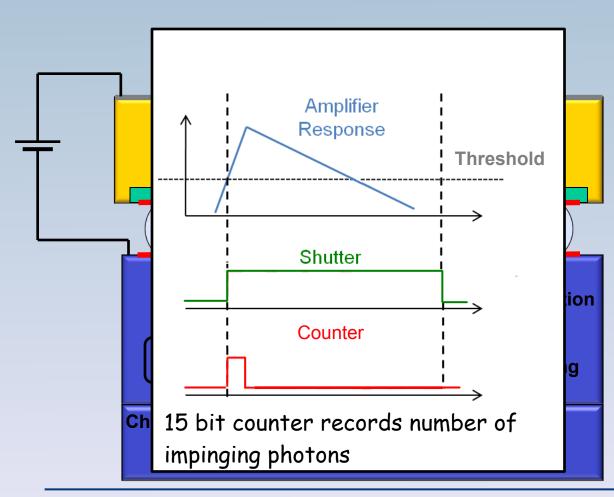


sensor Analogue amplification Digital processing Chip read-out

Idea: take advances in HEP and apply them to photon counting for medical physics

Intensity counter for photons, using individual pre-amp, comparator and counter per pixel

Operates in "camera" mode, reading out the entire pixel array when the shutter closes



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sensor Analogue amplification Digital processing Chip read-out

Timepix design requested and funded by EUDET collaboration

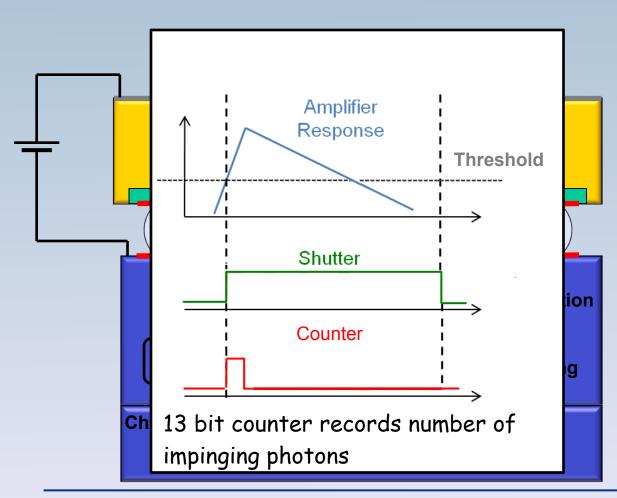
Conventional Medipix2 counting mode remains.

Addition of a clock up to 100MHz allows two new modes.

Time over Threshold

Time of Arrival

Pixels can be individually programmed into one of these three modes



Timepix design requested and funded by EUDET collaboration

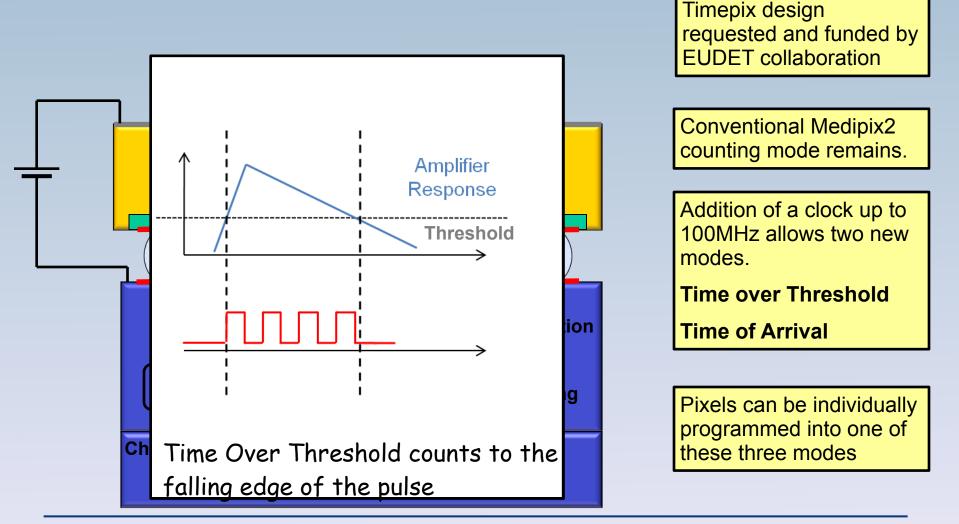
Conventional Medipix2 counting mode remains.

Addition of a clock up to 100MHz allows two new modes.

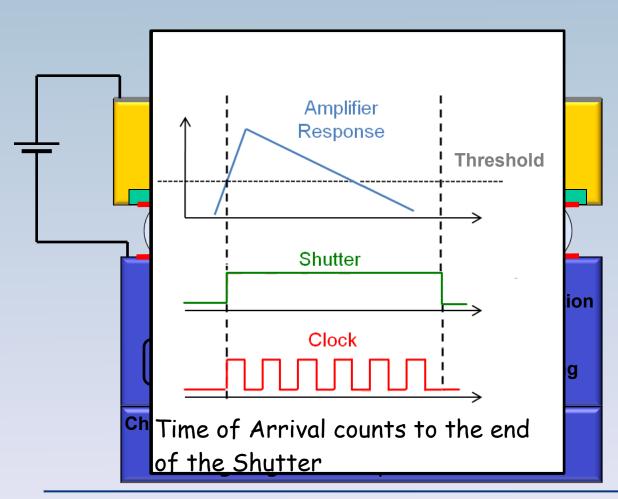
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Timepix design requested and funded by EUDET collaboration

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Addition of a clock up to 100MHz allows two new modes.

Time over Threshold

Time of Arrival

Pixels can be individually programmed into one of these three modes

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Low energy threshold (4 keV) enables imaging of very low contrast media, like flowers, with high resolutions

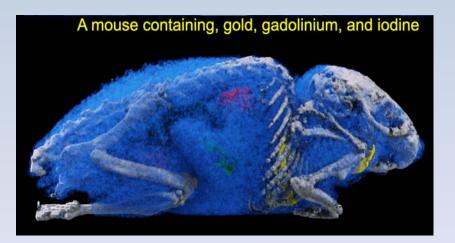
Medipix3: Convolvulus arvensis 3.1 M pixels, 55 µm pixel pitch Credits: Simon Procz,, Ph.D. Thesis, University of Freiburg

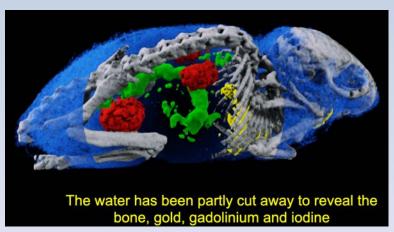
Spectral Imaging with MARS

Spectral imaging allows different materials to be identified and quantified

Separate map (data channel) made for each material Each map gives the partial density (g/cm3) for the material Each material assigned a colour for easy visualisation

A phantom containing Au, Gd, Iodine, Lipid, Water and hydroxyapatite

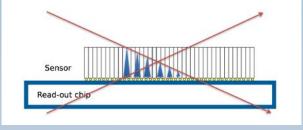




Timepix3 Specs - particle tracking

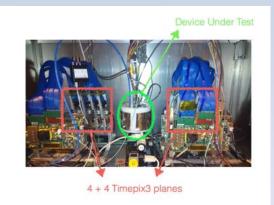
Timepix, and then Timepix3, applied to particle tracking

CMOS node	130nm		
Pixel Array	256 x 256		
Pixel pitch	55μm		
Charge collection	e-, h+		
Pixel functionality	TOT (Energy) and TOA (Arrival time)		
Preamp Gain	~47mV/ke [_]		
ENC	~60e-		
FE Linearity	Up to 12ke ⁻		
TOT linearity (resolution)	Up to 200ke [.] (<5%)		
TOA resolution*	Up to 1.6ns		
Time-walk	<20ns		
Minimum detectable charge	~500e [.] \rightarrow 2 KeV (Si Sensor)		
Max Analog power (1.5V)	500 mA/chip		
Digital Power (1.5V)	~400mA data driven		
Maximum hit rate	80Mhits/sec (in data driven)		
Readout	Data driven (44-bits/hit @ 5Gbps)		



tracking in single Si layer conceivable

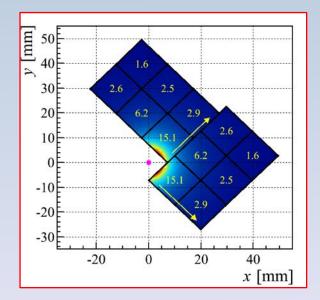
X ray materials analysis, gamma camera, compton camera, electron microscopy, neutron and photon imaging... and particle tracking for the Timepix3 telescope



VELOPix for LHCb Upgrade I

ASIC challenges: data rate & radiation hardness

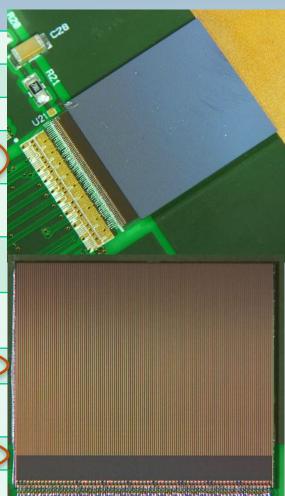
- Sensor and ASIC exposed to high, non-homogeneous, radiation fluence
 - Only part of the pixel matrix gets the full dose of ~ 370 Mrad
 - TID at periphery of chip is factor 10 lower
- For data rates calc. we assume collisions in every LHCb bunch crossing
 - in reality only 2/3 of bunches collide
 - would require a lot of memory to level out
 - \rightarrow assume peak rates for ASIC design
- Data flow simulations using physics Monte Carlo data
- No trigger, all data sent off chip
- Hottest ASIC gives ~20 Gbps
- ASIC design starting point: Timepix3



VeloPix for LHCb Upgrade I

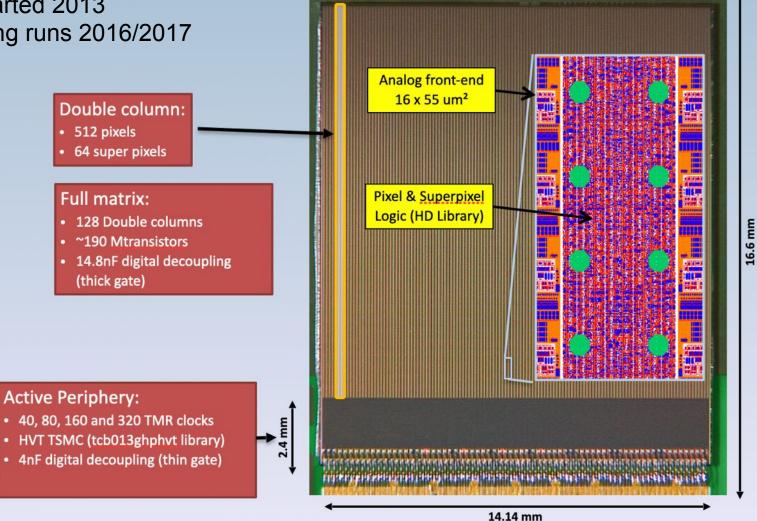
Derived from Timepix3 and dedicated to LHCb.

	Timepix3 (2013)	VeloPix (2016)
Pixel arrangement	256 x 256	
Pixel size	55 x 5	55 μm²
Peak hit rate	80 Mhits/s/ASIC	800 Mhits/s/ASIC 50 khits/s/pixel
Readout type	Continuous, trigger-less, TOT	Continuous, trigger-less, binary
Timing resolution/ range	1.5625 ns, 18 bits	25 ns, 9 bits
Total Power consumption	<1.5 W	< 3 W
Radiation hardness	(400 Mrad, SEU tolerant
Sensor type	Various, e- and h+ collection	Planar silicon, e- collection
Max. data rate	5.12 Gbps	20.48 Gbps
Technology	IBM 130 nm CMOS	TSMC 130 nm CMOS



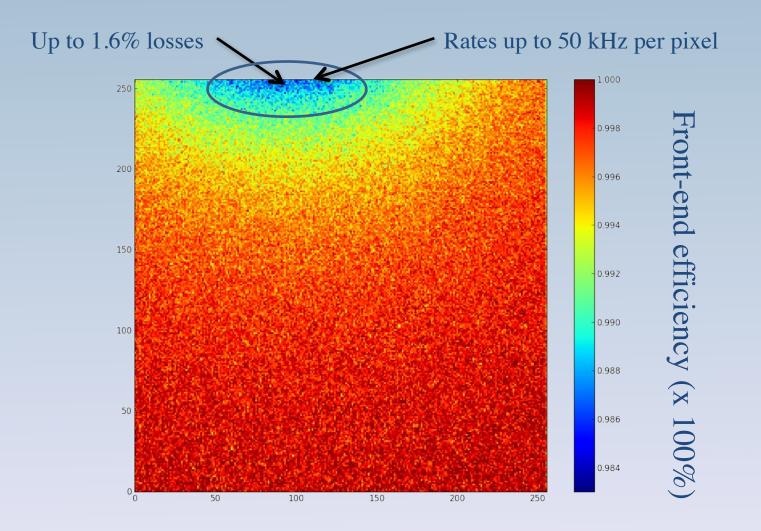


Design started 2013 Engineering runs 2016/2017



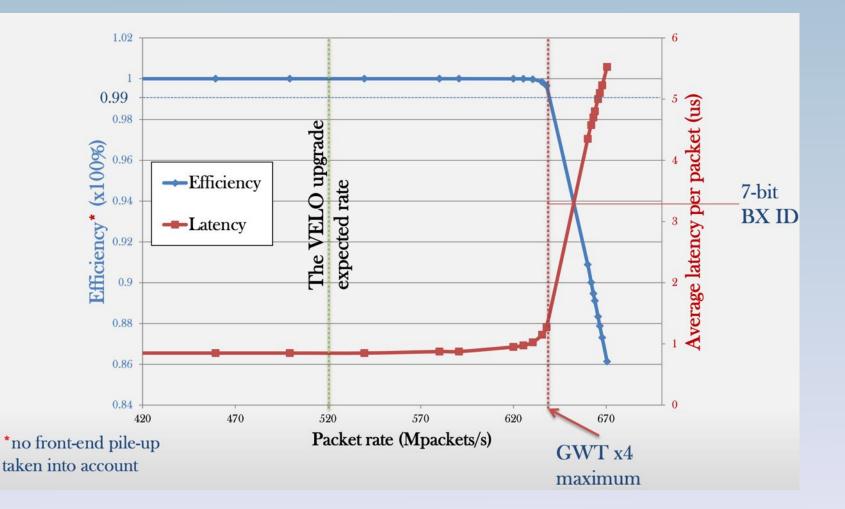
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Analog Front End Pileup (simulated)



LHCb VELO Upgrade Programme, IHEP Seminar

Data Transfer Efficiency (simulated)



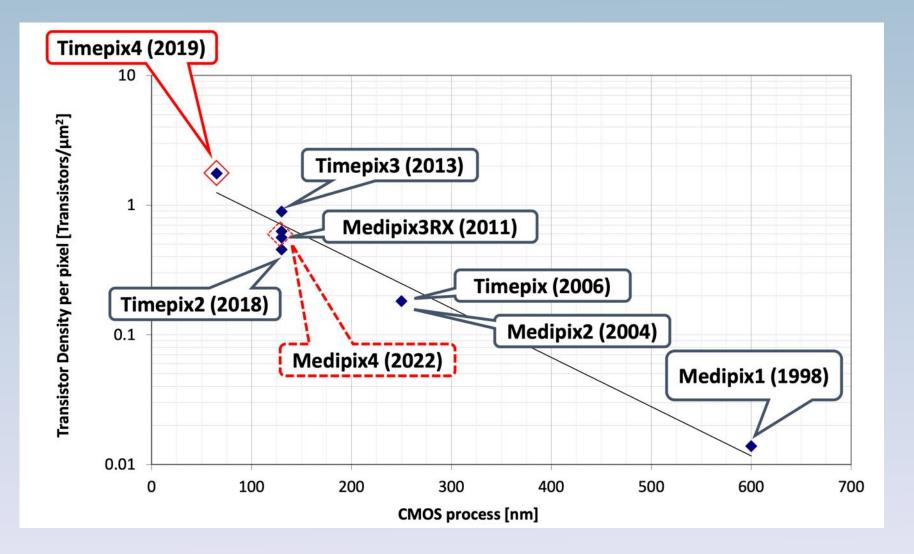
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VELO pix lab performance (ECS)

- Measured power consumption (@nominal settings):
 - Analog supply < 480 mW</p>
 - Digital: Periphery < 380mW, matrix ~ 300 mW at high rate (simulated)
 - ✓ Total= ~1.5W @High rate

Pixel gain	~24.6 mV/Ke-
Pixel to pixel gain variation	~3.3%
Pixel ENC	62.9 e-
Pixel to pixel threshold mismatch	410 e-rms
Pixel to pixel threshold mismatch calibrated (Threq)	40.3 e-rms
Expected minimum threshold	> 450 e-

Timepix4



Timepix4

Timepix4: A 4-side tillable large single threshold particle detector chip with improved energy and time resolution and with high-rate imaging capabilities

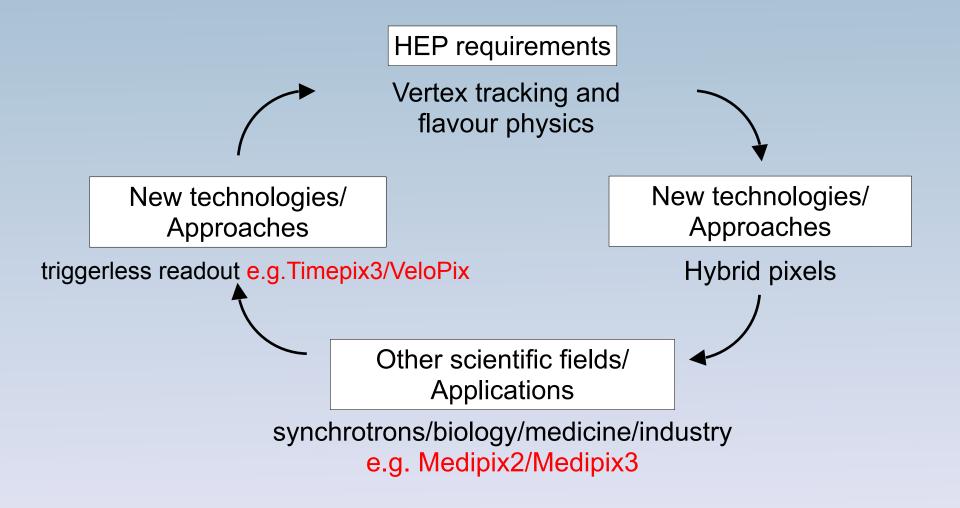
			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 μm	55 x 55 μm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	3.5x
Sensitive area			1.98 cm ²	6.94 cm ²	
S Data		Mode	TOT and TOA		
	Data driven	Event Packet	48-bit	64-bit	33%
Νοσ	Data driven (Tracking) Frame based	Max rate	0.43x10 ⁶ hits/mm ² /s	3.58x10 ⁶ hits/mm ² /s	0
nt P		Max Pix rate	1.3 KHz/pixel	10.8 KHz/pixel	8 x
Fran (Ima		Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
	Frame based (Imaging)	Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel add	ir)
	(imaging)	Max count rate	~0.82 x 10 ⁹ hits/mm ² /s	~5 x 10 ⁹ hits/mm²/s	6 x
TOT energy resolution		ion	< 2KeV	< 1Kev	2 x
Time resolution			1.56ns	195.3125ps	8x
Readout bandwidth		n	≤5.12Gb (8x SLVS@640 Mbps)	≤163.84 Gbps (16x @10.24 0	Gbps)
Target global minimum threshold		num threshold	<500 e⁻	<500 e⁻	

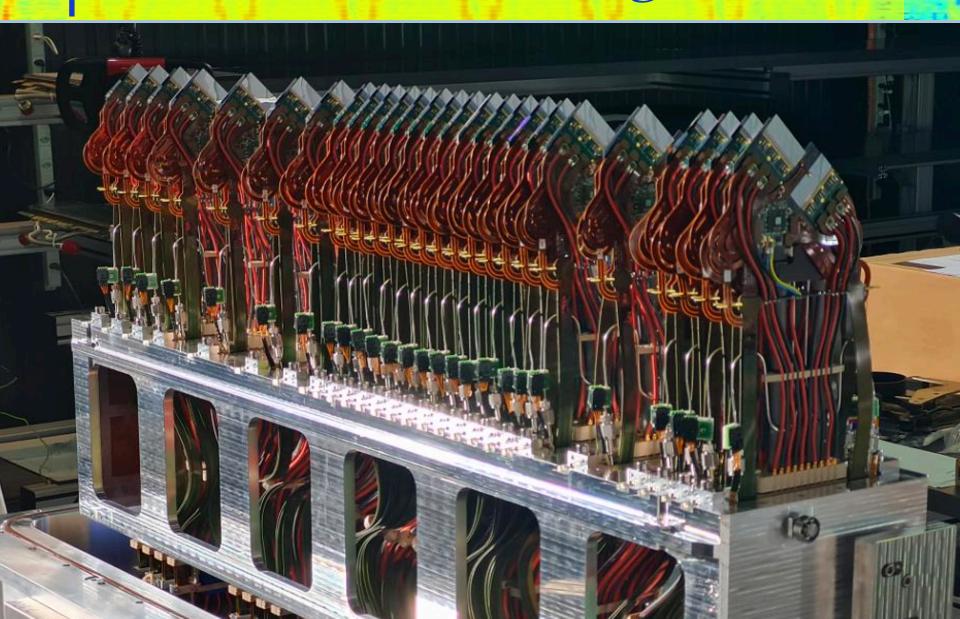
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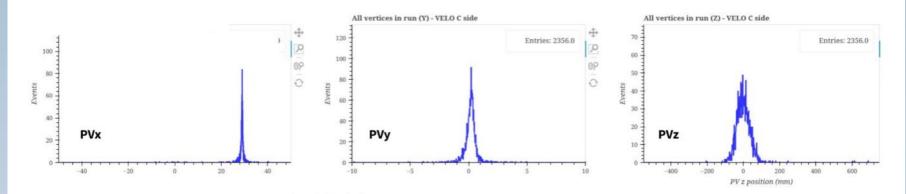
2x

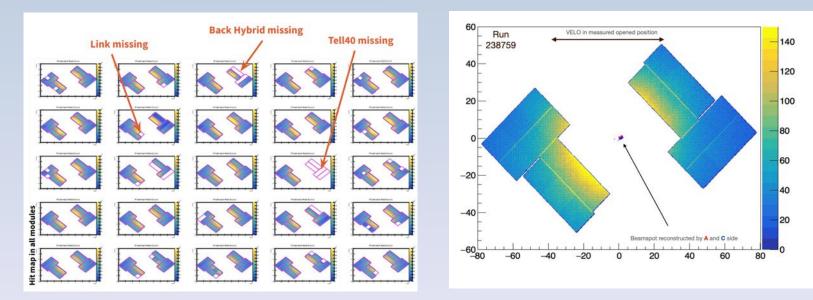
Timepix / HEP cycle of innovation





VELO is 98% up and running, and reconstructing tracks and vertices independently from the two halves. Pixel calibrations and time alignment being finalised to bring efficiency up to 100%



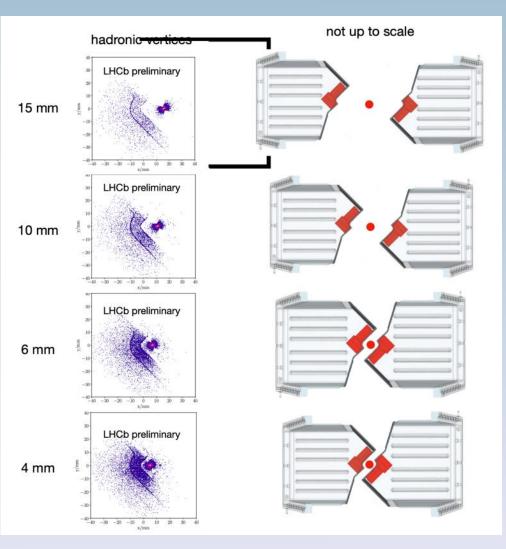


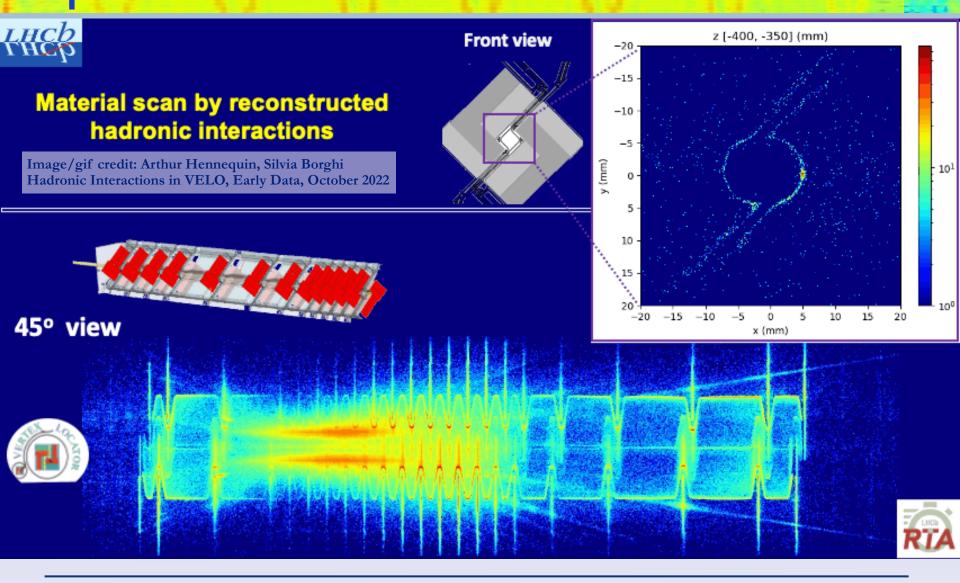
19/10/22

First test closure to within 2 mm of nominal position: October 2022

Image credit: Rizwaan Mohammed, Valeria Lukashenko Hadronic Interactions in VELO, Early Data, October 2022

First full closure scheduled for today! The 400 MJoule LHC beams will have to thread their way through a meter long tube no thicker than a pencil

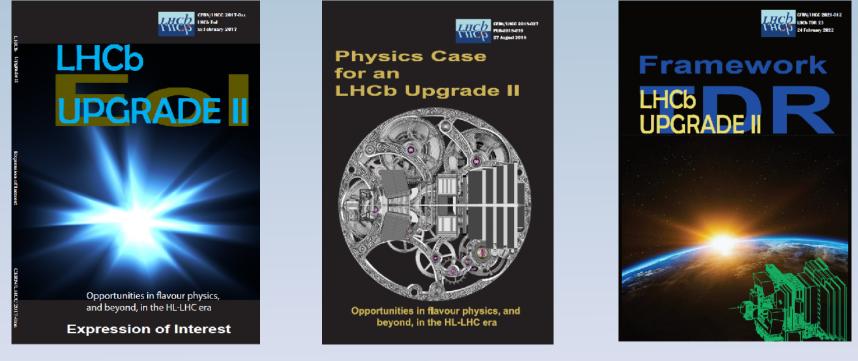




19/10/22

LHCb Upgrade II

Upgrade I will not saturate precision in many key observables \rightarrow a further upgrade is necessary to fully realise the flavour-physics potential of the HL-LHC There is steady progress towards plans for an Upgrade II, that will operate in Runs 5 and 6.



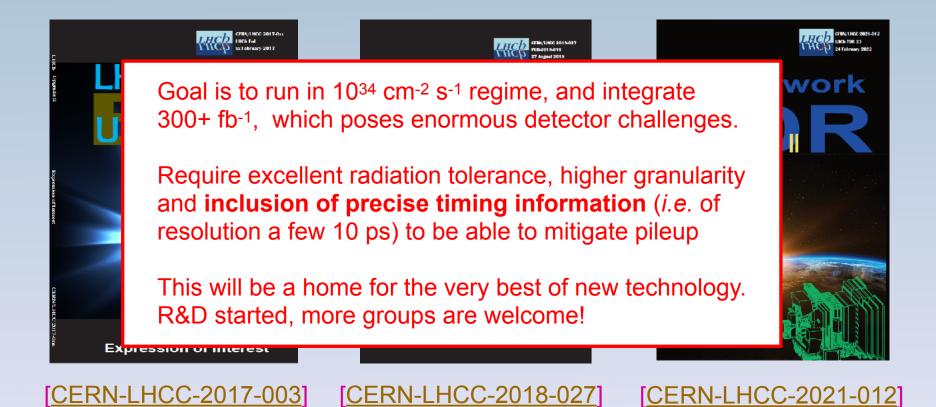
[CERN-LHCC-2017-003] [CERN-LHCC-2018-027] [CERN-LHCC-2021-012]

Now part of the CERN baseline plan. Framework TDR recently approved by LHCC.

19/10/22

LHCb Upgrade II

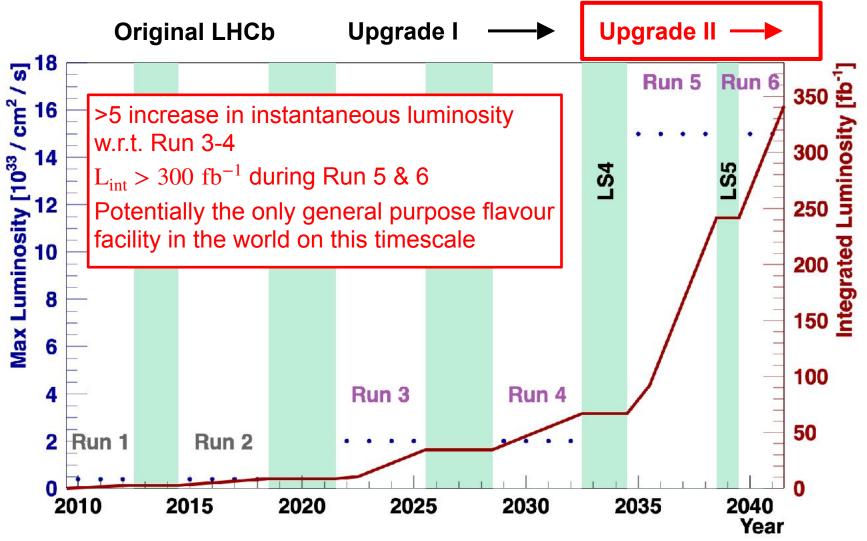
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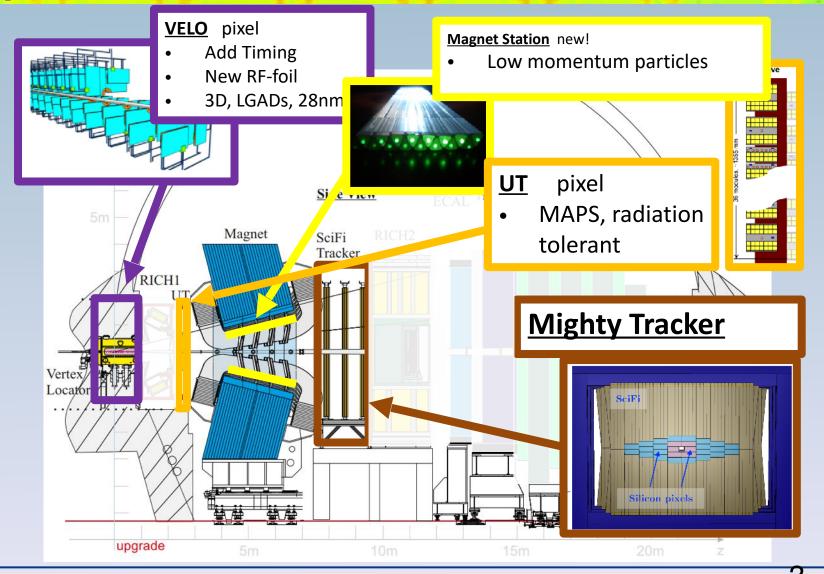
Now part of the CERN baseline plan. Framework TDR recently approved by LHCC.

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Upgrade II Timeline



Upgrade II Tracking System

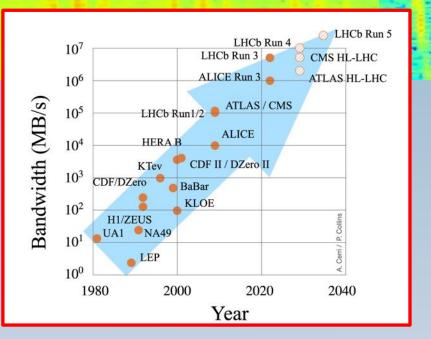


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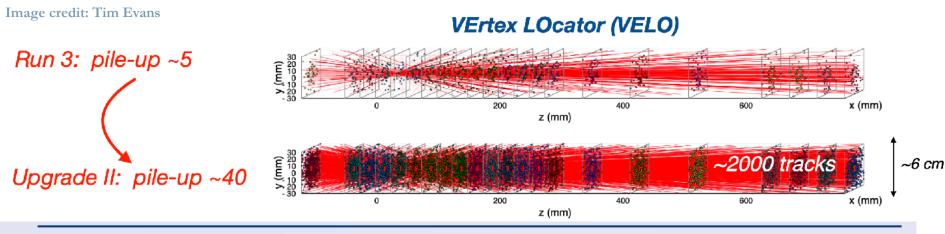
UII Detector

Upgrade II performance must equal or surpass that of Upgrade I, with

- Pile-up reaching values of 40
- 200 Tb/s of produced data
- charged particle densities up to $1 \times 10^{12}/cm^2$



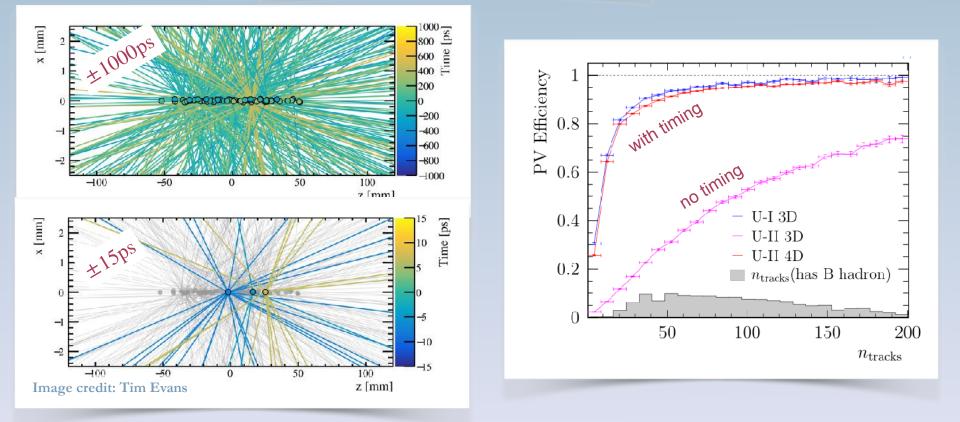
This is the **intensity frontier**! New, lightweight technologies with high granularity, timing, radiation resistance and innovative data processing all necessary to go to $\mathscr{L} \sim 1 \times 10^{34} \text{ sec}^{-1} \text{cm}^{-2}$



19/10/22

Upgrade II Detector Opportunity

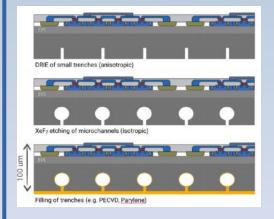
Timing to the Rescue



Alternatives to microchannels

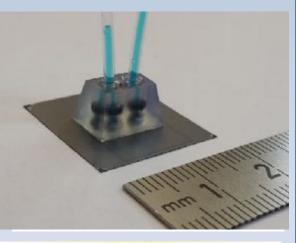
Address production cost (yield related)

- Alternative Bonding (anodic bonding..)
- Avoid mask based photolithographic techniques
- Smaller cooling plates
- Handle wafer bonded to active silicon (IFIC/MPI-HLL)
- Buried microchannels (CERN/.EPFL)



CMOS compatible process potential post processing step Holds 110 bars, leak tight to 10⁻⁸ mbar l/s

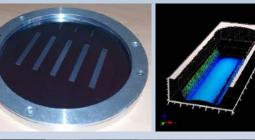
AIDA-2020-NOTE-2020-003



Most ambitious approach: bring the cooling to the tiles

R&D @ CPPM

- Laser etching and anodic bonding
- 5 x 10 channels per wafer
- 200µm x 70µm x 4.5cm per channel
- Next step: connector with anodic bonding





Alexandros Mouskeftaras, Stephan Beurthey, Julien Cogan, Gregory Hallewell, Olivier Leroy, et al.. Short-Pulse Laser-Assisted Fabrication of a Si-SiO2 Microcooling Device. Micromachines, MDPI, 2021, 12 (9), pp.1054. 10.3390/mil2091054. hal-03356892

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Alternatives to microchannels

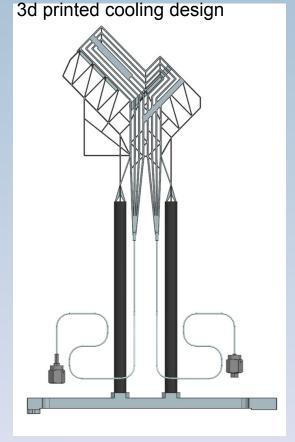
Grade 2 printed Ti: a lot of experience in industry (medical, dental)

Advantages

- strong, easy to handle, will not break
- easier to connect CO₂ pipes (welding, brazing)
- Restrictions integrated into inlet
- Fast turnaround for design changes (order of weeks)
- Fast production 25/batch, 1 batch/few days
- cheap (<500 Euro / module, including welding capillaries)

Challenges

- CTE match with silicon is worse (8.6 vs 2.6 ppm/K)
- smaller thermal conductivity (16 vs 150 W/mK)
- smaller radiation length (3.6 vs 9.4 cm)
- irregularities in printing; less flat surfaces?



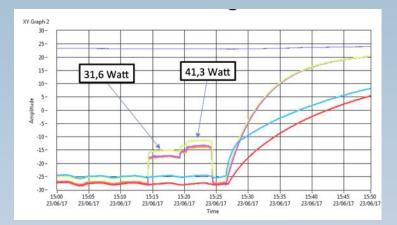
See <u>presentation</u> by Freek Sanders, "Design and Production challenges for the LHCb VELO Upgrade Modules", CERN Detector Seminar, February 2019

Alternatives to microchannels

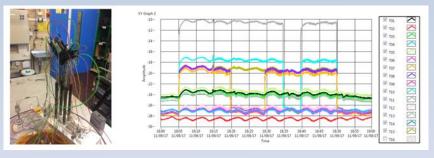


prototype fitted with heaters

- high pressure test to 250 bar
- Leak tight with 250 µm wall



successful cooling test (ΔT~13°C)



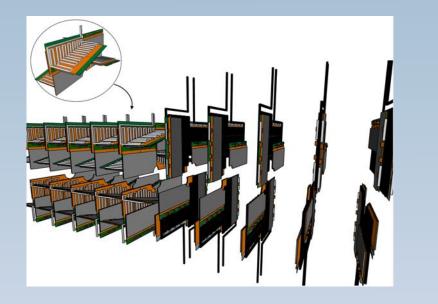
successful flow and stability test ($\Delta T \sim 13^{\circ}C$)

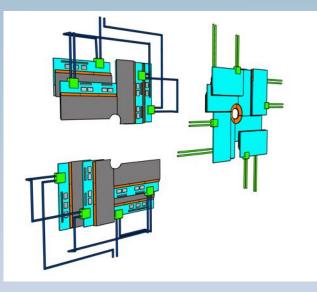
R&D 3d printed substrates made extremely rapid progress and were a credible backup alternative for LHCb. At the time of development the microchannels were sufficiently mature to be chosen as the implementation for Run3

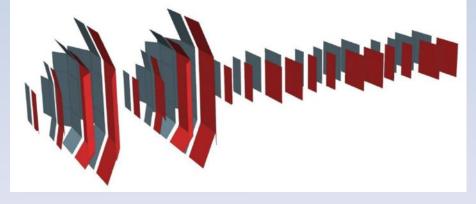
19/10/22

A bit of hist.

Many types of geometry possible...





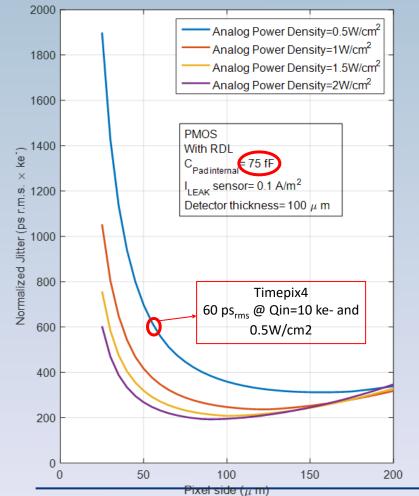


3d printed technology already in active development for UII May give the flexibility required for a cooling "skeleton" Many issues of connectivity to be solved

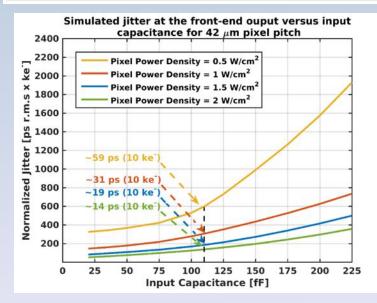
19/10/22

ASIC requirements & Limits

Slide complied by Vagelis Gkougkousis



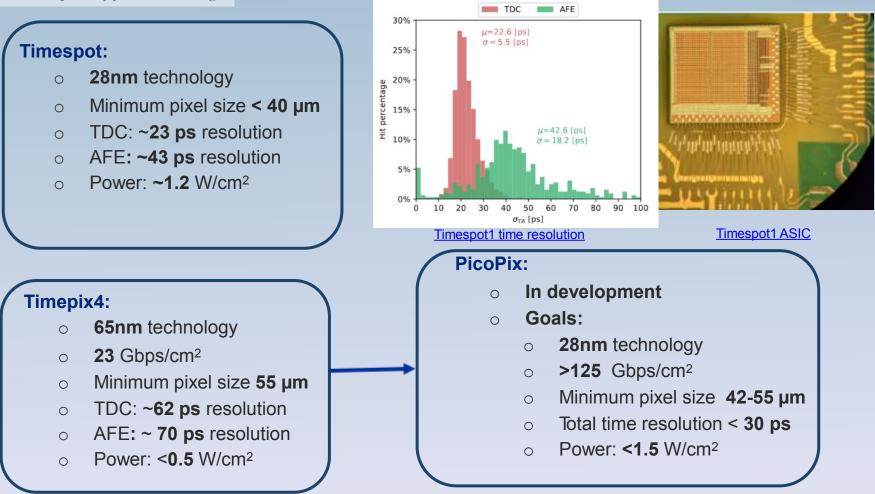
Requirement	scenario ${\cal S}_A$	scenario ${\cal S}_B$
Pixel pitch [µm]	≤ 55	≤ 42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget $[W/cm^2]$	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e ⁻]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of $2 \text{ cm}^2 \text{ [Gb/s]}$	> 250	> 94

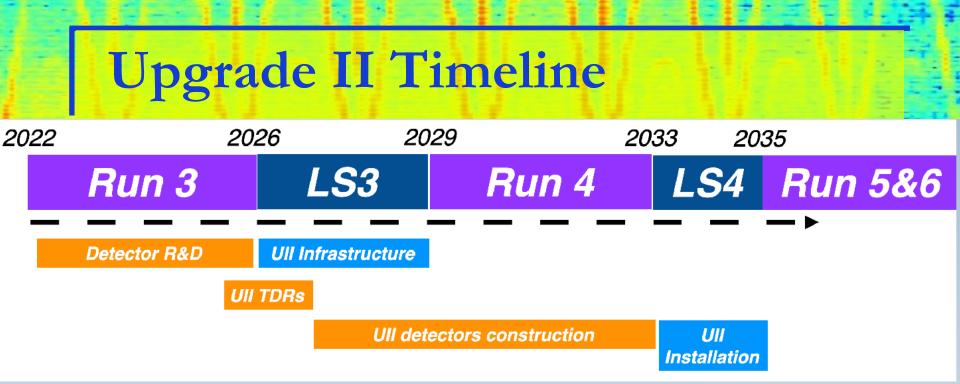


19/10/22

ASIC precursors

Slide complied by Jakob Heimberger





- ~4 year period for detector R&D, make technology choices and optimise the detector design
- TDRs expected at beginning of LS3, then ~6 year period for detector construction → being ready for LS4 installation is of primary importance
- Significant infrastructure preparation during LS3, to optimise LS4 duration
- Limited size detector consolidations also proposed for LS3 as anticipation of Upgrade II

Upgrade II needs a significant expansion of the collaboration

Conclusions

LHCb Upgrade I: Commissioning NOW!

VELO is fully installed and operational, first full closure TODAY!

LHCb Upgrade II: unique opportunity for an ultimate precision flavour physics and general purpose experiment in the forward region.

EOI, Physics Case and FTDR approved by LHCC/RB Strong support received in European strategy

Very challenging project \Rightarrow lots of R&D ongoing on all sub-systems New technologies needed, now is a great time to join the collaboration

Conclusions



19/10/22