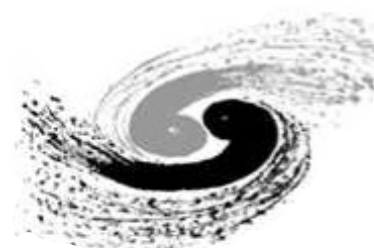


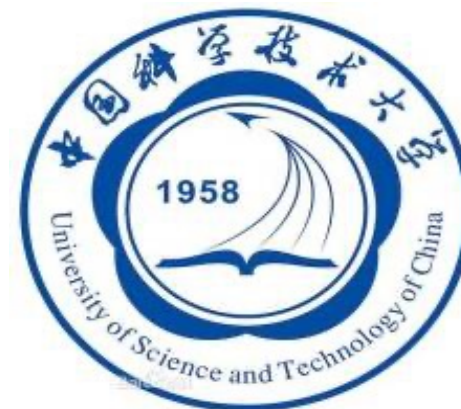
国家重点研发计划

R&D and Verification of Key Technologies for a High Energy Circular Electron-Positron Collider

Zhijun Liang for CEPC MOST2 vertex detector team

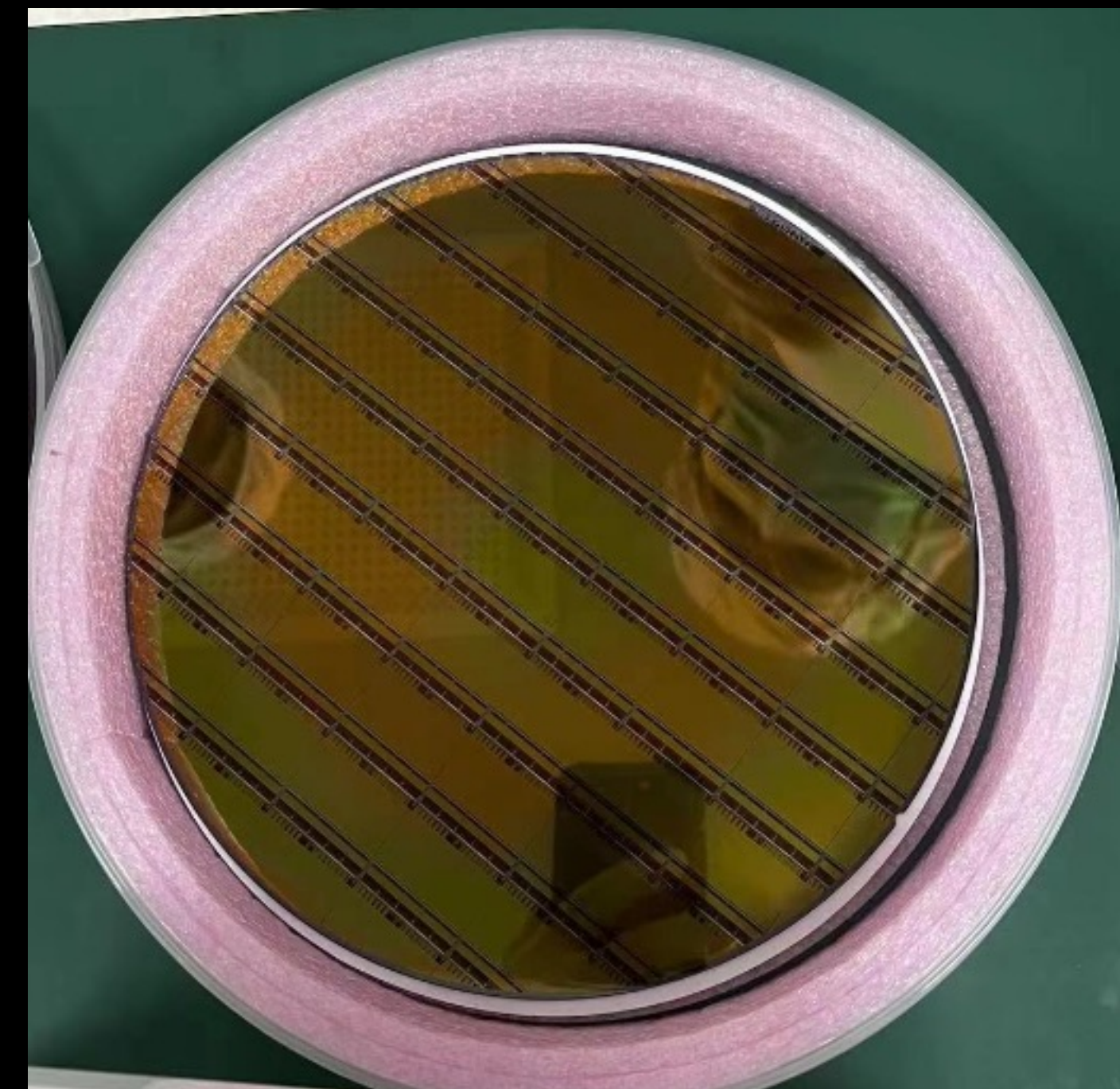


中国科学院高能物理研究所
*Institute of High Energy Physics
Chinese Academy of Sciences*



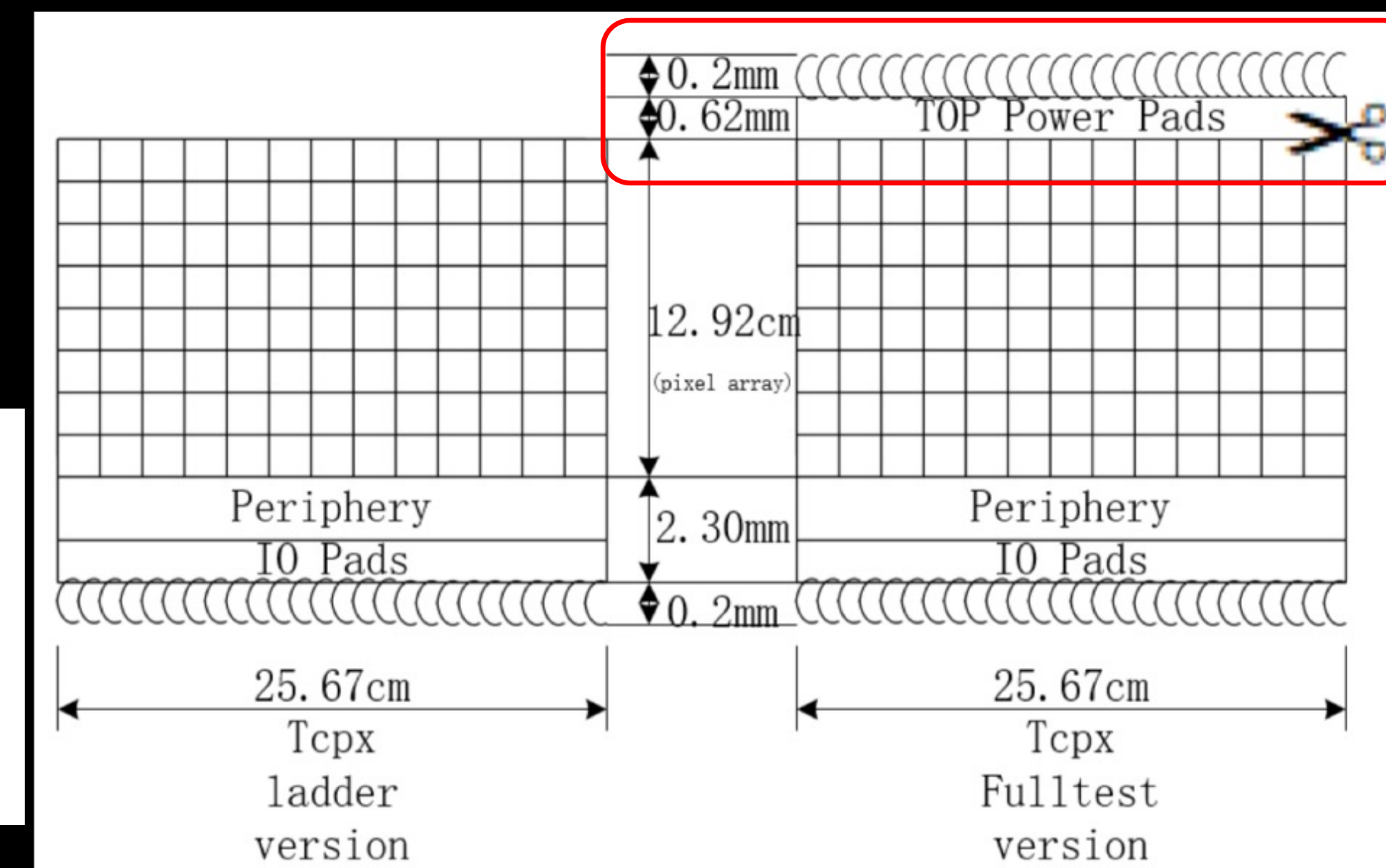
News about Taichupix3 production

- 6 Taichu3 wafers are ready.
 - Wafer arrival at IHEP in 5th July 2022
 - 3 wafers (standard process) + 3 wafers (modified process)
- Send 4 wafers to NCAP for wafer testing , thinning and dicing
- Send 1 wafers for thinning (150um) and dicing
 - 1st round: Send 5 chips for wired bonding, 2 boards working
 - 2nd round Send 5 more chip, ? working
 - 3 chips with normal dicing (top and bottom pads available)
 - 2 chips dicing without top pads
- IR drop is not a problem ?
 - Low resistance → after power on, resistance become normal ?



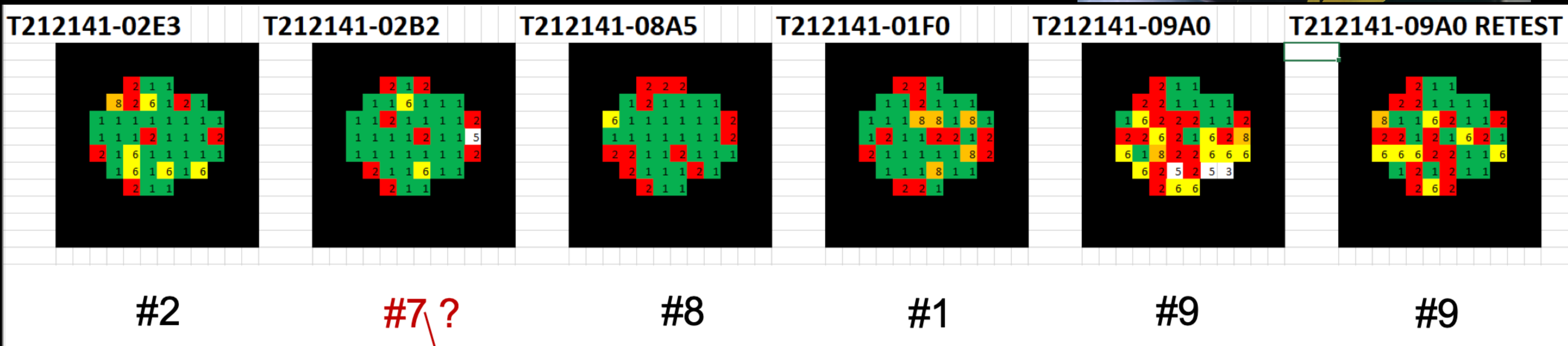
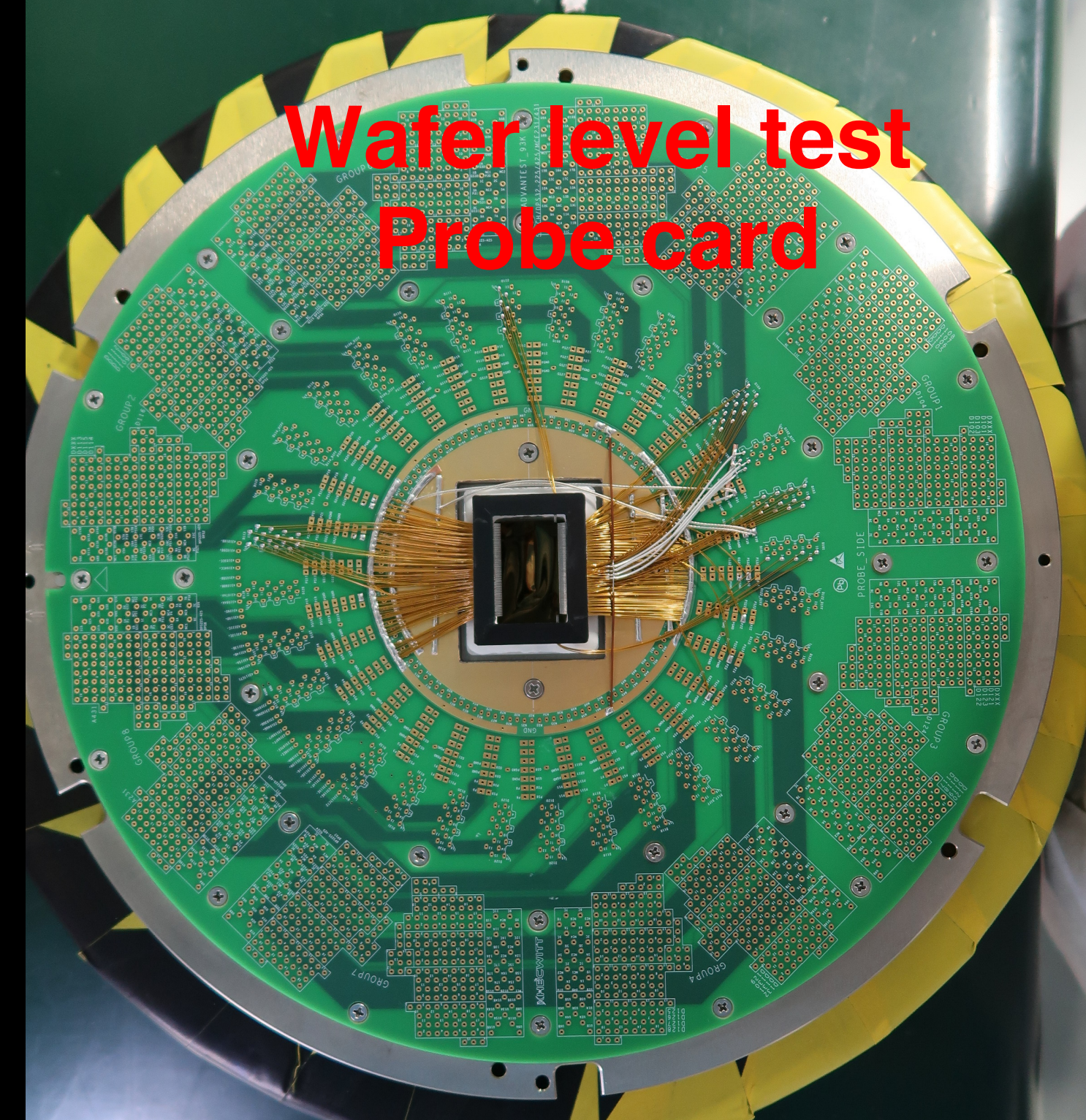
➤ After wire-bonding, around half of chips have low resistance (< 10 ohm) of DVDD

Chip num.		After gluing (ohm)	After bonding (ohm)	After power on
#8	AVDD		15k	4.4k
	DVDD	5	3	3.3k



Taichupix3 wafer-level testing

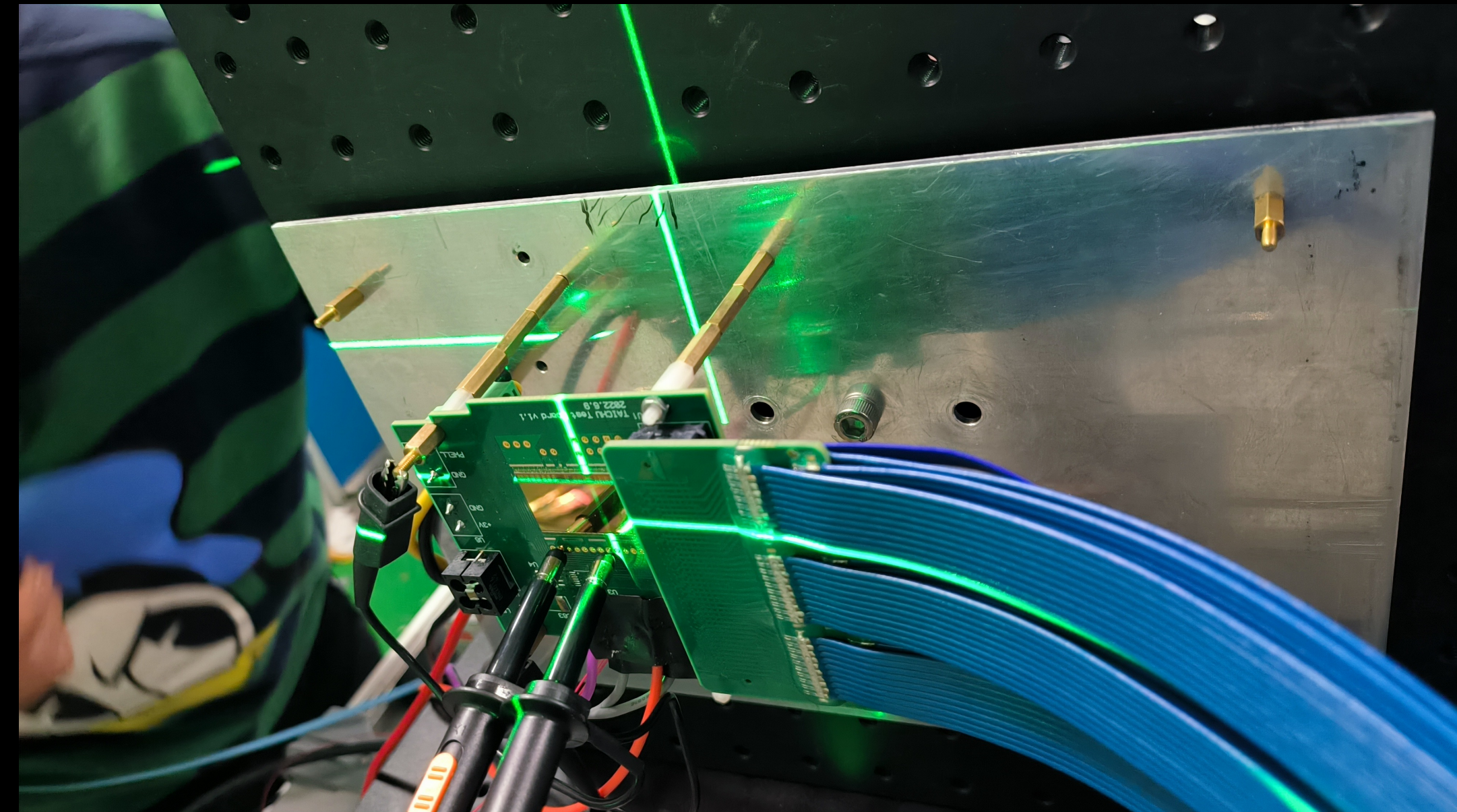
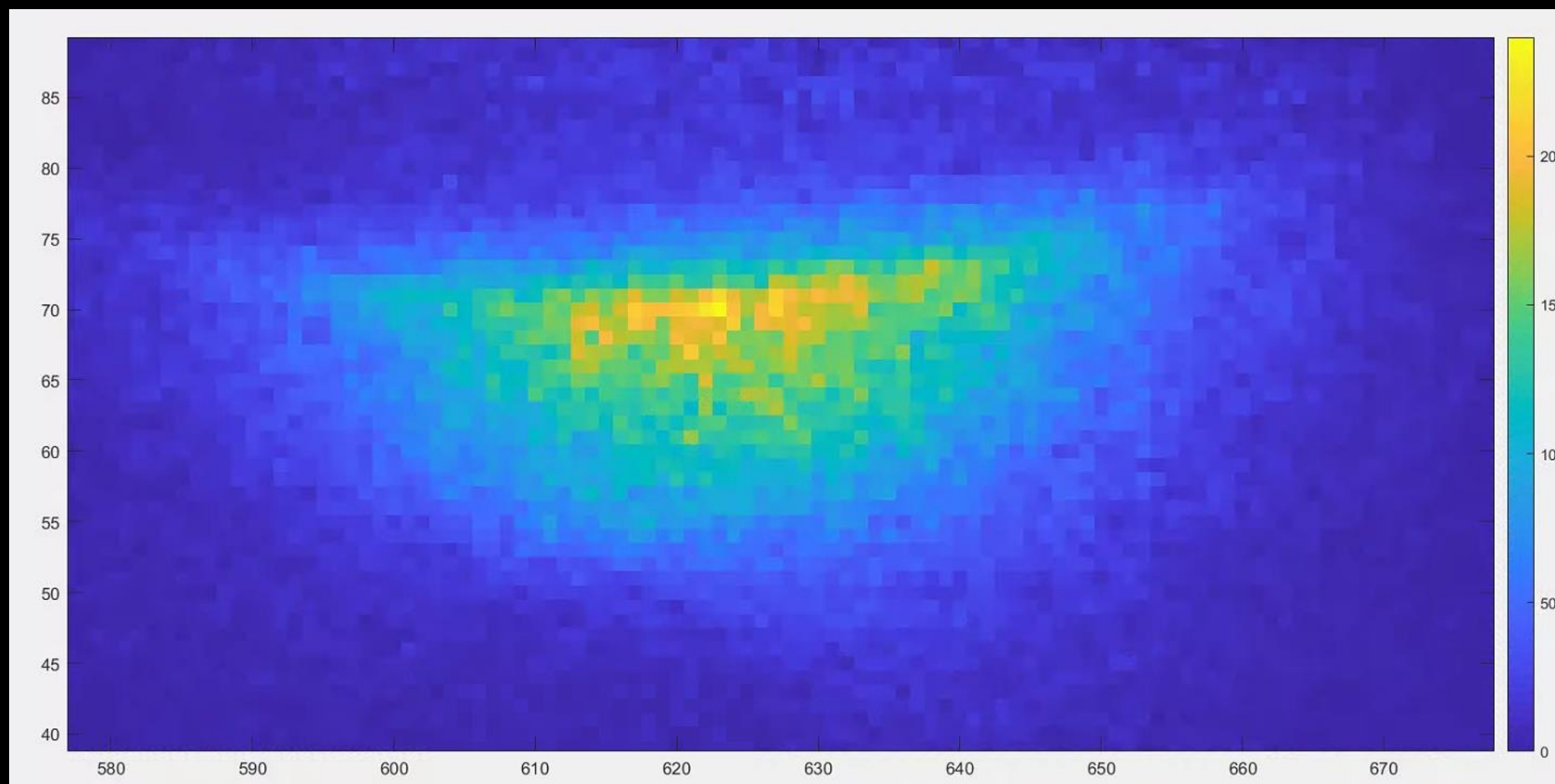
- Single chip test board testing on-going
- Wafer level testing in NCAP (on-going)
 - Reasonable yield in standard process (wafer 1,2,3)
 - Still need to check modified process (wafer 7,8,9)
 - May need to bias the sensor,not possible to bias it on the flex
 - Thinning



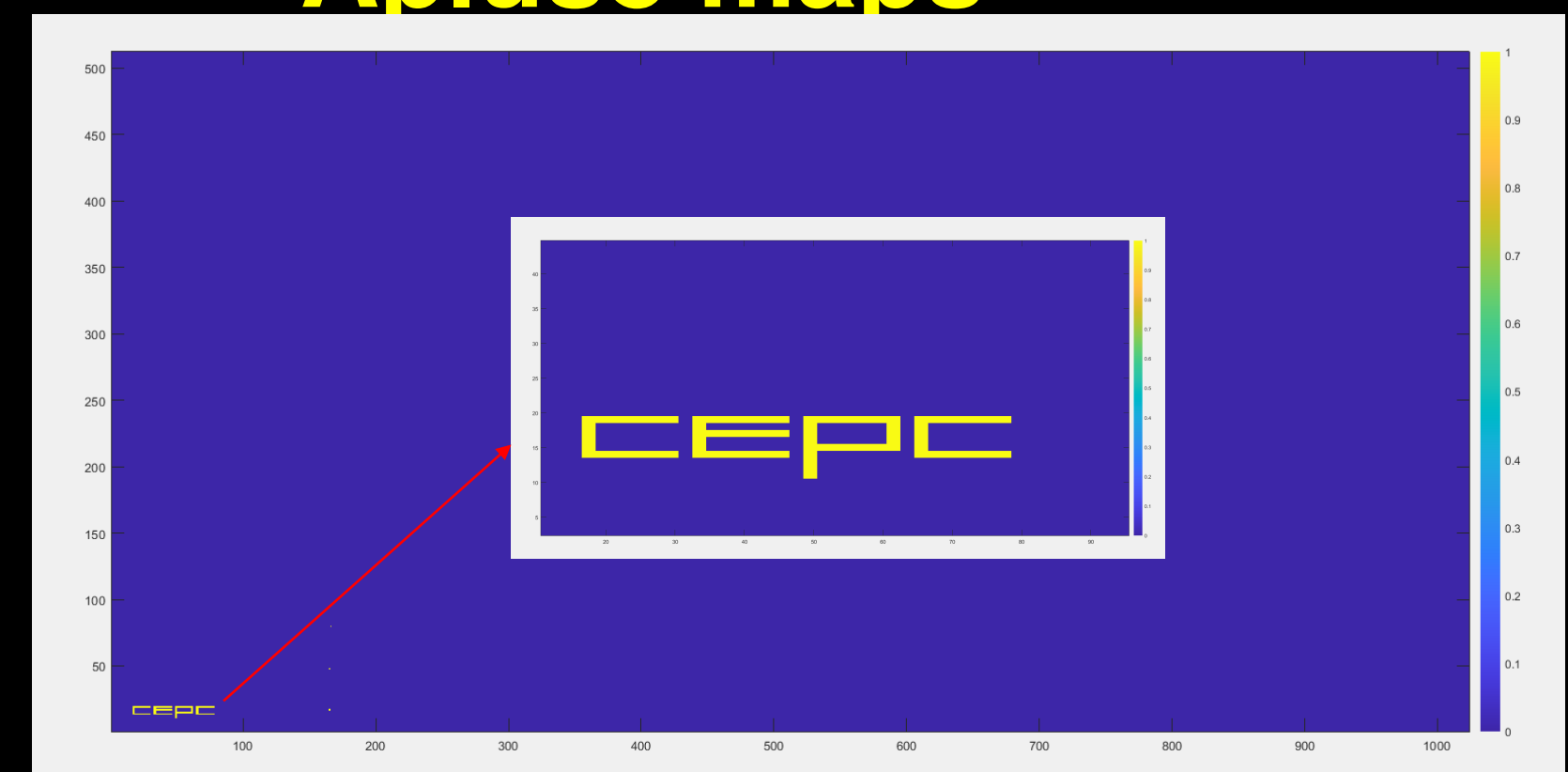
TaichuPix3 tests

- Functionality of the full signal chain proved with laser tests
- Threshold scan in Beta source tests
- Irradiation tests
 - Irradiation and Tests in BSRF
 - X ray machine is ready now ?

BSRF (new!)

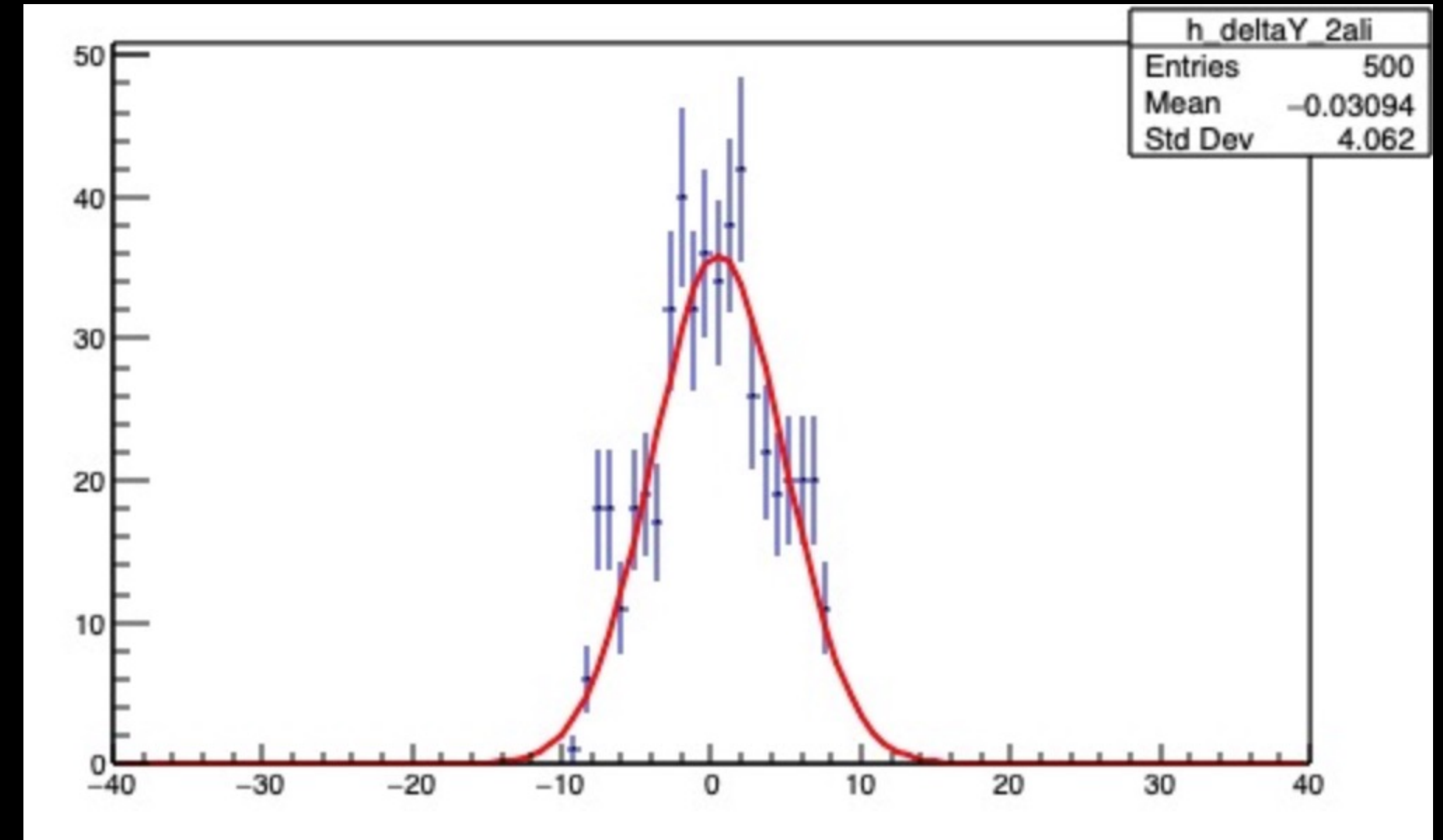
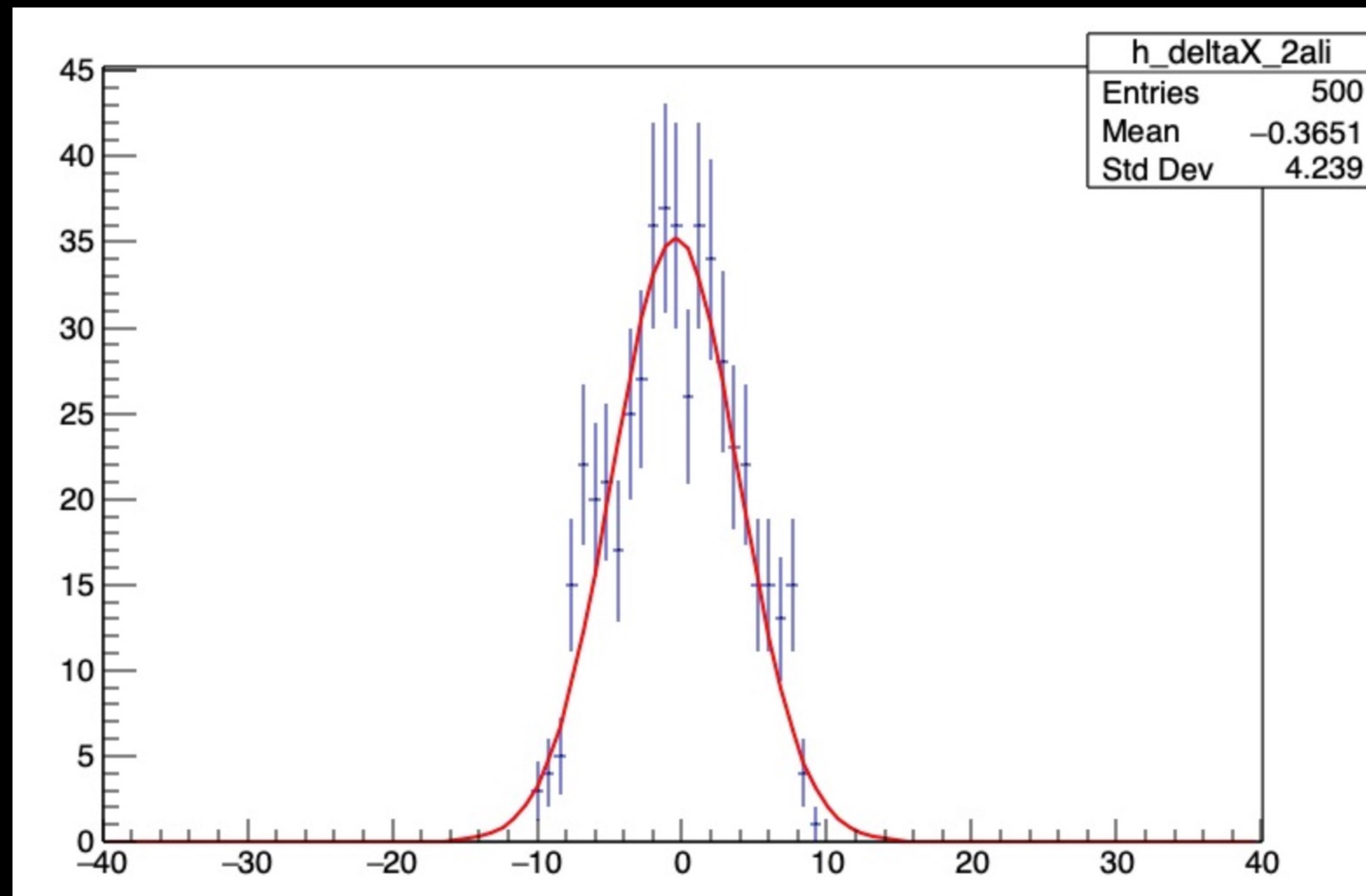


Apluse maps



Laser test with Taichupix2

- Reach 4.4um resolution using back-side infra-red laser injection.

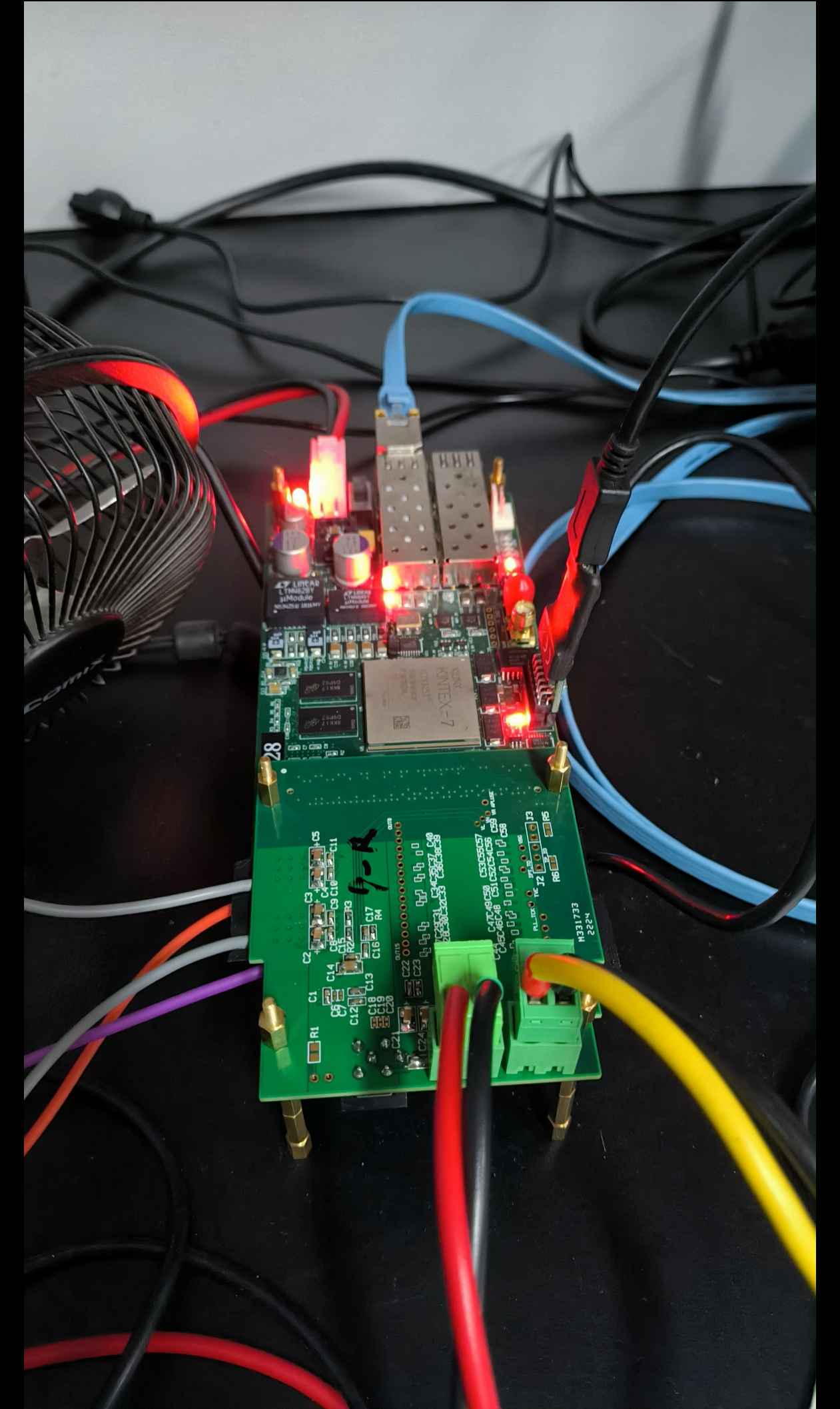
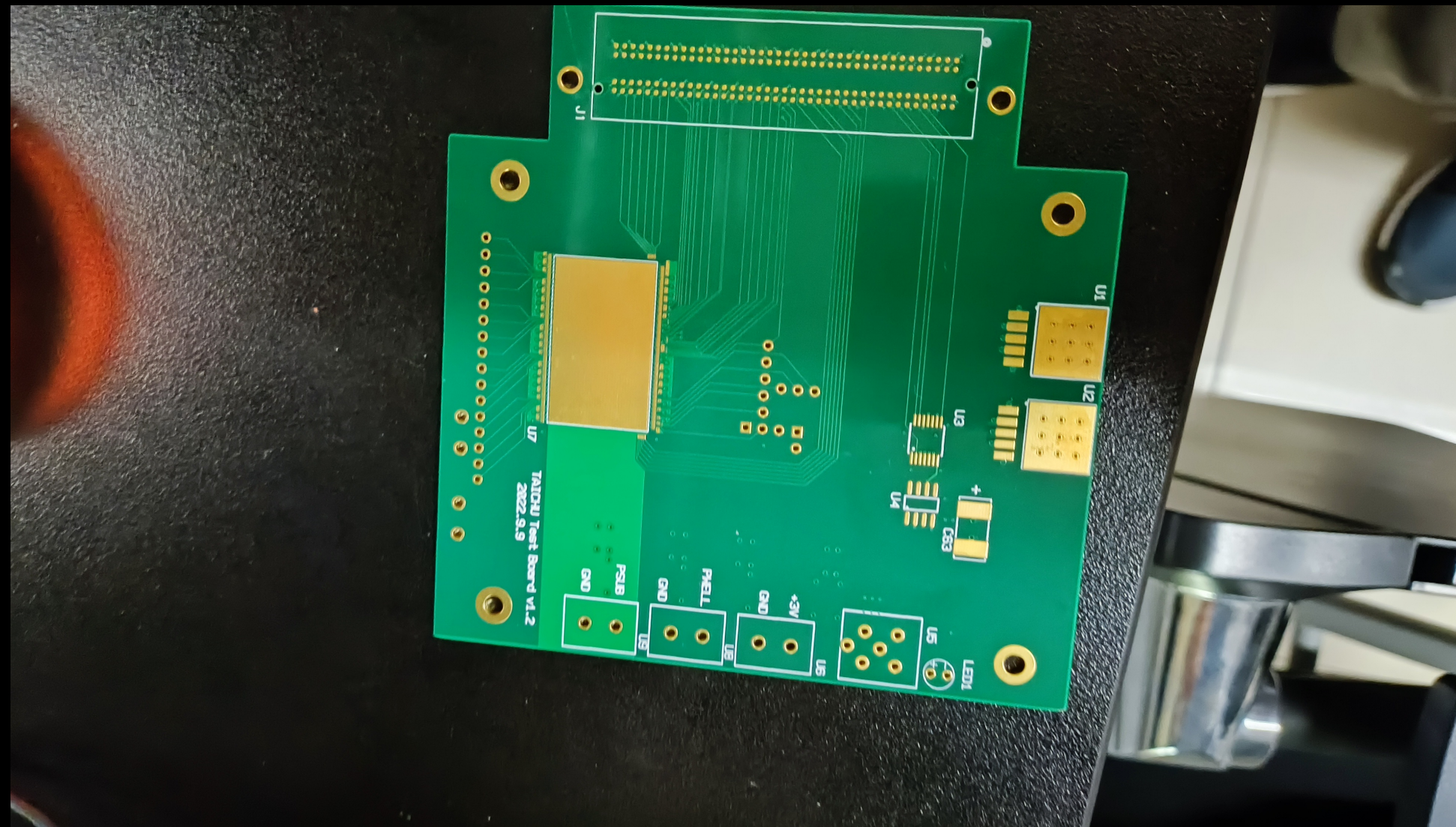


TID radiation test in BEPC BSRF in middle of Oct

- The current version of single chip board can be used ?
- Or shall we switch to 2nd version single-chip board
 - **Components are further away from TaichuPix chip**
 - **X ray can have larger distance to FPGA (safer ?)**
- Shall we try to overlay two single-chip boards
 - To catch some electrons events ?

current version of single chip board

2nd version of single chip board

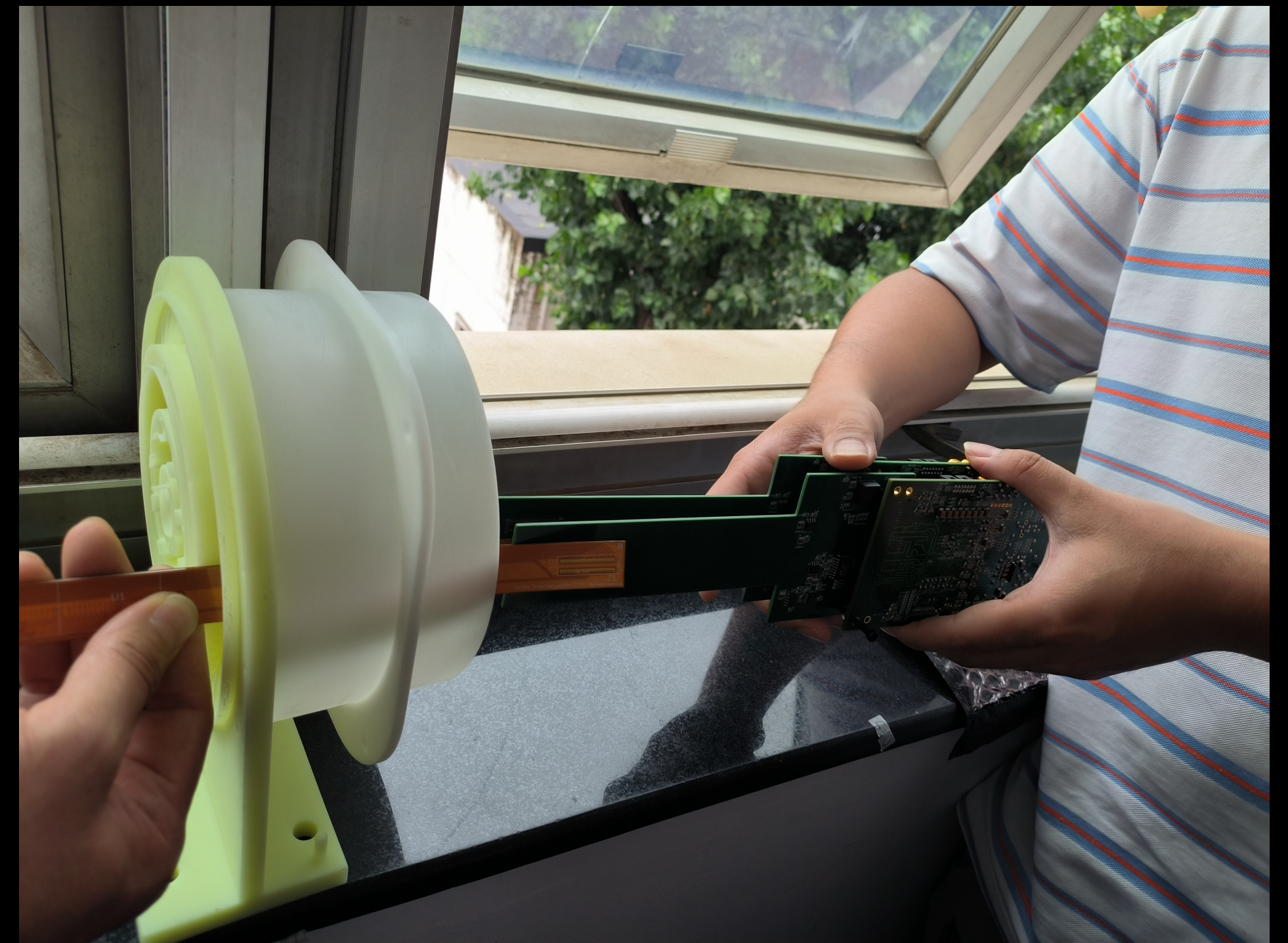
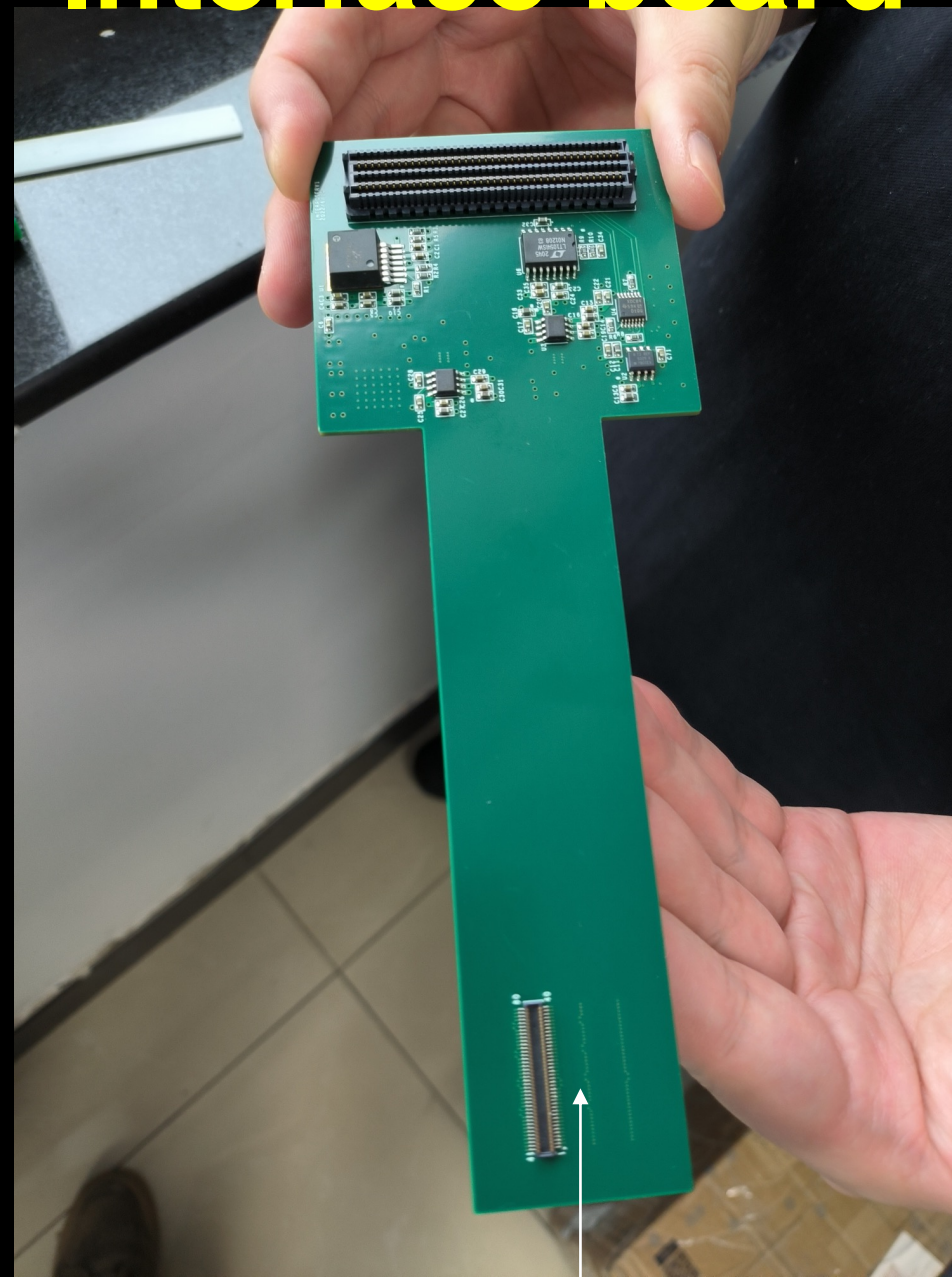


Flex and interface board

- Interface board was planned to have soft+hard PCB design
 - Interface board is to connected the flex and FPGA board
- Due to low yield, switched to hard PCB design, no flexible components
- Expect no much impact to support structure
- Time scale for 2nd version of interface board , ready
 - Connector position in 2nd version (better to be in the middle)
- Board for Clock and synchronization ~available, to be tested

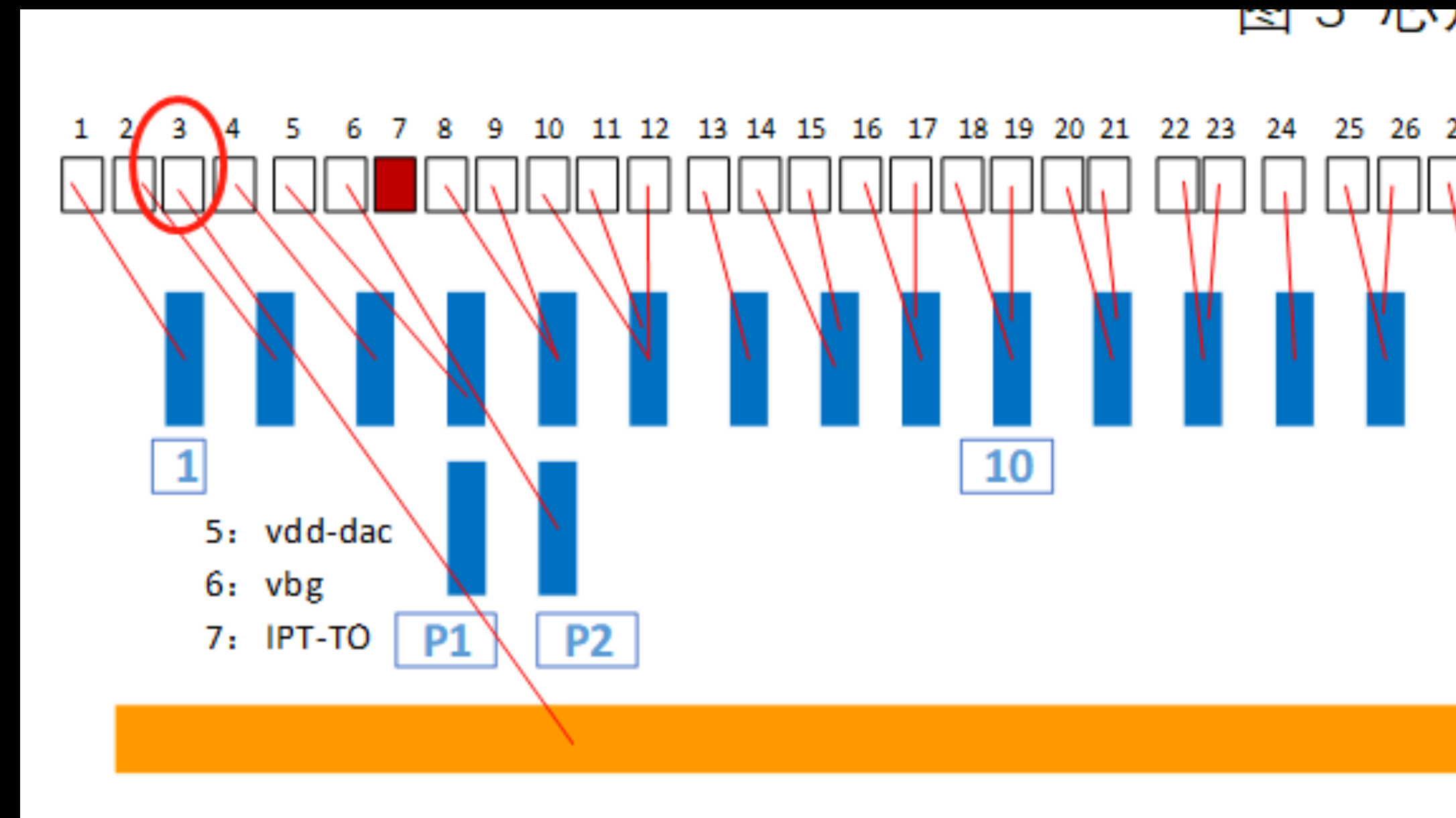
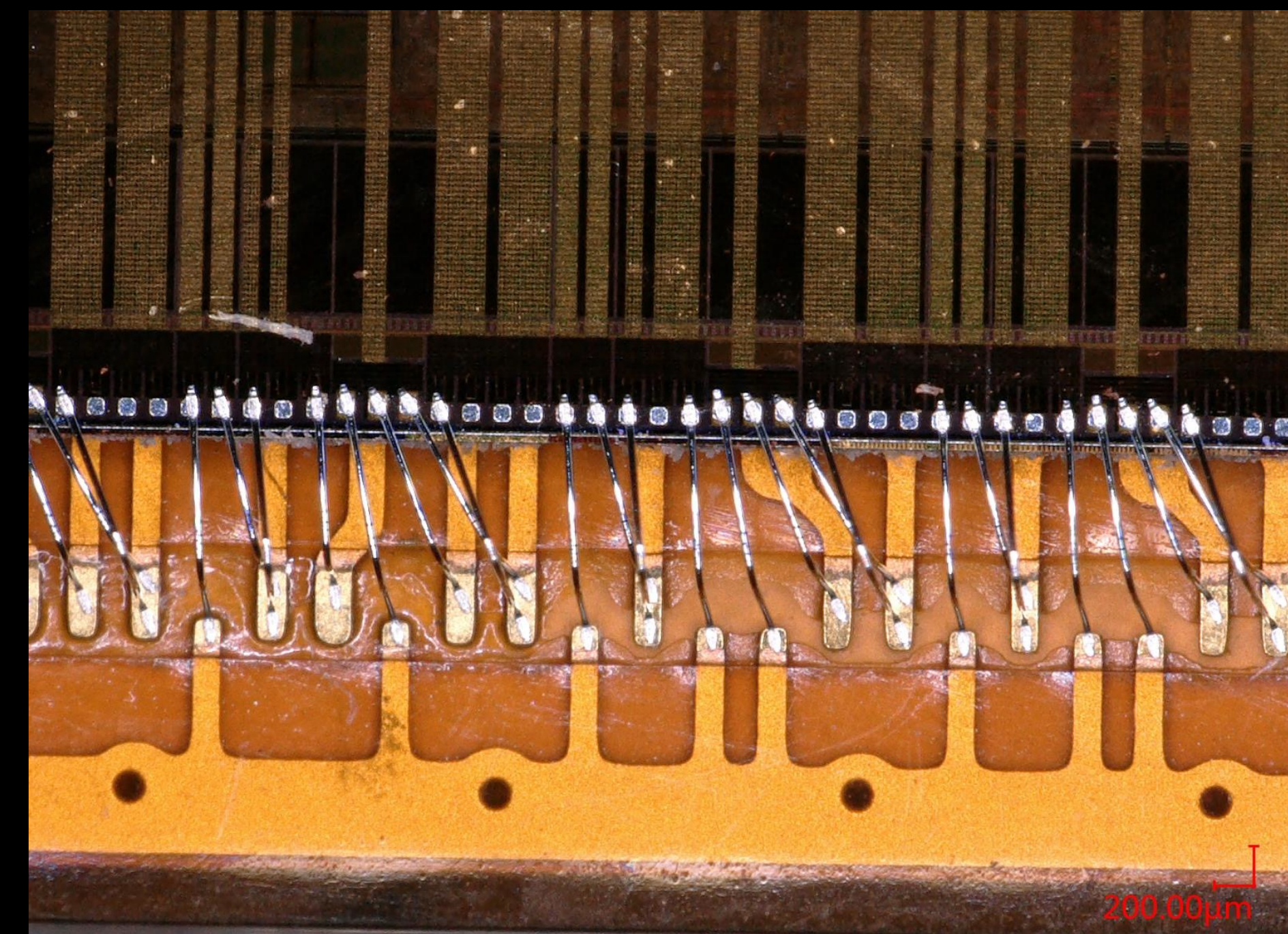
Interface board+FPGA +flex

Interface board



Flex and interface board

- 2nd version of the flex submitted. **Still not produced yet , expect this week**
- **Submitted date (September 18th)or two-layer design, Sep 26^t for 4th layer**
 - Enlarge opening of the pad on flex (100um * 400um)
 - Add bus for ground for wire bonding
 - Modified the position of the hole
- **Change the position of the connector (on the other side of the sensor)**
- Testing with single chip 1st version flex with wire bonding
 - **Large leakage current ? Resistance increased after powering on ?**

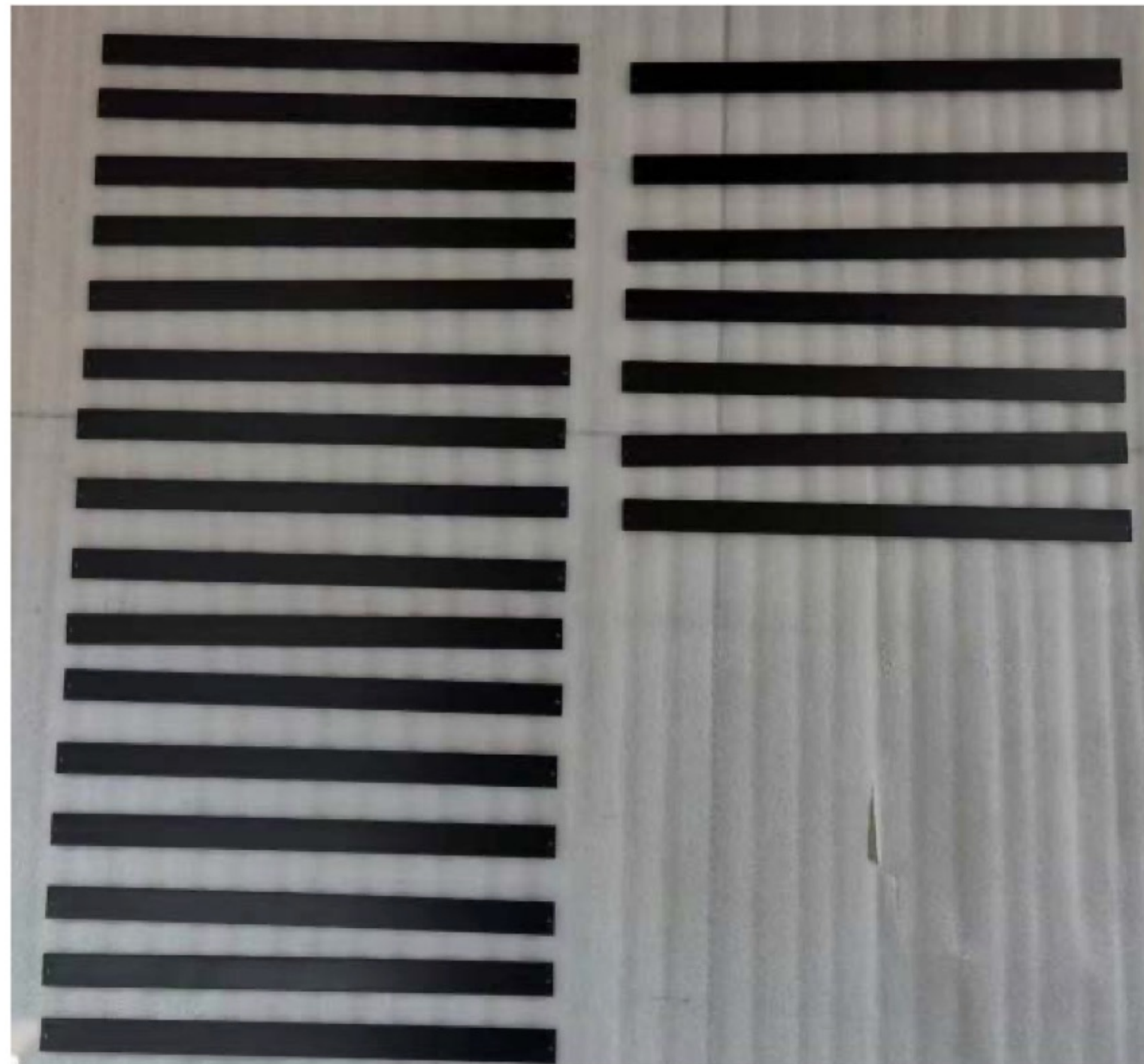


Support structure of the ladder

Ladder support production

- Production of ladder support with carbon fiber is in good progress
 - Half of the ladder support has been produced. (IHEP designed)
 - The yield of first batch of production is a bit low ($\sim 30\%$)
 - New batch of production has higher yield
 - Expected 120 good ladder support in this production

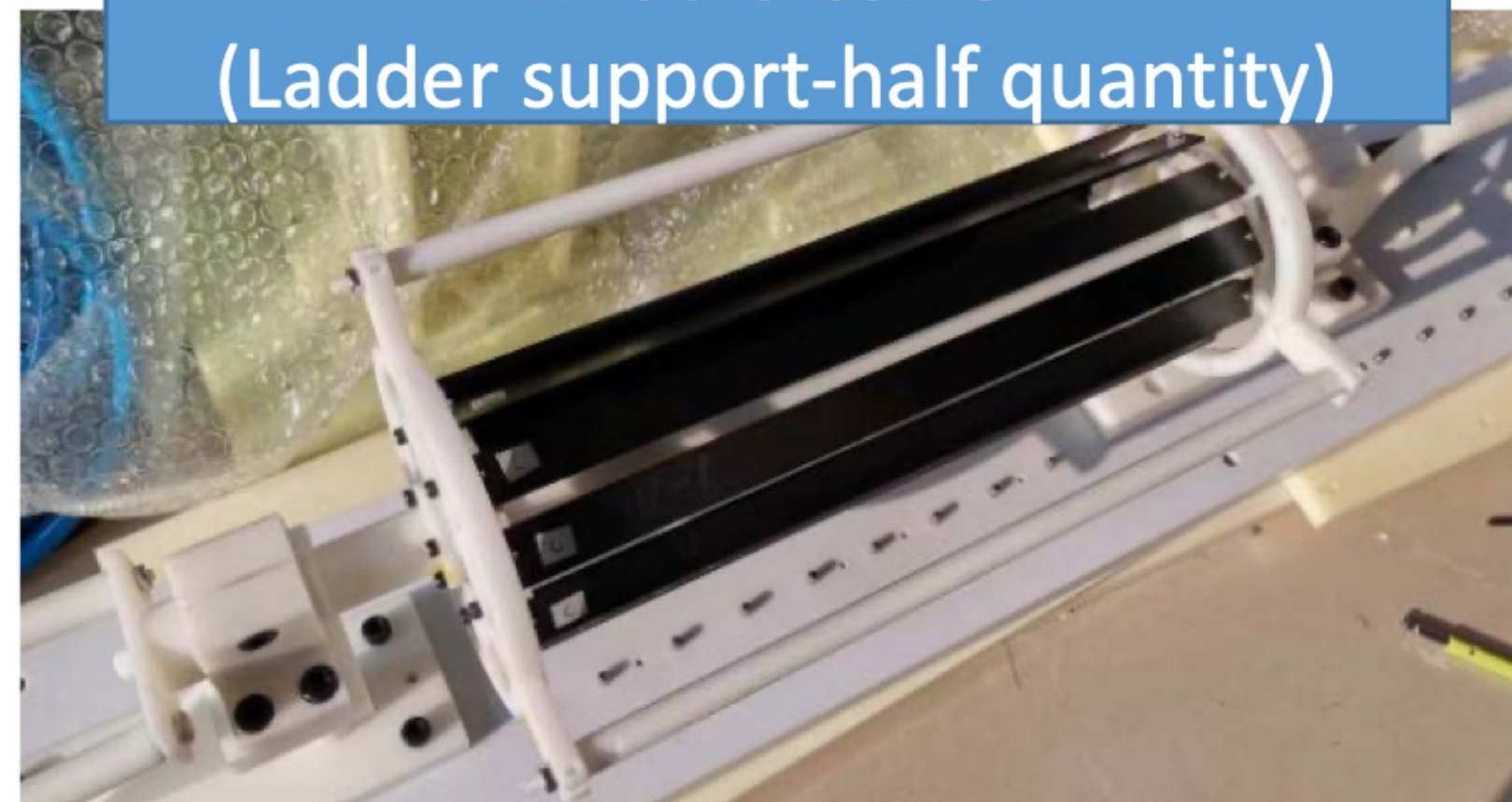
New batch ladder support



Inner barrel



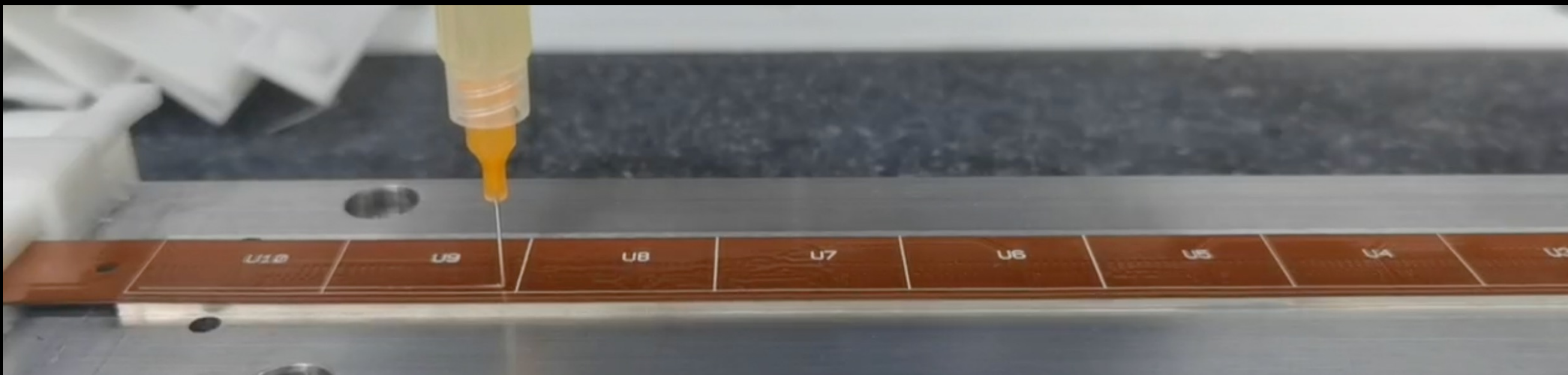
Middle barrel
(Ladder support-half quantity)



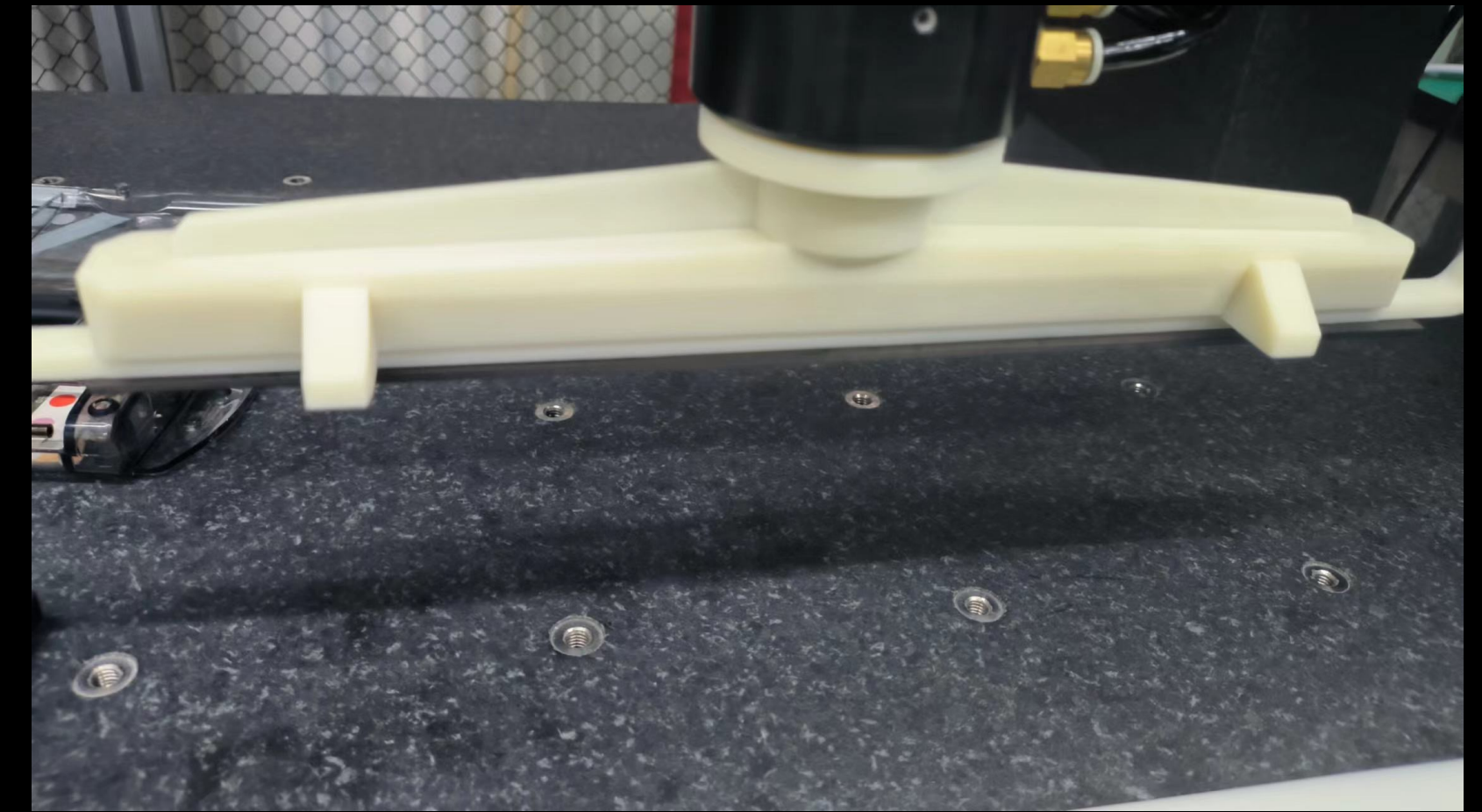
Detector module(ladder) assembly

- Progress in assembly in ladder
- **Dummy**
 - 2 flex with 10 glass dummy ASIC assembly
 - Automatic glue dispensing using gantry
- **Real chip**

Wire bonded one Taichu3 on flexible PCB
Jun and Ziyue are testing it with interface board



New pickup tools

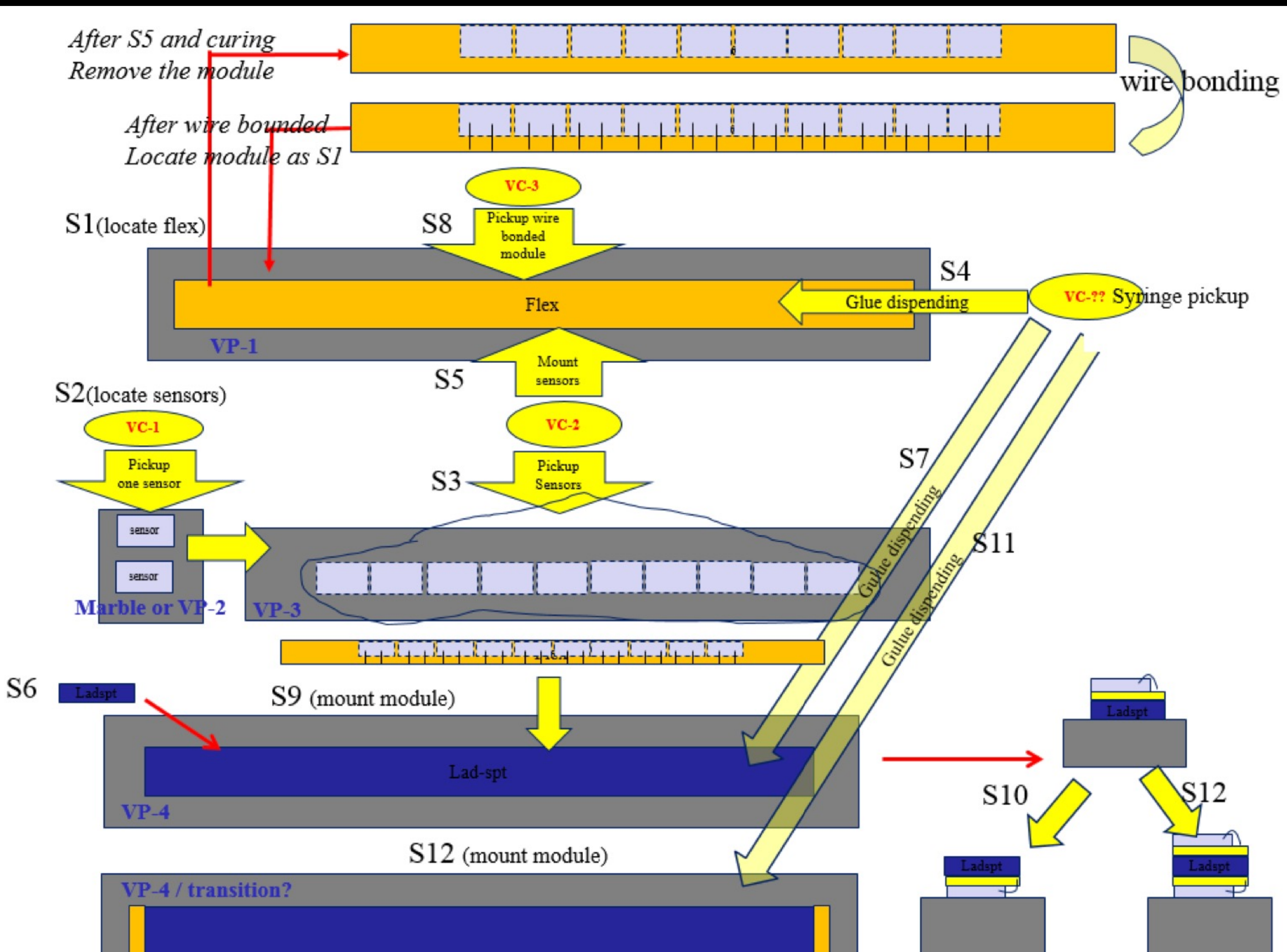


Setting up wire bonding station For full-size detector module(ladder)



Ladder assembly

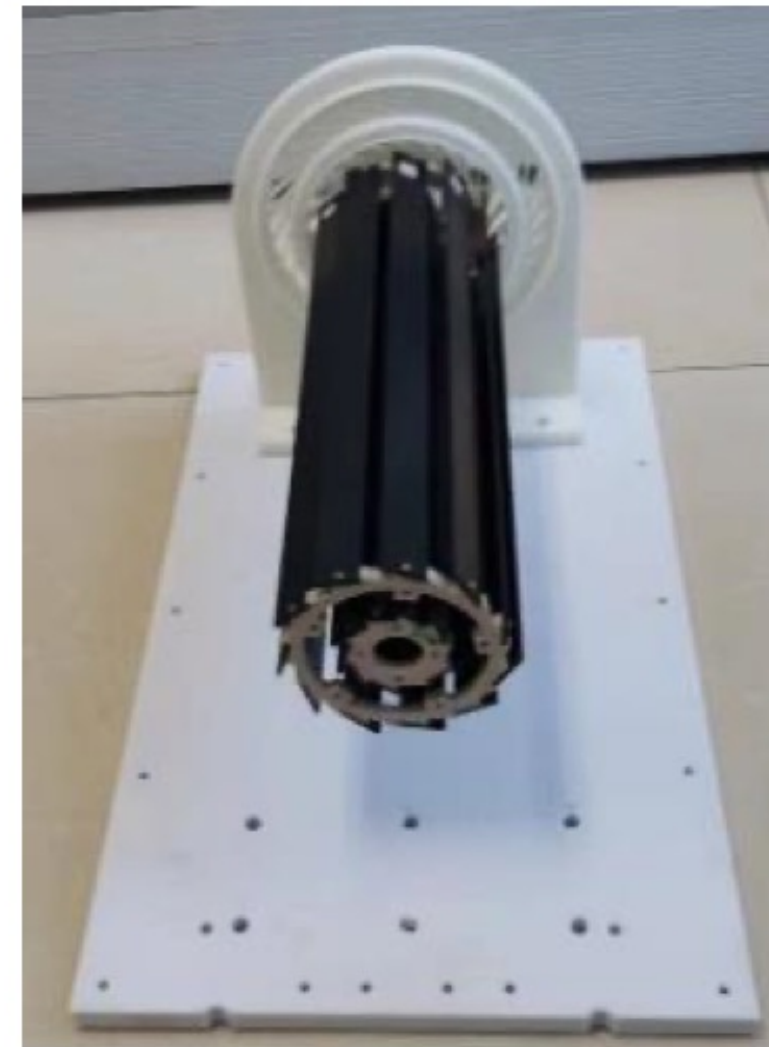
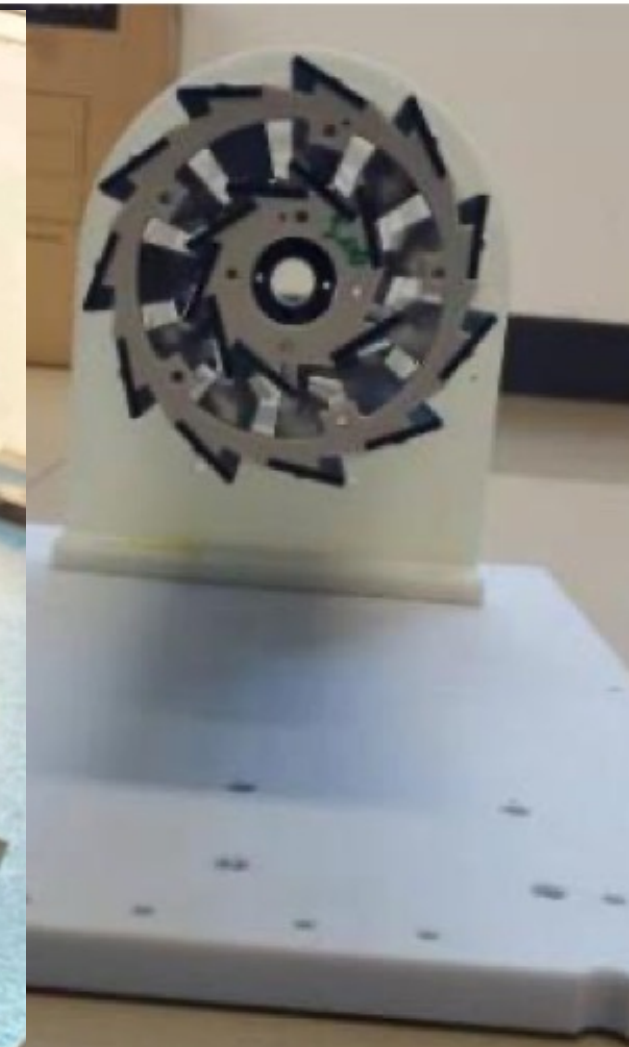
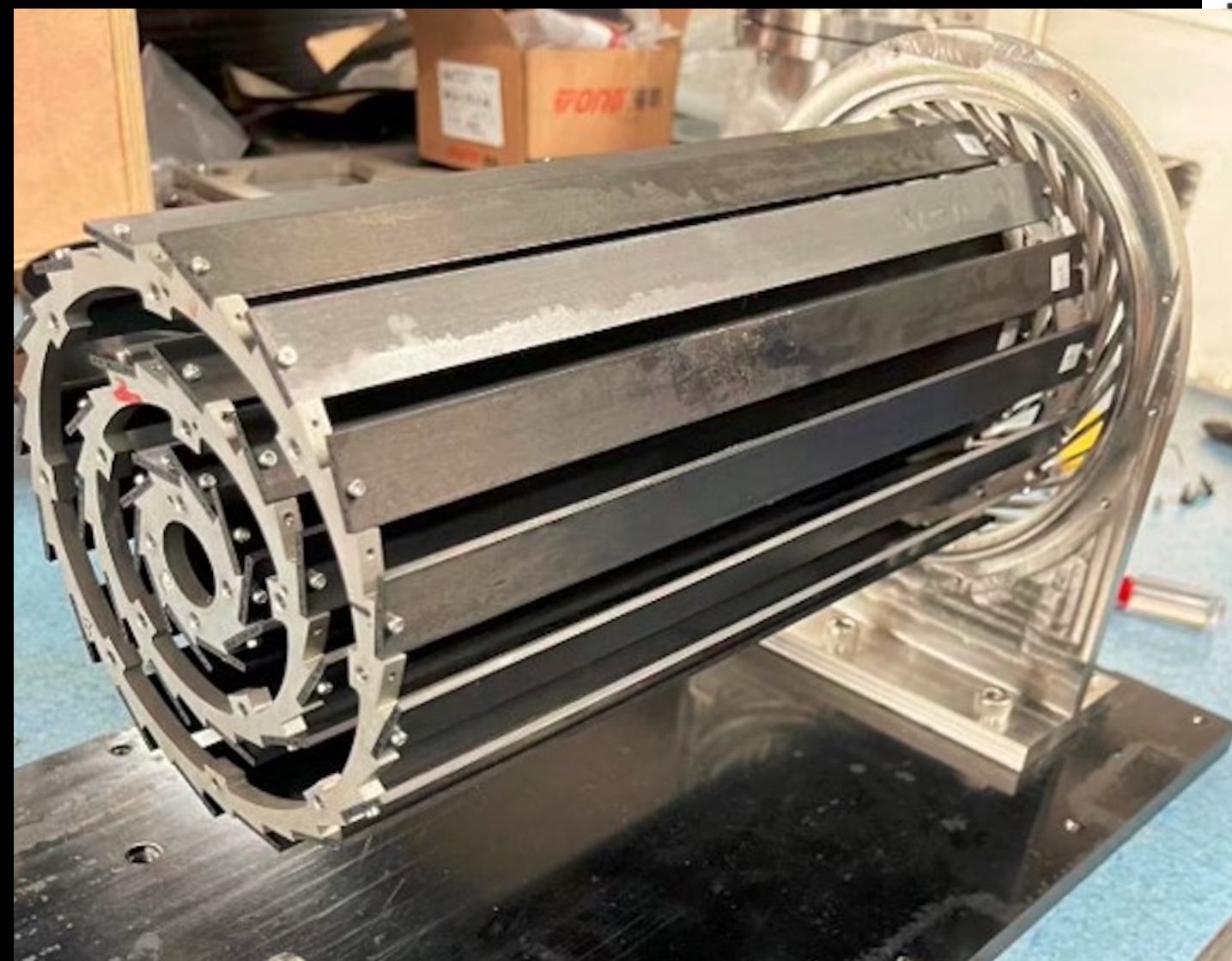
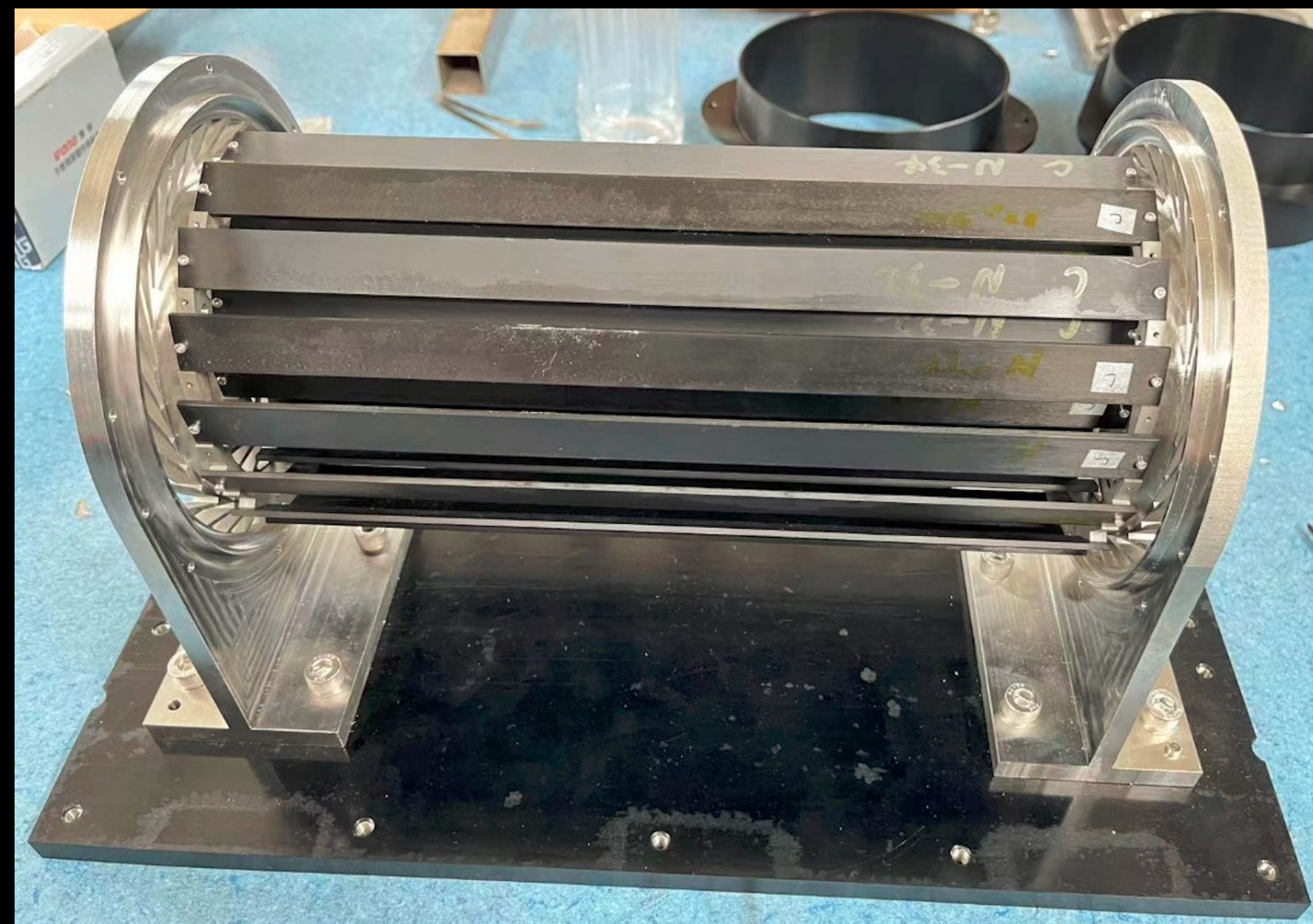
- Ladder (double side)= 20 ASIC chips + two flexible PCB + carbon fiber support
- Ladder assembly procedure verified with dummy ASIC (glass)



Vertex detector prototype assembly procedure

- Ladder installation procedure designed
- Mockup with 3D printing production done
- Assembly with 3D mockup model
- Production with aluminum machining done
 - Will be at IHEP early Oct

Prototype support with aluminum machining

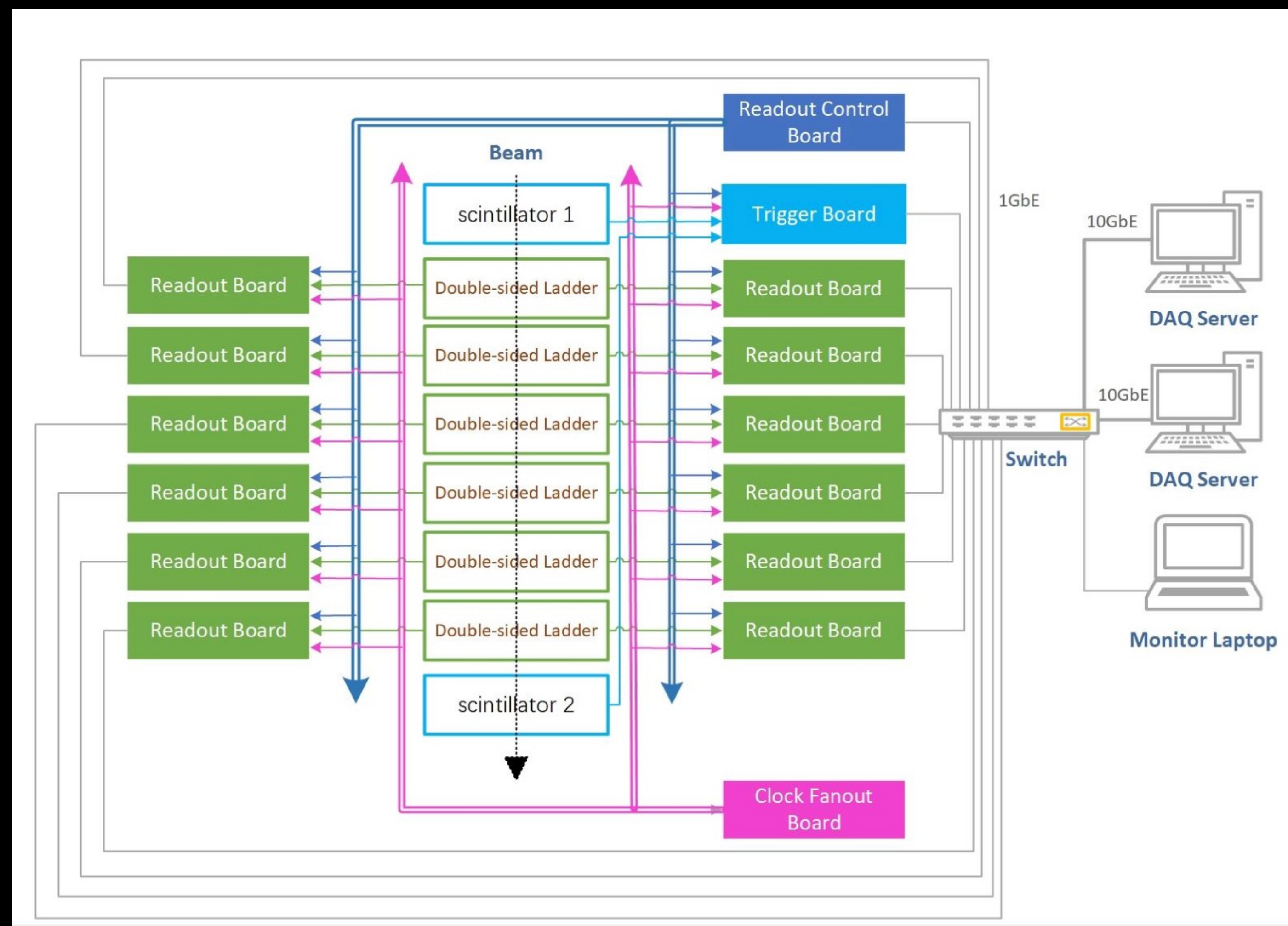
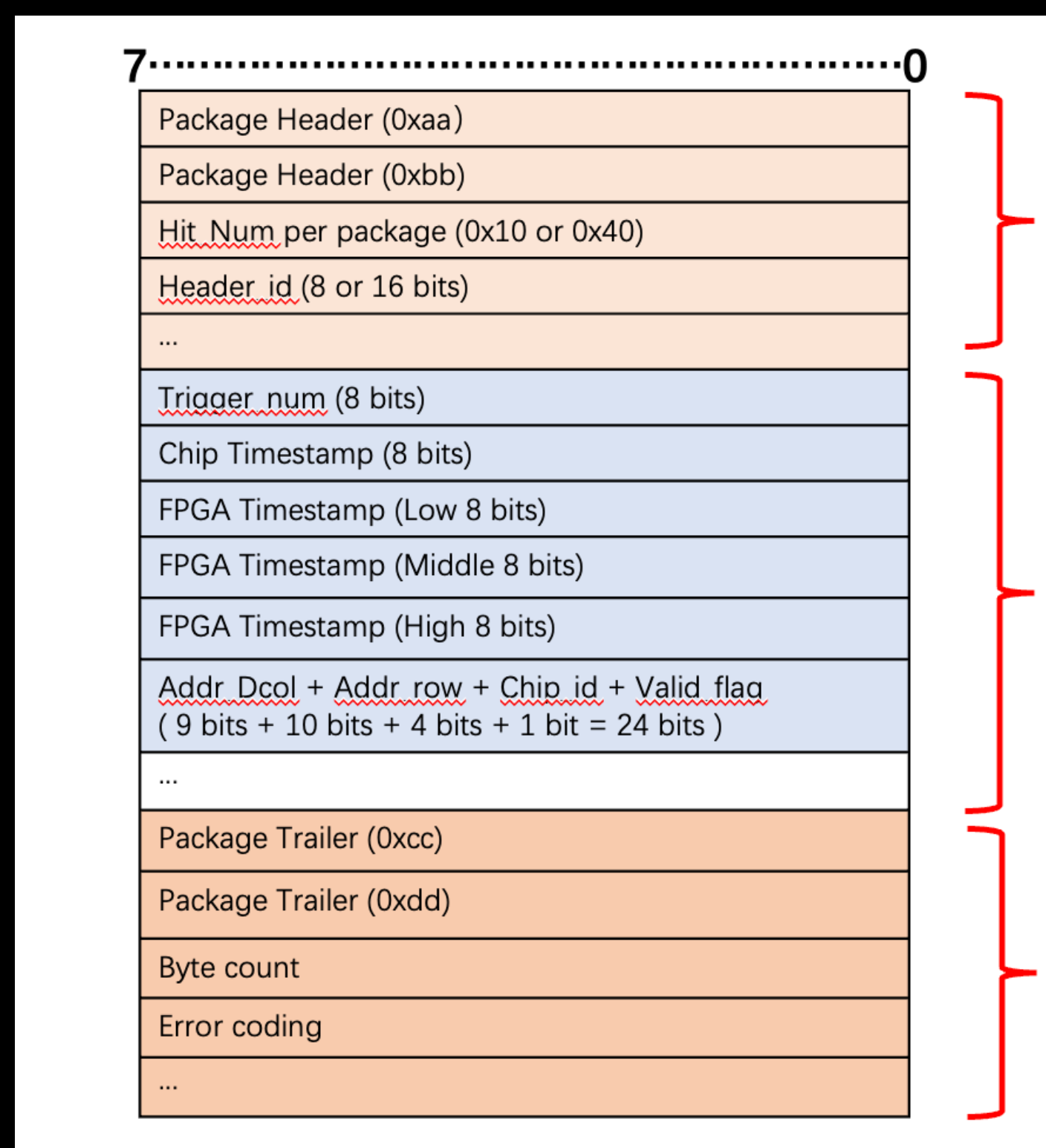


DAQ Architecture development

- Try to config single chip test board and data handling with DAQ software (done)
- Purchase DAQ PC for data taking (done)
- **Parallel processing multi-chip (next step)**
- Hit maps on-line monitoring

DAQ

data structure

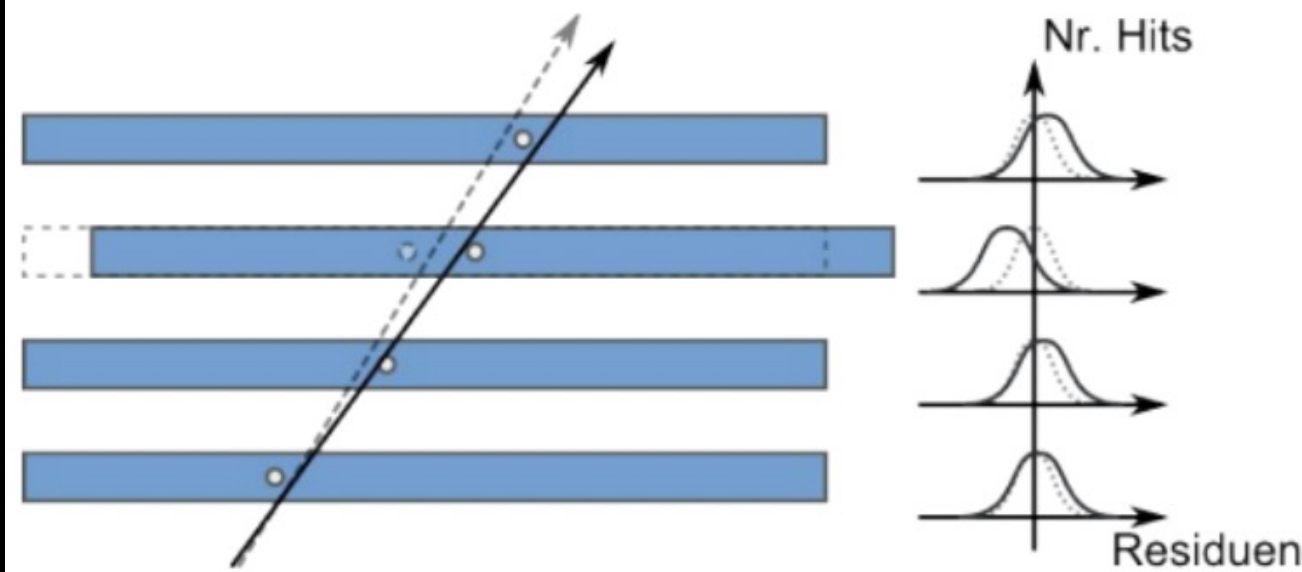


offline reconstruction

- Dedicated discussion with Linhui Wu, Gang Li, Shuqi, Hao Zeng
- Alignment strategy will be presented today

track alignment

Residual: distance of hit with intersection point of track in a module.



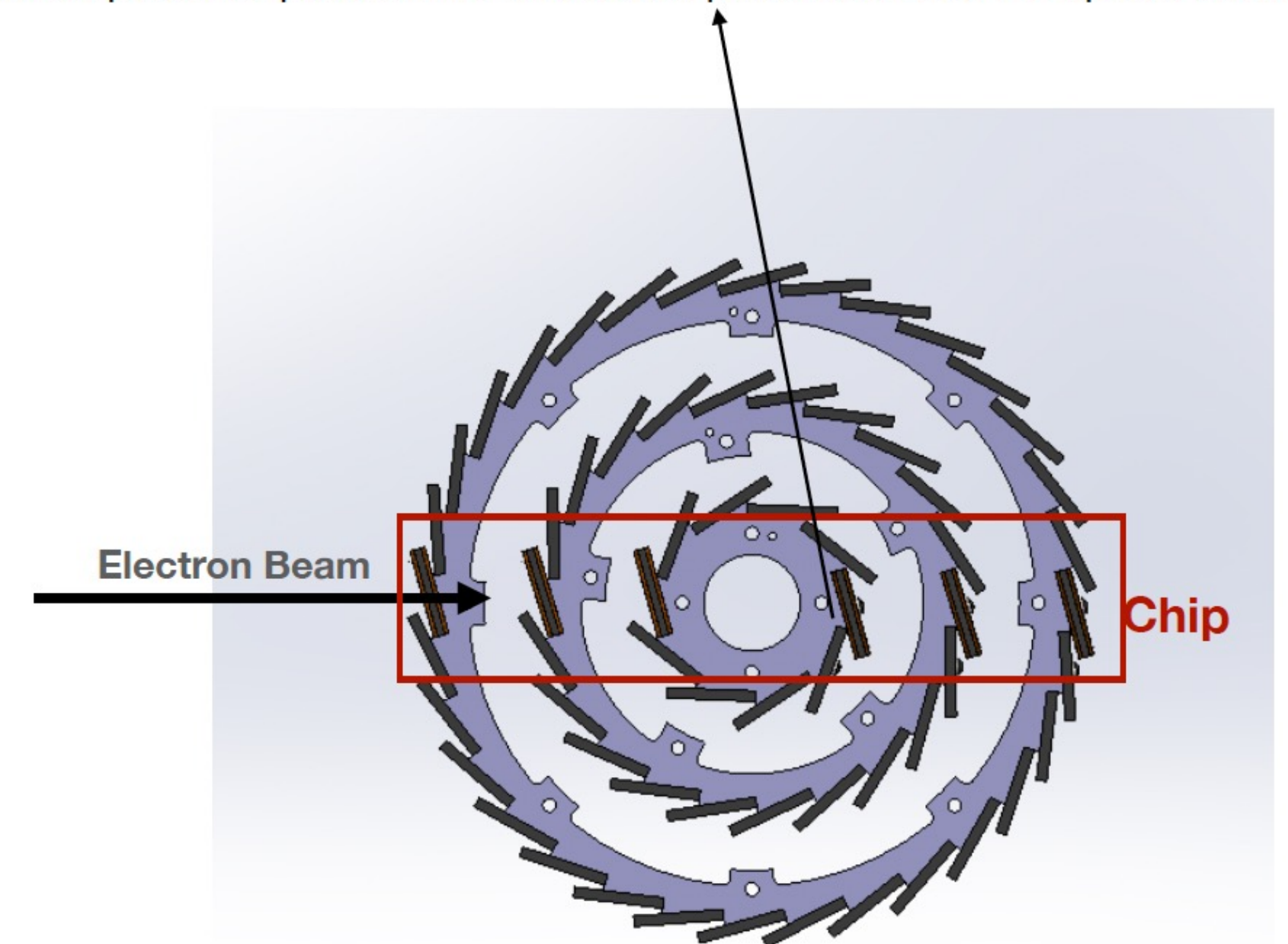
Ideal: Exact positions of modules are known.

➡ Residuals follow a gaussian distribution

In reality: Known positions of modules are $\pm 100 \mu\text{m}$

➡ Residual is shifted because hit position is shifted.

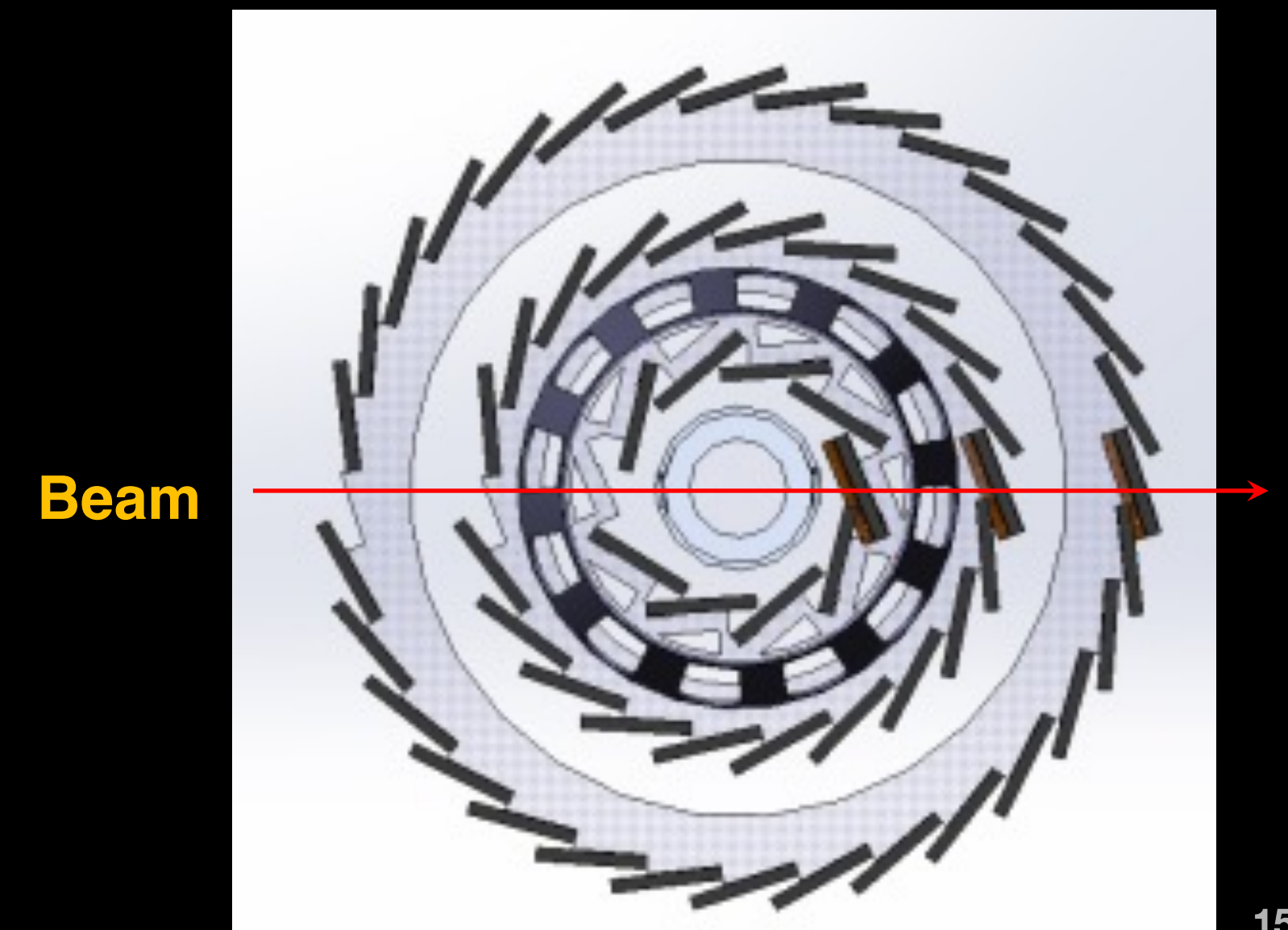
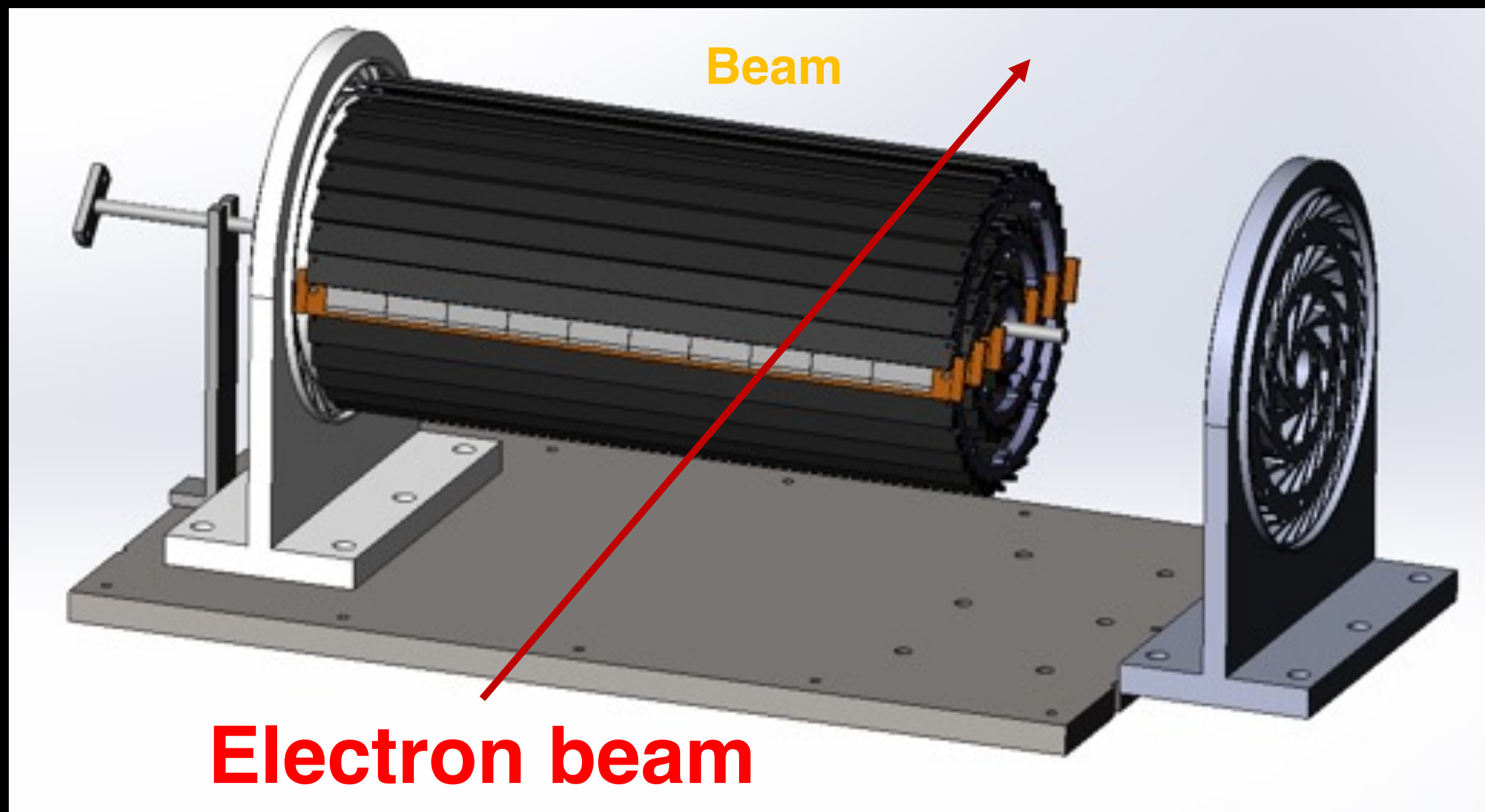
a medium chip will not participant track reconstruction
the residual plot of fit position and measured position decide the spatial resolution



Plan for test beam

- Expect to perform beam test in DESY(3 - 7GeV electron beams)
 - IHEP test beam facility as backup plan (1-2 GeV electrons)
- Enclosure for detector with air cooling is developed for beam test
 - Beam is shooting at one sectors of vertex detectors
- List of people
 - Request for Invitation letter
- List of equipment

DESY test beam



Plan for test beam

- Person power, expertise
 - Ming Qi (NJU, overall)
 - Joao (IHEP, overall)
 - Zhijun Liang (IHEP, overall)
 - Tianya Wu(IHEP, ASIC)
 - Xiaomin Wei(NWPU, ASIC)
 - Jia Zhou (IHEP ,DAQ)
 - Ziyue Yan (IHEP ,firmware)
 - Xinhui Huang (IHEP, mechanism)
 - Shuqi Li (IHEP, offline)
- Requesting Invitation letters (almost ready)
- Application Passports

Plan for test beam



Equipment for Test beam

- Instrumentations
 - 1. vertex detector prototype
 - 2. FPGA boards (15 boards including JTAG adapter)
 - 3. Test PC (2 personal computers. one for test one for backup)
 - 3 PC for DAQ, electronics , offline ?
 - 2T harddisk , 交换机switcher (24 channels, 8 channels ...),
 - temp monitoring slow control (PC needed)
 - Power adaptors ..., 4-5 DC power supply ?
 - 4. Several DC power supply (borrow it from DESY?)
 - 5. Several network cables and other cables.
 - 6. Borrow one oscilloscope for debug

Timeline

- **ASIC**
 - ASICs arrive to IHEP (June)
 - Dicing and Thinning (one wafer dicing before wafer-level tests) (June)
- **Single ASIC testing**
 - PCB under production (Done)
 - Wire-bonding on test PCB ... (Done)
 - **Laser tests, Functional Tests ... (on-going)**
 - **Beta source test (on-going)**
 - Irradiation test (Oct, two days)
- **Wafer level testing**
 - **Wafer level test of ASICs (on-going)**
 - Dicing , (thinning ?)

Timeline

- **Ladders Mechanics:**
 - Now: Carbon support samples available
 - **Pre-production carbon support ladders available**
 - September: Production of final carbon support ladders (if needed)
- **Ladders Assembly:**
 - May: Flex cable available
 - May: Test of wire bonding and gluing on carbon support
 - Tooling design and production (June)
 - Dummy sensor (Glass) assembly on flex (JUNE)
 - **Jig tool , Wire bonding tests on flex (done)**
 - Assembly of ladders with chips (Sep)

Time line

- Barrel Prototype:
 - June: Installation mock-up (3D printed)
 - Received large part of 3D models from Jinyu today, printing now
 - July: Barrel support parts fabricated
 - August: Assembly first Barrel with ladder support only
 - September: mounting readout ladders
 - October: finished mounting the ladders, and readout tests
 - Earlier November: Finish assembly of prototype
 - November: Cosmic ray testing or BEPC beam test
- December: DESY test beam

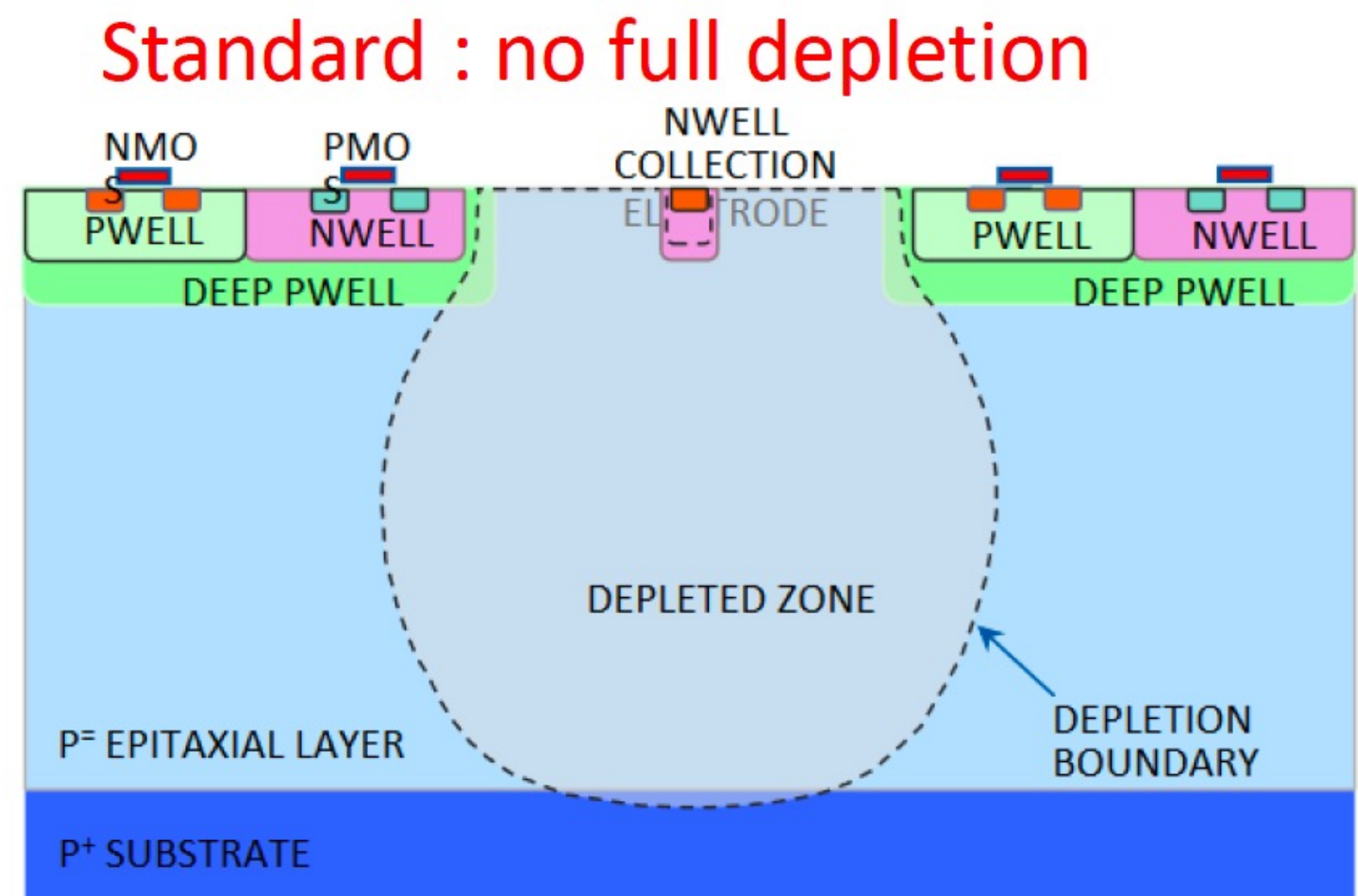
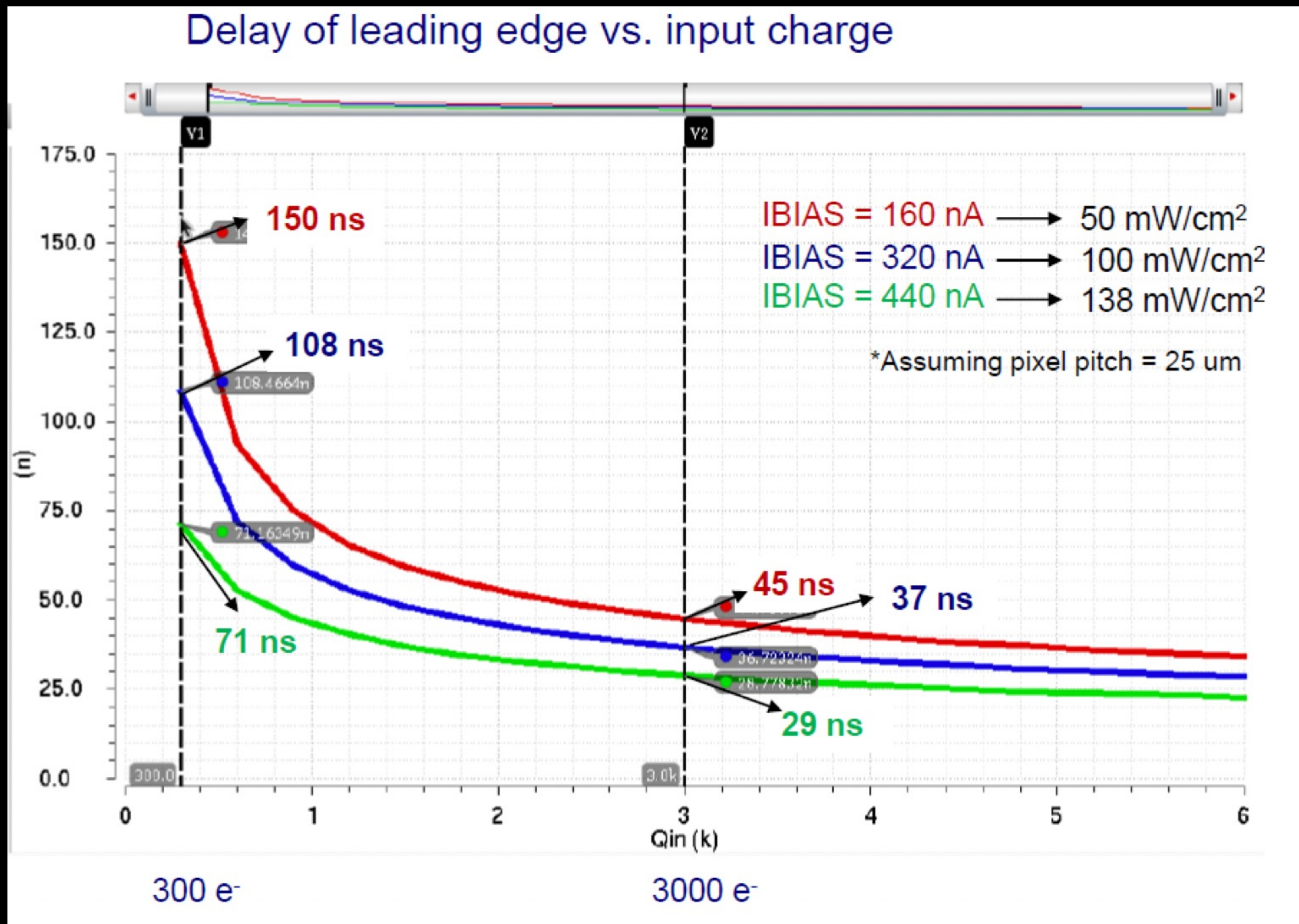
Global Schedule

- August: Assembly first Barrel with ladder support only
- September: mounting readout ladders
- October: finished mounting the ladders, and readout tests
- Earlier November: Finish assembly of prototype
- November: Cosmic ray testing or BEPC beam test
- December 12-22: **DESY test beam (test beam time slot reserved for two weeks)**

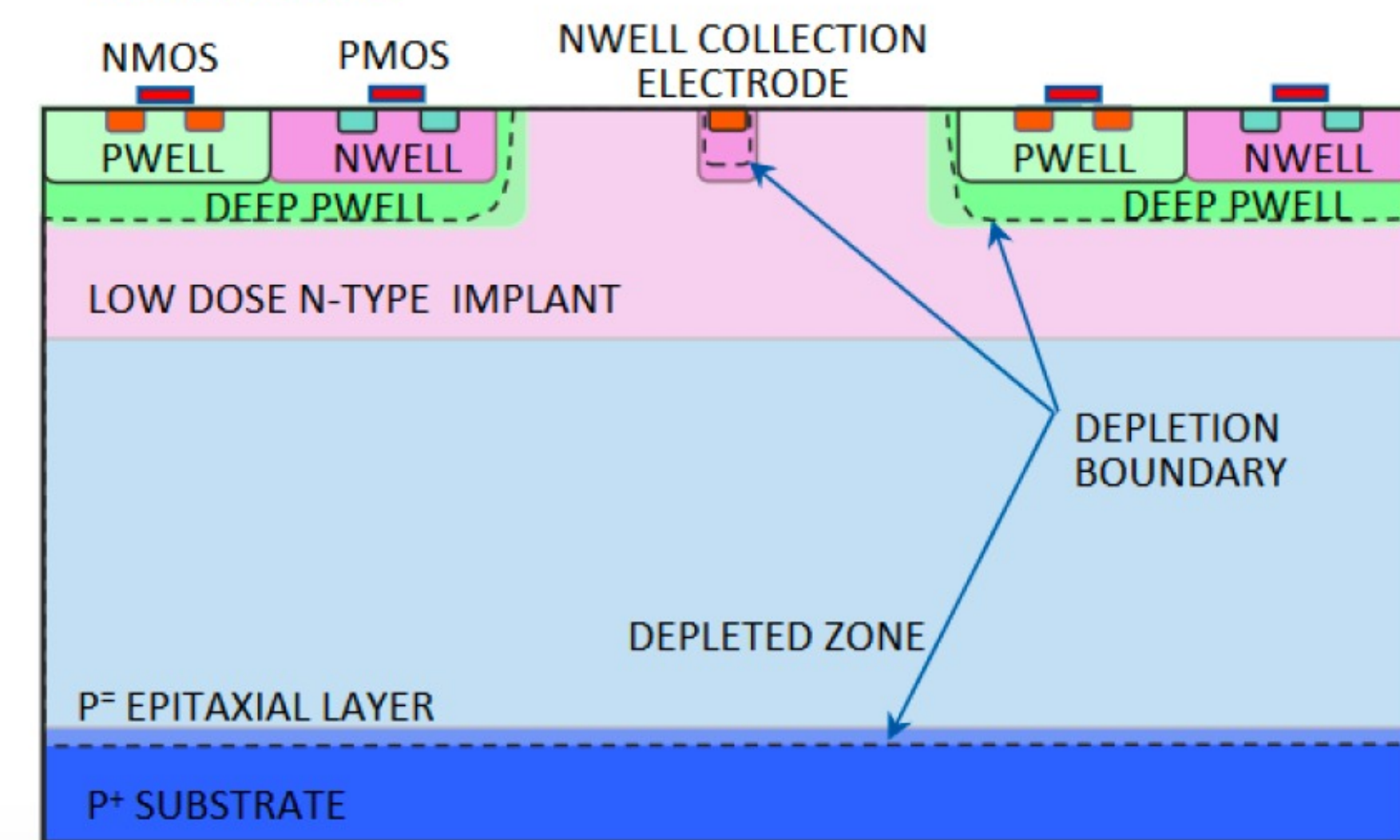
5-Dec-22	49		CMS-InnerTracker	X			
12-Dec-22	50		CEPC Vertex	X	HVMAPS	X	
19-Dec-22	51	Beam till 22/12 0800	CEPC Vertex	X	HVMAPS	X	
26-Dec-22	52		Shutdown				

Pixel Analog design

- CEPC time stamping precision requirement:
 - 25-100ns, better to time stamping each collision at Z pole
- Taichu-1 pixel analog design:
 - 50ns~150ns (based one standard CMOS MAPS tech.)
 - Consider to use depleted CMOS MAPS



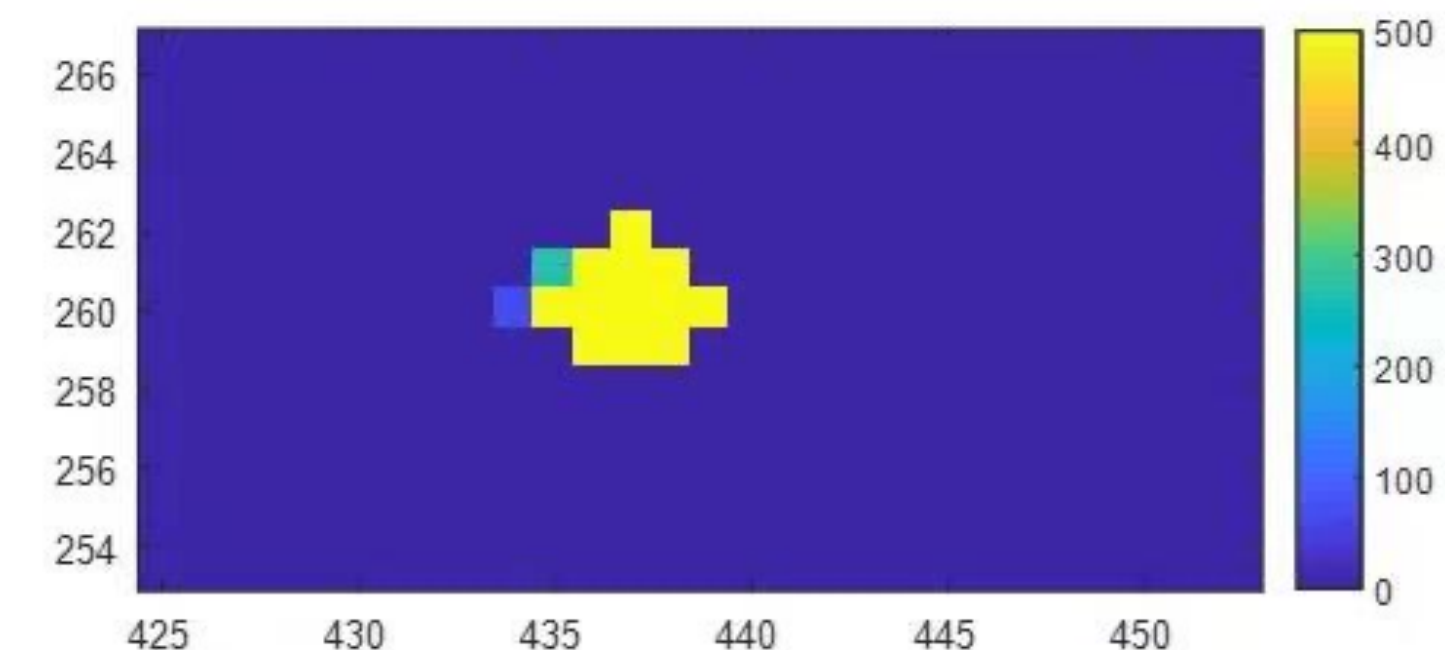
Modified : full depletion, faster charge collection



News about Taichupix3 testing

- Single chip test news
 - Charge injection done
 - S curve scan in next step
 - Need to mask off noise pixel
 - Laser tests
 - Source tests (next step)
 - Threshold tuning
 - IR drop tests? (next step)
 - Top pad need ? → dicing
- Irradiation tests
 - BSRF beam time in Oct 2022
 - X ray machine ?

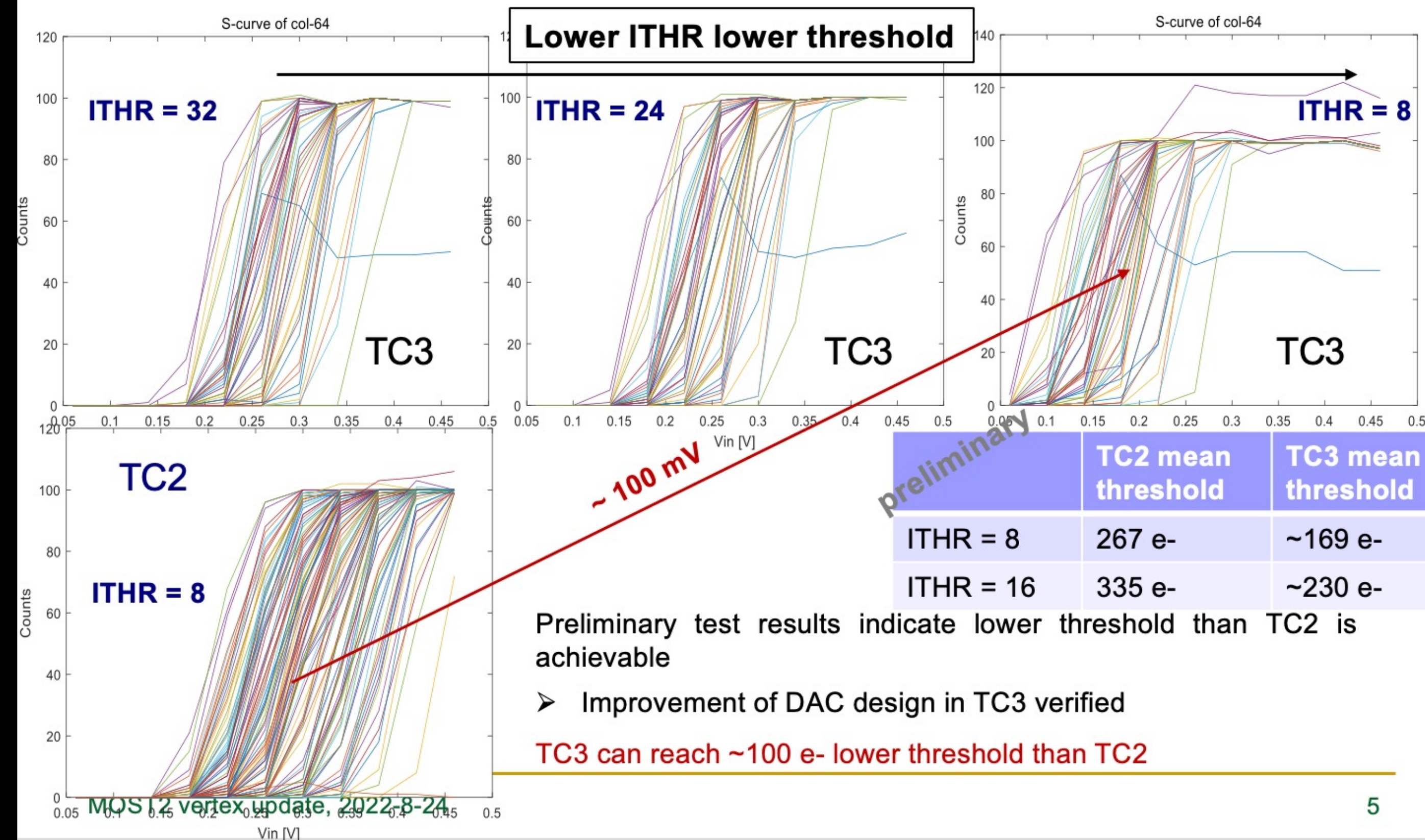
First Laser tests



Pixel threshold tuning

- Opening pixel <0:53, 63> with other pixels masked

➤ Perform s-curve measurements with different bias current (ITHR) setting



Preliminary TaichuPix-3 test

- Single chip test system built
- Taichipix3 can reach **~100 e-** lower threshold than Taichu2
 - Improvement of DAC design in TC3 verified

Taichu2 mean threshold	Taichu3 mean threshold
267 e-	~169 e-

