Status of the MOST2 vertex detector prototype R & D

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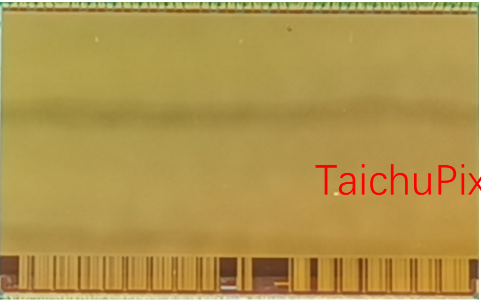
On behalf of the CEPC MOST2 Vertex detector study group

2022/11/16

Overview of MOST2 vertex detector R&D

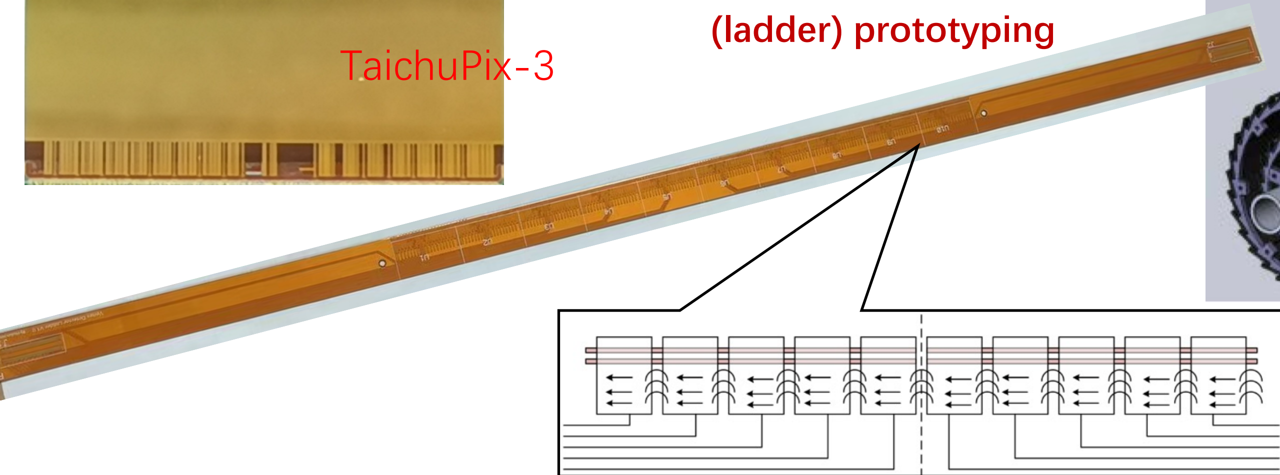
- **Can break down into sub-tasks**
  - CMOS Pixel Sensor chip R&D
  - Detector layout optimization, ladder and vertex detector support structure R&D
  - Detector assembly
  - Data acquisition system R&D

CMOS pixel sensor prototyping



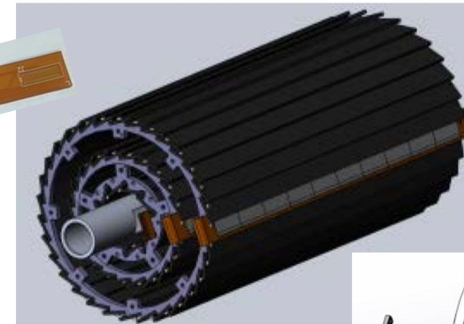
TaichuPix-3

Detector module (ladder) prototyping

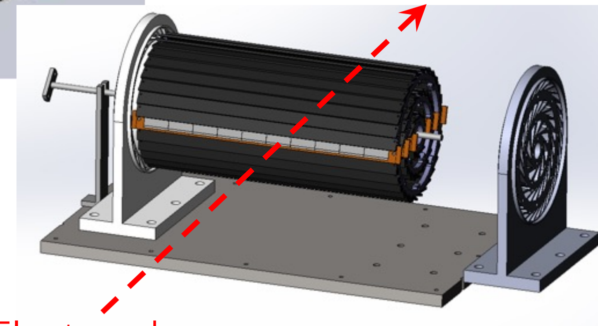


Double sided ladder
10 sensors/ladder side, read out from both ends

Full size vertex detector prototype



Beam test to verify its spatial resolution

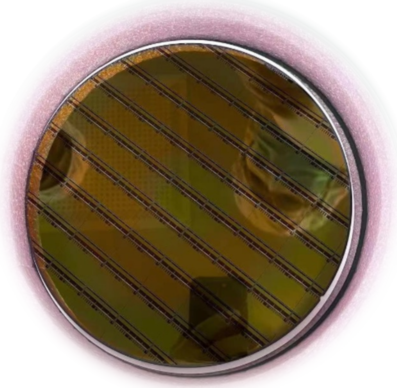


Electron beam

Large-scale sensor TaichuPix-3

Chip size：26 ×16 mm
Pixel size：25μm × 25μm

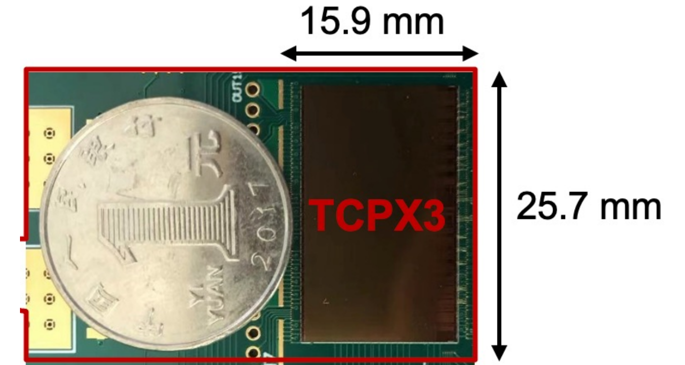
- **6 TaichuPix-3 wafers arrived at IHEP in July**
  - **All wafer thinned down to 150 μm and diced**



8-inch wafer

Wafer after thinning and dicing

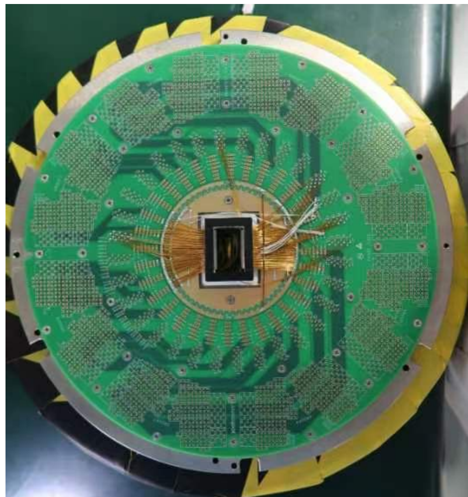
Thickness after thinning



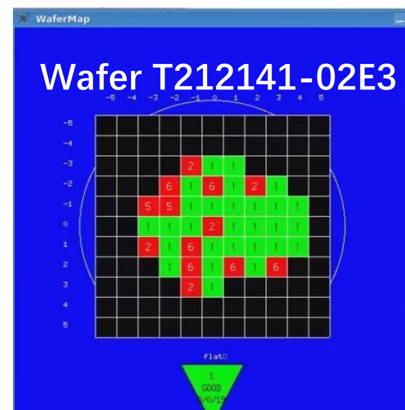
TaichuPix-3 chip vs. coin

- **Complete wafer testing on probe-station** → chip selecting & yield evaluation

Wei Wei, Ying Zhang



Probe card for wafer test



An example of wafer test result

5 wafers tested

- 2 wafer based on standard process
  - Reasonable yield achieved
- 3 wafer based on modified process
  - lower yield than the std. process

TaichuPix3 test with ^{90}Sr

- **TaichuPix3 has a matrix size of 1024x512, an algorithm was developed to configure pixels one by one.**
- **Chips without top-IO work normally under exposure to ^{90}Sr source**

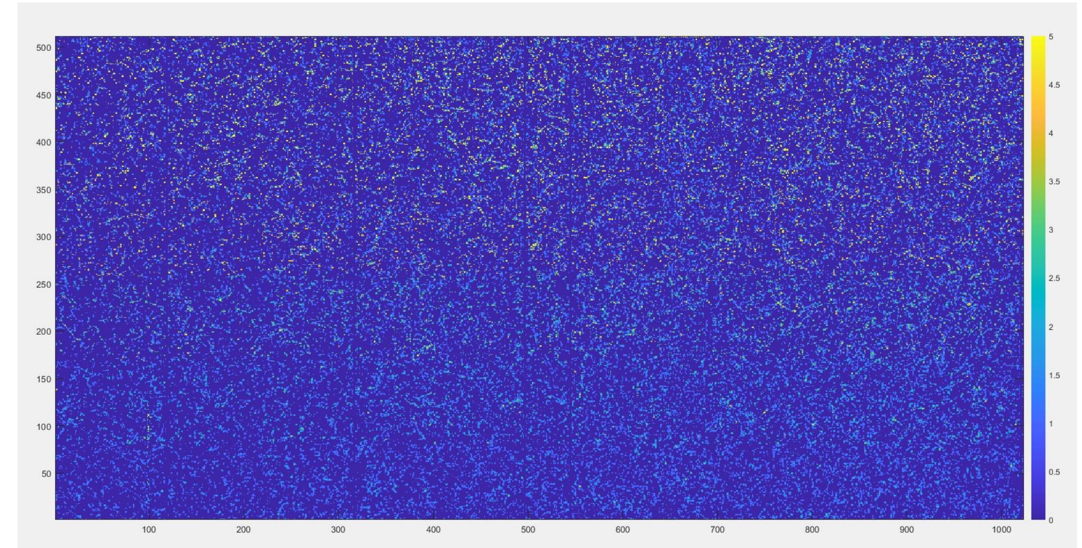


Fig.2 TaichuPix3 without top-IO was injected to the full matrix by ^{90}Sr

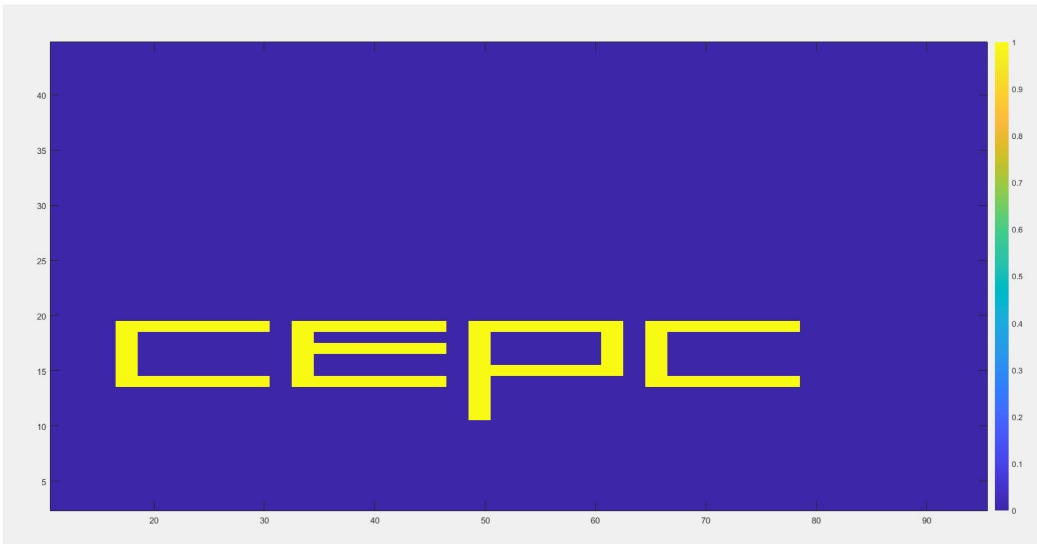
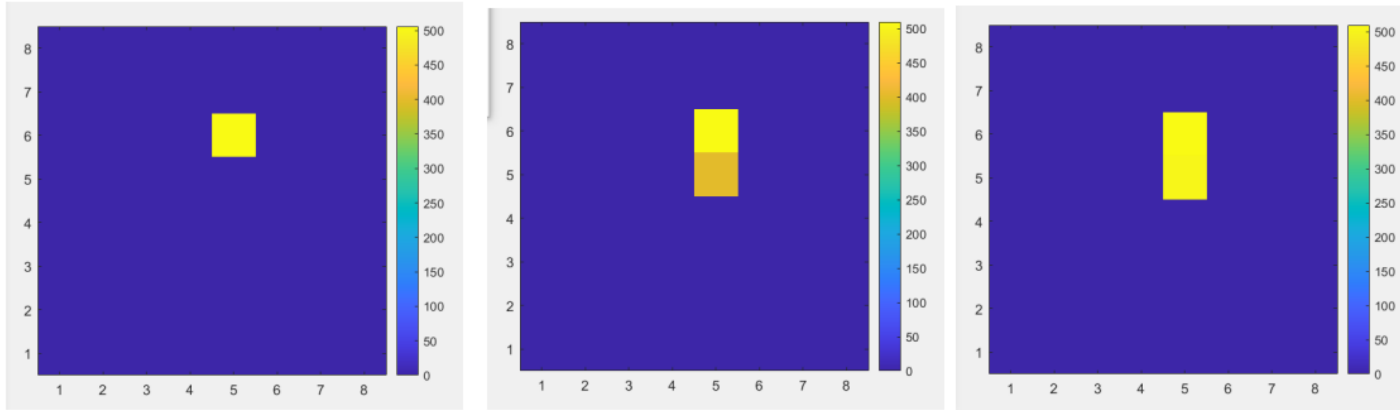


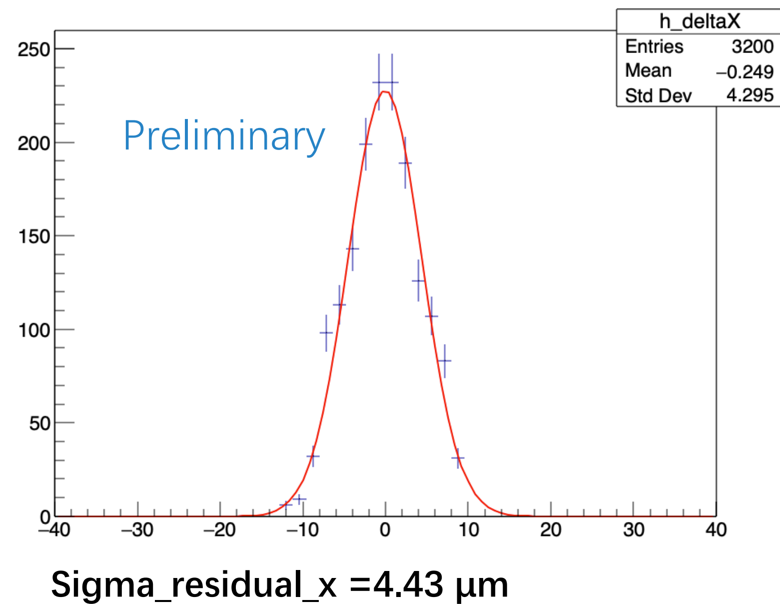
Fig.1 TaichuPix3 self-test with only several pixels turned on

- At the ITHR = 32; Preliminary cluster size calculated is 1.87
- More Cluster size test with a ^{90}Sr on-doing

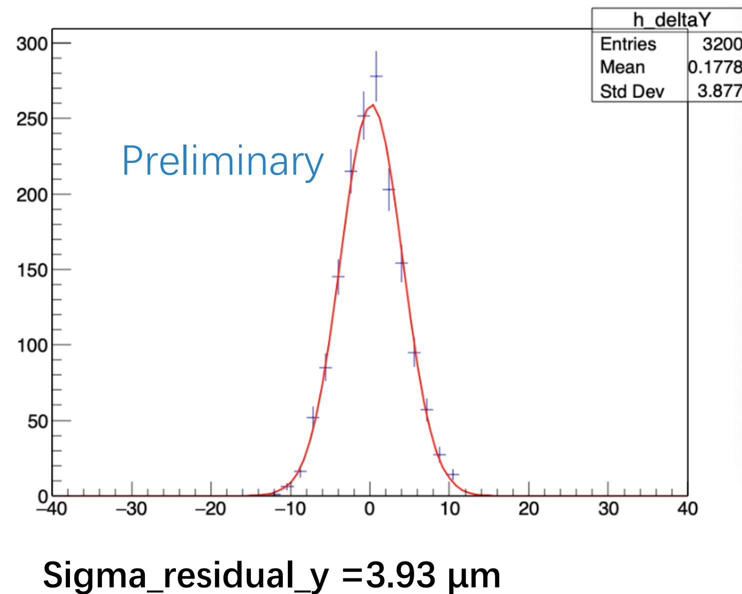
Tianya Wu

Preliminary spatial resolution with laser





Sigma_residual_x =4.43 μm



Sigma_residual_y =3.93 μm

- Laser was scanning with a step of 1 μm on the back of the TaichuPix2.
- Trace of two pixels' response can be figured out clearly on the hit map.
- Preliminary analysis of the data shows a spatial resolution less than 4.5 μm

Wei Wang

TID test on TaichuPix3

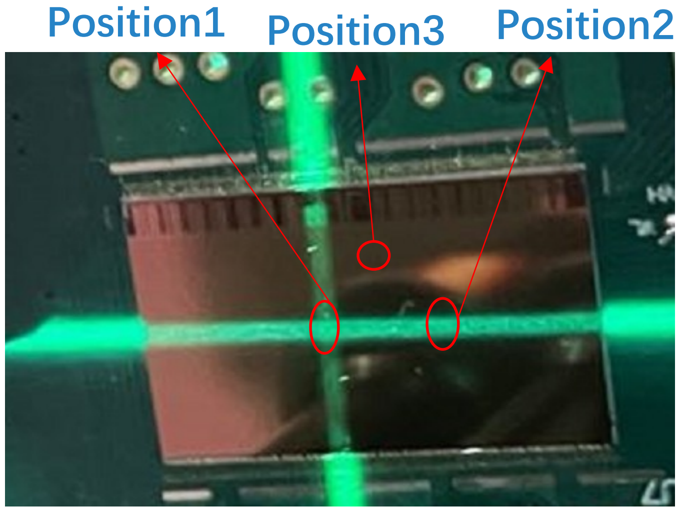


Fig.1 TaichuPix3 irradiated at BSRF 1W2B beamline (12 keV X-ray)

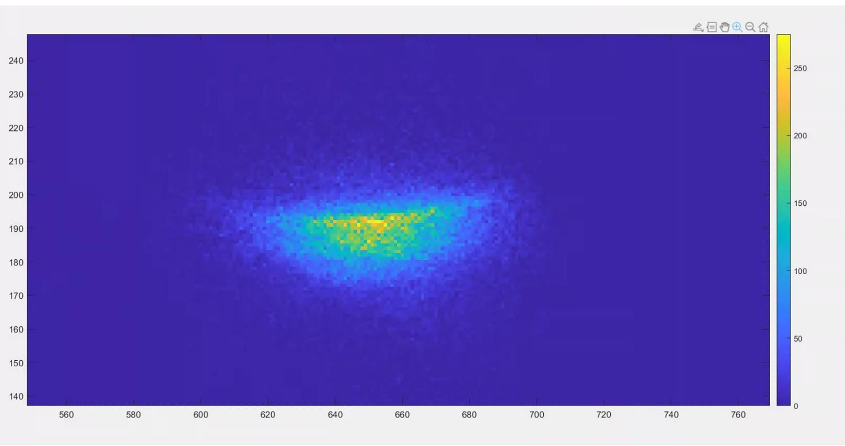


Fig.2 Full image of the X-ray beam spot(position 1)

- Dose rate ~1.2rad/min for the first 12 min, in order to find the position of beam spot.

→ The size of beam spot agrees with the expectation of 1mm x 0.6mm

- Dose rate ~43.3 krad/min for 69 min until total dose over 3 Mrad.
- Chip was exposed with full working condition: power, bias, clk, …

- All three irradiation regions indicated a good performance to 3 Mrad TID

Tianya Wu

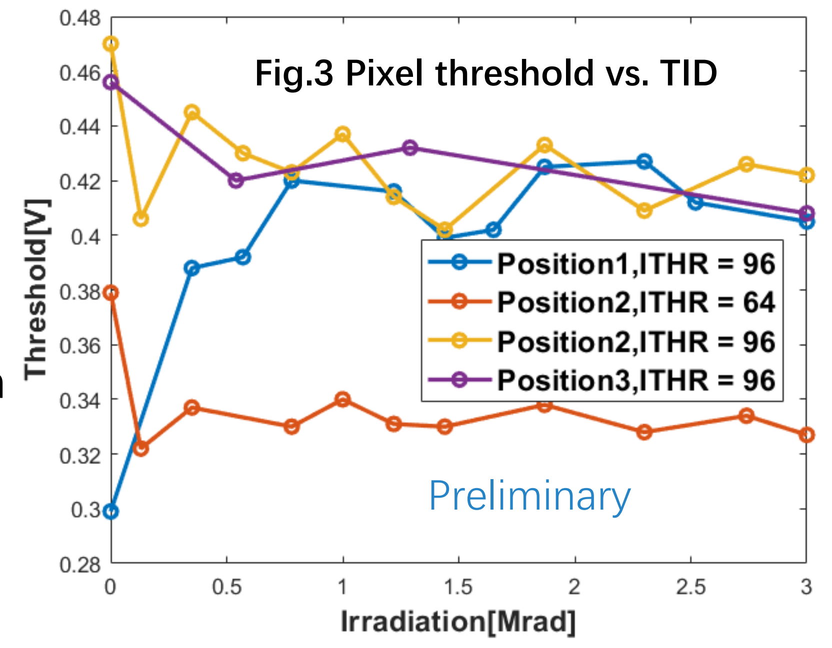
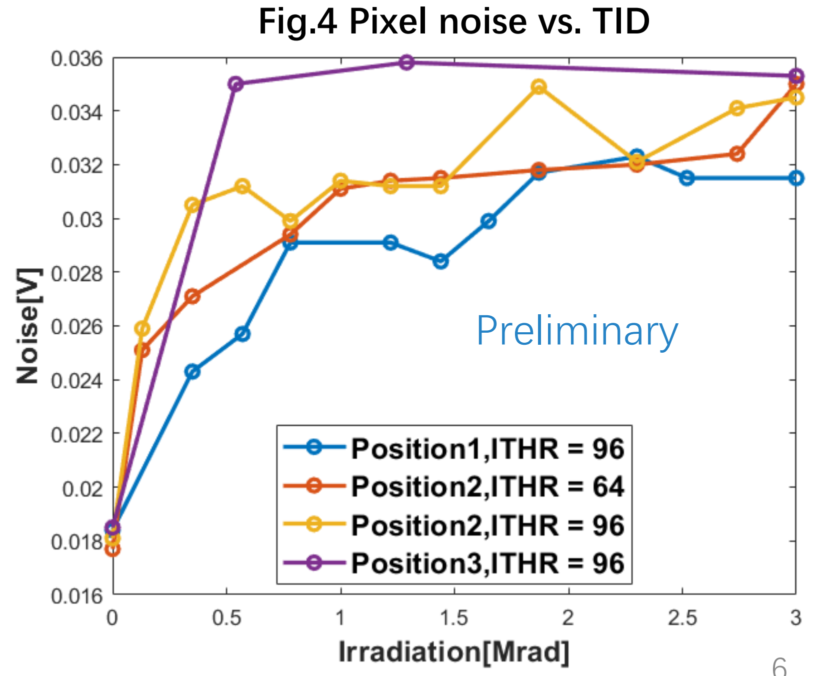


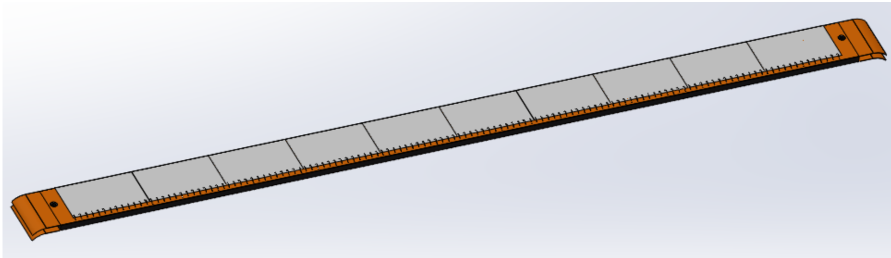
Fig.4 Pixel noise vs. TID



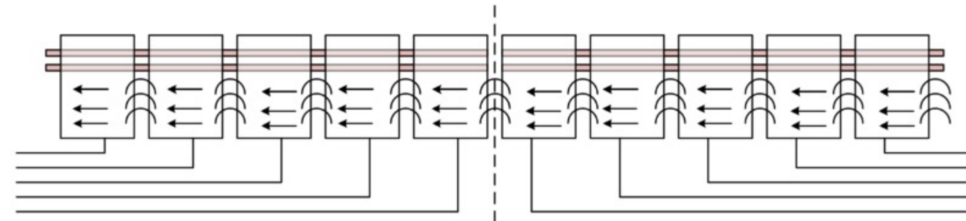
Detector module (ladder) R&D

- **Completed preliminary version of detector module (ladder) design**
  - Detector module (ladder) = 10 sensors + support structure + flexible PCB + control board
  - Sensors will be glued and wire bonded to the flexible PCB
  - Flexible PCB will be supported by carbon fiber support structure
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB

3D module of the ladder

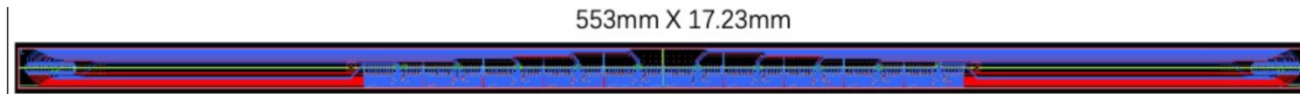


Schematic of ladder readout



Double sided ladder
10 sensors/ladder side, read out from both ends

Flexible PCB design



Profile of flexible PCB

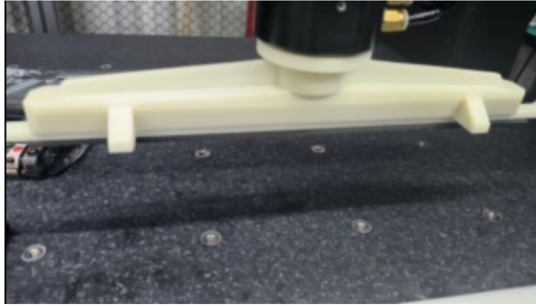
	Achieved Thickness (μm)	Optimization goals (μm)
Polyimide	25	12
Adhesive	28	15
Plating Cu	17.8	17.8
kapton	50	50
Plating Cu	17.8	17.8
Adhesive	28	15
Polyimide	25	12

Jun Hu

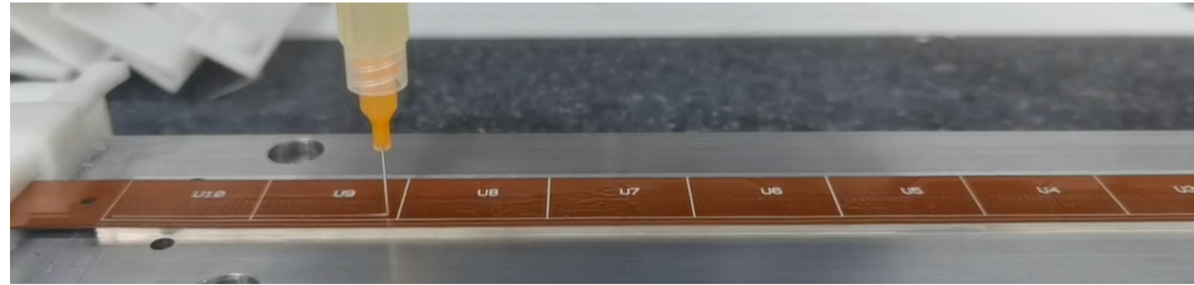
Detector module (ladder) assembly

- **Ladder (double side)= 20 ASIC chips + two flexible PCB + carbon fiber support**
- **Ladder assembly procedure verified with dummy ASIC (glass) using gantry**

New pickup tools



Dummy ladder glue automatic dispensing using gantry



Ladder on wire bonding machine

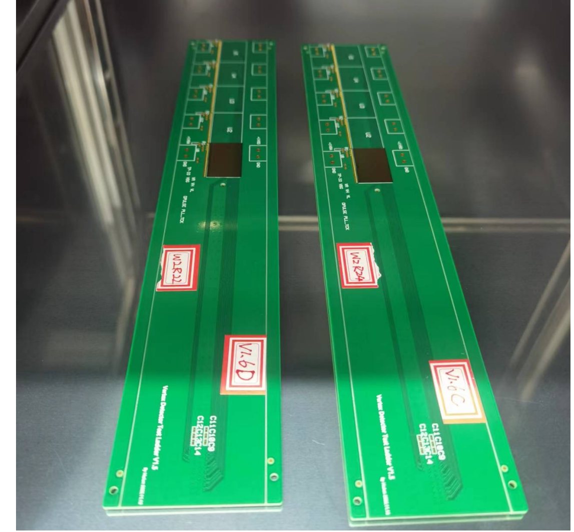
Dummy Ladder on holder

Electronics test in ladder

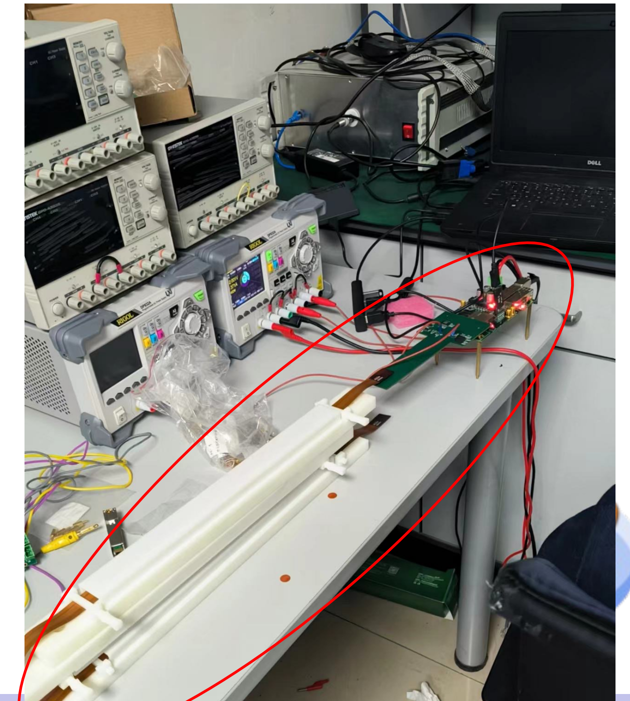
Jun Hu
Ying Zhang
Yiyue Yan

- Testbench setup: 2~3 chips wire bonded on one flex
  - Can communicate with TaichuPix in OCT mode (self-checking mode)
  - Issue: Readout lots noise in charge injection mode
  - Challenge:
    - Long flex cable (~70cm)→ some issue with power distribution and delay
    - Missing test point to debug the communication issue
  - Next step
    - Made a hard PCB with test point, try to under the issue

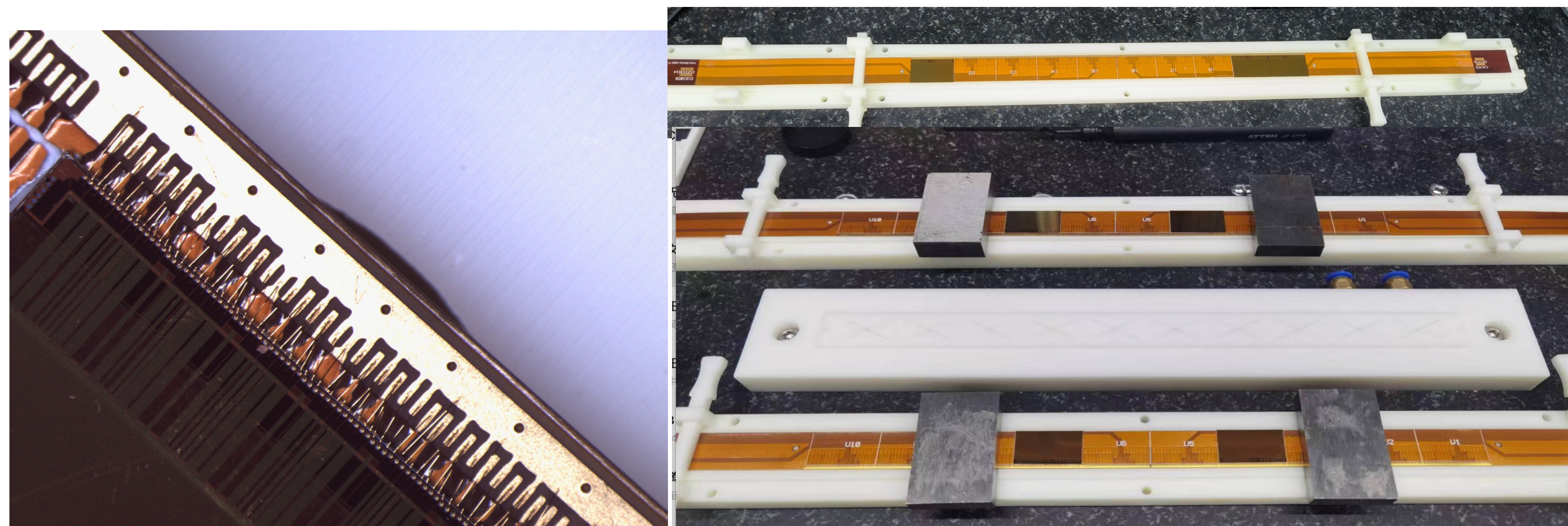
Hard PCB with test points



Electronics test bench



2~3 Taichu chips wire bonded on one flex

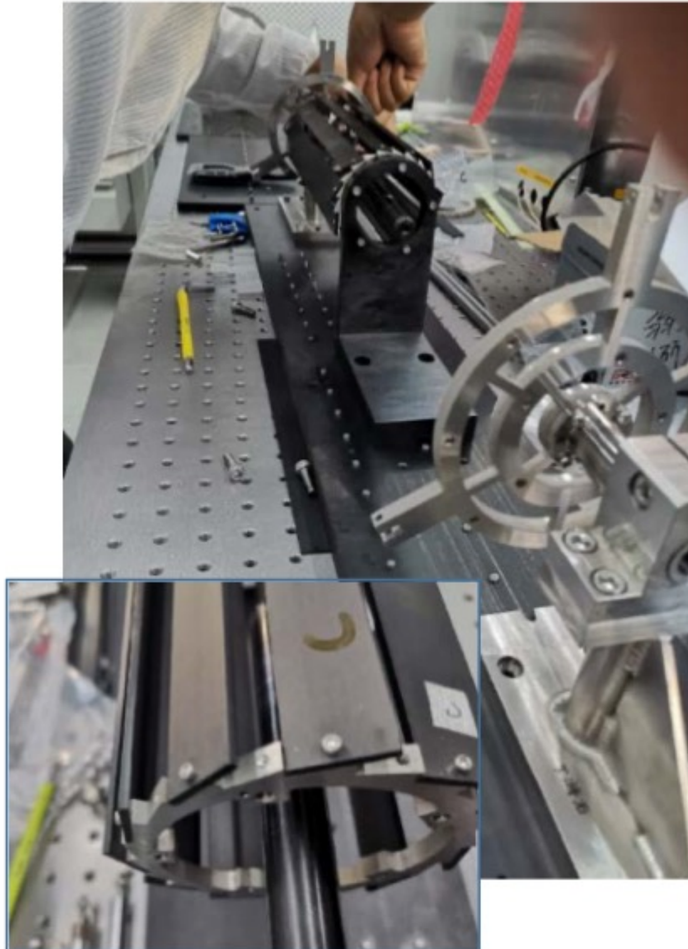


Vertex detector prototype assembly procedure(1)

- **Installation procedure of 3 double layer of vertex detector**

Inner barrel

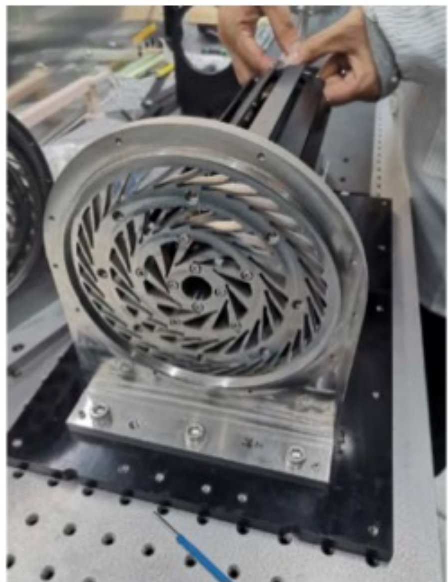
Middle barrel
(half number of ladders)

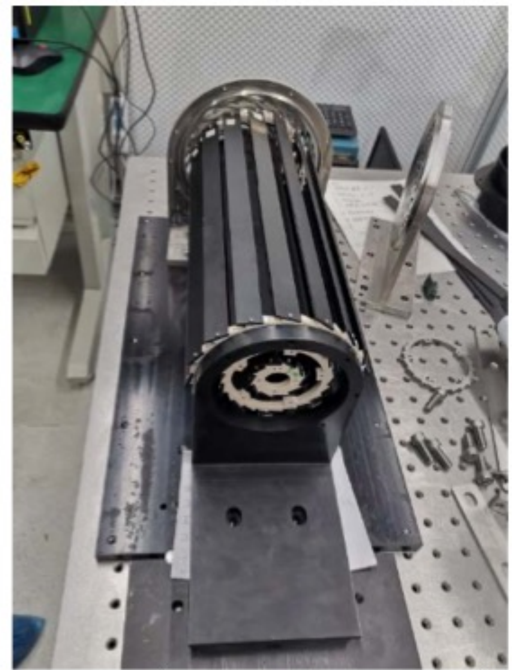


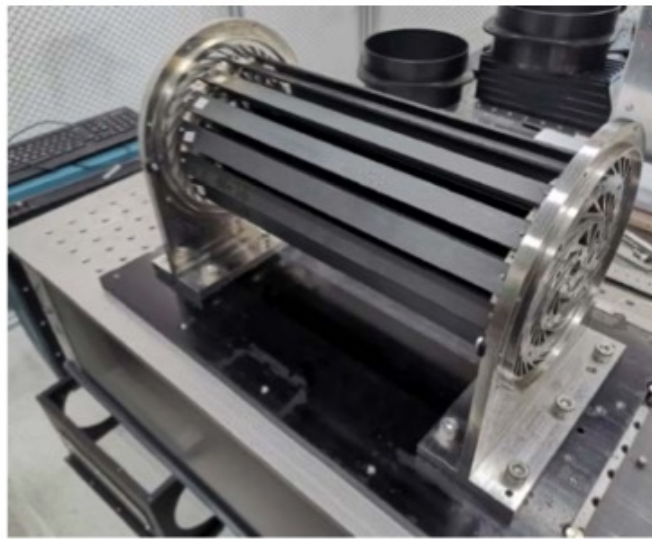
Outer barrel
(half number of ladders)

Jinyu Fu

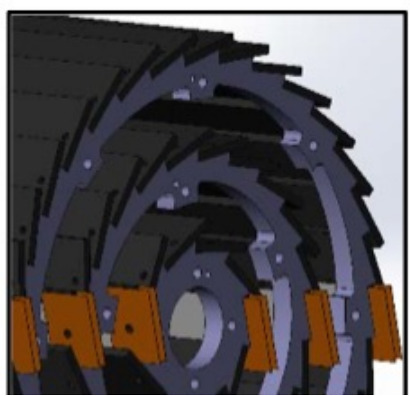
Vertex detector prototype assembly procedure(2)

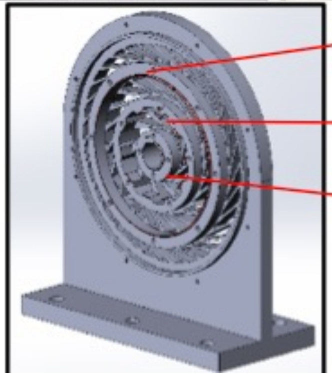


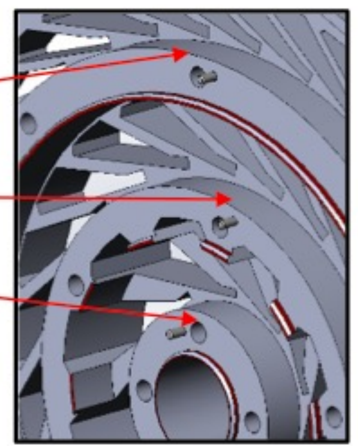




Jinyu Fu



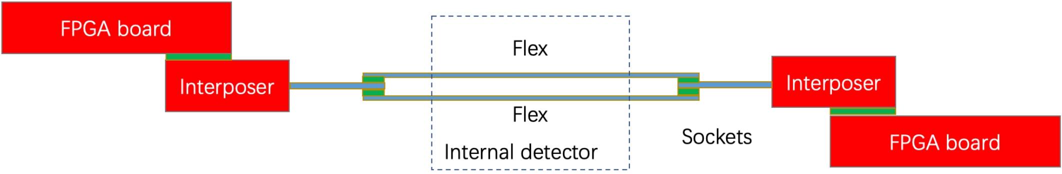




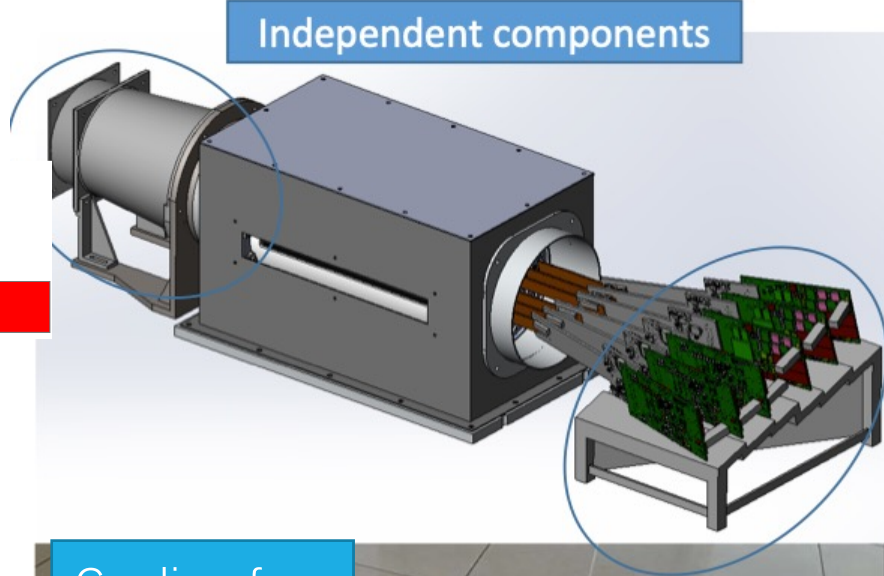
Readout electronics for vertex detector prototype

- **FPGA board is connected to flexible PCB through interface board**
- **Support structure and cooling for vertex detector prototype has been prototyped**

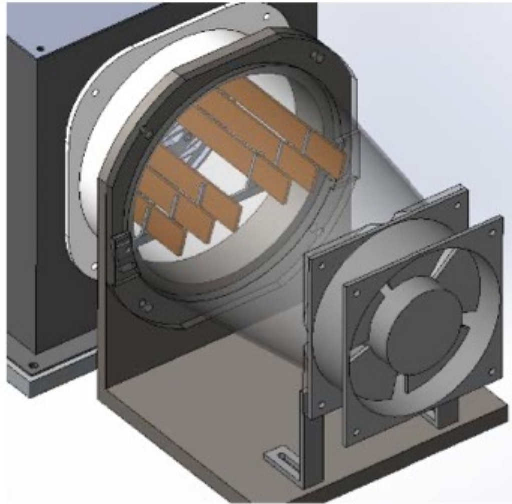
Jinyu Fu



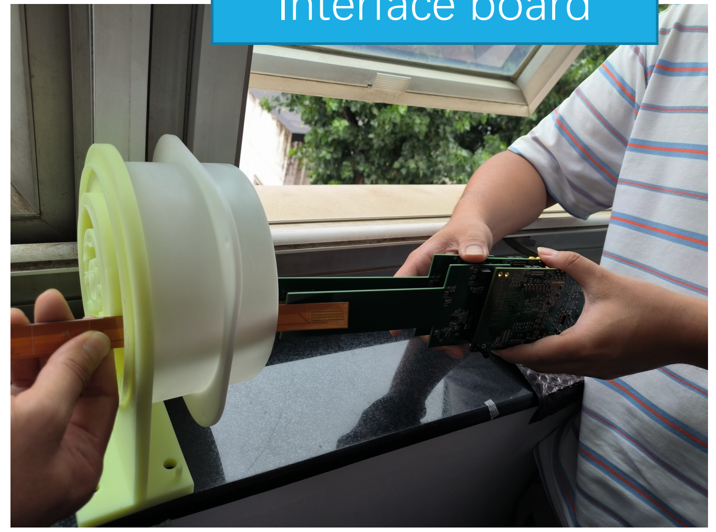
Independent components



Cooling fans



Interface board



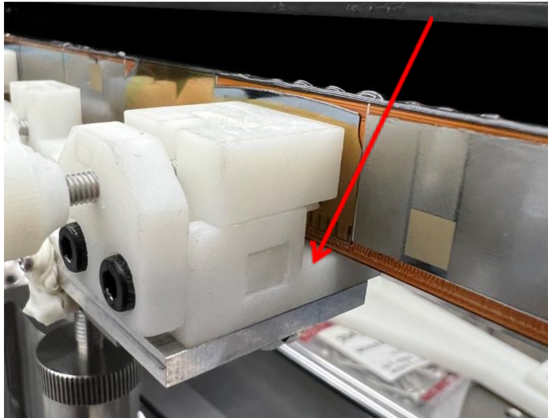
Cooling fans

Ladder loading

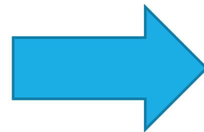
- **Loading procedure of ladder on vertex detector has been tested**
- **Ladder with one Taichu3 chip with wirebonds and 9 dummy silicon chip**
- **Wire-bonding was protected during loading**

Jinyu Fu

Wire-bonding



Ladder support tools



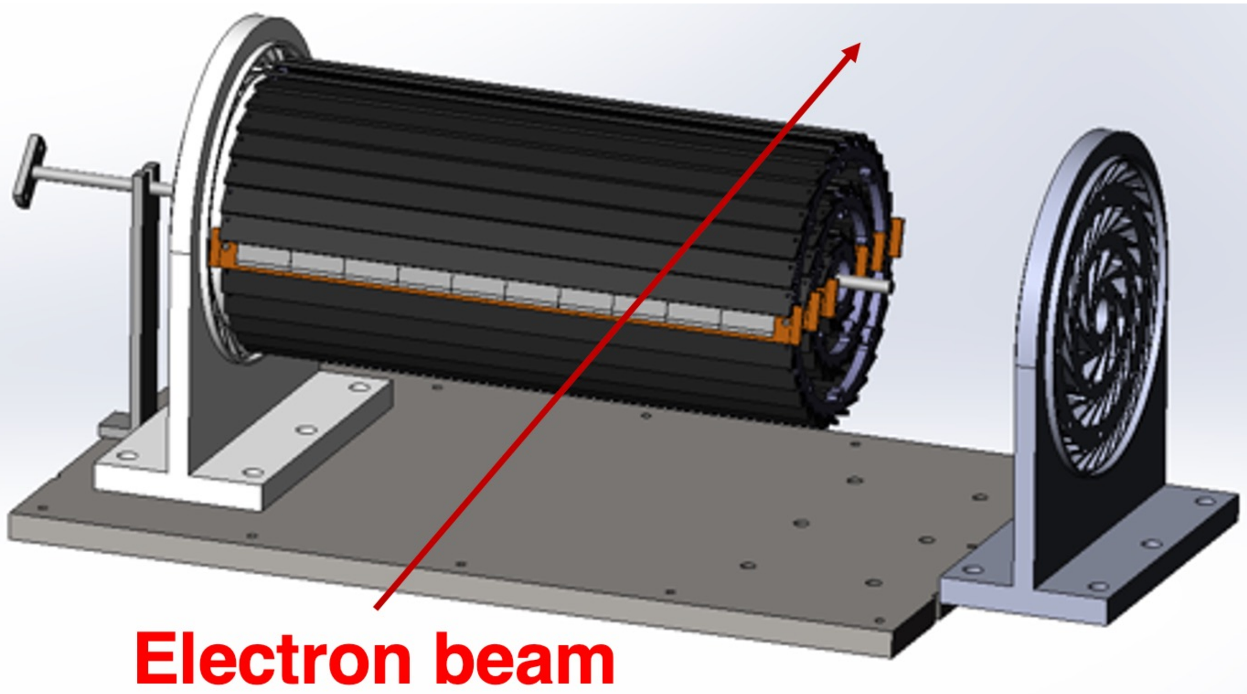
Ladder loaded on vertex detector

Plan for test beam

- **Plan to perform beam test at DESY in December this year**
  - 3-7 GeV electron beam
  - Plan to install 6 real ladders on prototype, Plan to install all the carbon fiber support structure detector
- **Rehearsal testbeam at Beijing Synchrotron Radiation Facility (BSRF)**
  - 1~2 GeV electron beam

DESY testbeam：Dec 12-22,2022

5-Dec-22	49		CMS-InnerTracker	X			
12-Dec-22	50		CEPC Vertex	X	HVMAPS	X	
19-Dec-22	51	Beam till 22/12 0800	CEPC Vertex	X	HVMAPS	X	
26-Dec-22	52		Shutdown				



Comparison of DESY and BSRF

	DESY	IHEP E3 beam	BSRF
Momentum	1-6 GeV	<1 GeV secondary beam	1~2.5 GeV
Particles	electrons	Protons/ Pions/ /Electrons	electrons
Trigger rate	4000 Hz/cm^2	0.6 Hz/cm^2	~50 Hz/cm^2

BSRF testbeam

- 4W1A is a X-ray Imaging beamline and locate at IV quadrant of BEPC and 12# experimental hall. It's mainly used for crystal morphology and Phase-contrast imaging.

Beamline Specs

Source	Wiggler
Imaging Mode	Phase contrast imaging
Energy Range	6-22 keV
Flux (photons/sec)	10^{10}@ 8keV
Spatial Resolution	10 μm
Beam Size (HxV)	20mm x 10mm
Imaging Mode	Nano-resolution Imaging
Energy Range	5-12 keV
Flux (photons/sec)	10^{8}@ 8keV
Spatial Resolution	30nm, 50nm, 100nm
Beam Size (HxV)	10μm x 10μm, 15μm x15μm, 60μm x60μm

Overview of the beam test setup

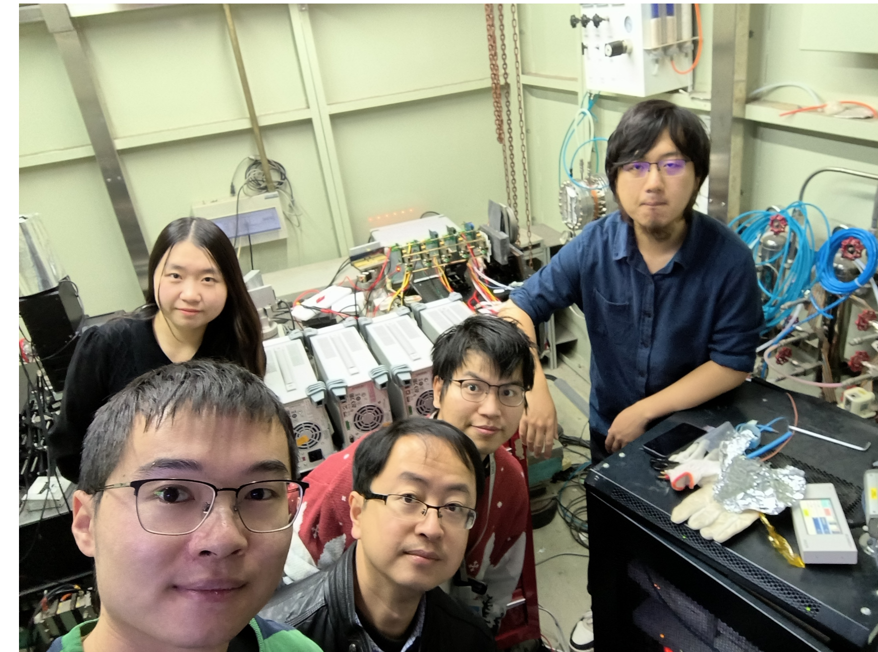
- MOST2 vertex detector team setup electrons beam in BSRF
- TaichuPix3 in upstream position
- Jadepix3 in downstream

Beam source

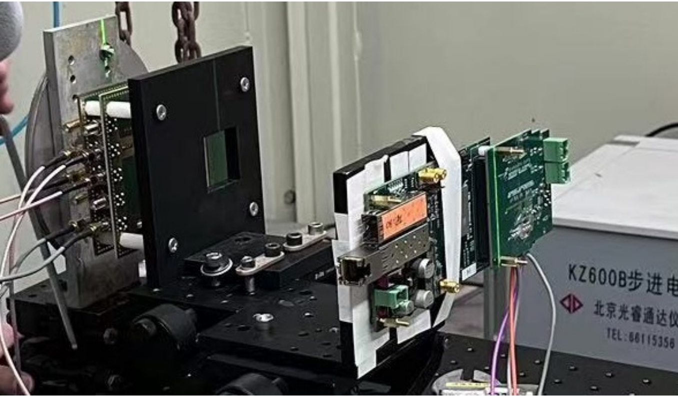
2 layers LGAD

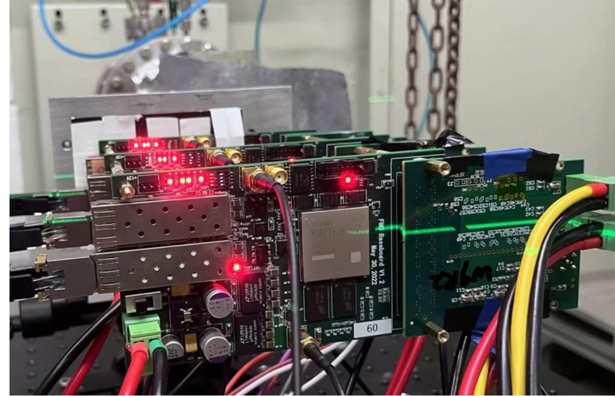
2~5 layers TaichuPix3

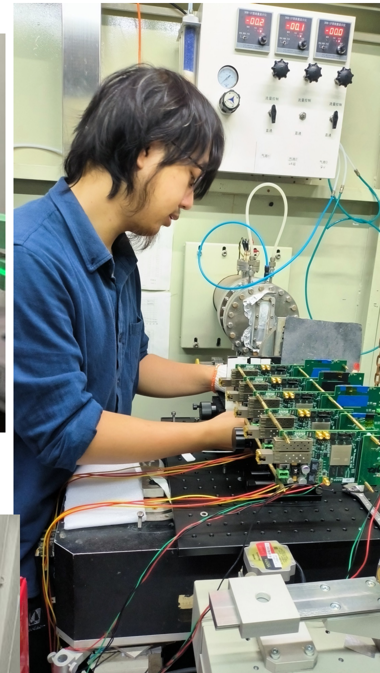
4 layers JadePix3



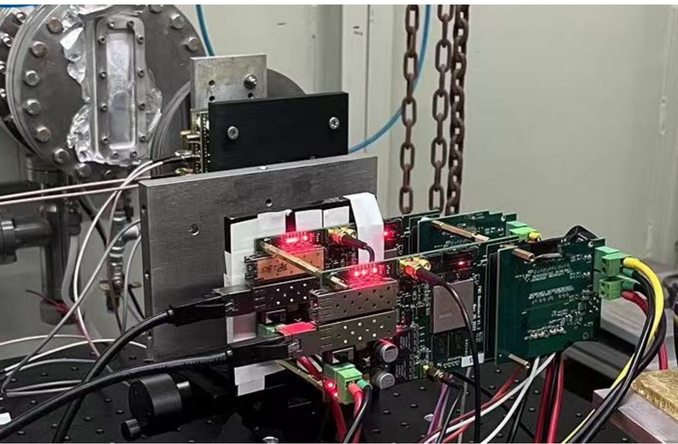
TaichuPix3 setup

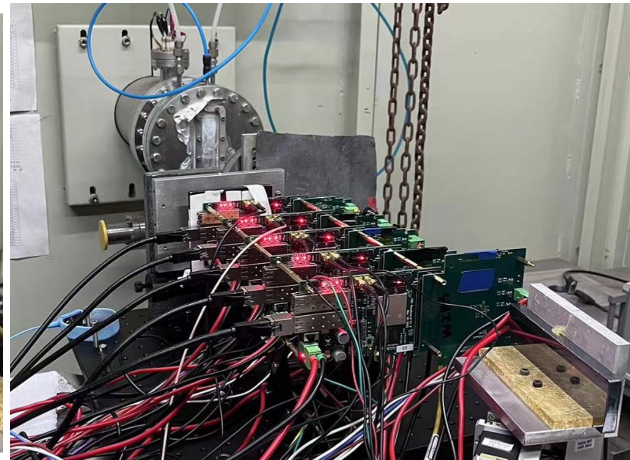






- TaichuPix3 test board installation was step by step, from one to five.
- the threshold ITHR was set to 32, which corresponding to 300 e-





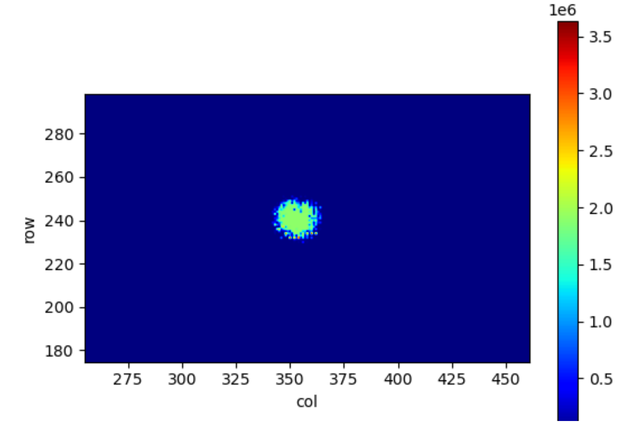
- Beam spot was set to 4mmx2mm
- 21-layer steel plate (1mm/layer） and 3 layers of lead （1mm/layer) was used to block X ray

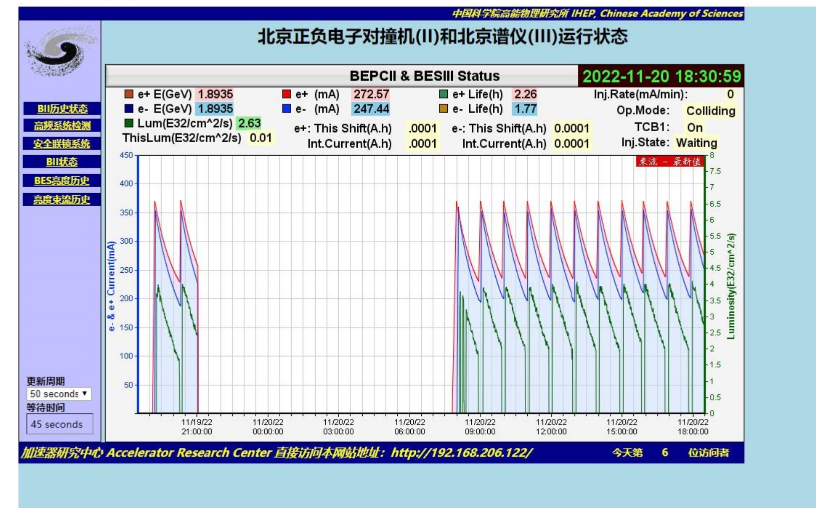
CEPC

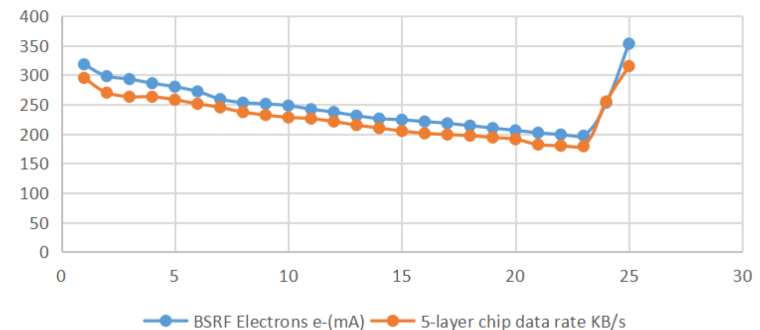
Data Acquisition

- A new DAQ software was used to acqiure data. Laser test verified a capacity of 15MB/s for a chip (under 10KHz of infared laser)
- The peak data rate was around 315 KB/s from 5 layers of TaichuPix3 board.
- The DAQ will be stopped automatically when there is no hit last for 5 seconds

- The data rate is consistent with the trend of electron energy changes



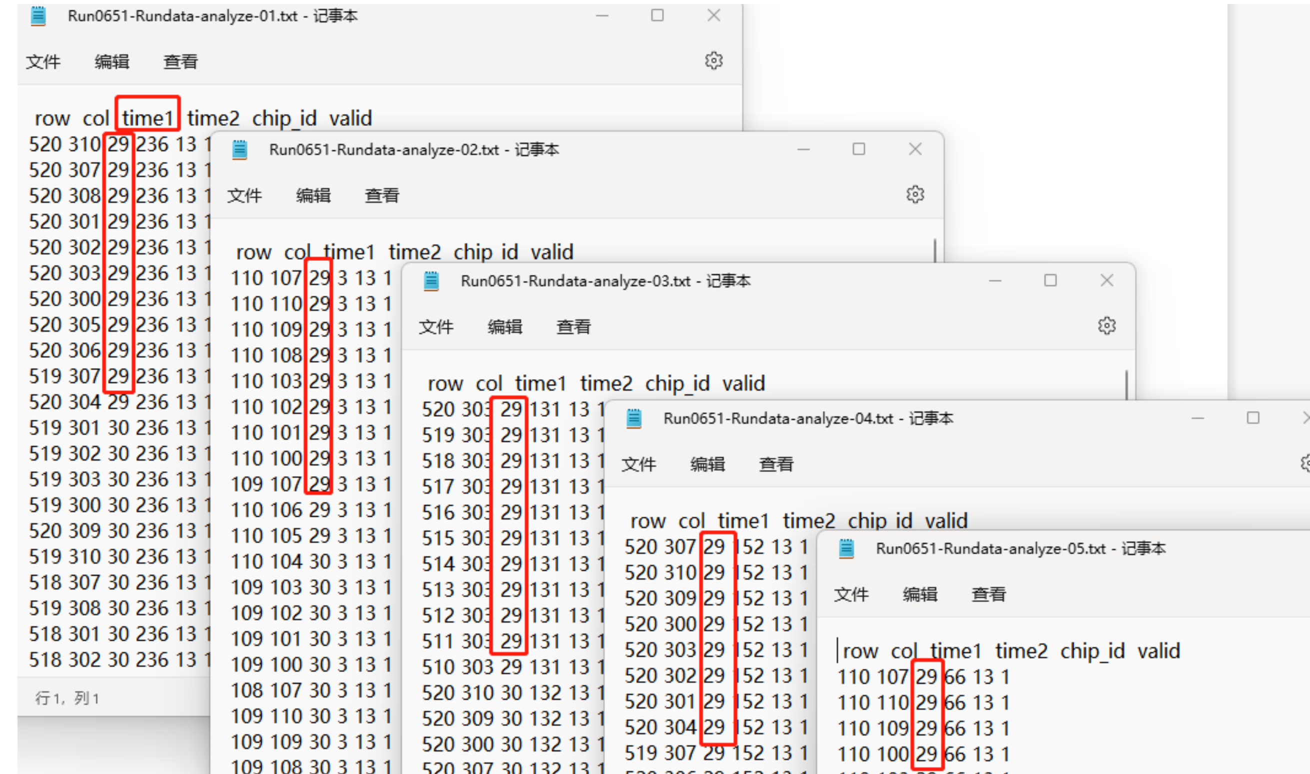




Hongyu Zhang
Jia Zhou

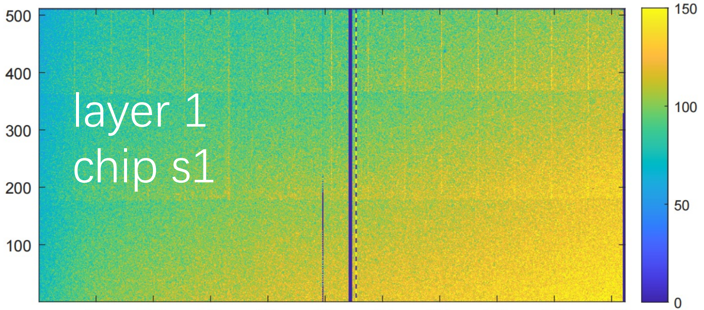
Timestamp calibration

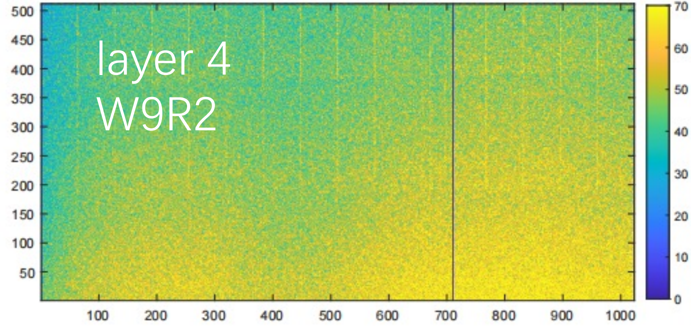
- For timestamp calibration, a chip self-test is necessary before the beam test.The chip level timestamp (time1) is normalized
- Clock of timesatamp is running with 20MHz
- The coincidence data will be figured out by the same chip level timestamp, which recognized by a range of 3 time1(±1 time1)

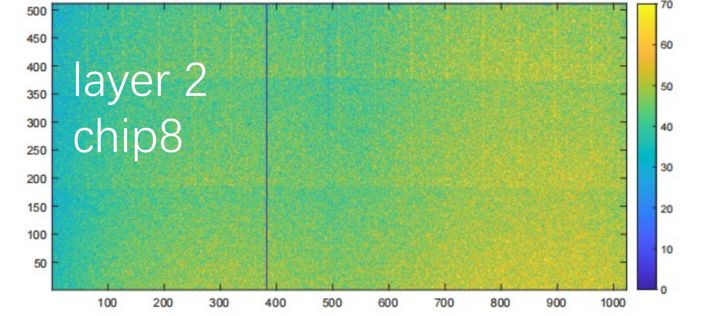


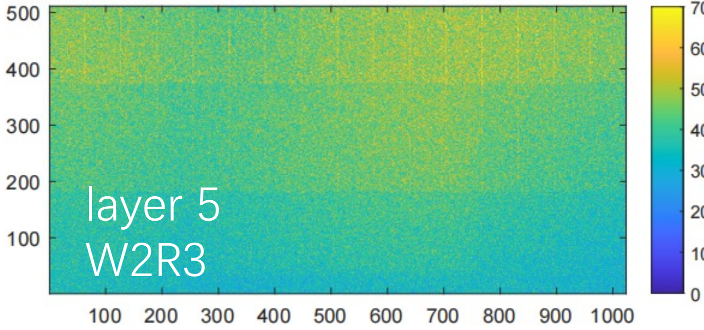
Hitmap of 5 layer TaichuPix3 chips

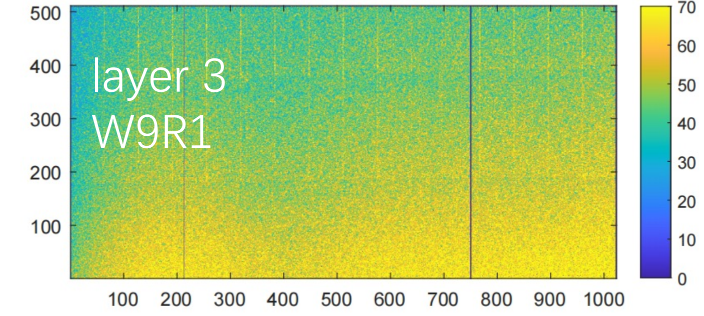
Tianya Wu
Jia Zhou

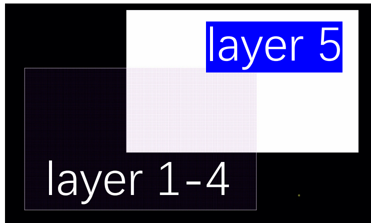












- 4 PCBv1.1- 1 PCBv1.2
- layer1 and layer2 were the standard chip fabrication process, the threshold is around 300 e-
- layer3 and layer 4 was with modified process
- layer5 has a different positon and with 25% region overlap to first 4 layers
- The hitmap agrees with our expectation

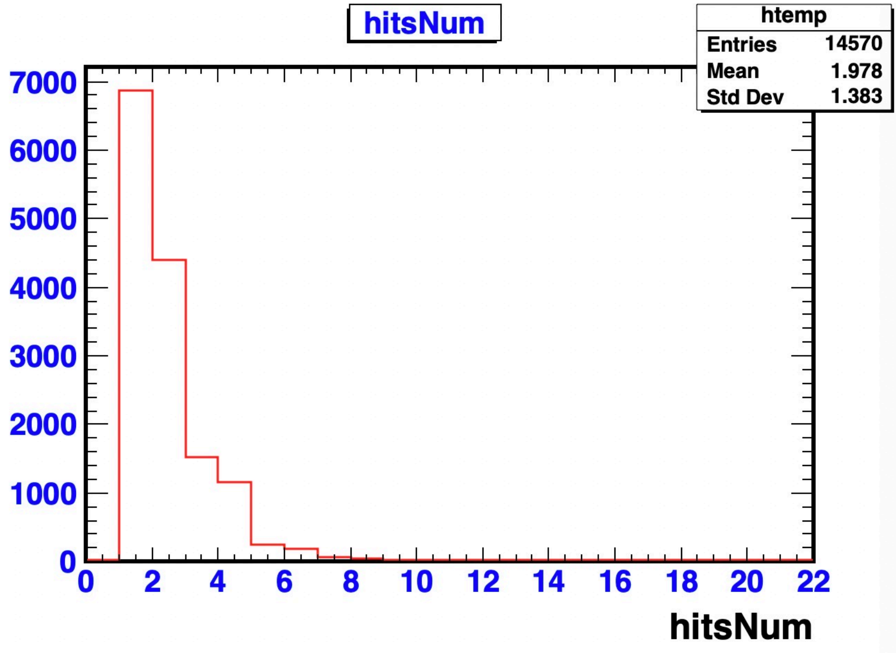
ITHR	chipS1	chip8	W2R3	W2R1 0	W2R1 1	W9R1	W9R2
32	304.6	292.9	305.2	276.6	-	168.9	161.5

Preliminary Coincidence eletrons analysis

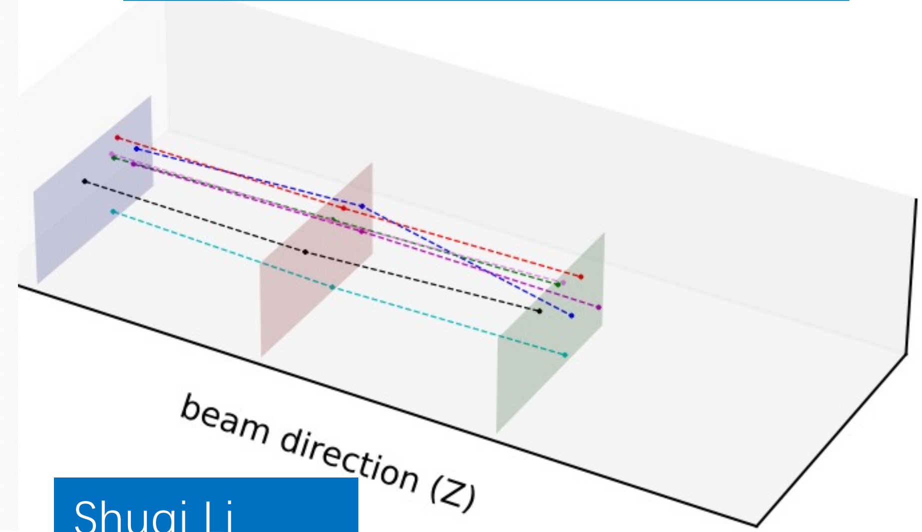
- >300k coincidence events were recorded
- The 3D figure and projection shows the preliminary coincidence track without alignment, more results will be presented later.

BEPC energy	detector Area	Total tracks collected	Event Rate
1.89GeV	2.56cm x 1.28cm	>300k	>1Hz/cm2

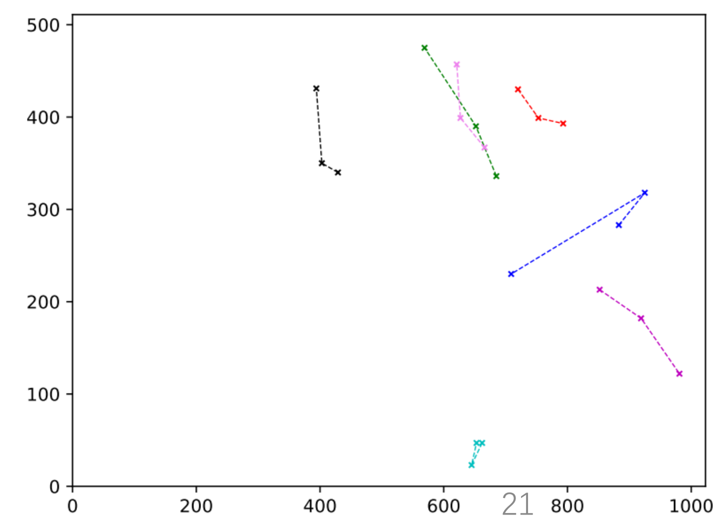
Cluster size



3D track event display



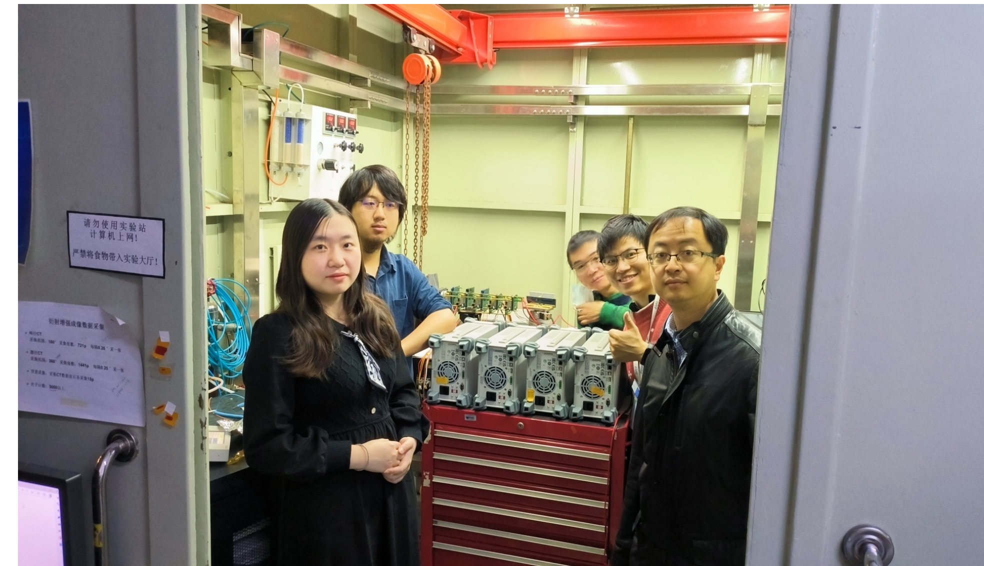
track projection



Shuqi Li

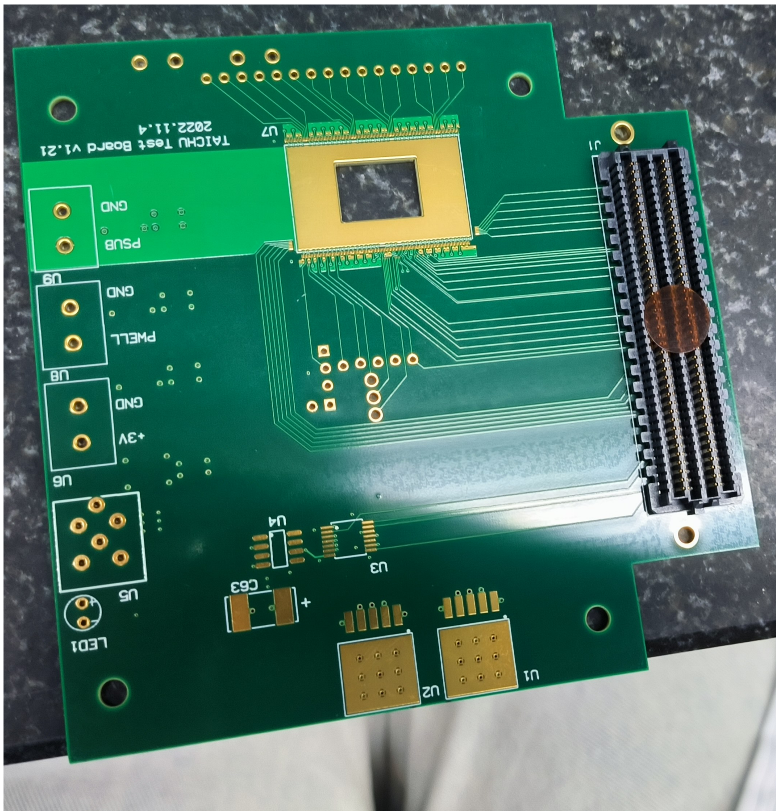
Summary

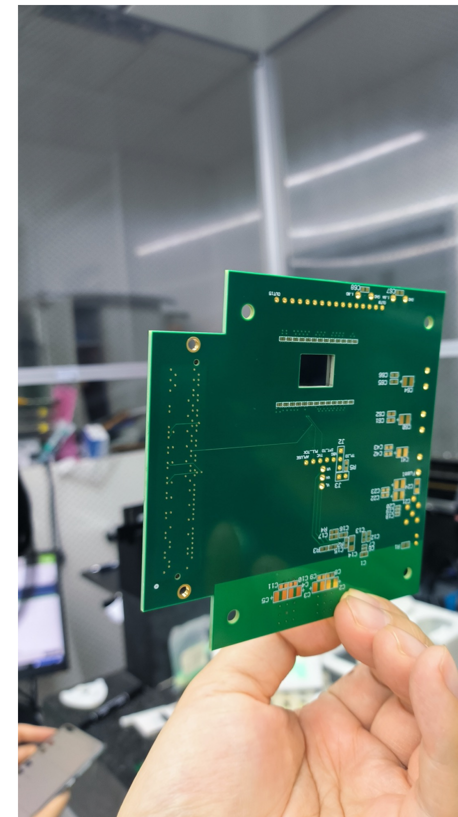
- **Large-scale sensor chip (TaichuPix-3) from engineering run ready**
- **Detector module (ladder) assembly in progress**
  - ➢ There is still some issue in reading out the signal in normal communication mode
- **Full vertex detector prototype assembly in process**
- **Rehearsal test beam using Taichu3 telescope at BSRF was successful**
- **To Do**
  - ➢ Working on communication with chips on flex (ladder)
  - ➢ DESY Test beam in middle Dec
    - Taichu3 single board telescope ready
    - Working on vertex detector prototype



Thanks for your attention!

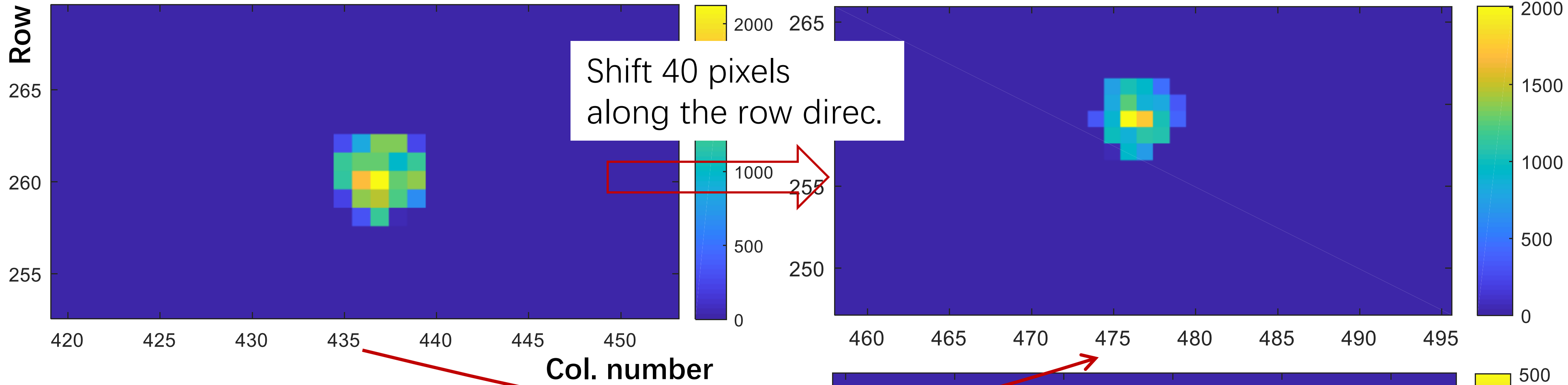
Backup : Test boards with hole for testbeam

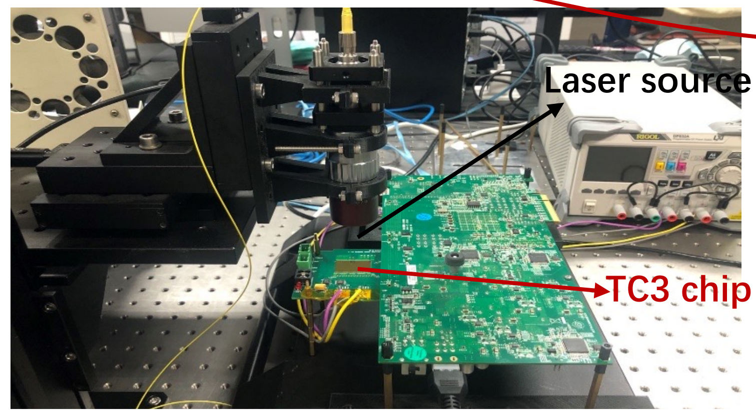


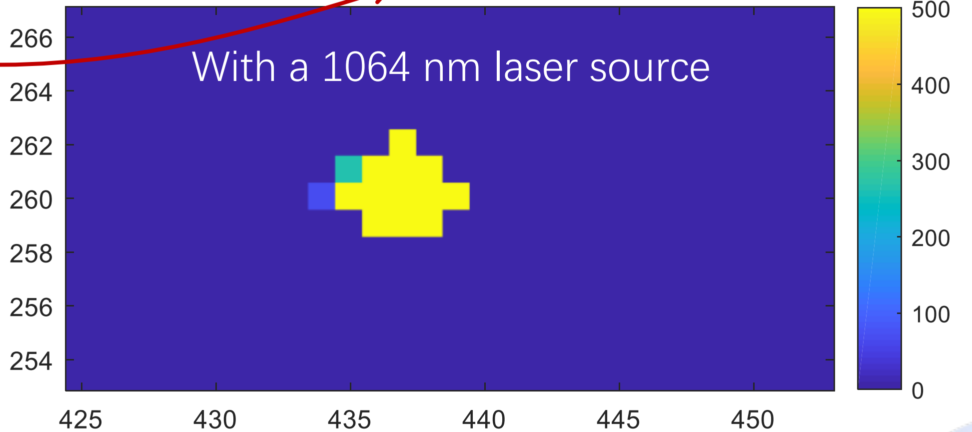


First laser tests on TaichuPix3

- **Using laser sources to verify the functionality**
  - ➢ With a 653 nm laser source & all pixels unmask







- **Functionality of the full signal chain proved**
  - ➢ Sensor+ pixel analog + pixel digital + periphery readout + data interface

TaichuPix3 test with ^{90}Sr

- **TaichuPix3 has a matrix size of 1024x512, an algorithm was developed to configure pixels one by one.**
- **Chips without top-IO work normally under exposure to ^{90}Sr source**

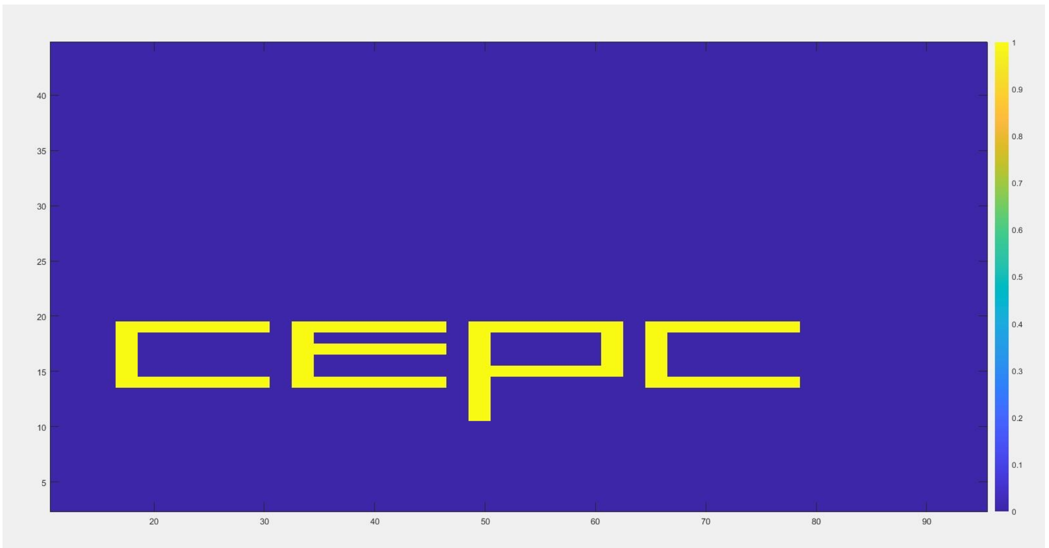


Fig.1 TaichuPix3 self-test with only several pixels turned on

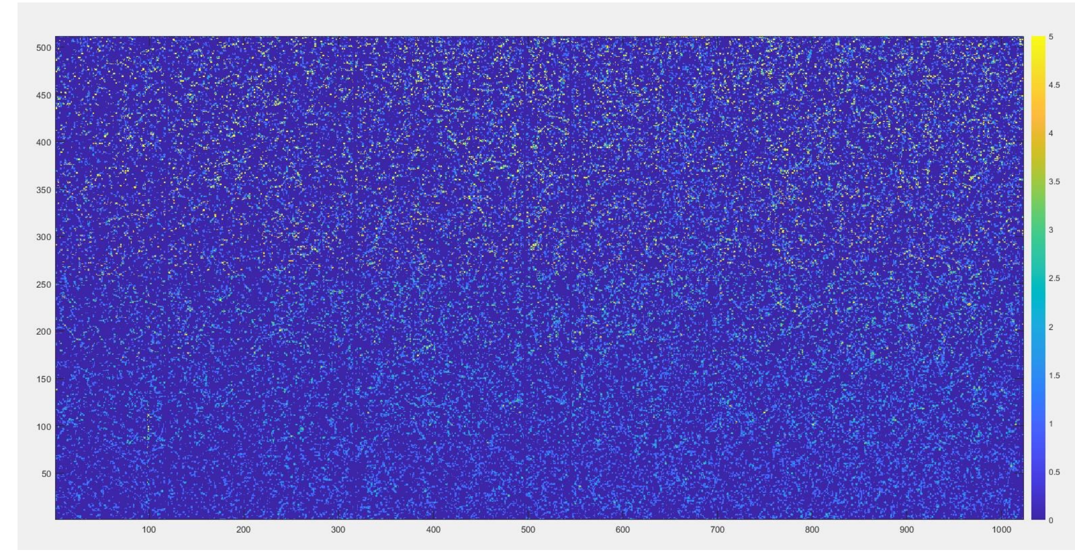
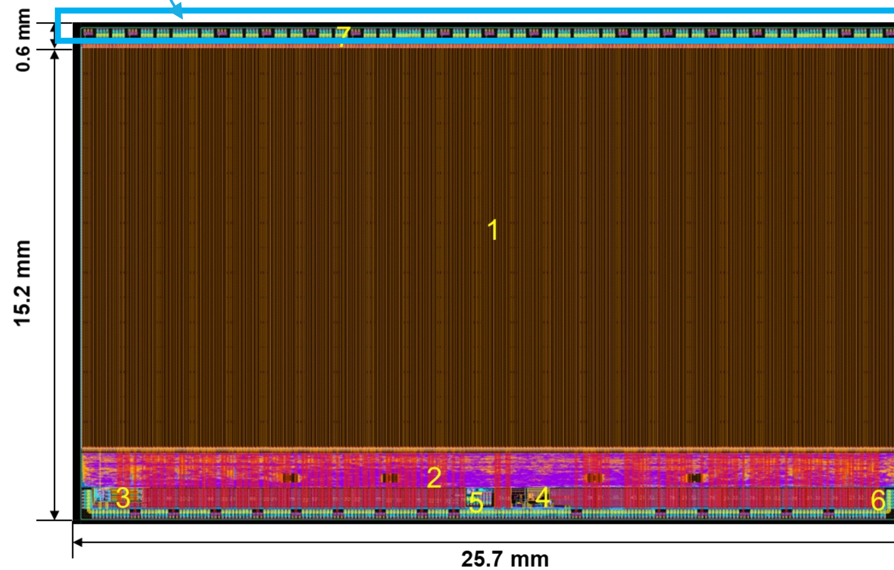


Fig.2 TaichuPix3 without top-IO was injected to the full matrix by ^{90}Sr

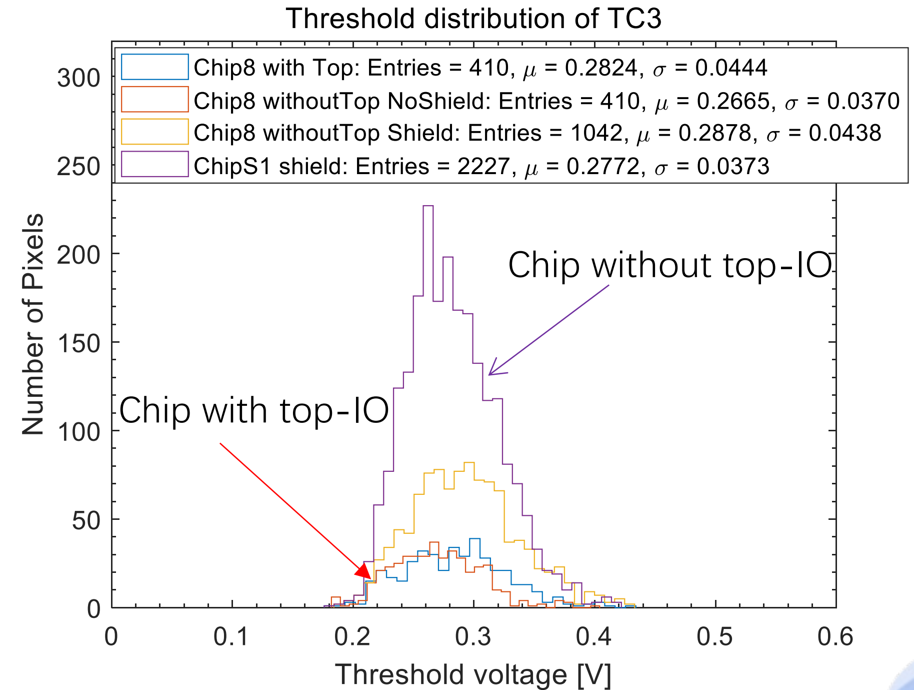
- At the ITHR = 32; Preliminary cluster size calculated is 1.87
- More Cluster size test with a ^{90}Sr on-doing

Power IR-drop study of large-scale sensor

- **Power pads and power/bias rails at the top to help ease the IR Drop**
  - ➢ 2 levels dice-able for complete power study
    - ● Top IO (400 µm) + power rails (200 µm) : full testability at the test board
    - ● Only with power rails:
      - Extra power path; extra bias connection make the resistance half
    - ● Can be fully diced, 600 µm smaller in height



TaichuPix-3



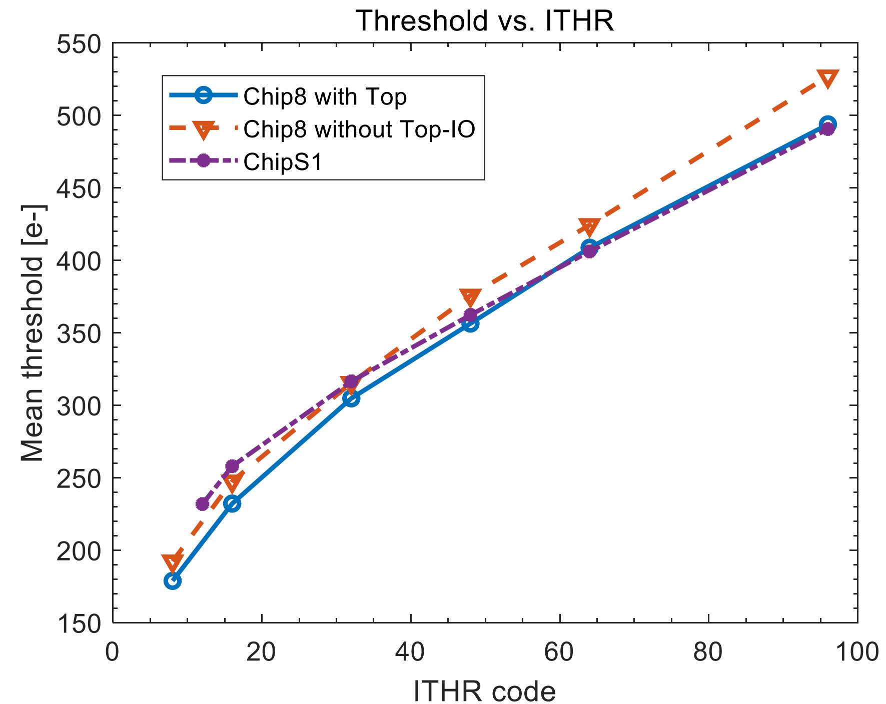
- **Chips without top-IO work normally thanks to good power net arrangement**

Threshold and noise of TaichuPix-3

- **S-curves measured for different chips**

	Mean threshold	Threshold rms	Mean noise	Noise rms
Chip8 with top IO bonding	310.4 e	48.8 e	21.1 e	4.8 e
Chip8 without top bonding	316.2 e	48.1 e	21.4 e	4.8 e
ChipS1 (no top-IO)	304.6 e	41.0 e	19.3 e	4.4 e

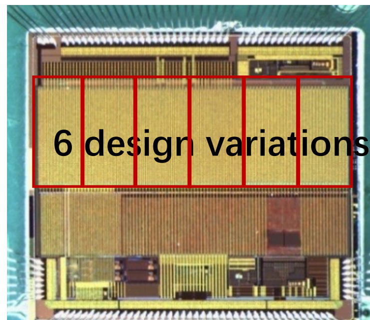
- **Top-IO has minor effect on threshold and noise**
  - ➢ Minimum mean threshold need to be further verified with more chips



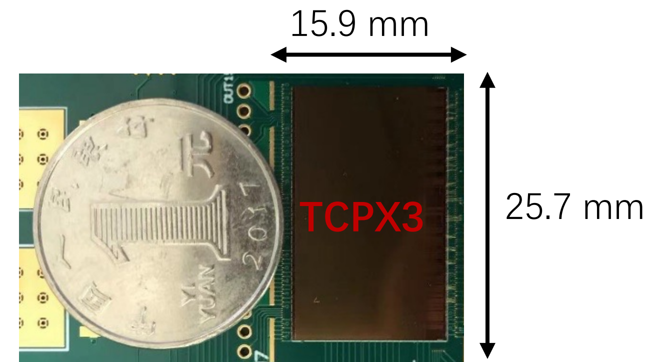
TaichuPix sensor prototyping

- **Major challenges for the CMOS sensor**
  - ➢ Small pixel size → high resolution (3-5 μm)
  - ➢ High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - ➢ Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 round of sensor prototyping in TJ-CIS 180 nm process**
  - ➢ Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019.06 – 2019.11
    - TaichuPix-2: 2020.02 – 2020.06
  - ➢ 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022

TaichuPix-1

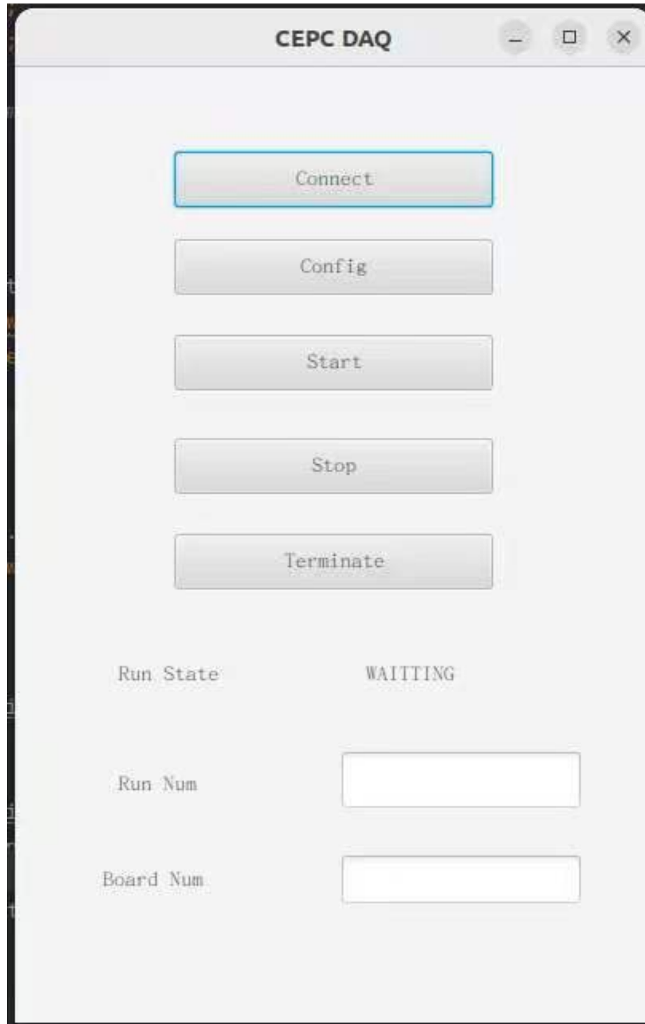


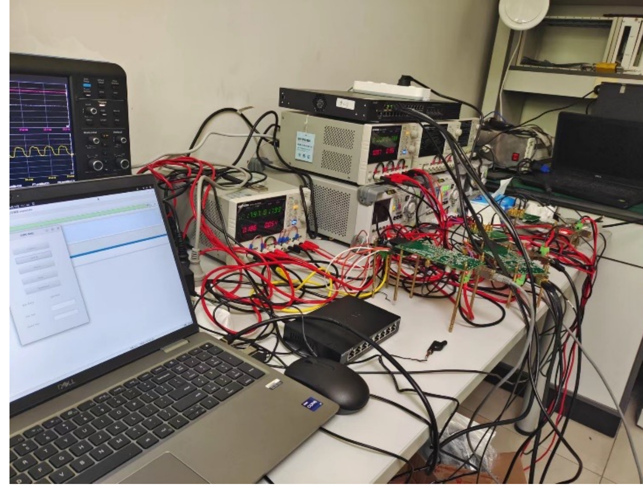
TaichuPix-2



TaichuPix-3
Pixel size：25 μm × 25 μm

Development of Data acquisition system





- CEPC DAQ system is under developing

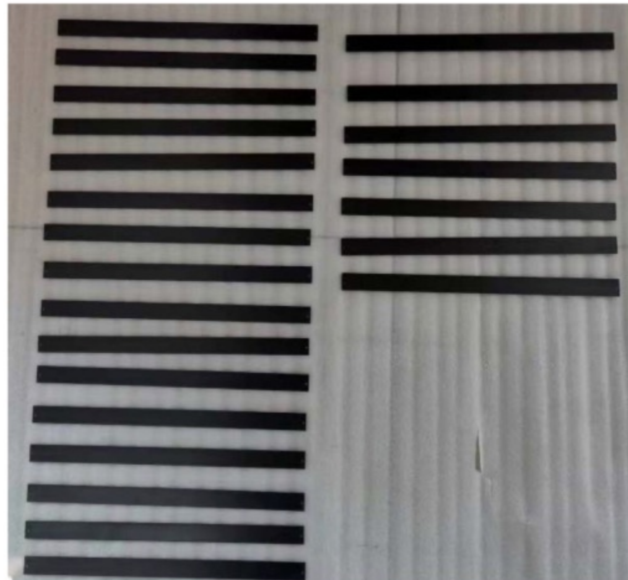
➢ Two test boards were configured by DAQ
➢ Ultimate DAQ will be used to configure all the chips

Next phase:
➢ To configure one flexible board with 10 chips

Support structure of the ladder

- **Production of ladder support with carbon fiber is in good progress**
  - Half of the ladder support has been produced
  - The yield of first batch of production is a bit low (~30%)
  - New batch of production has higher yield
  - Expected 120 good ladder support in this production

New batch ladder support



Inner barrel

Middle barrel
(Ladder support-half quantity)

CEPC

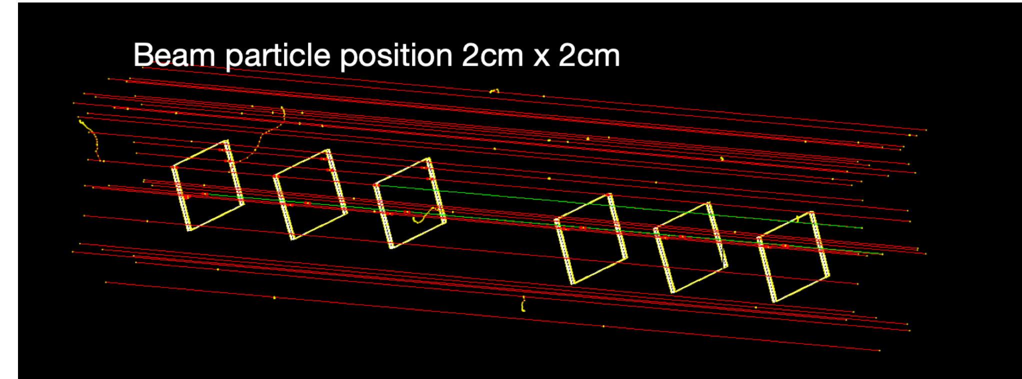
MOST2 offline reconstruction and alignment

Track Reconstruction

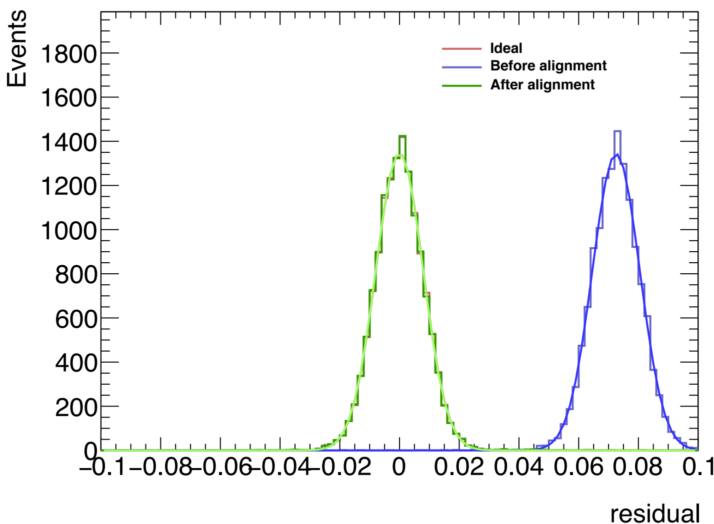
- No magnetic field
- Least squares fitting (Straight line fit)
- No considering multi-scattering now

Alignment

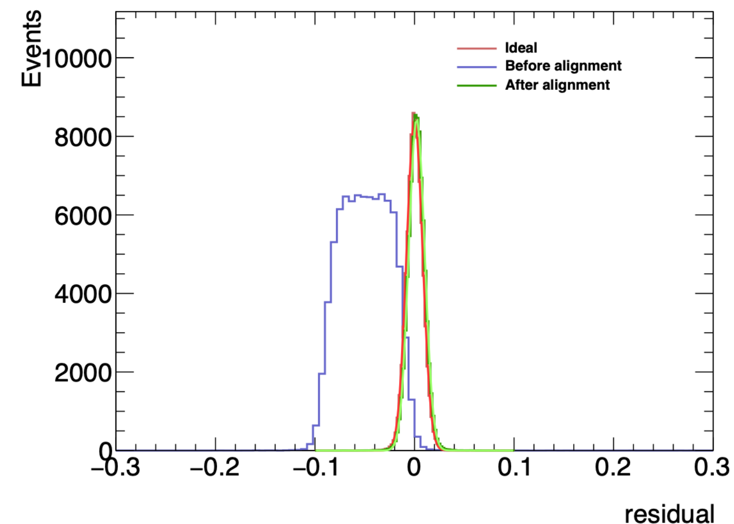
- Using Millepede (c++ version) matrix method
- Correct for the misalignment chip position
- Evaluate the influence of different alignment parameters on spatial resolution



- If the chip translation on X and Y

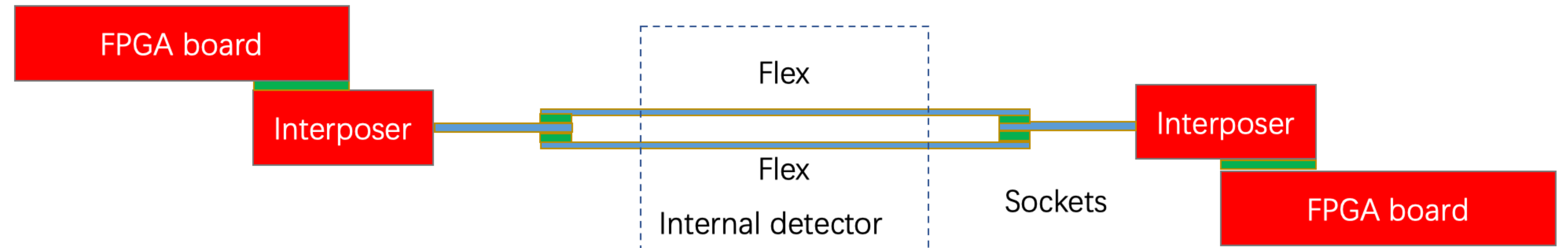


- If the chip rotation around beam direction



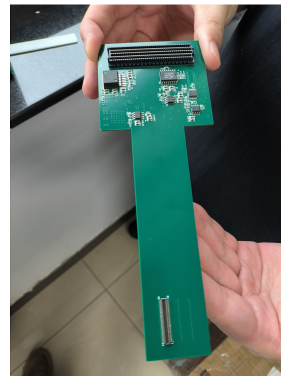
Ladder readout design

- **Flex board**
  - 1st version produced, glue and wire bonding performed at IHEP with dummy chips
  - 2nd version submitted (2-layer version and 4-layer version)
- **Interposer board**
  - First version ready (rigid PCB)
  - Connecting flex to FPGA boards

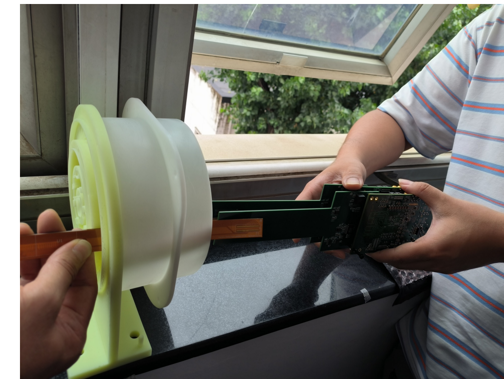


Dummy TaichuPix-3 bonded to the flex board

Interface board

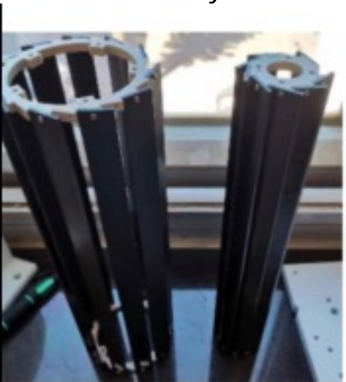


Ladder readout in vertex detector mockup

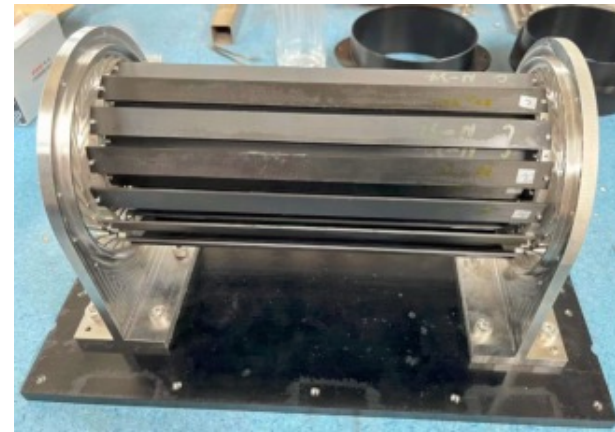


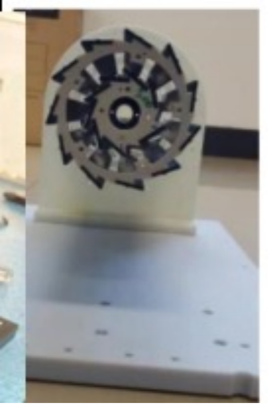
Vertex detector prototype assembly procedure

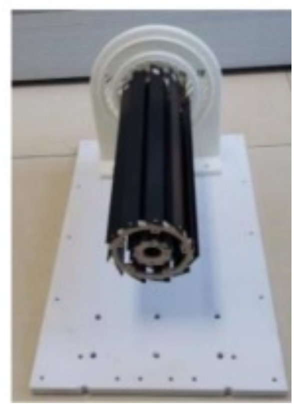
- **Mockup with 3D printing production done**
  - Assembly with 3D mockup model verified the installation procedure
- **Production with aluminum machining done**
  - Assembly will be performed at IHEP early Oct

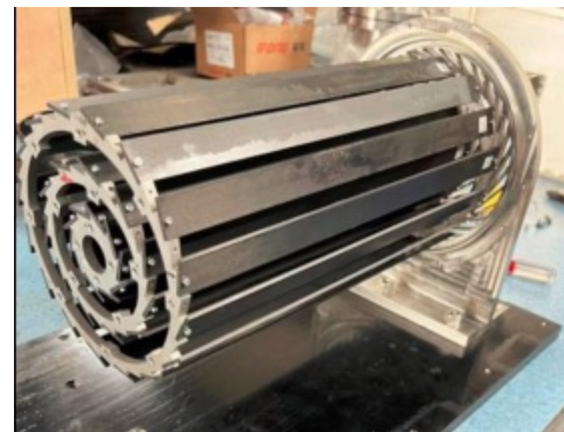


Prototype support with aluminum machining



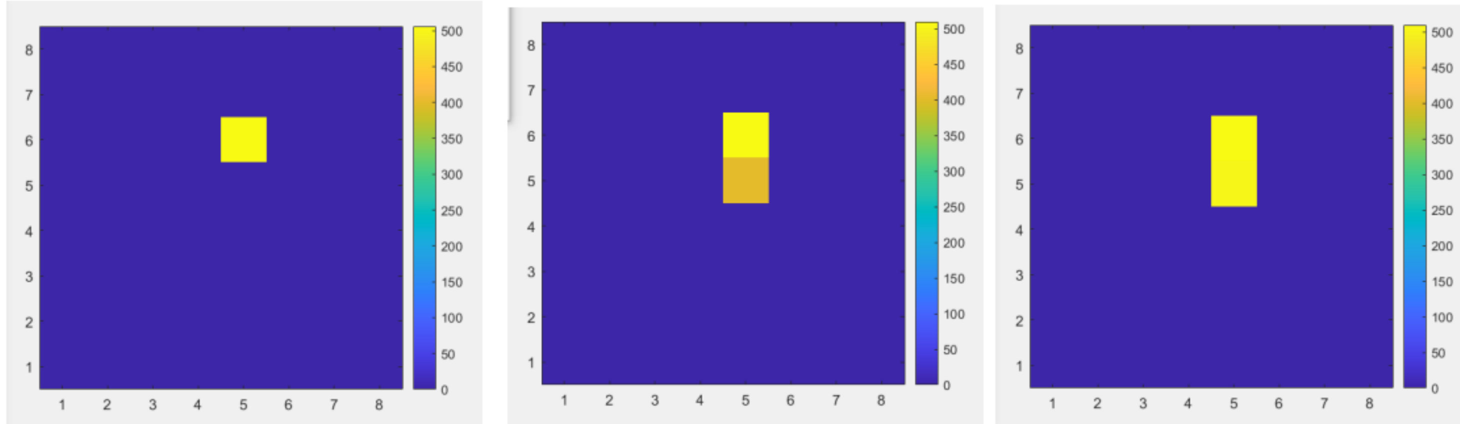




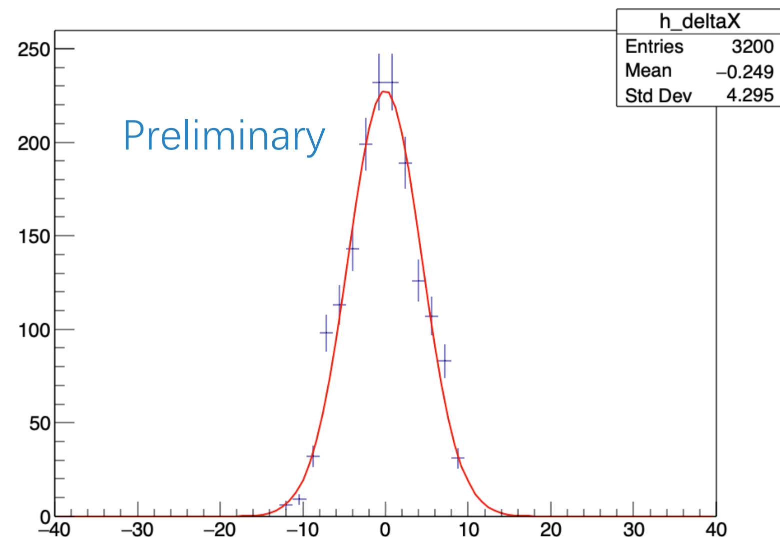


CEPC

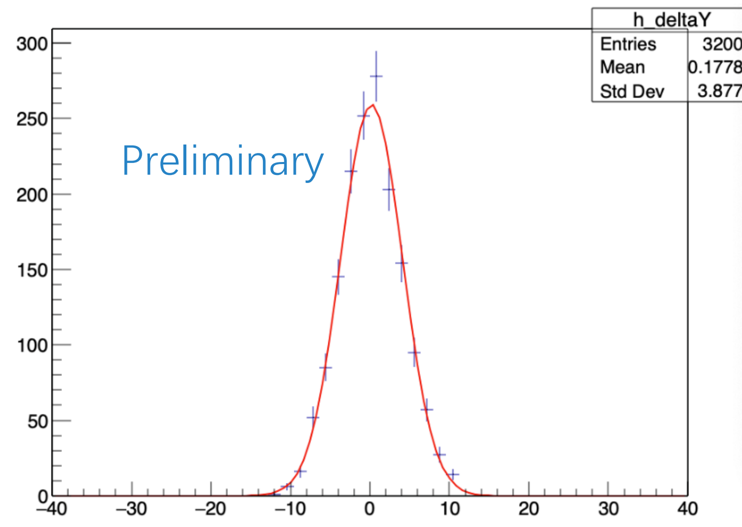
Preliminary spatial resolution with laser



- Laser was scanning with a step of 1 μm on the back of the TaichuPix2.
- Trace of two pixels' response can be figured out clearly on the hit map.
- Preliminary analysis of the data shows a spatial resolution less than 4.5 μm



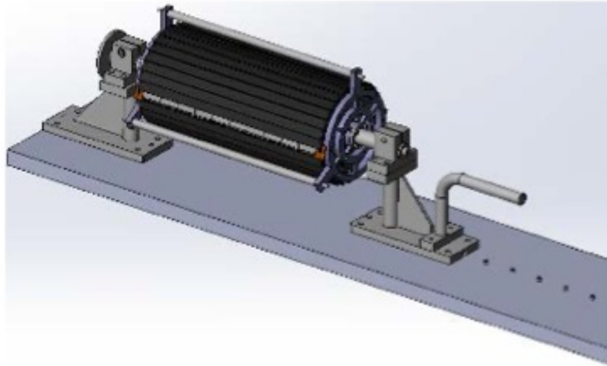
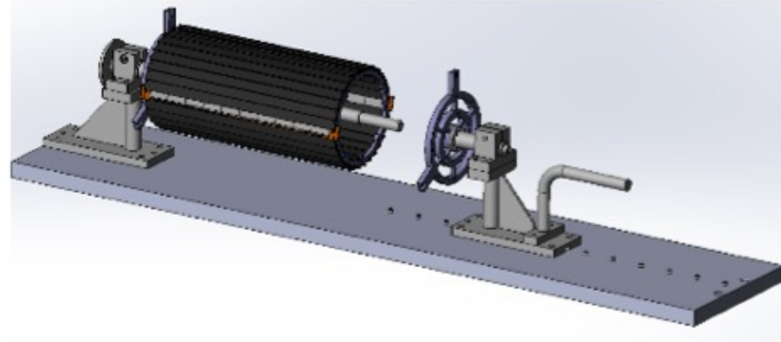
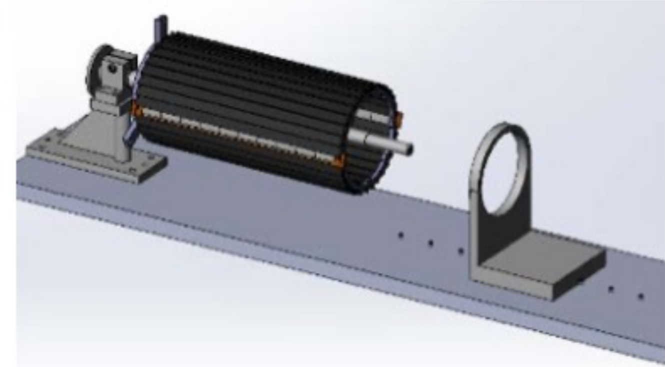
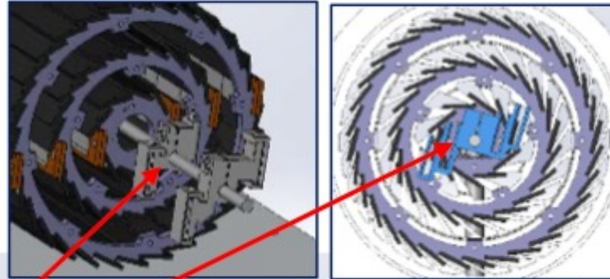
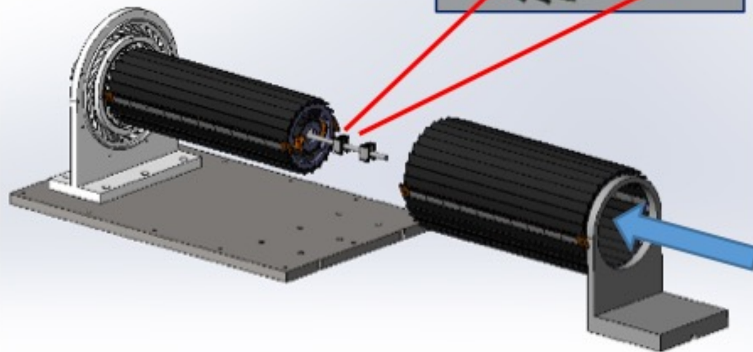
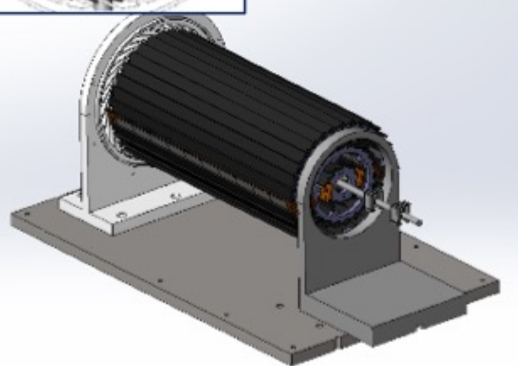
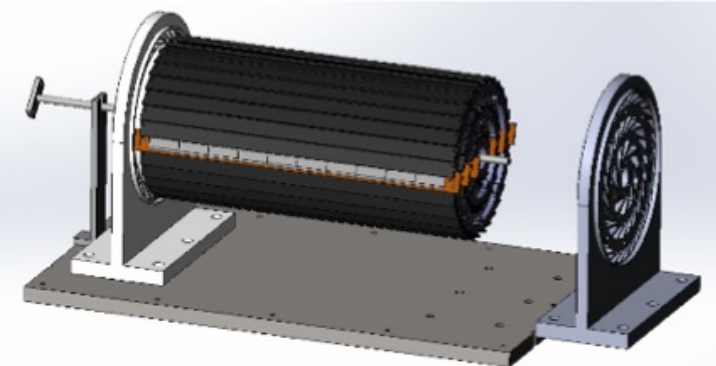
Sigma_residual_x =4.43 μm



Sigma_residual_y =3.93 μm

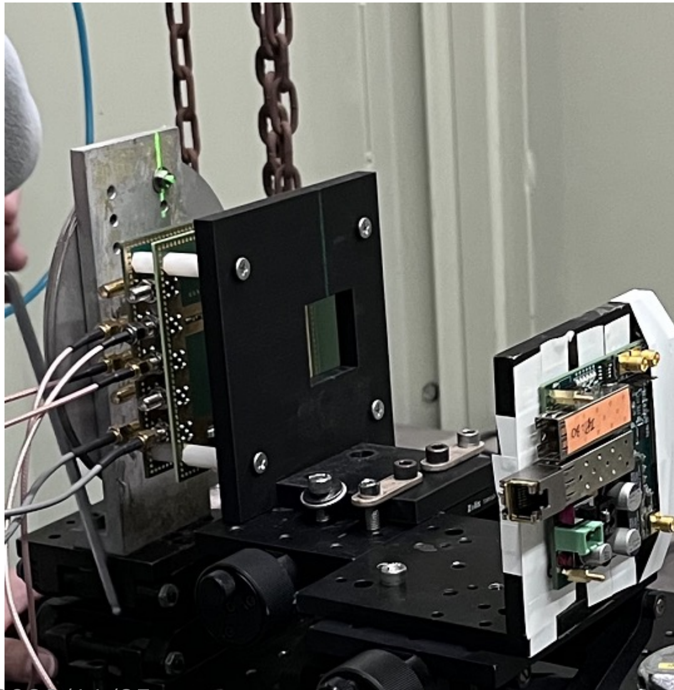
Vertex detector prototype assembly procedure

- **Installation procedure of 3 double layer of vertex detector**

Response from LGAD

- LGAD area：frontend with 2.6mmx2.6mm, backend with 6.5mmx6.5mm
- Coincidence Hit rate: around 20 hit coincidence per miniute,average to 0.34 conincide
  hit per second



Hitmap of 5 layer TaichuPix3 chips

layer 1
W2R3

layer 4
W9R1

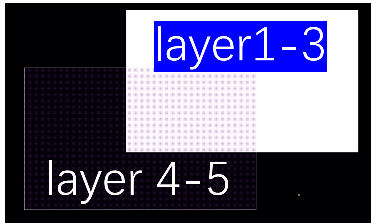
layer 2
W2R11

layer 5
W9R2

layer 3
W2R10

- 3 PCBv1.2- 2 PCBv1.1
- layer1-layer5: W2R3/W2R11/W2R10/W9R1/W9R2

- layer1 to layer3 were the standard chip fabrication process.
- layer4 and layer 5 were with modified process
- layer4/5 has a different positon and with 25% region overlap to first 3 layers
- The hitmap agrees with our



ITHR	chipS1	chip8	W2R3	W2R10	W2R11	W9R1	W9R2
32	304.6	292.9	305.2	276.6	-	168.9	161.5