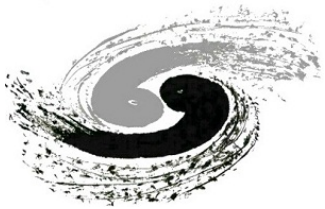
Silicon Tracker status

Yiming Li (IHEP)
on behalf of Silicon Tracker Group



CEPC Day, 25 Nov 2022

Content

- Introduction
- Recent progress
  - ATLASPix3 testbeam and analysis
  - MPW with SMIC 55nm process
- Summary and plan

Silicon tracker for CEPC

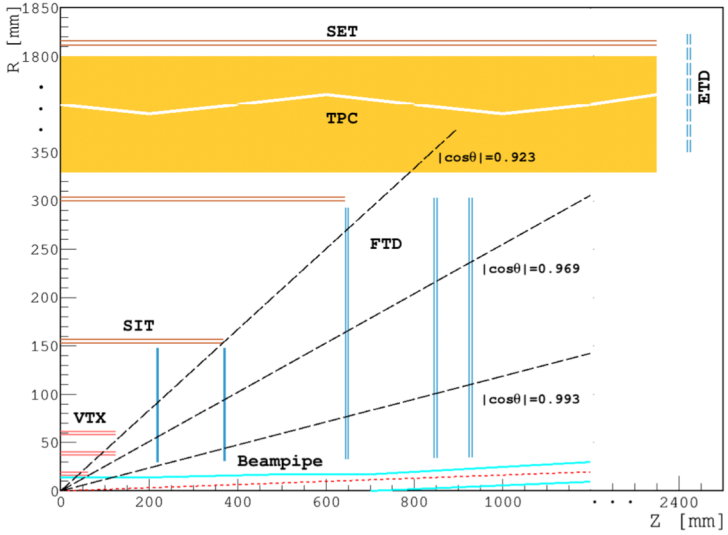
- CEPC requires a high-resolution and low-material tracking system
- Large area of silicon
  - > 70 m^2 for baseline design: Silicon + TPC
  - ~ 140 m^2 for Full Silicon Tracker

$$\sigma_{1/p_T} = a \oplus \frac{b}{p \sin^{3/2}\theta} \quad [\mathrm{GeV}^{-1}]$$

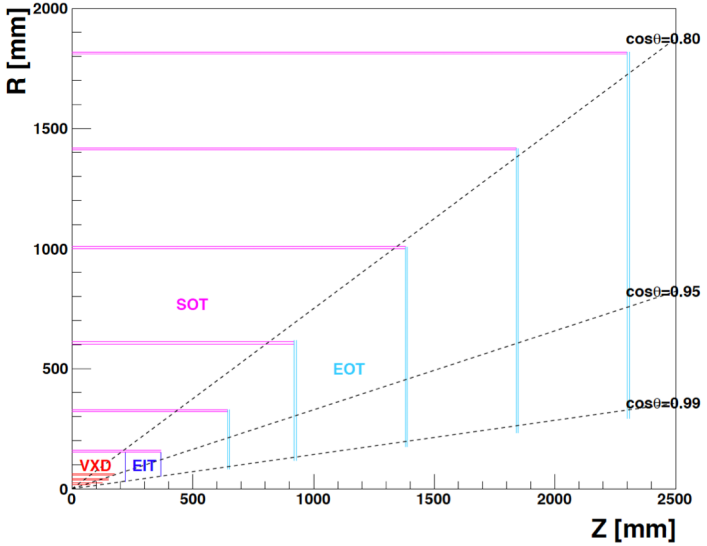
$$a \sim 2 \times 10^{-5}\ \mathrm{GeV}^{-1}$$

$$b \sim 1 \times 10^{-3}$$

- CMOS is a promising technology for performance and cost-effectiveness



Baseline design



Full Silicon Tracker

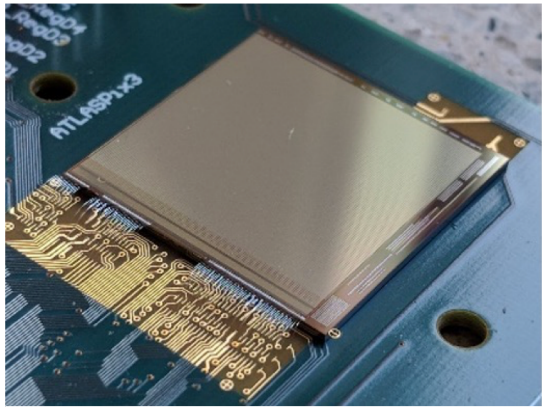
CMOS Silicon tracker collaborators

Convenors: Harald Fox (U. Lancaster), Meng Wang (SDU)

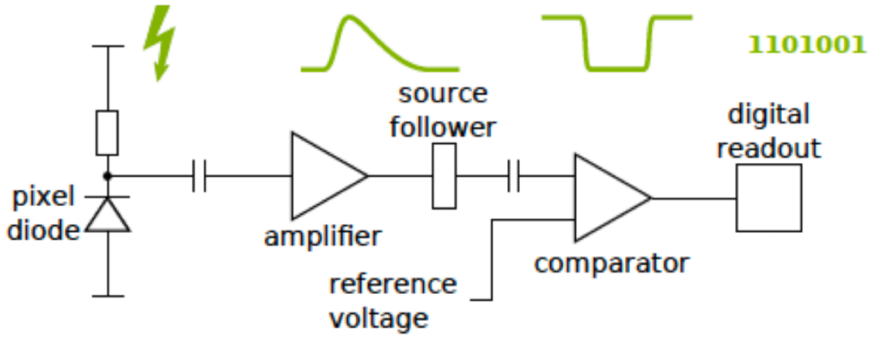
- Australia
  - University of Adelaide
- China
  - Harbin Institute of Technology
  - Institute of High Energy Physics, CAS
  - Northwestern Polytechnical University
  - Shandong University
  - T. D. Lee Institute – Shanghai Jiao Tong University
  - University of Science and Technology of China
  - University of South China
  - Zhejiang University
- Germany
  - Karlsruhe Institute für Technologie
- Italy
  - INFN Sezione di Milano, Università degli Studi di Milano e Università degli Studi dell' Insubria
  - INFN Sezione die Pisa e Università di Pisa
  - INFN Sezione di Torino e Università degli Studi di Torino
- UK
  - Lancaster University
  - Queen Mary University of London
  - STFC – Daresbury Laboratory
  - STFC – Rutherford Appleton Laboratory
  - University of Bristol
  - University of Edinburg
  - University of Liverpool
  - University of Oxford
  - University of Sheffield
  - University of Warwick

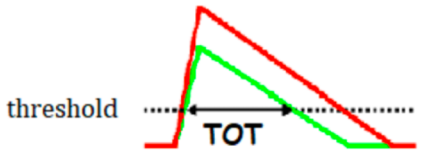
ATLASPix3 sensor

- Prototyping & characterization carried so far with ATLASPix3, a HVCMOS sensor
  - TSI 180nm HV process on 200 Ωcm substrate
  - Pixel size 50 × 150 μm^2
  - 132 columns × 372 rows (20.2 × 21 mm^2 chip)
  - Triggerless/triggered readout possible
  - Binary with ToT information
  - Power consumption ~140 mW/cm^2
- ATLASPix3.1 delivered in 2021
  - Optimised design in metal layers, reduced capacitance of amplifier, reduced timewalk



I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021 https://ieeexplore.ieee.org/document/9373986

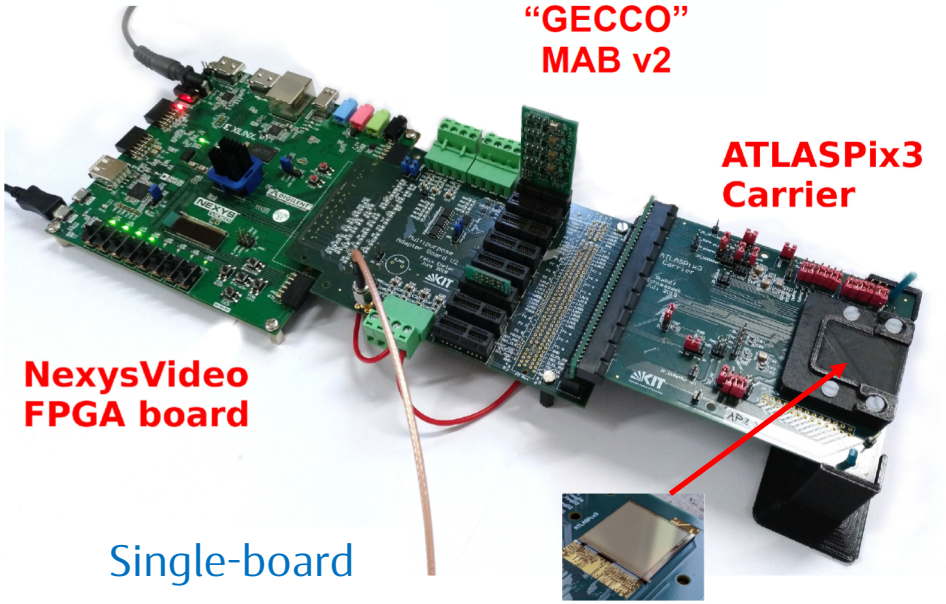




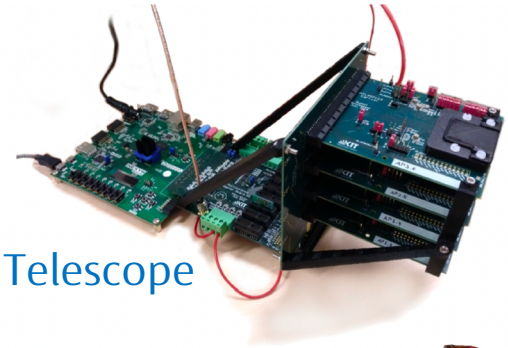
Time-over-Threshold (ToT) as proxy of signal amplitude

Readout system

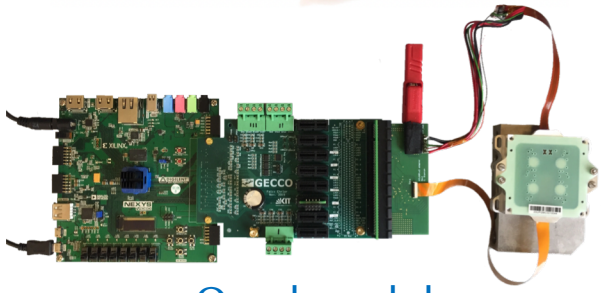
- GEneric Configuration and COntrol System - designed at KIT
- Can be adapted to
  - Single board
  - Telescope config (4 chips in parallel)
  - Quad module (4 chips sharing bias and readout)



Single-board



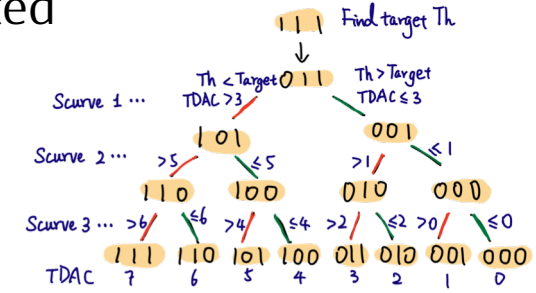
Telescope



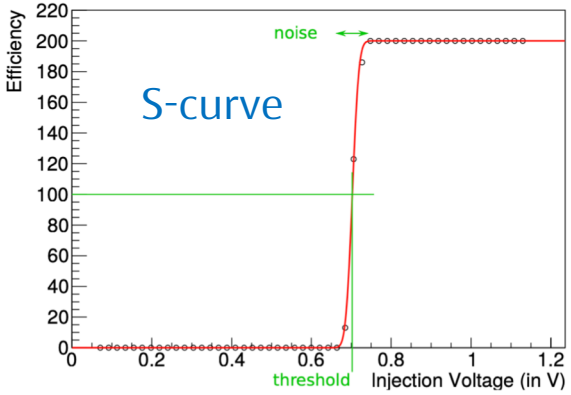
Quad module

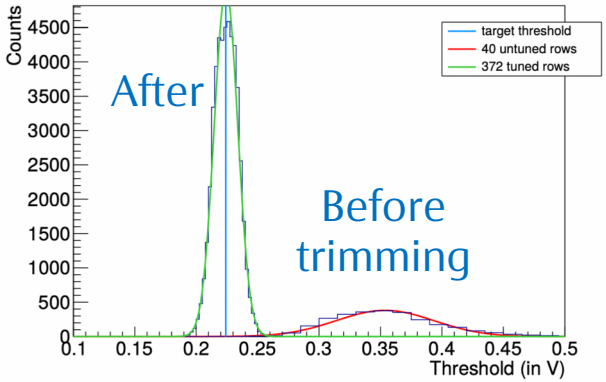
Trimming and optimisation

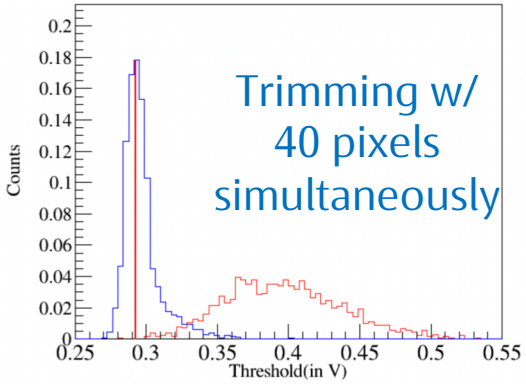
- Each ATLASPix3 pixel contains 3-bit TDAC tunable to achieve equalized threshold across the pixel array
  - Threshold scan performed for all pixels S-curves fitted
  - Repeat until reaching targeted threshold
- Trimming a whole pixel is time-consuming
  - Efforts made to understand+shorten the process
  - ~10h → ~4h by trimming 40 pixels simultaneously



Mingjie Feng, Jinyi Sun



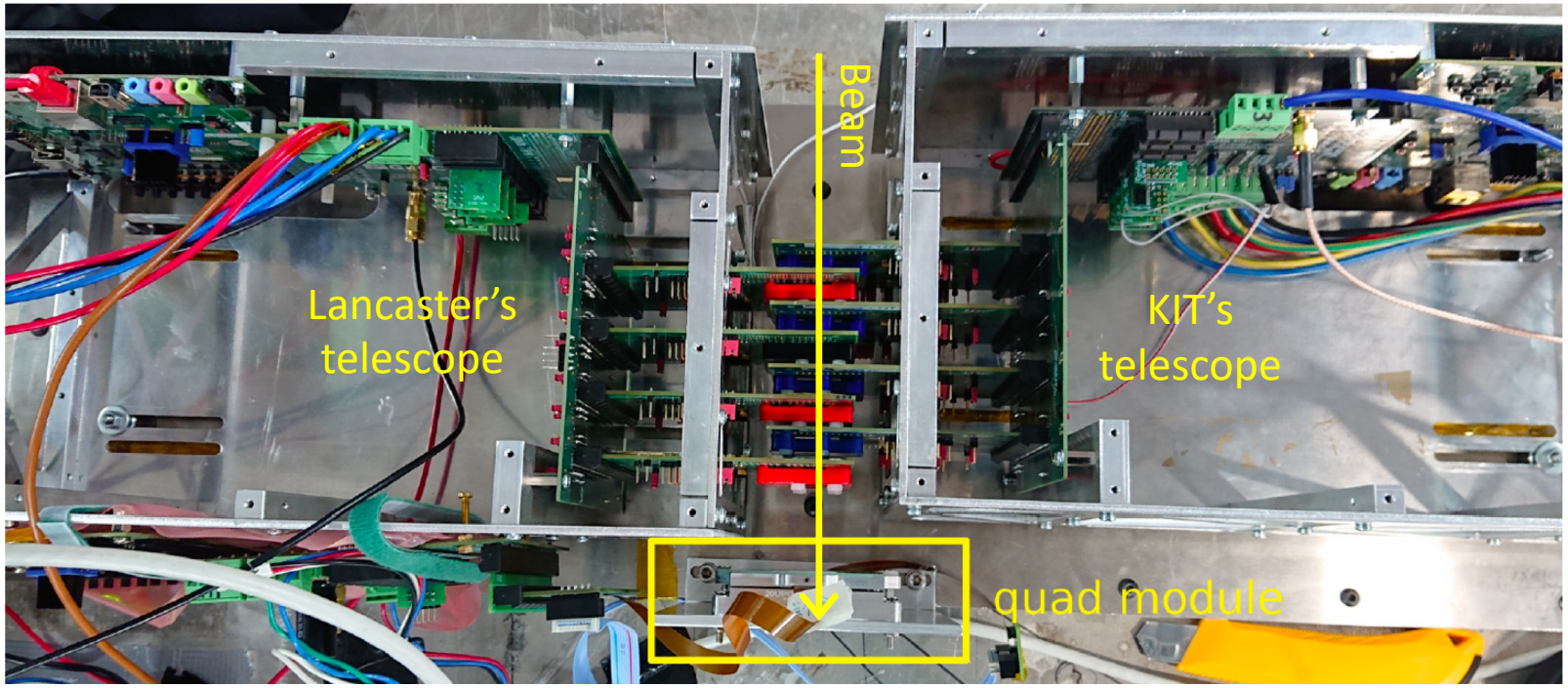




Testbeam

Bristol, Edinburgh, IHEP,
KIT, Lancaster, RAL ⋯

- Testbeam at DESY using 6 GeV e- beam in April 2022
- Two telescope systems+ a quad
  - Beam energy scan: 1-6 GeV
  - Angle scan: 0~>80 degree
  - HV scan: up to -48.6V
  - Two telescopes interleaving

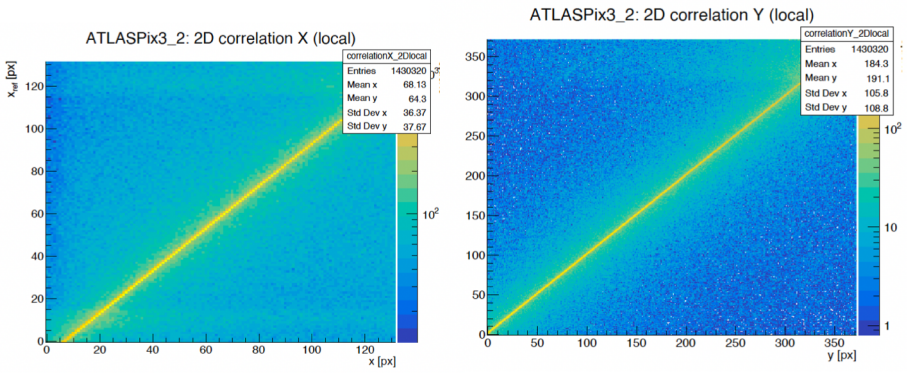


Lingxin Meng @ VERTEX 2022, Oct
Ruoshi Dong @ CEPC day, Jun

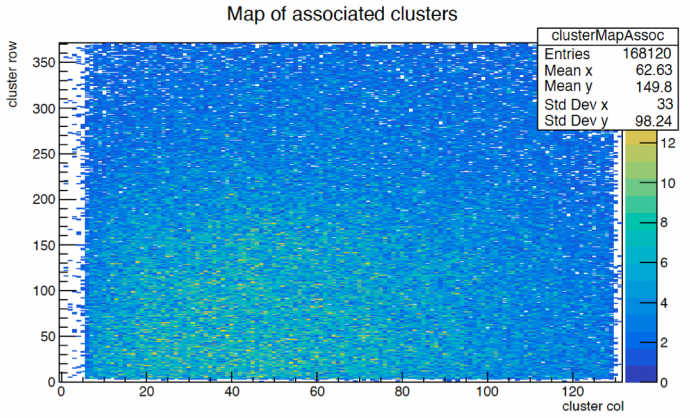
Preliminary results

- Track reconstruction using Corryvreckan
- Using 3 layers in a telescope as tracking planes, 1 as DUT

Lingxin Meng @ VERTEX 2022, Oct



Correlation in X and Y between two neighbouring layers

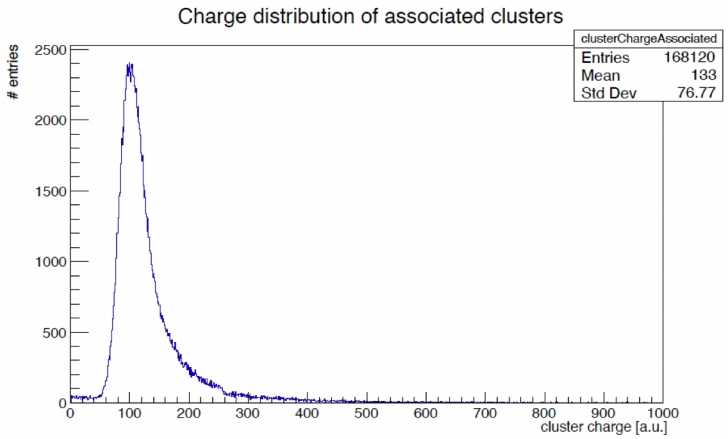


Clusters associated with tracks

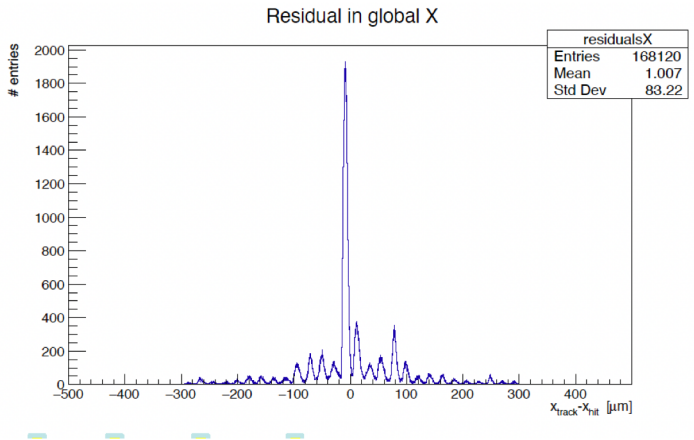
Preliminary results

Lingxin Meng @ VERTEX 2022, Oct

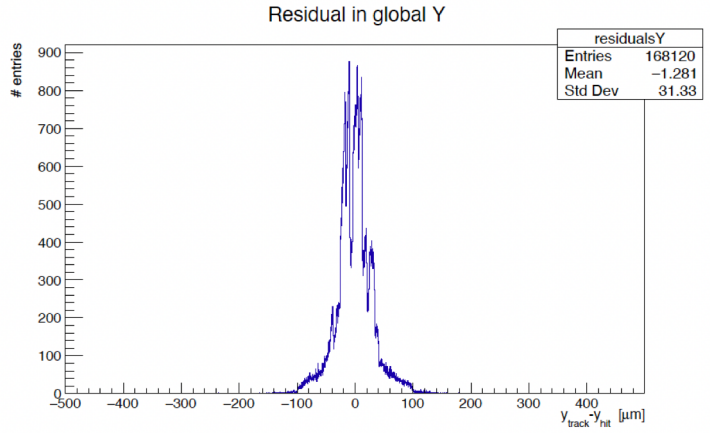
- Mostly single-pixel clusters
- Peaking structure in both residuals
  - Mainly due to single-pixel cluster



Cluster charge assc. w/ tracks



Residuals in X

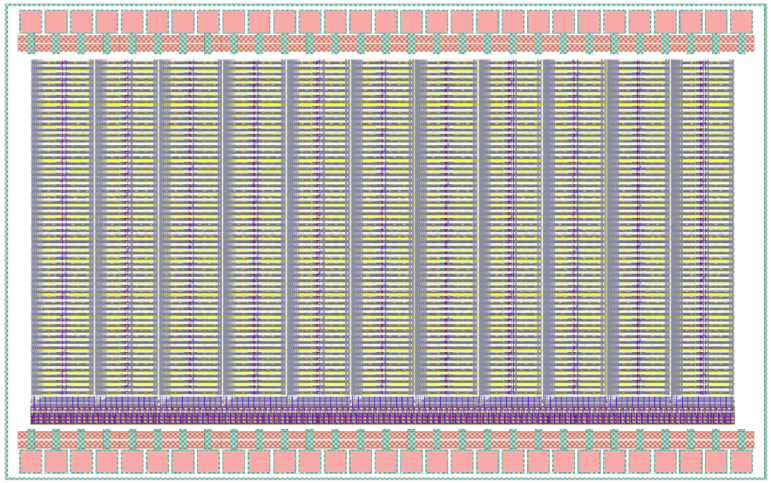


Residuals in Y

Sensor development

- ATLASPix was developed with TSI 180nm HV process, new sensor development for CEPC should be pursued
  - Smaller pitch, lower power consumption, lower noise …

- Attempt to contact potential foundries in China
- HLMC 55nm HV process
  - Seeking MPW opportunity with input (pixel-matrix design) from KIT
  - Caveat: wafer with high-resistance substrate not yet supported
- SMIC 55nm process
  - HV and normal (Low-Leakage) process available
  - Possible to use high-resistance wafer

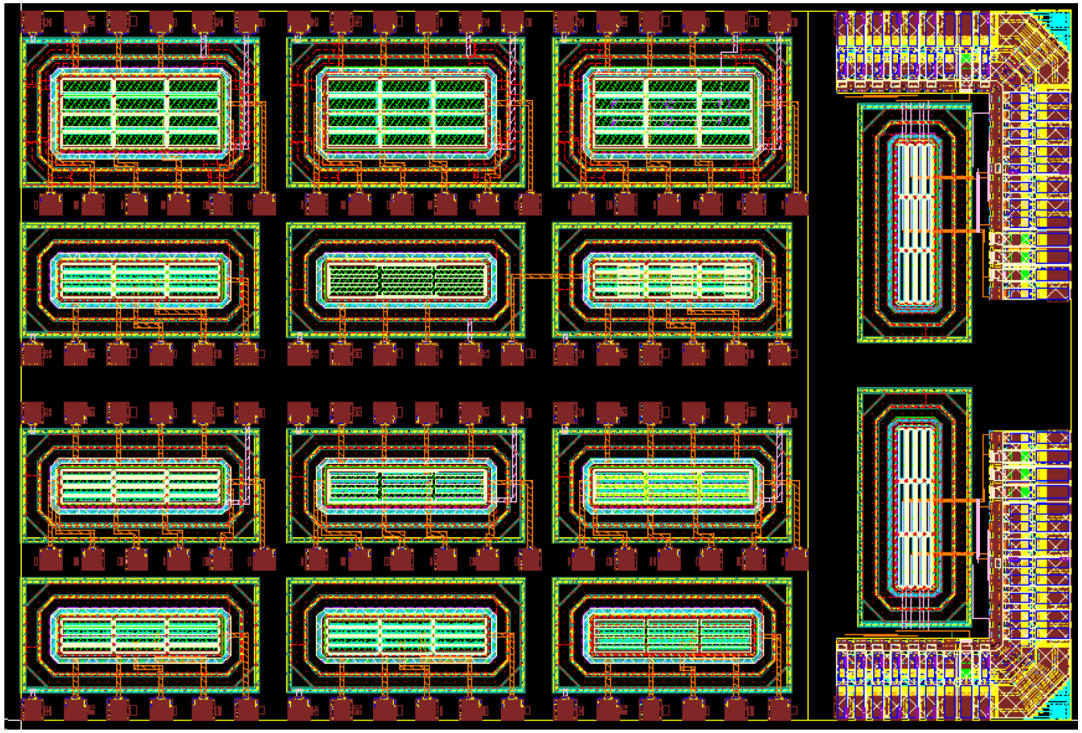


KIT design of test matrix for HLMC MPW

MPW with SMIC 55nm process

IHEP, HNU, ZJU

- In October, design submitted for MPW with SMIC 55nm LL process
  - Short-noticed, 2-month spent on design
  - An area of 3×2 mm^2 is targeted
  - Expected to deliver in ~5 months
- Simple design with passive sensor diodes + a couple of amplifiers

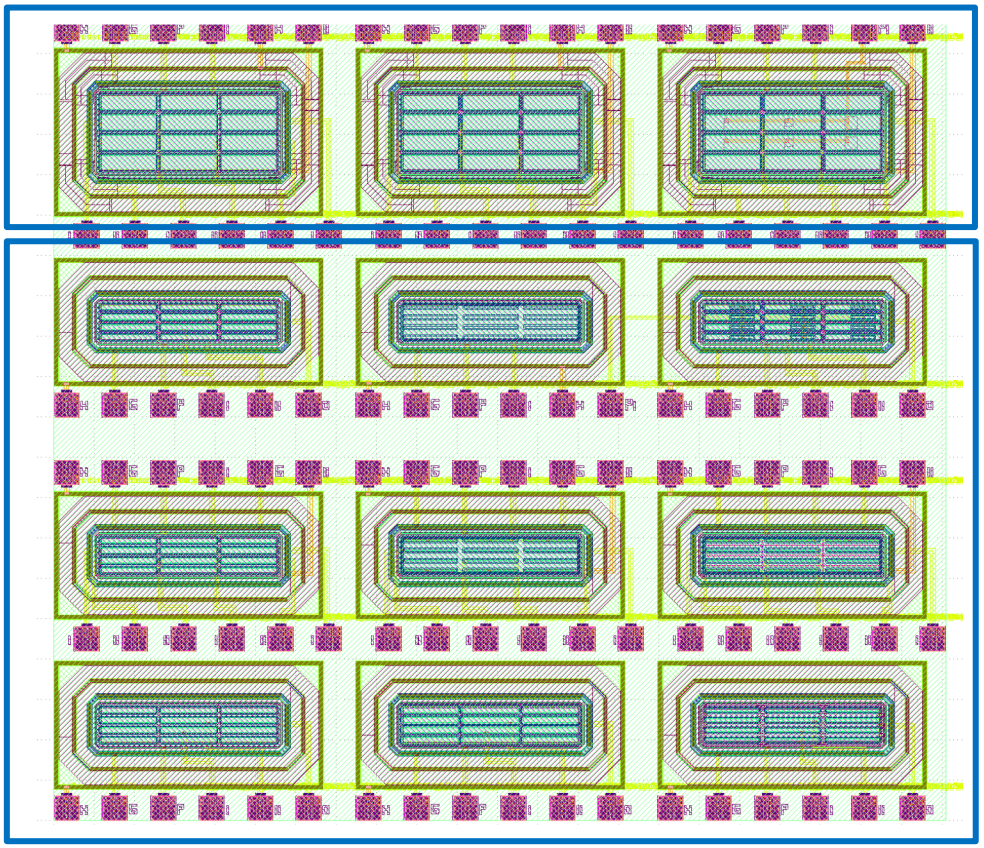


Passive sensor arrays

Mei Zhao

- NB: no HR substrate
  - Limited charge generation
- 12 layout design
- Pixel size：
  - 25x150um, 50x150um
- Pixel array： 3x4
  - For charge sharing study
- Different design:
  - P stop between pixels:
    - With/without
  - Space between pixels:
    - 5um, 10um, 15um
  - Connection method
  - Pwell area in Dnwell:
    - Capacitance affect

Pixel size:50x150um

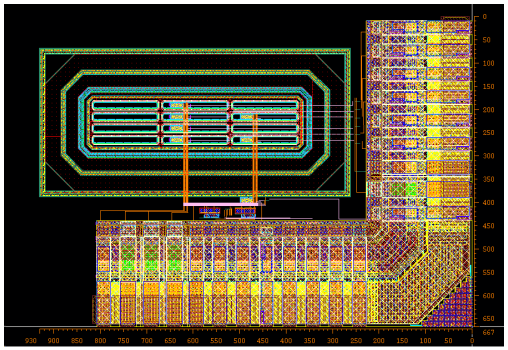


Pixel size:25x150um

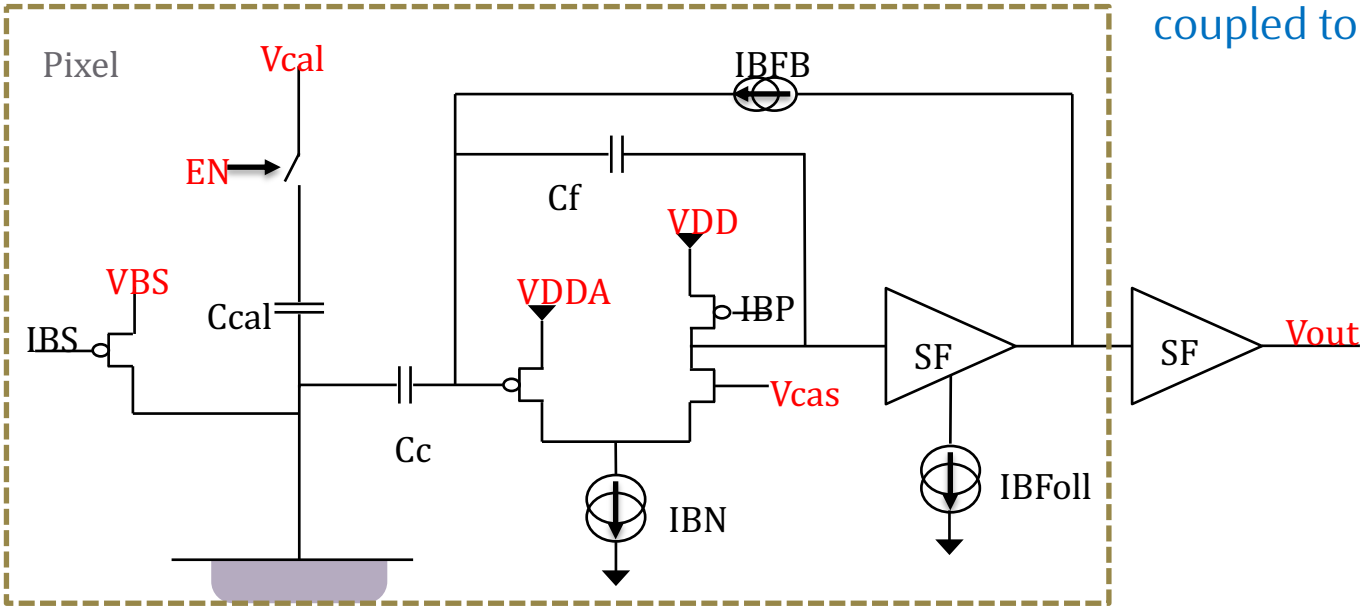
Schematic

Weiguo Lu

- Sensor biased with active resistor
- Calibration capacitor integrated
- Charge Sensitive Amplifier structure
  - Two power supplies
  - Folded cascode amplification stage
  - Constant feedback current
- Two stage source follower used to drive the signal out



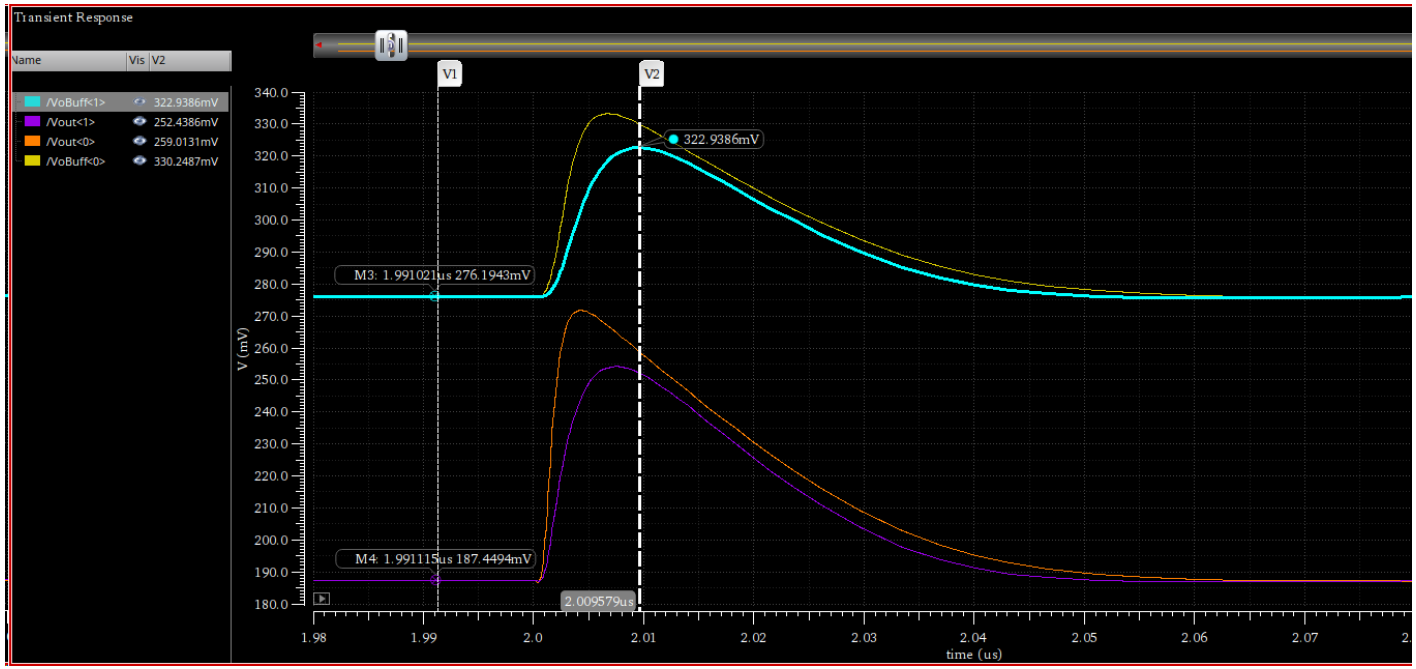
6 channels AC coupled to sensors



Current reference + bias

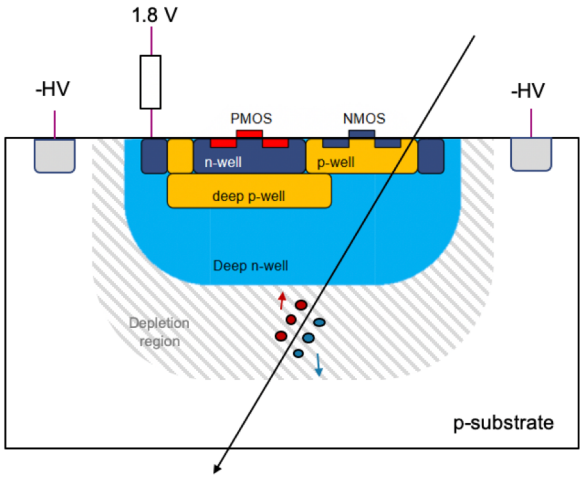
CSA simulation

- Typical parameters
  - Cd:~100fF, Ileak:~10pA
  - Cf=2fF, Cc=450fF, Ccal=1fF
  - Power:~4uW per CSA
  - SNR:~13 for 1638e-(Fe55)
  - Rise time:~10ns



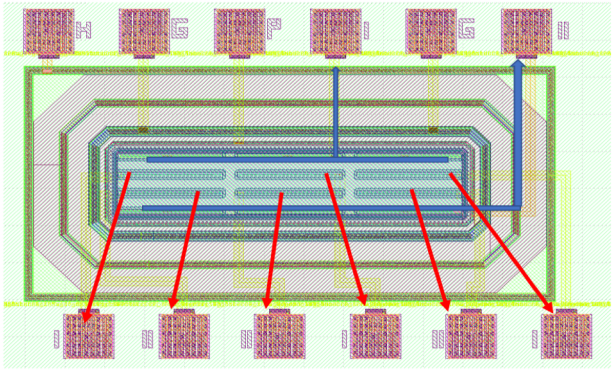
Remarks

- HR substrate (>100 Ohm m) is essential for signal generation
- LL process rules might not allow bias which is very high
  - To be tested
  - Future R&D with HV process should be pursued
  - Experience accumulated with this MPW is invaluable

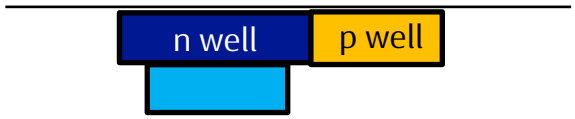


Working principle of HV-CMOS sensors.

HV process



Array with small electrodes



Deep n well

LL process

Summary and plan

- Lab test with ATLASPix3 with single/4-chip
  - Trimming process is long but improved
  - In the longer term efforts will made on prepare VLDB-compatible readout
- Testbeam at DESY in April successful
  - Preliminary results presented
  - A lot more analysis ongoing
- Sensor R&D using Chinese foundry ongoing
  - MPW submitted to SMIC 55nm process
  - More follow-up test and development expected