



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

TaichuPix-3 test

Ying ZHANG

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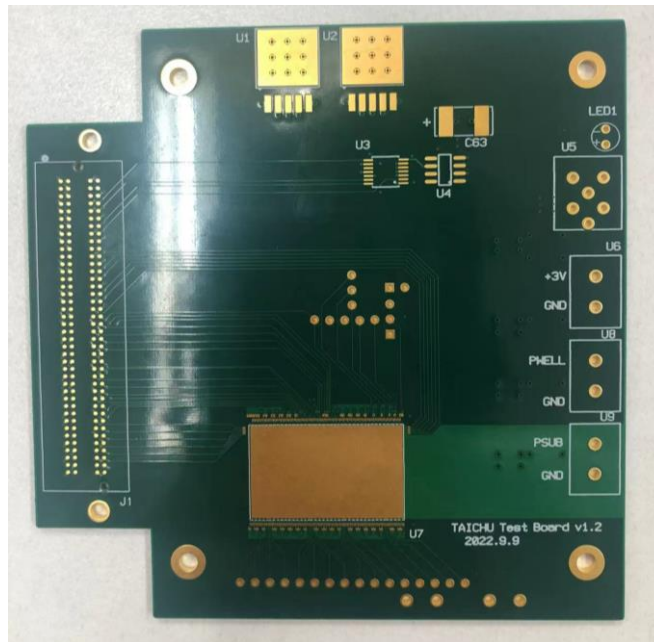
TC3 test on the new version board

■ Testboard v1.2 ready

- Power supply for substrate of chip is possible

■ 5 chips boned on the testboard v1.2

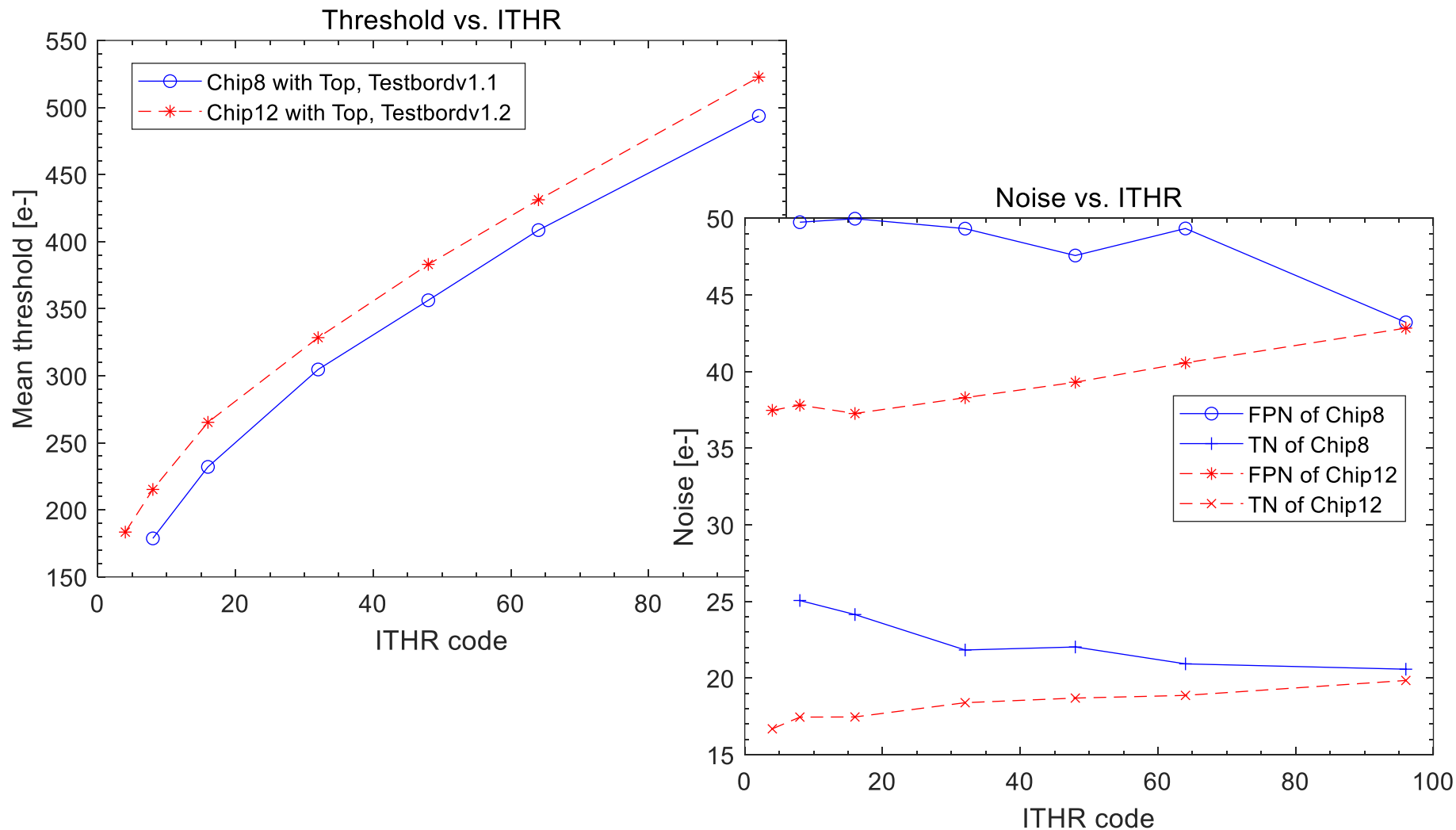
- 3 chips with top-IO: **chip12, chip13**, chip14
- 2 chips without top-IO: S3, S4
- Chip 12&13 work, the others have power short problem



Test board v1.2

Comparison of different versions of testboard

■ ITHR scanning



Issue of pixel array mask

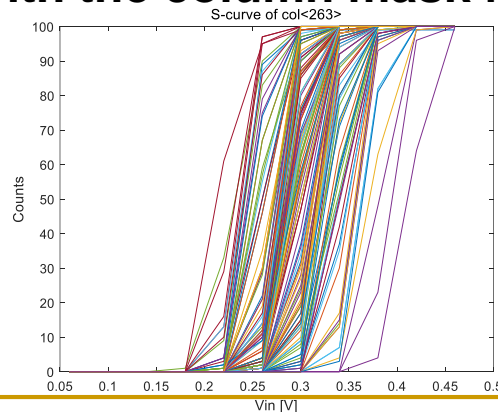
■ Readout abnormal with normal pixel array mask for chip 12 & 13

- Whatever the input (apulse/dpulse/no input with light-shield), 3 cases of output
 - Output pixel <317, 1023>, most possible case, this pixel was actually masked with array mask configuration

	1	2	3	4	5	6	7	8	9
1	1	0	317	1023	0	42	118	143	209
2	1	0	317	1023	0	42	118	143	209
3	1	0	317	1023	0	42	118	143	209
4	1	0	317	1023	0	42	118	143	209
5	1	0	317	1023	0	42	118	143	209
6	1	0	317	1023	0	42	118	143	209
7	1	0	317	1023	0	42	118	143	209

- Output pixel <237, 0>
- No output

■ If mask column <317> with the column mask function, then chip works normal



Summary

- **Test board v1.2 works normal for standard chips**
 - Test board v1.21 with board opening underneath of chip, in production

- **Pixel array mask failed for some pixels in several chips, need to be understood**
 - Chips 12 & 13 on test board v1.2
 - Found in the beginning of test
 - Modified Chip W9R2
 - Found in the beginning of test

 - Chip 2 on test board v1.1
 - Works normal in the beginning, issue found after one month