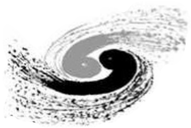
国家重点研发计划

R&D and Verification of Key Technologies for a High Energy Circular Electron-Positron Collider

Zhijun Liang for CEPC MOST2 vertex detector team



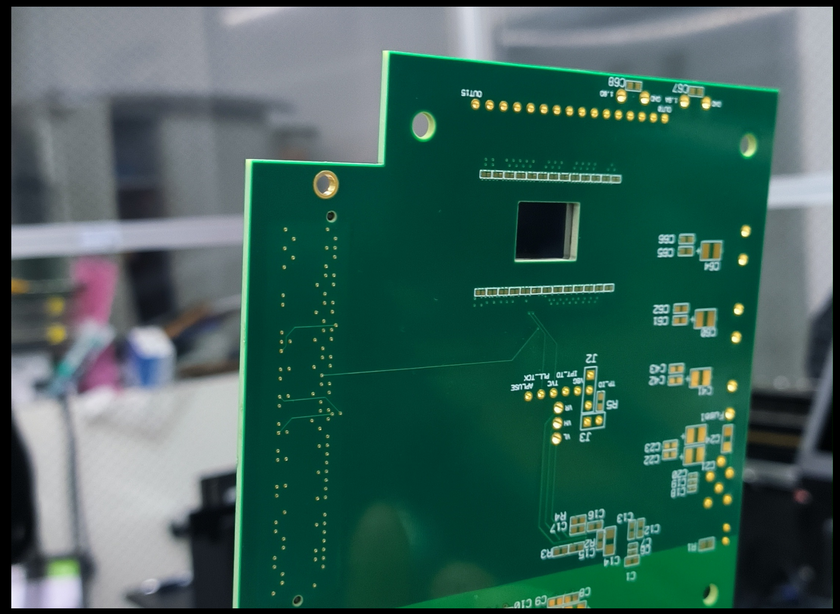
中国科学院高能物理研究所

Institute of High Energy Physics
Chinese Academy of Sciences

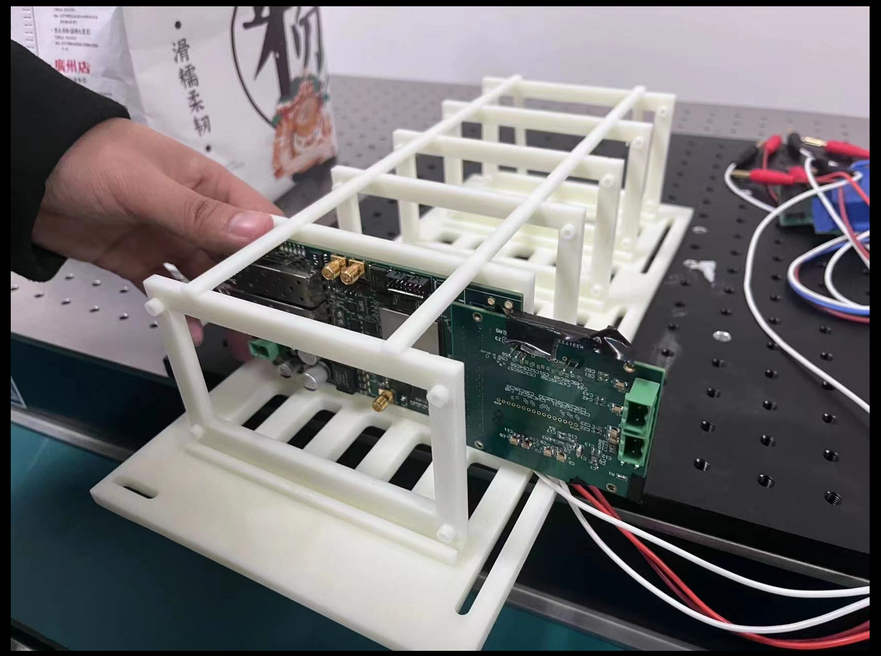
南京大学

Next milestone

- Testbeam at DESY (Dec 8th ~ Dec 22nd)
  - Telescope with 6 single chip boards (v1.21)
    - Planning to take 12 boards (for replacements)
  - Departing at evening of next Thursday (Dec. 8th)
  - Ladders readiness ?



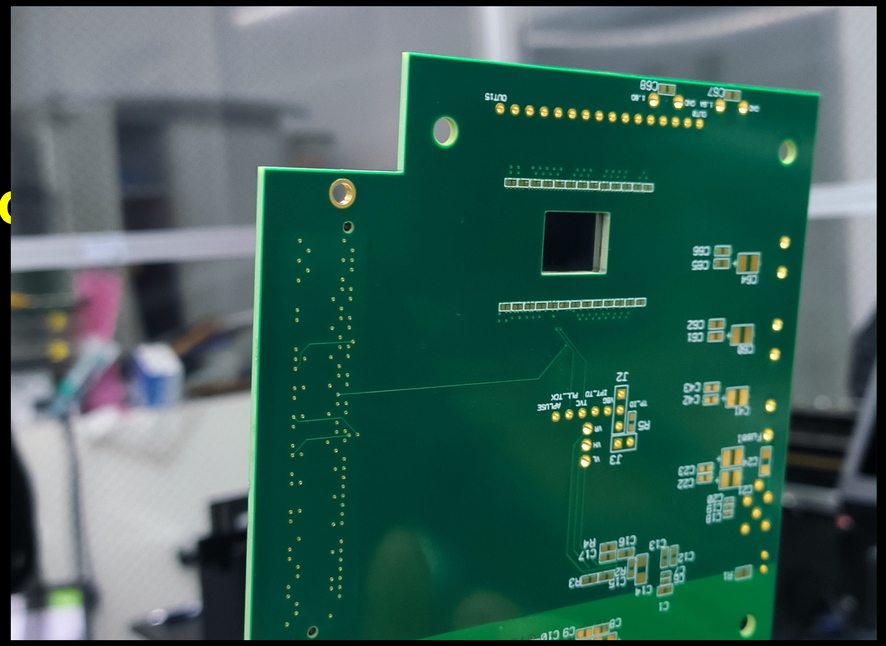
- Full vertex detector prototype
  - Aim for detector assembly at Feb 2023
  - Schedule another testbeam at BSRF
    - Depending on the status of ladder readout



Single chip board testing

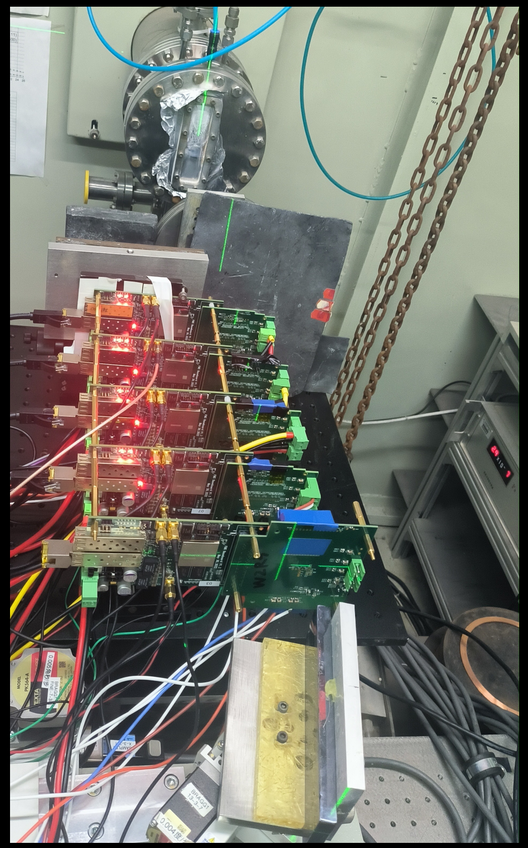
- 3rd version of single chip board (v1.21)
  - 1st batch: 5 boards tested (Standard process Taichu3), All functional
    - Aiming to take all 5 boards from 1st batch
  - 2nd batch : 10 board (6 std process, 4 modified process)
    - Aiming to take 5-7 boards from 2nd batch

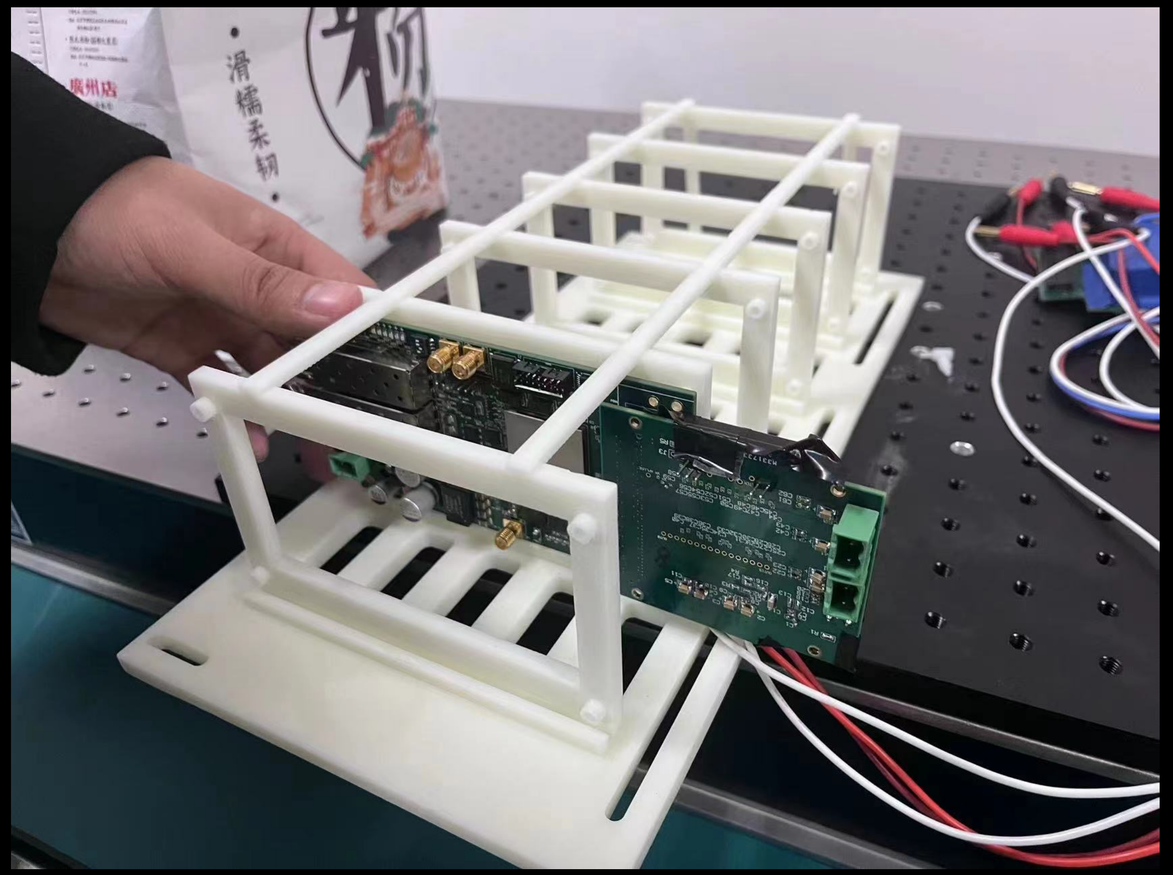
3rd version of single chip bo
V1.21



Mechanics

- Framework for telescope at DESY has been developed
  - To be tested next Monday
- Cooling fans for cooling channels for the boards (if needed)

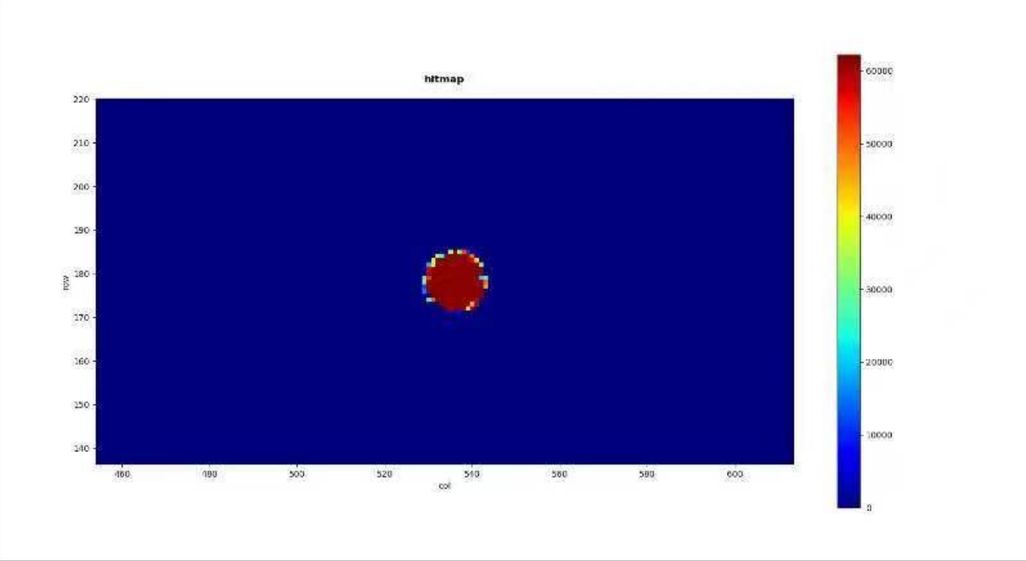




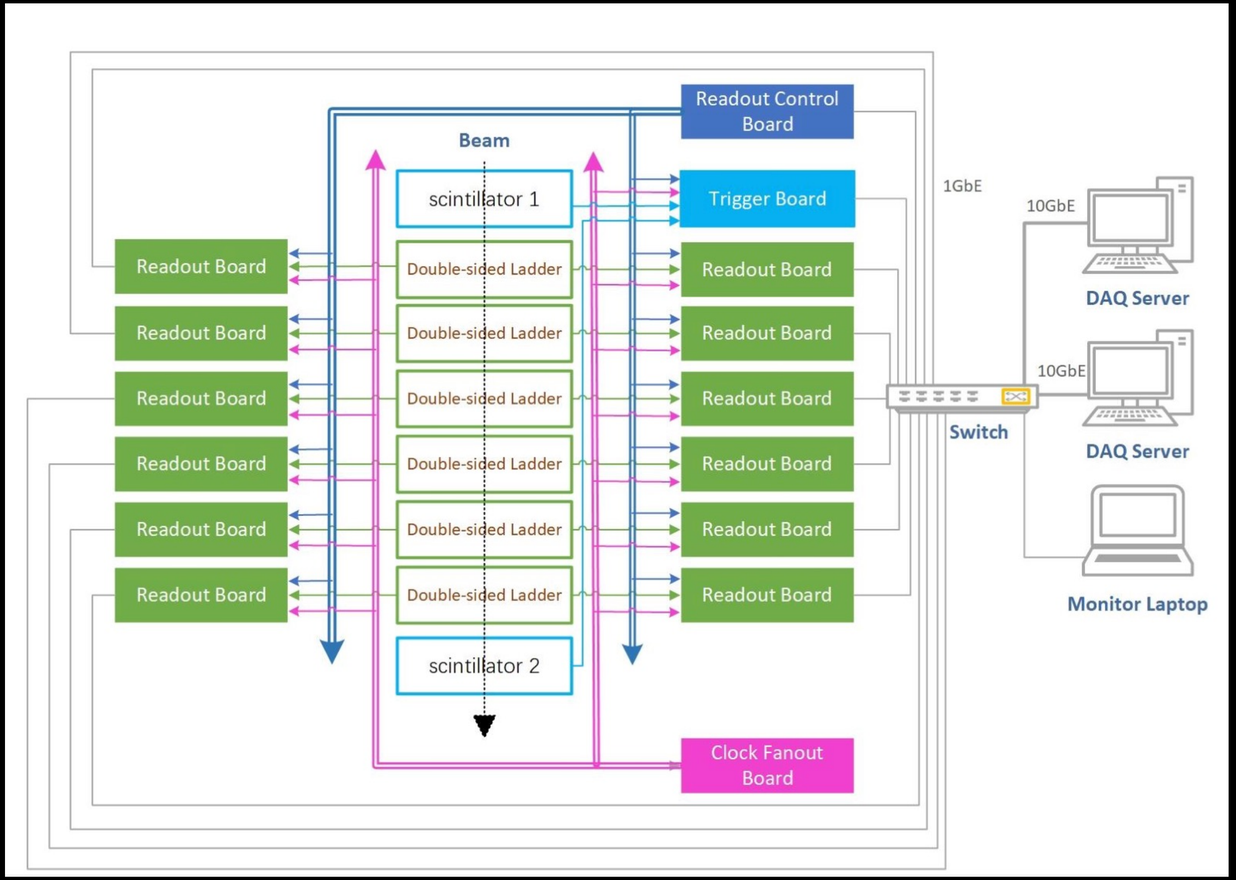
DAQ and firmware

- Firmware :
  - Need a stable version, validated by BSRF testbeam or beta test

- DAQ



DAQ

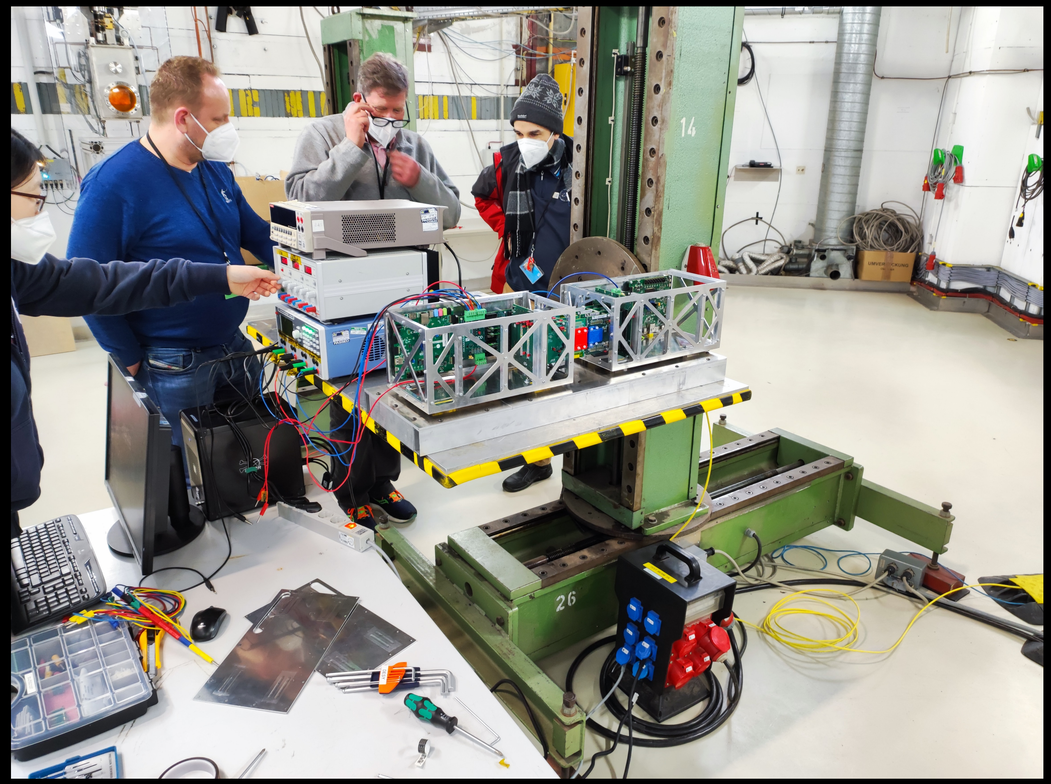


Shifters training

- Two kind of shifts training early next week
  - Detector operation (Tianya Wu, Jia Zhou):
    - How to operate the detector
    - What to record during the run
    - Online monitoring
  - Offline data quality (Shuqi Li): more shifters are needed
    - Full chain of data reconstruction
    - Document of what to check (time stamps , events, coincidence …)

material for test beam

5 DC power supples (purchased from Amazon.de , will ship to DESY next Monday)
16 channels customized power supply
10-12 PCB with TaichuPix3
12 FPGA boards（3 controllers，6 for daq，4 for backup）
1 Ethernet Switch and 3 DAQ PC
Connecting cables（50）、Network cables（12）、SMA cables（50）
Eletricity Sockets（10）
1 firmware PC and 1 offine PC
5TB HDD（10）: 50T
Hex wrench(M2-M5), Screwdriver(M1-M5);
Screws, Nuts and Gaskets(M2-M5);Pilers;
Copper column(M2-M3)



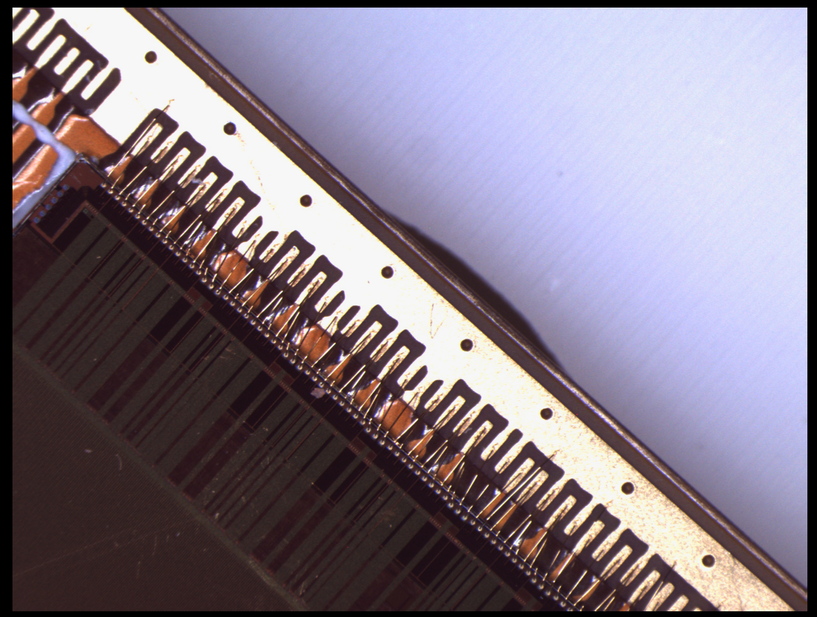
Plan for test beam

Flex and interface board

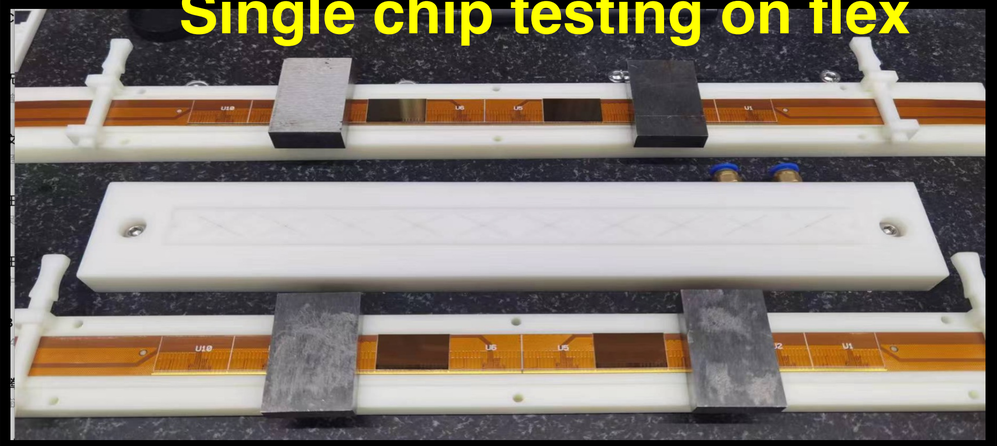
- 2nd version of the flex received. (2 metal layer version)
  - 12 flex available now， 4 metal layer flex will be available in one week ?
  - Single chip testing on flex (on-going)
    - 10 chips on flex available for testing
    - Data communication in OCT mode , still has some problem in normal mode
  - Hard PCB with test points
    - Just received this week (in middle of wire-bonding)

Hard PCB with test points

Wirebonding



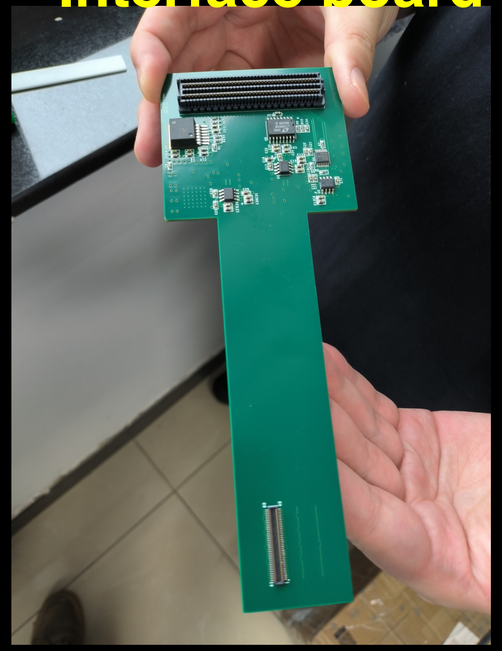
Single chip testing on flex



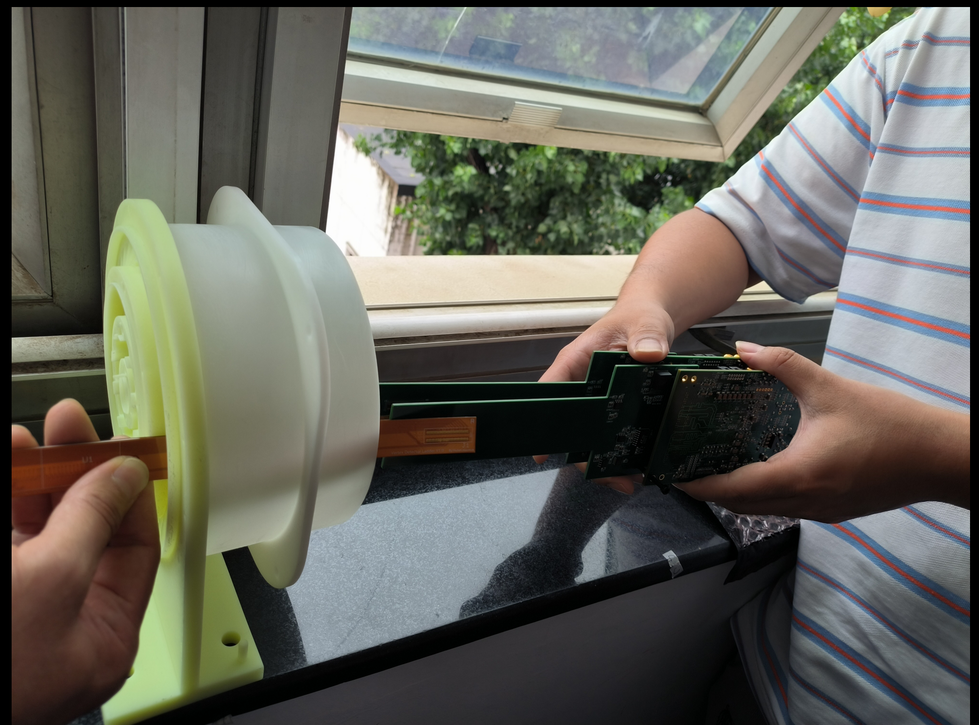
interface board

- Interface board was planned to have soft+hard PCB design
  - Interface board is to connected the flex and FPGA board
- 2nd version of interface board received
  - To fix the pins issue for connection with flex
  - Move the connector to the middle

Interface board



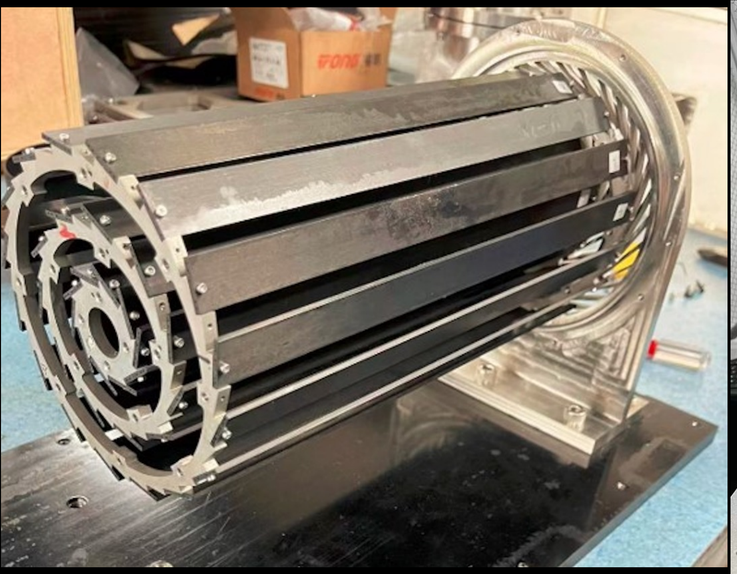
Interface board+FPGA +flex

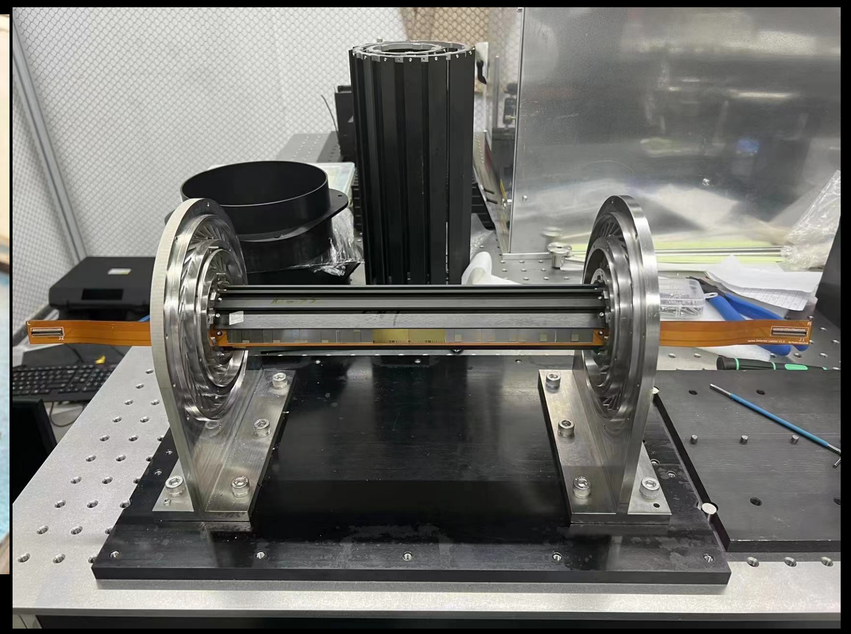


Vertex detector prototype assembly procedure

- Prototype support ready
- Mounting a dummy ladder with glass (done)
- Mounting dummy chip ladder with wire bond (Early Nov)
- Mounting real ladders (End of Nov)

Prototype support with aluminum machining





backup

Plan for test beam

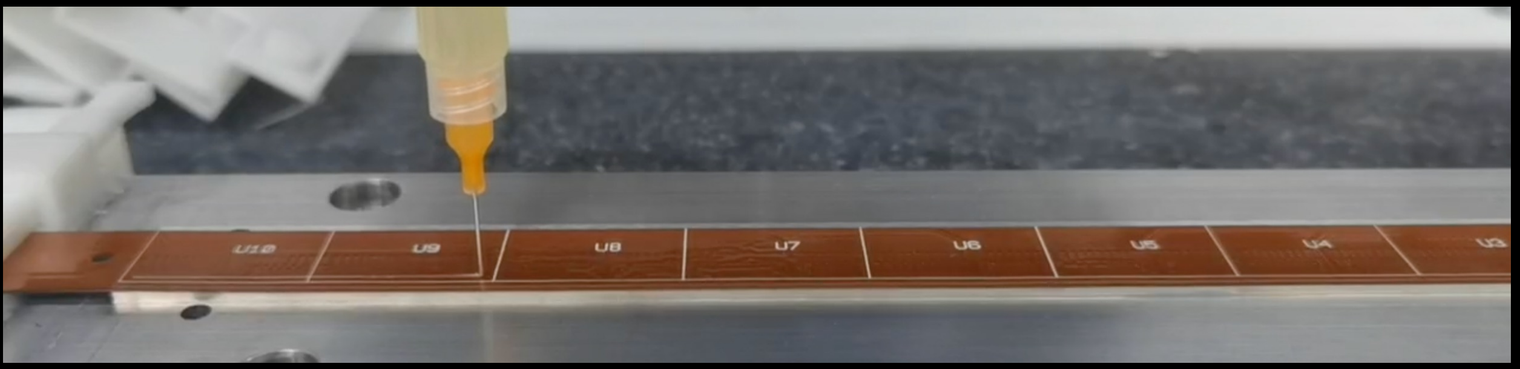
- Person power, expertise
  - Ming Qi (NJU, overall)
  - Joao (IHEP, overall)
  - Zhijun Liang (IHEP, overall)
  - Tianya Wu(IHEP, ASIC)
  - Xiaomin Wei(NWPU, ASIC)
  - Jia Zhou (IHEP ,DAQ)
  - Ziyue Yan (IHEP ,firmware)
  - Xinhui Huang (IHEP, mechanism)
  - Shuqi Li (IHEP, offline)

- Requesting Invitation letters (almost ready)
- Application Passports

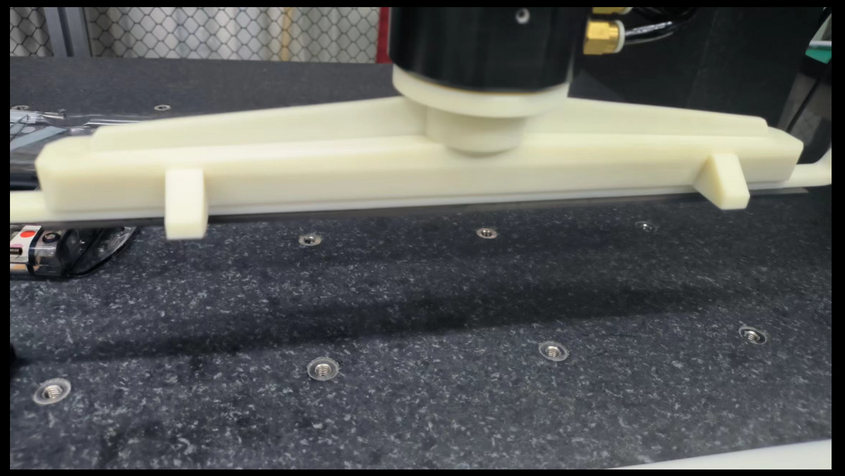
Detector module(ladder) assembly

- Progress in assembly in ladder
- Dummy
  - 2 flex with 10 glass dummy ASIC assembly
  - Automatic glue dispensing using gantry
- Real chip

Wire bonded one Taichu3 on flexible PCB
Jun and Ziyue are testing it with interface board



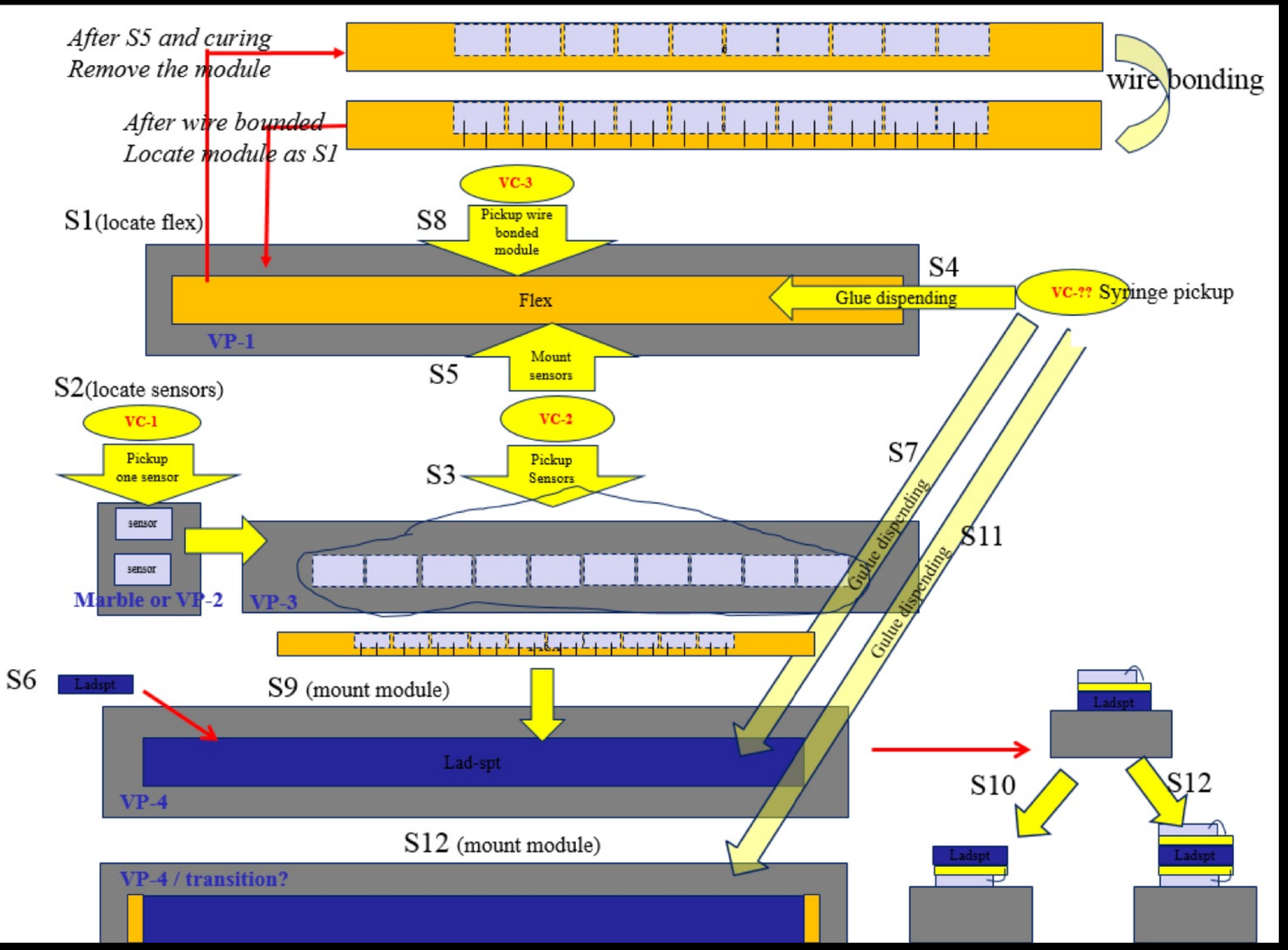
New pickup tools



Setting up wire bonding station
For full-size detector module(ladder)

Ladder assembly

- Ladder (double side)= 20 ASIC chips + two flexible PCB + carbon fiber support
- Ladder assembly procedure verified with dummy ASIC (glass)



Equipment for Test beam

- Instrumentations
  - 1. vertex detector prototype
  - 2. FPGA boards (15 boards including JTAG adapter)
  - 3. Test PC (2 personal computers. one for test one for backup)
    - 3 PC for DAQ, electronics , offline ?
    - 2T harddisk , 交换机switcher (24 channels, 8 channels …),
    - temp monitoring slow control (PC needed)
    - Power adaptors …, 4-5 DC power supply ?
  - 4. Several DC power supply (borrow it from DESY?): 12 channels DC power supply
  - 5. Several network cables and other cables.
  - 6. Borrow one oscilloscope for debug