中国科学院高能物理研究所
Institute of High Energy Physics
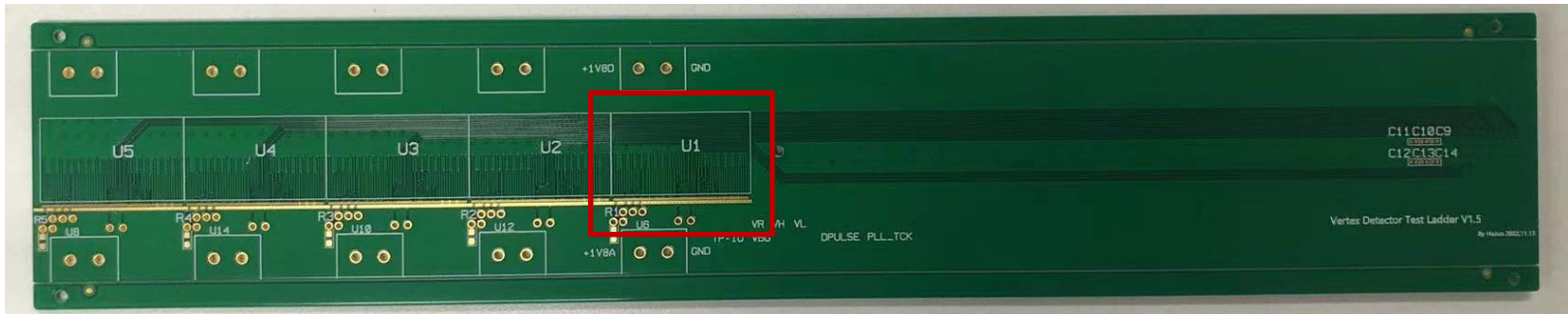*Chinese Academy of Sciences*

TaichuPix-3 test
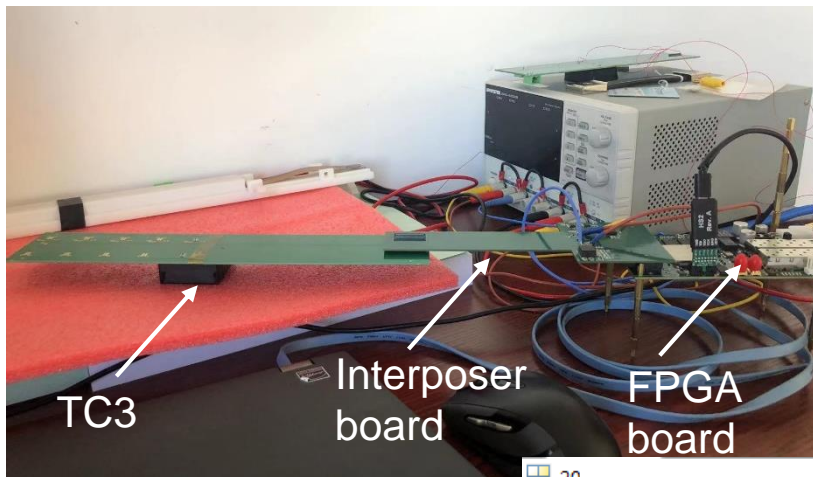
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Test ladder V1.5

- **Test ladder V1.5 produced to debug the flex**
  - ➢ Same design as flex V1.3 (2 layers), but is a 6-layer rigid PCB, with some test points and closer power supply socket

Test ladder V1.5

- **2 test ladder boards bonded with TC3**
  - ➢ Each one has a TC3 chip on position 'U1'
    - FlexV1.5-6D: VBG and bias voltage of pixel are normal, no output
    - FlexV1.5-6C: test results shown in the following

FlexV1.5-6C test results

- **Setup1**

- **OCT mode**

  - Supposed to output <0,323>, <128,323>, <256,323>, <511,323>, but some error code observed

  - Same phenomenon in flexV1.3

	Valid	ts	Col.	Row	Pattern	6	7	8
1	1	229	128	323	0	1	225	252
2	255	187	170	0	4	0	96	0
3	255	170	187	64	0	0	5	40
4	1	229	256	323	0	1	225	252
5	1	250	511	323	0	1	225	252
6	1	250	0	323	0	1	225	252
7	1	15	128	323	0	1	225	252
8	1	15	256	323	0	1	225	252
9	1	15	511	323	0	1	225	252
10	1	36	0	835	0	33	225	252
11	1	36	128	323	0	1	233	253
12	1	57	320	835	0	33	249	253
13	1	57	511	835	0	33	225	252
14	255	187	170	0	4	0	96	0
15	255	170	187	64	0	0	5	40
16	1	57	0	323	0	1	225	252
17	1	78	128	323	0	1	225	252
18	1	78	256	323	0	1	225	252

Apulse read test

- **With Setup1**
  - Unmask pixels <63, 0:69> , enable "apulse-in" for these pixels only
  - Mask all the other pixels
  - Output abnormal

	Valid	ts	Col.	Row	Pattern	6	7	8	9
1	0	214	276	511	0	1	196	27	97
2	0	192	240	1023	8	1	196	27	97
3	1	208	294	510	8	1	196	27	97
4	0	192	498	509	0	1	196	27	97
5	0	191	93	1020	8	1	196	27	97
6	1	130	140	511	8	1	196	27	97
7	0	178	137	1022	0	1	196	27	97
8	0	214	474	1021	0	1	196	27	97
9	1	126	94	1022	8	1	196	27	97
10	0	192	382	511	8	1	196	27	97
11	0	178	139	1020	0	1	196	27	97
12	1	129	484	511	8	1	197	27	97
13	1	192	284	1022	0	1	196	27	97
14	0	193	76	1022	0	1	196	27	97
15	0	130	335	1022	8	1	196	27	97
16	1	182	461	511	8	1	196	27	97
17	0	191	46	1022	0	1	196	27	97
18	0	193	244	1023	8	1	196	27	97
19	1	98	137	1023	8	1	196	27	97
20	0	193	192	511	0	1	196	27	97
21	0	193	61	1023	8	1	196	27	97
22	1	131	76	510	8	1	196	27	97

Apulse read test

- **With Setup2**
  - Same chip setting as in Setup1, connect DPULSE to 0V
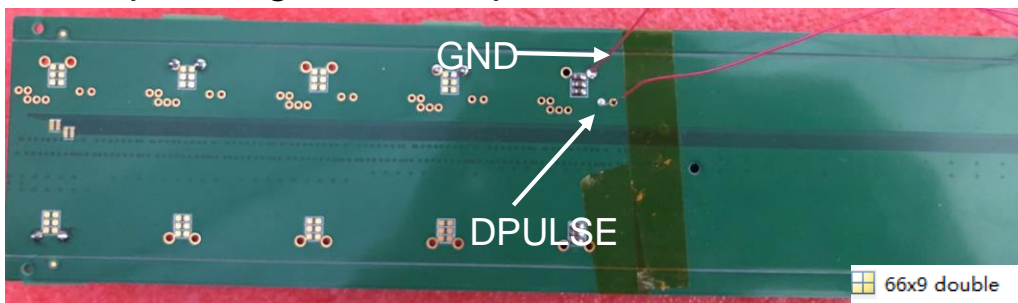
  - Output nearly normal
    - Read out most of pixels <63, 0:69>, a few lost
    - Several masked pixels were read out

- **Other different kinds of setup tried**
  - Closer power supply
  - Higher power voltage
  - Different chip settings,

  i.e. bias, mask/Calen configurations

66x9 double					
	1	2	3	4	5
1	1	151	63	815	0
2	1	151	63	787	0
3	1	134	63	554	0
4	1	151	63	518	0
5	1	134	62	97	0
6	1	134	63	69	0
7	1	134	63	68	0
8	1	134	63	67	0
9	1	134	63	66	0
10	1	134	63	64	0
11	1	134	63	63	0
12	1	134	63	62	0
13	1	135	63	61	0
14	1	135	63	60	0
15	1	134	63	59	0
16	1	134	63	58	0
17	1	134	63	57	0
18	1	134	63	56	0

Connect DPULSE to 0V is currently the only setup with which shows a normal response to 'apulse'

Summary

- **Whether chip has a normal response to 'apulse' indicated a strong relationship with status of DPULSE**
  - Plan to be confirmed with a single chip testboard