High spatial resolution pad and pixelated TPC technology R&D

Huirong Qi

Yue Chang, Liwen Yu, Xin She, Jian Zhang , Zhiyang Yuan, Hongliang Dai, Jinxian Zhang

Linghui Wu, Gang Li, Manqi Ruan and some good inputs from LCTPC

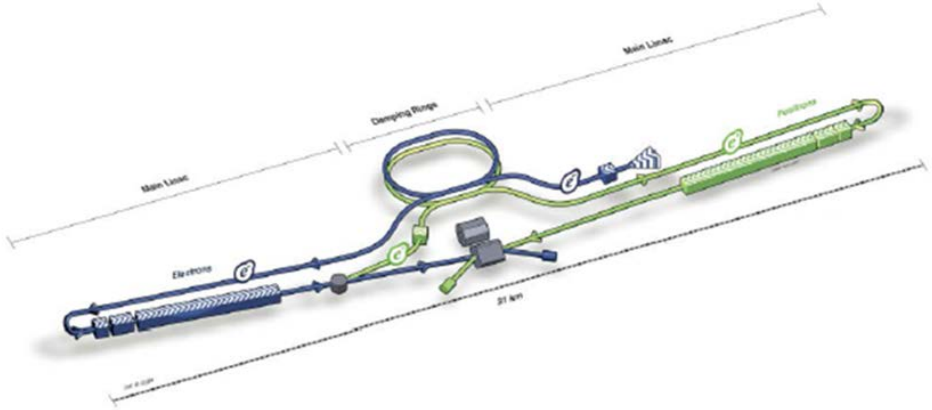
CEPC Day, 19 December, 2022

Content

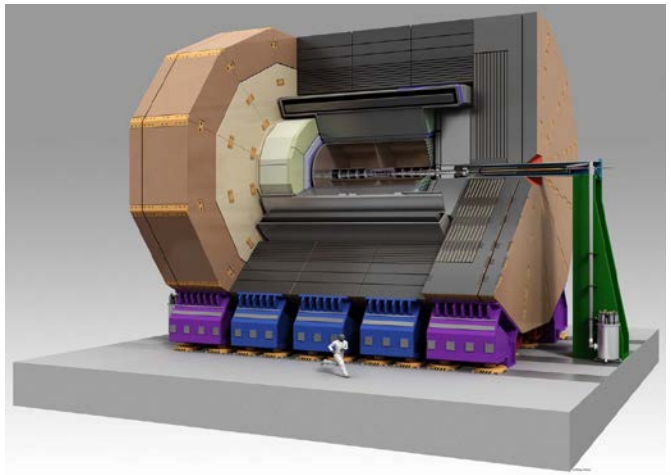
- **TPC detector for e+e- colliders**
- **High spatial resolution pad readout TPC**
- **Pixelated readout TPC R&D**
- **Summary**

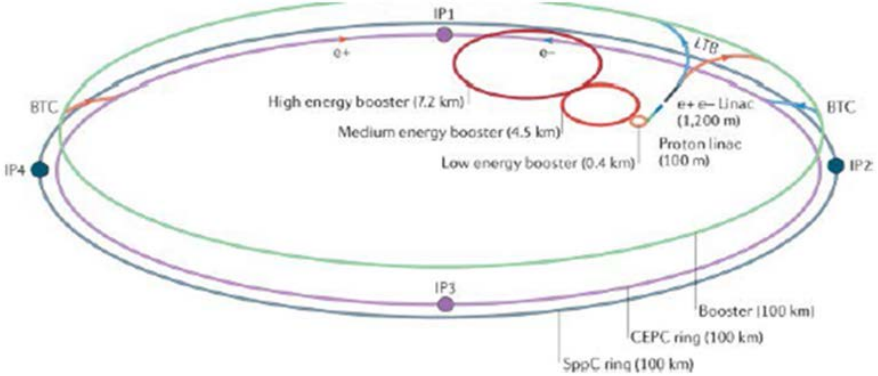
TPC technology for the future e+e- colliders

- A TPC is the main tracking detector for **some candidate experiments at future e+e- colliders**
  - ILD at ILC and the baseline detector concept of CEPC
- TPC technology can be of interest for other future e+e- colliders

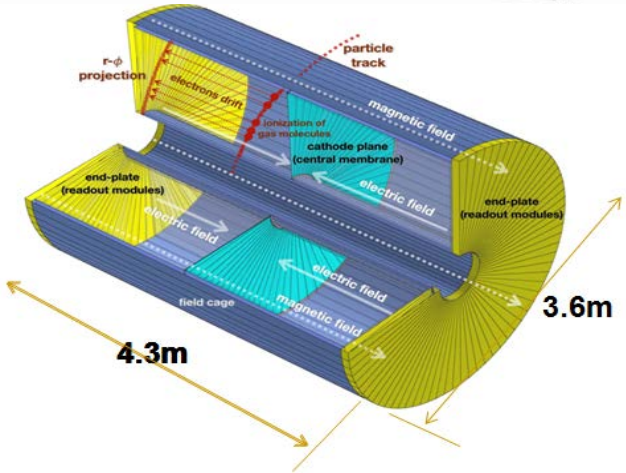


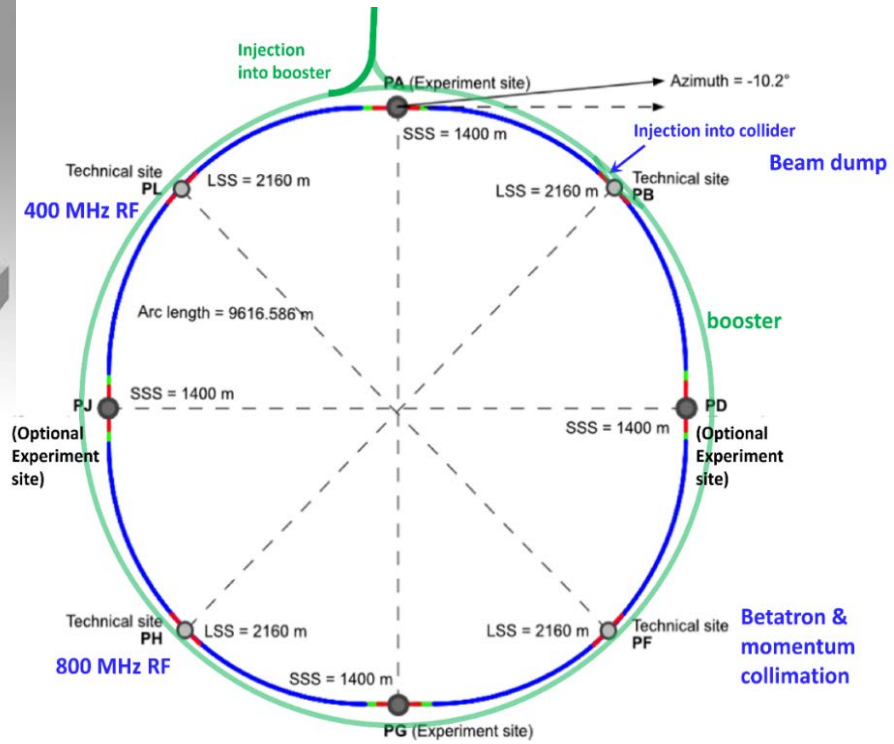
International Linear Collider (ILC)





Circular Electron Positron Collider (CEPC)



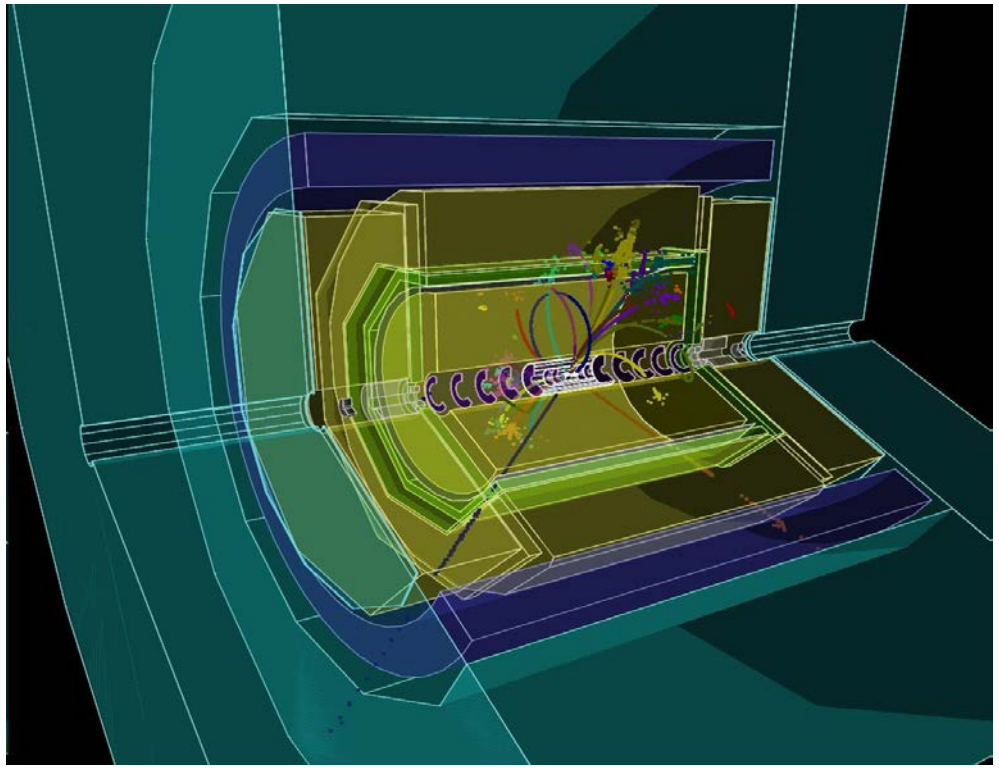


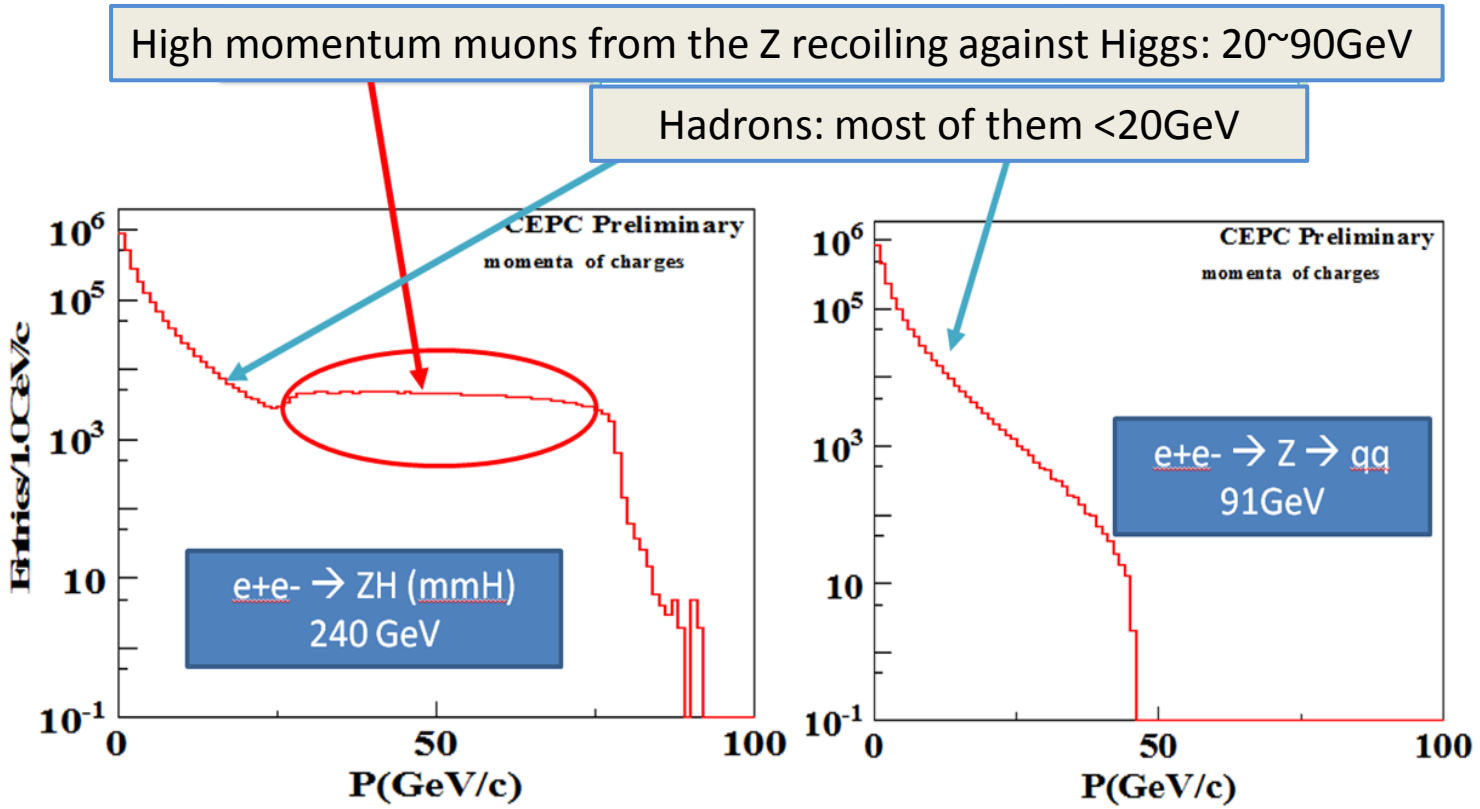
Future Circular Collider (FCC-ee)

https://arxiv.org/abs/2203.06520

TPC requiremetns from e+e- Higgs/EW/Top factories

- TPC can provide hundreds of hits (for track finding) with high spatial resolution compatible with PFA design (**very low material** in chamber)
  - $\sigma_{1/pt}$ ~10^{-4} $(GeV/c)^{-1}$ with TPC alone and σ_{point}<100μm in rϕ
- **Provide dE/dx and dN/dx with a resolution** <4%
  - Essential for Flavor physics @ Z run
  - Beneficial for jet at higher energy





Pad and pixelated readout TPC technology

- TPC as the main tracker detector to satisfy the physics requirements :
  - For Higgs, W and top running, **no problem** for all TPC readout technologies.
- For high luminosity **(2 ×10^{36})** Z running
  - Pixelated readout TPC is a good option at **high luminosity** on the circular e+e- collider
  - Pixelated readout TPC is a realistic option to provide
    - High spatial resolution **under 2T or 3T magnetic field**
    - Better momentum resolution
    - High-rate operation (MHz/cm^2)
    - dE/dx and Cluster counting (**in space**)
    - Excellent two tracks separation

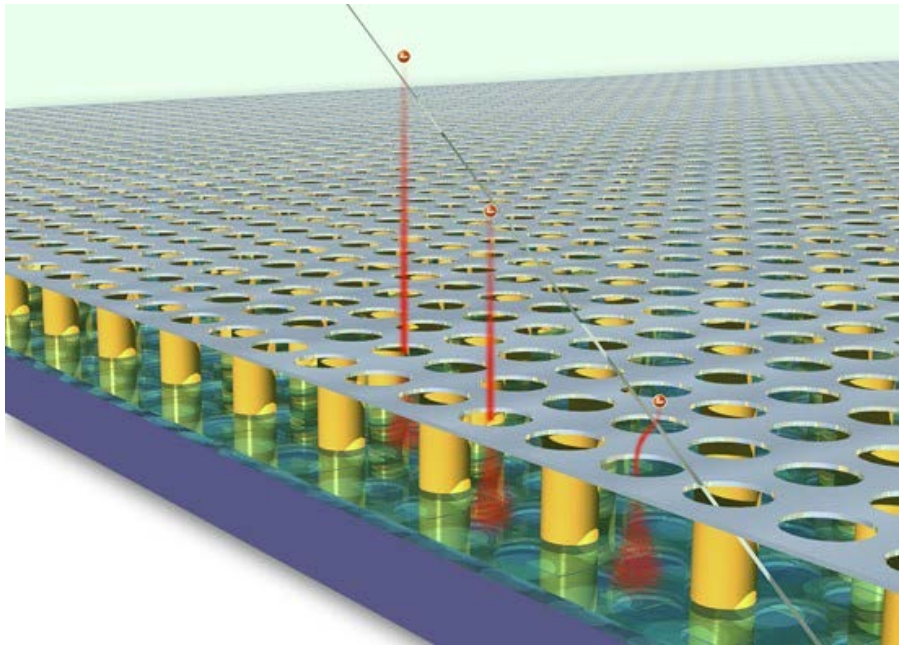
Standard charge collection:

Pads (1 mm × 6 mm)/ long strips

Pixelated readout:

Bump bond pads are used as charge collection pads.

55μm × 55 μm or larger



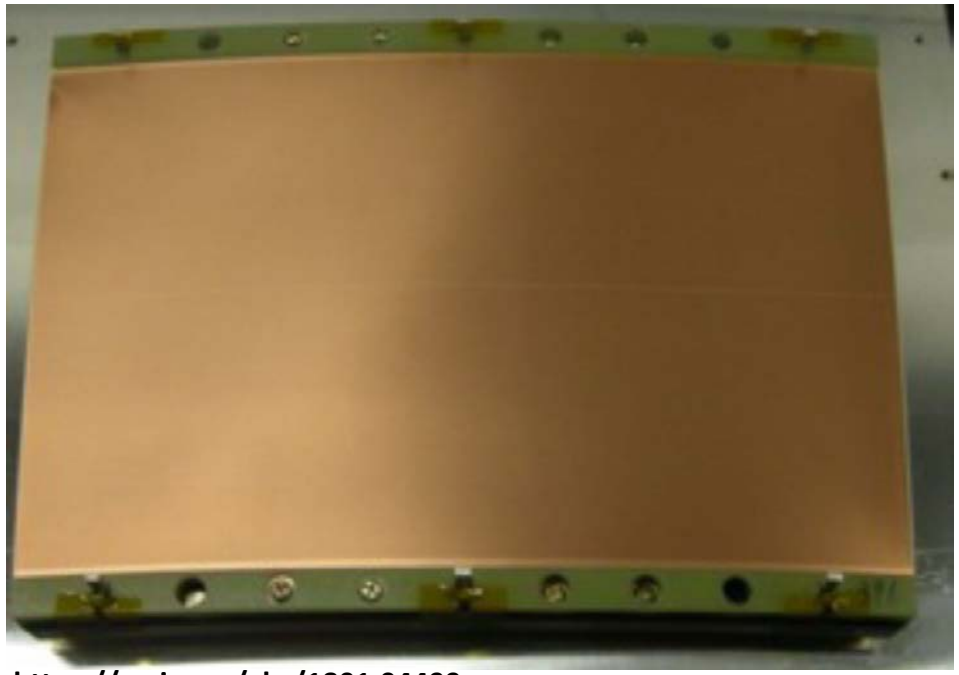
- High spatial resolution pad TPC technology

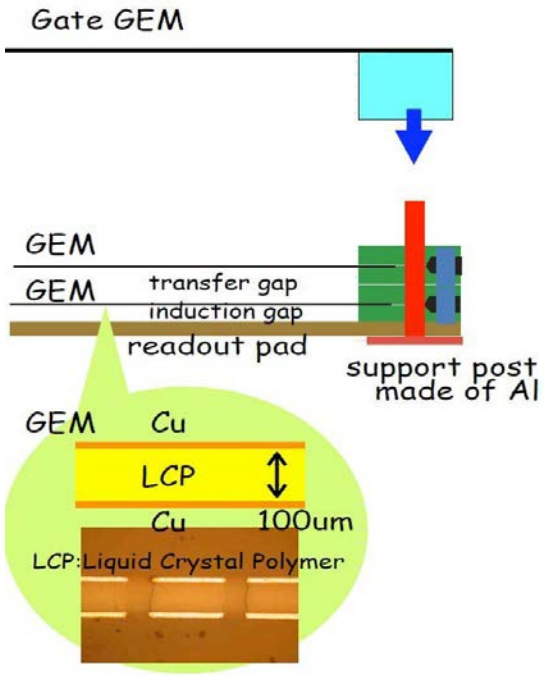
Pad TPC technology - double GEMs

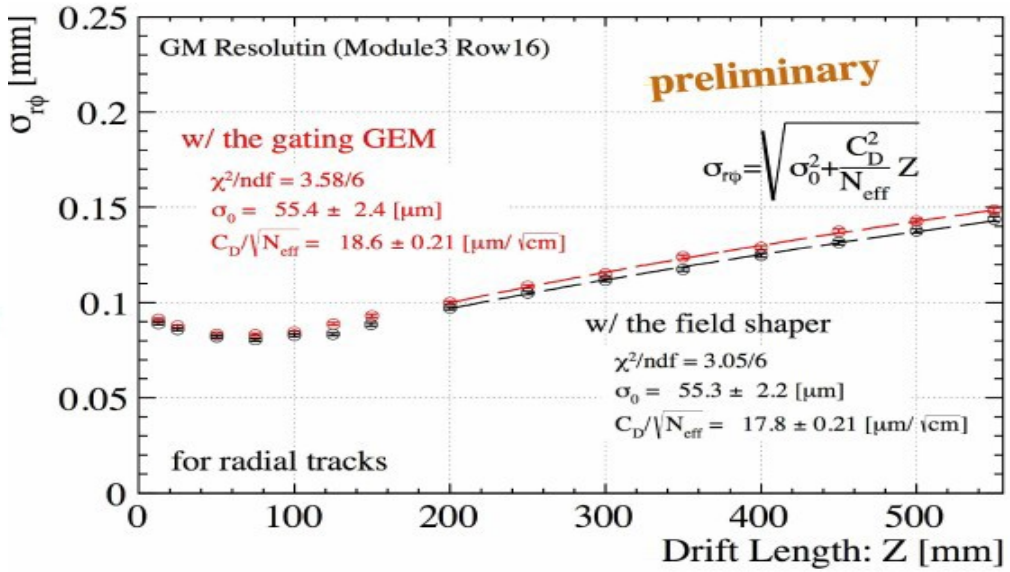
- GEMs: copper-insulator- copper sandwich with holes
- Double GEMs module are being tested:
  - GEMs with 100μm LCP insulator
  - Standard GEM from CERN
- Design idea of the GEM Module:
  - **No frame** at modules both sides
  - Spatial resolution of $\sigma_{r\phi} \leq 100$ μm, more stability by the broader arcs at top and bottom

GEM Module 1:

- 2 GEMs made of 100 μm thick LCP
- 1.2×5.4mm^2 pads



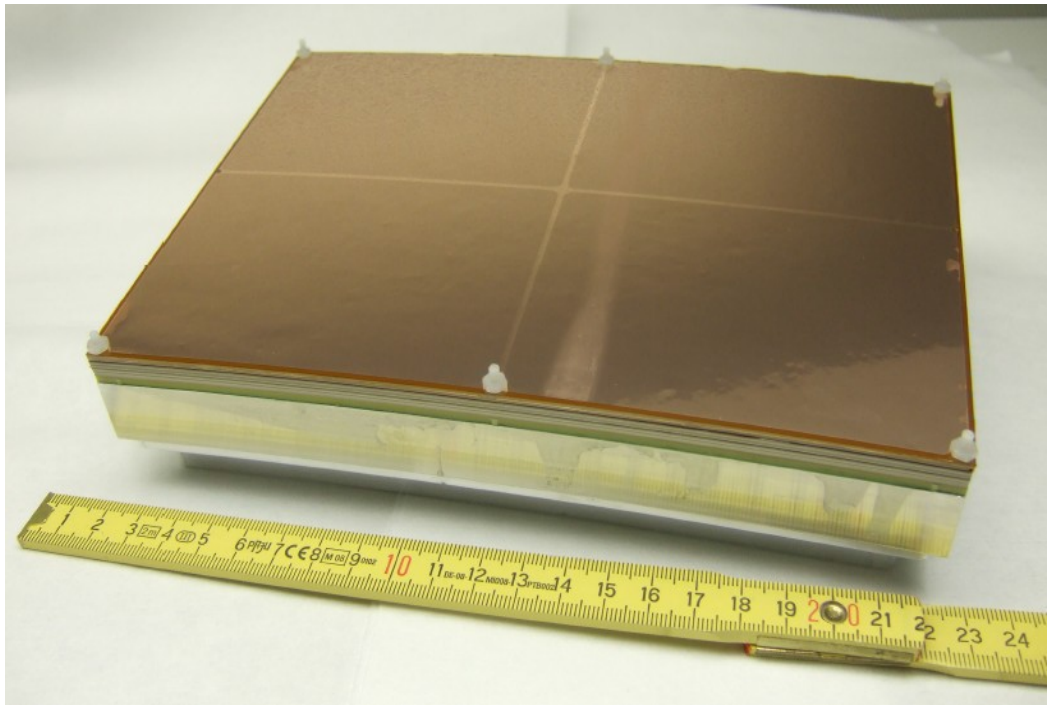




https://arxiv.org/abs/1801.04499

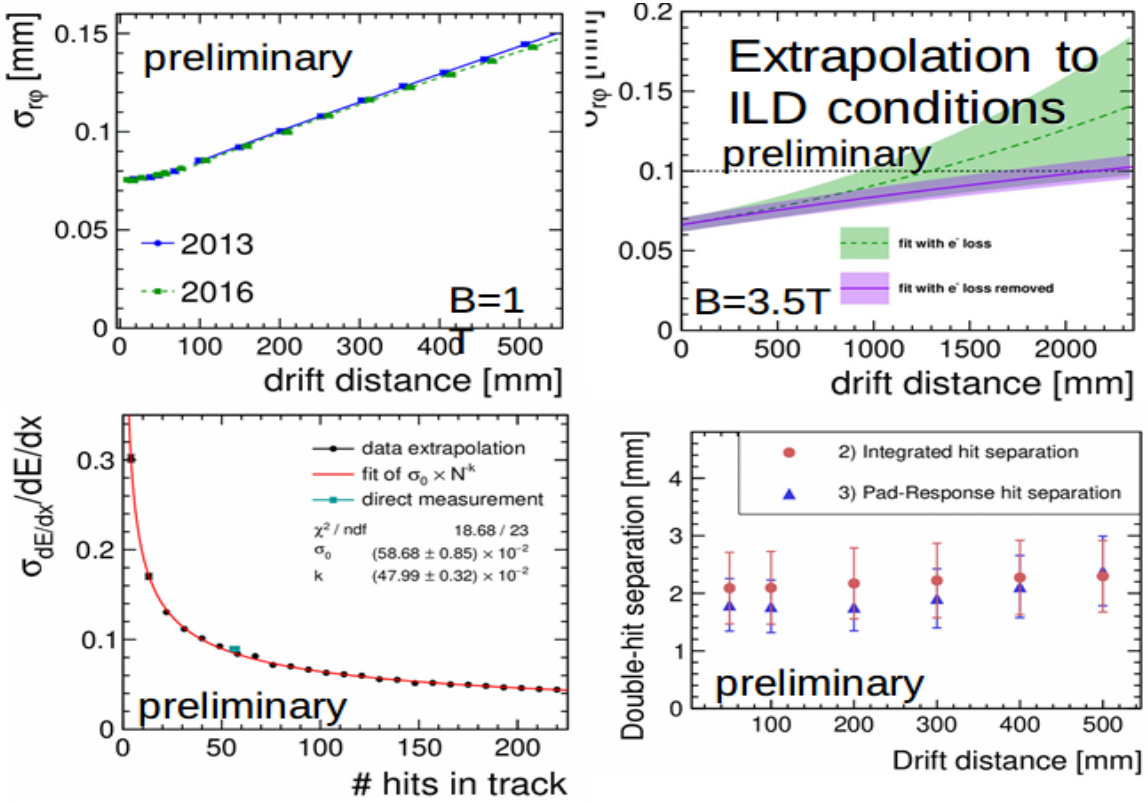
Pad TPC technology - triple GEMs

- Design idea of GEM Module 2:
  - Minimize dead area
  - **Without frame** to stretch GEMs, but a 1 mm grid to hold GEM
- Spatial resolution of $\sigma_{r\phi} \leq 100$ μm, **and double track resolution and dE/dx calculated** in dependence on the pad sizes



GEM Module 2:

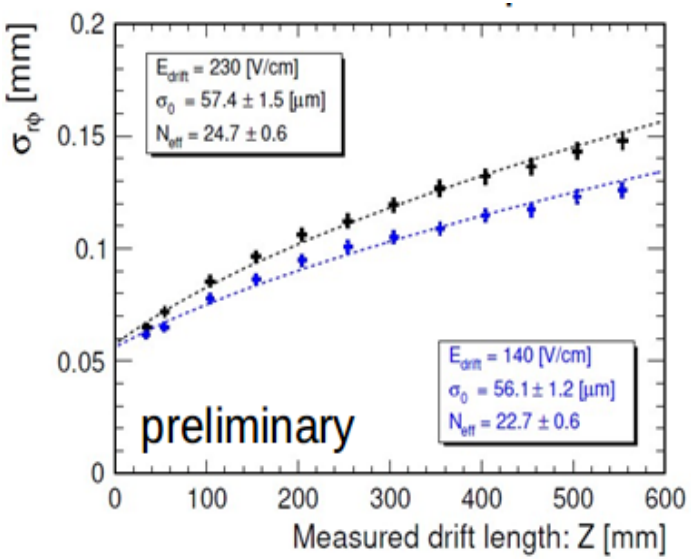
- 1.26 × 5.85mm2 pads – staggered
- Field shaping wire on side of module to compensate the field distortions

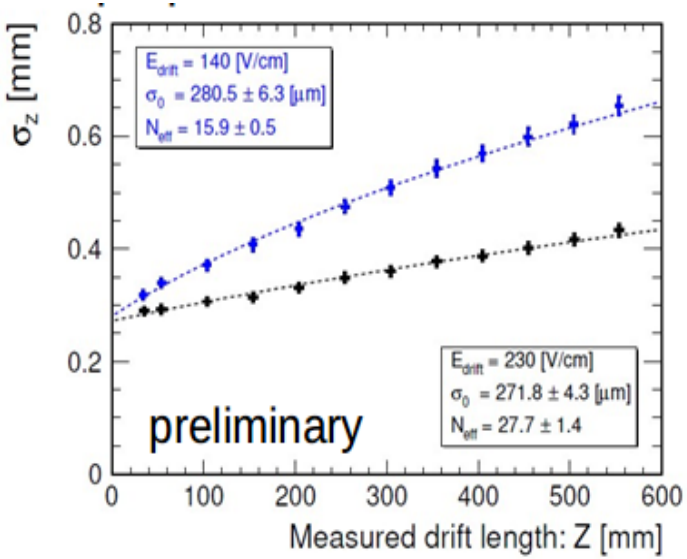


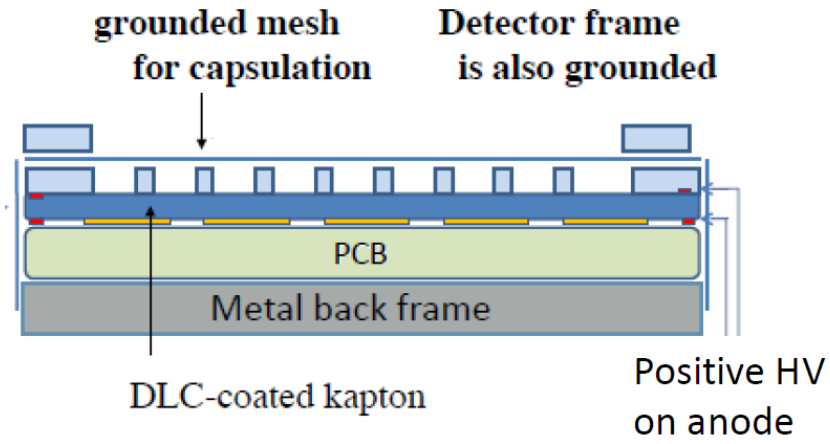
https://arxiv.org/abs/2203.03435

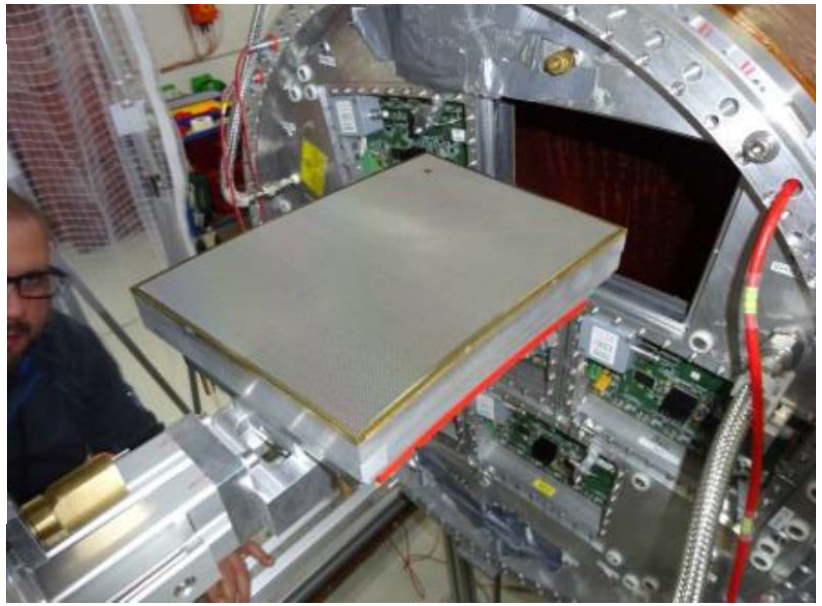
Pad TPC technology - Resistive Micromegas

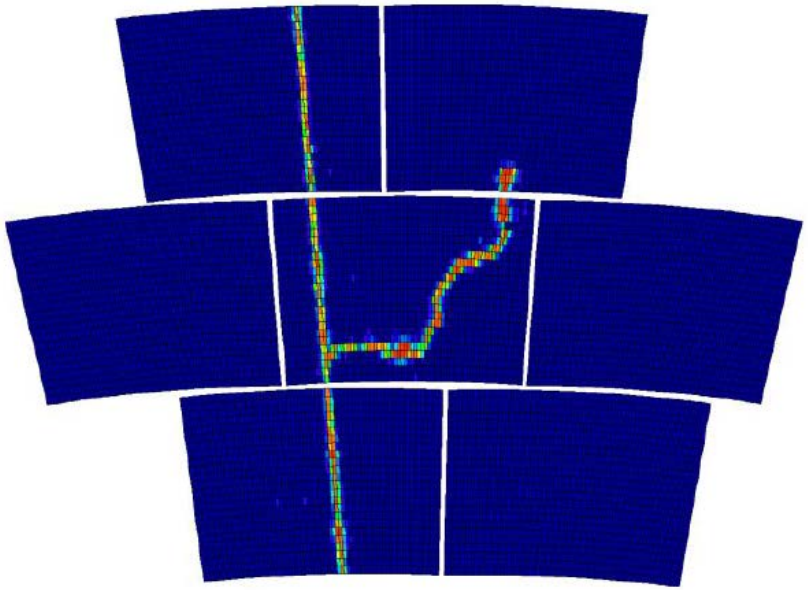
- Resistive Micromegas:
  - Bulk-Micromegas with 128 µm gap size between mesh and resistive layer (**developed in LCTPC**)
- A new HV scheme of the module (ERAM) places grid on ground potential
  - Reduces **field distortions** between modules by a factor of 10







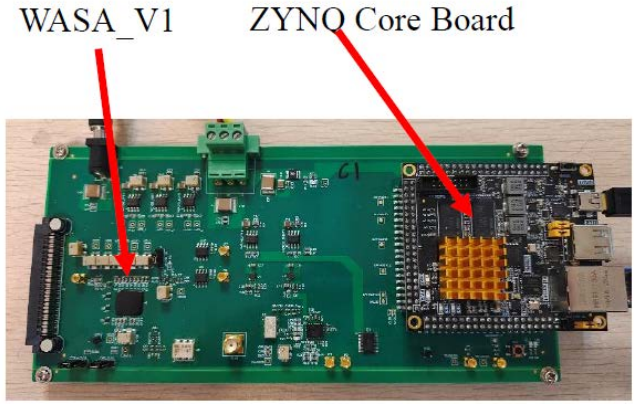


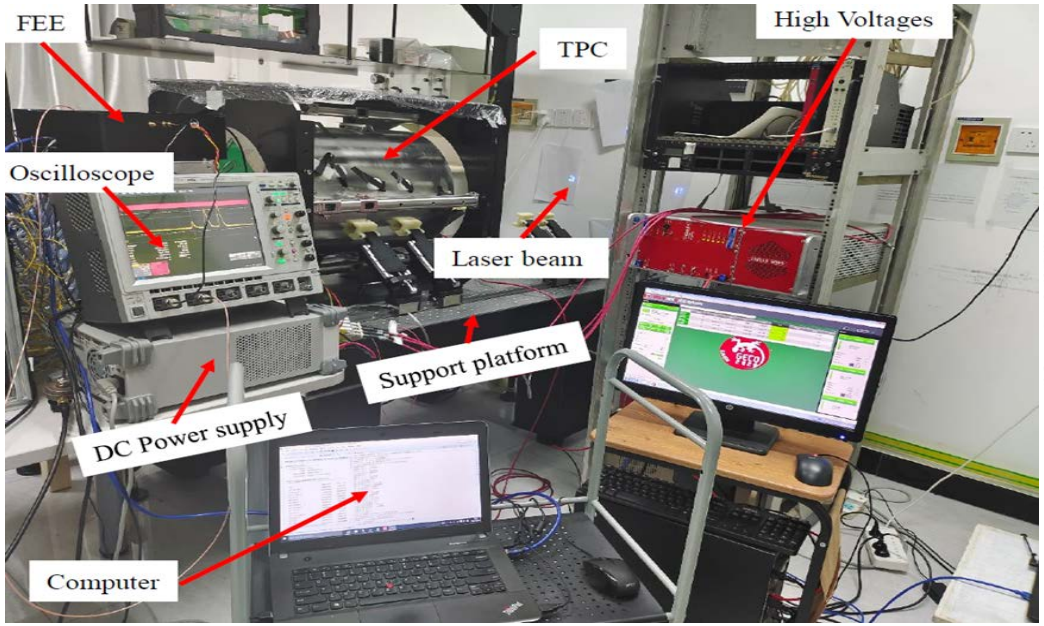


https://doi.org/10.1016/j.nima.2019.162798

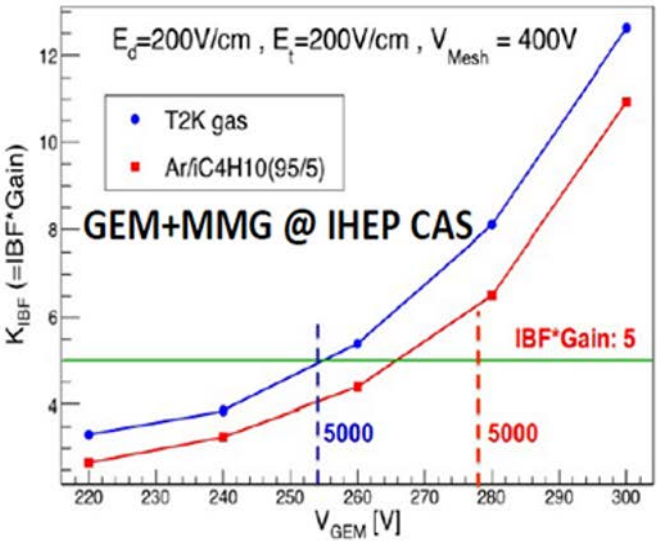
CEPC TPC detector prototyping roadmap

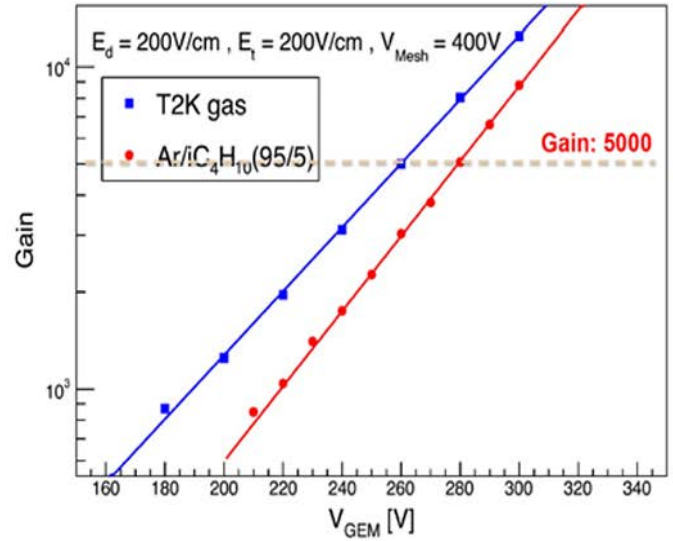
- From TPC module to TPC prototype R&D for beam test
  - Low power consumption FEE ASIC (**reach <5mW/ch** including ADC)
- Achievement by far:
  - Supression ions hybrid GEM+Micromegas module
    - IBF×Gain **~1 at Gain=2000** validation with GEM/MM readout
  - Spatial resolution of **$\sigma_{r\varphi}$≤100 μm** by TPC prototype
  - dE/dx for PID: <4% (as expected for CEPC baseline detector concept)





Low power consumption readout

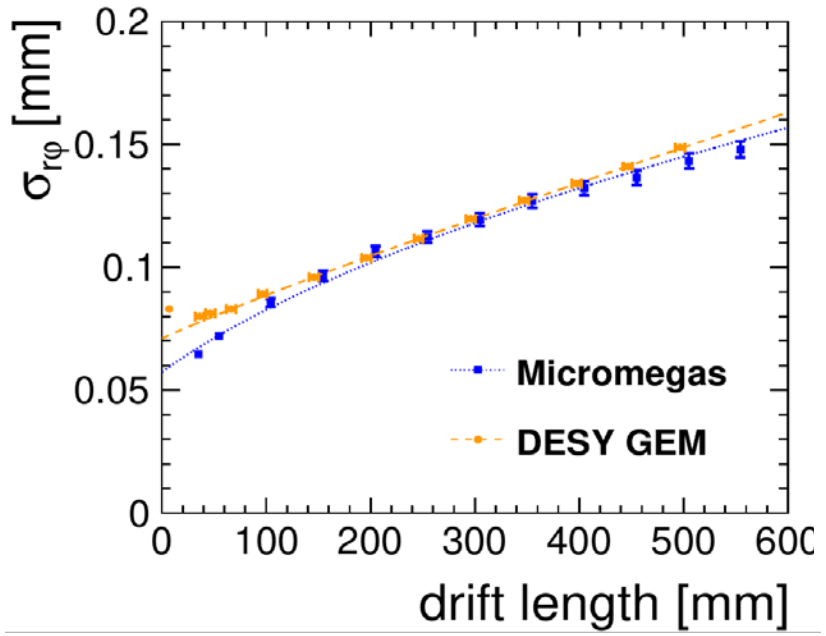


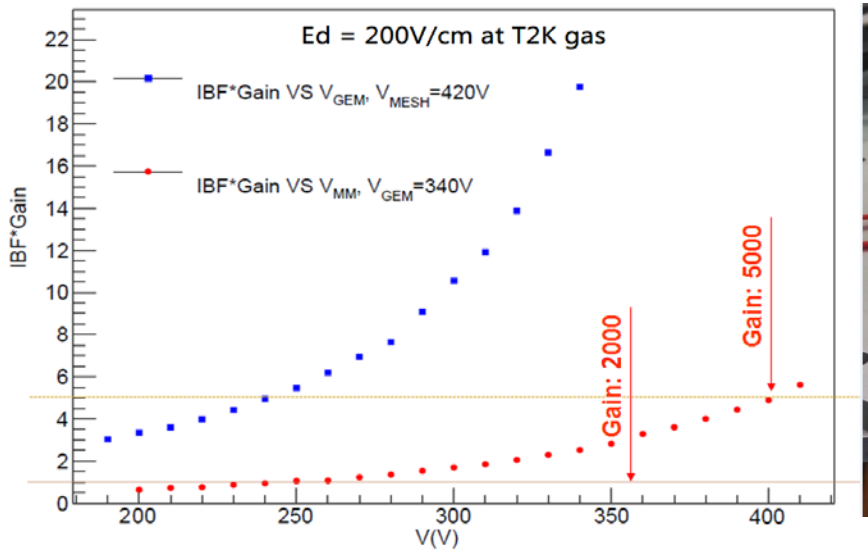


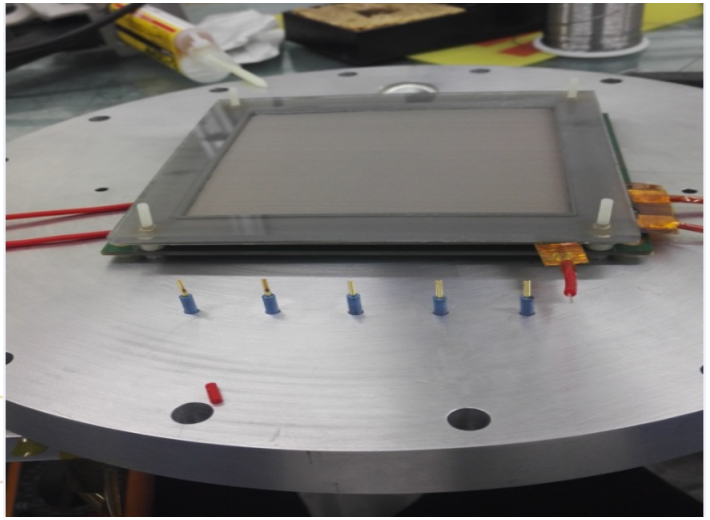
GEM+Micromegas module R&D

Pad TPC technology – GEM+Micromegas

- **GEM and Micromegas** groups have finished analysis of test beam data with previous set of detector modules. Both technologies show **very similar performance**.
- LCTPC want to implement improvements in a **new generation of modules** => **common modules**
  - Common readout electronics (sALTRO)
  - Only the gas amplification stage differs
- Combined Micromegas + GEM readout has been developed, which promises a **lower ion backflow** (IBF) at CEPC TPC group without gating.
  - IBF×Gain ~ 1 at total gain of 2000

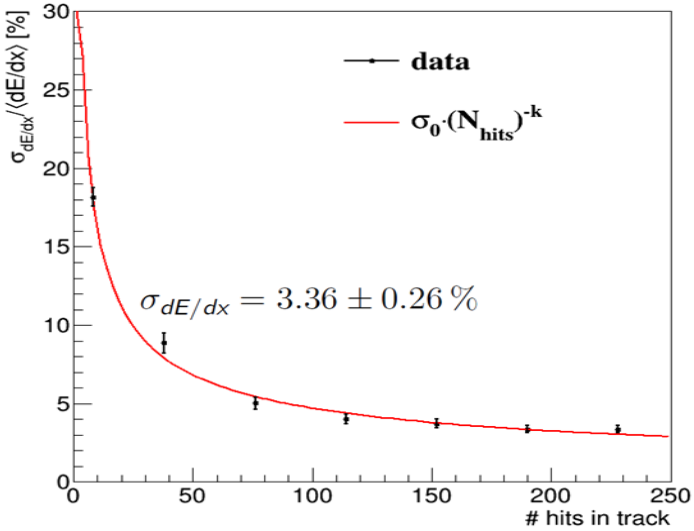


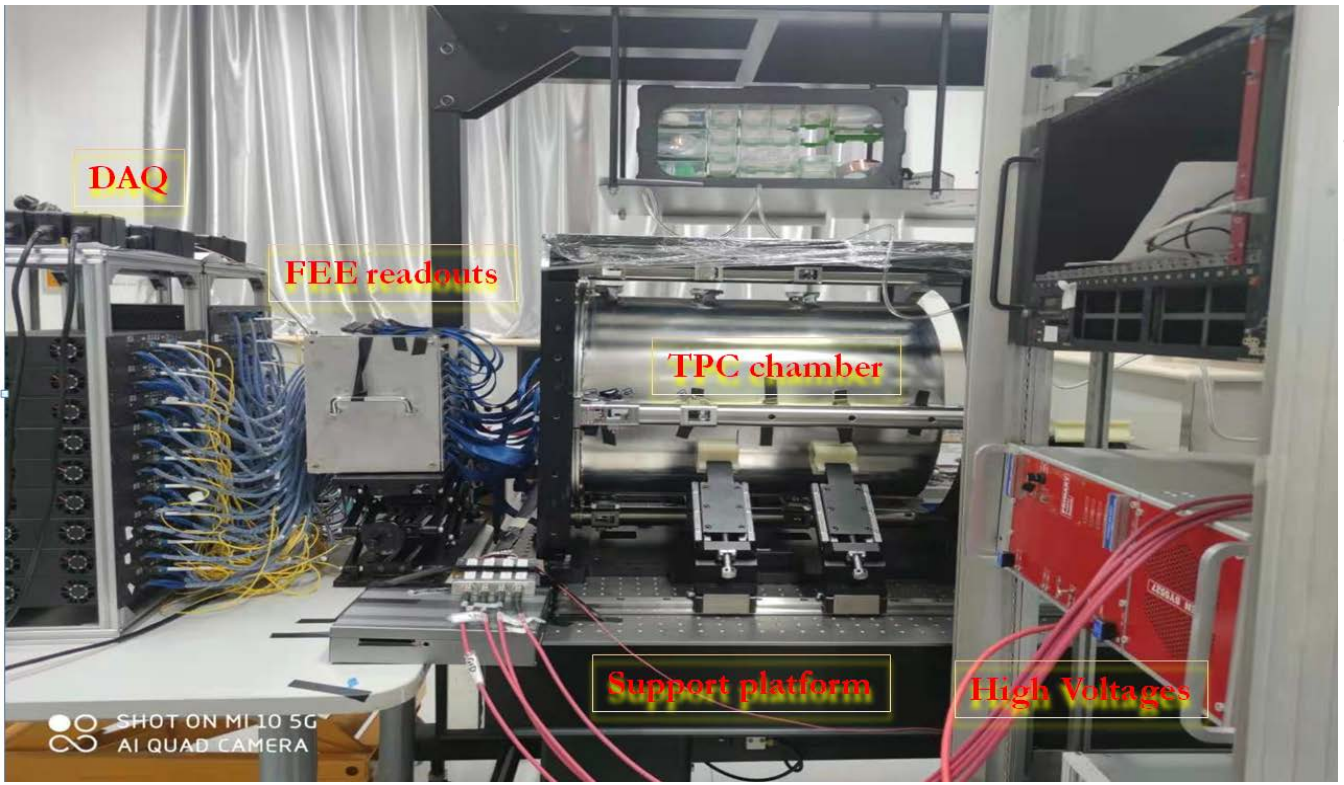


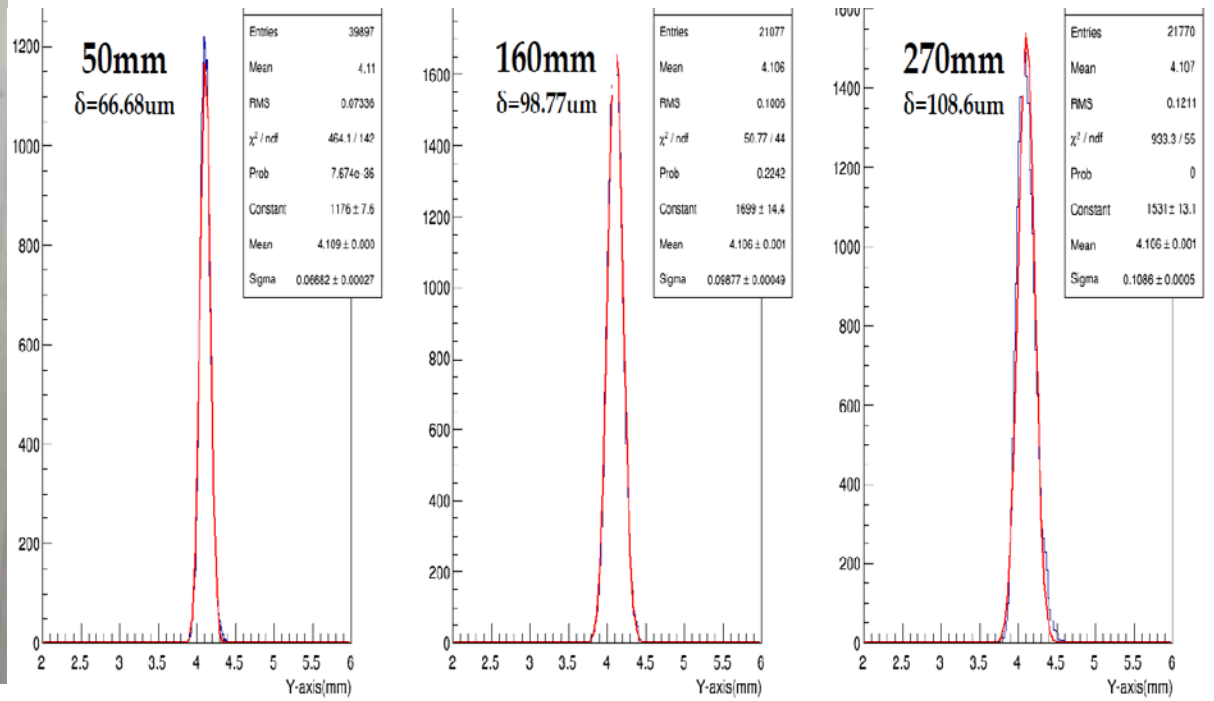


TPC prototype with 266nm UV laser tracks

- The TPC prototype integrated 266nm UV laser tracks has successfully developed.
- Analysis of UV laser signal, the spatial resolution, dE/dx resolution
  - Spatial resolution can be less than **100 μm along the drift length** of TPC prototype
  - Pseudo-tracks with 220 layers (**same as the actual size of CEPC baseline detector concept**) and dE/dx is about 3.4 ± 0.3%







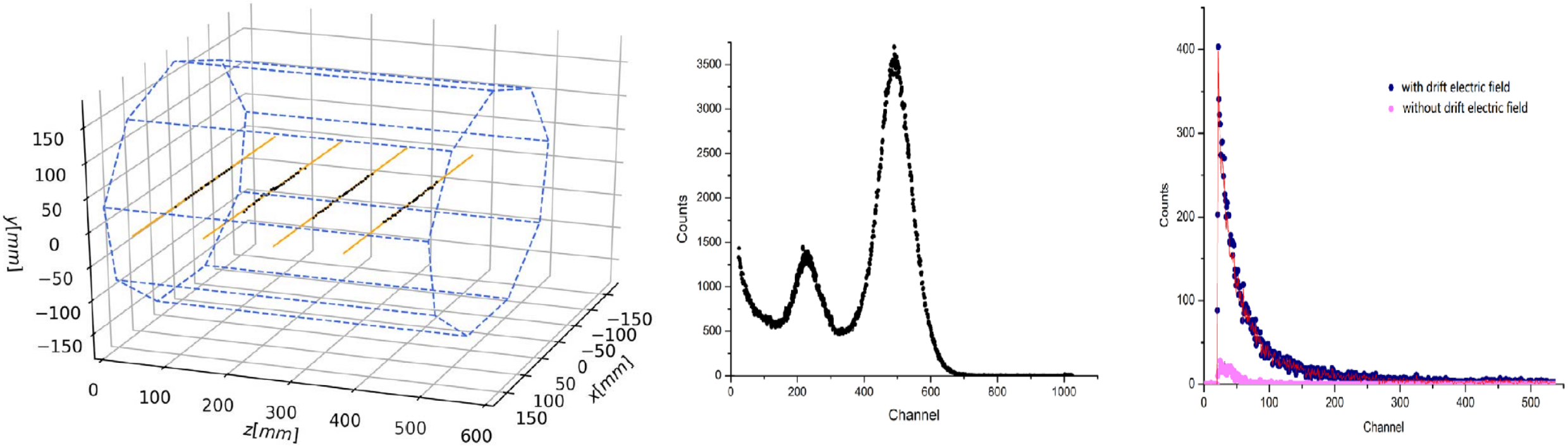
https://doi.org/10.1016/j.nima.2022.167241

Reconstruction event and energy spectrum of ^{55}Fe/Cosmic ray

- TPC detector prototype can study the UV laser track, 55Fe radiation source and the cosmic ray.
- TPC prototype was checked after one year development
  - ^{55}Fe X-ray spectrum profile is very good
  - **Detector gain just shift 2% than one year before.**
- The Landau distribution of the cosmic ray's energy spectrum was successfully obtained.

Summary of the event selection cuts.

Laser energy monitor	Variation range	$E_{mean} \pm \sigma$
TPC detector	Hit ToA	layer#1 2.6 ~ 2.9 μs
		layer#2 5.7 ~ 6.0 μs
		layer#3 8.2 ~ 8.5 μs
		layer#4 10.5 ~ 11.0 μs
	Trigger pads	≥ 2 for each column
Laser and detector	The laser control chassis triggers the energy monitor and DAQ system at the same time.	

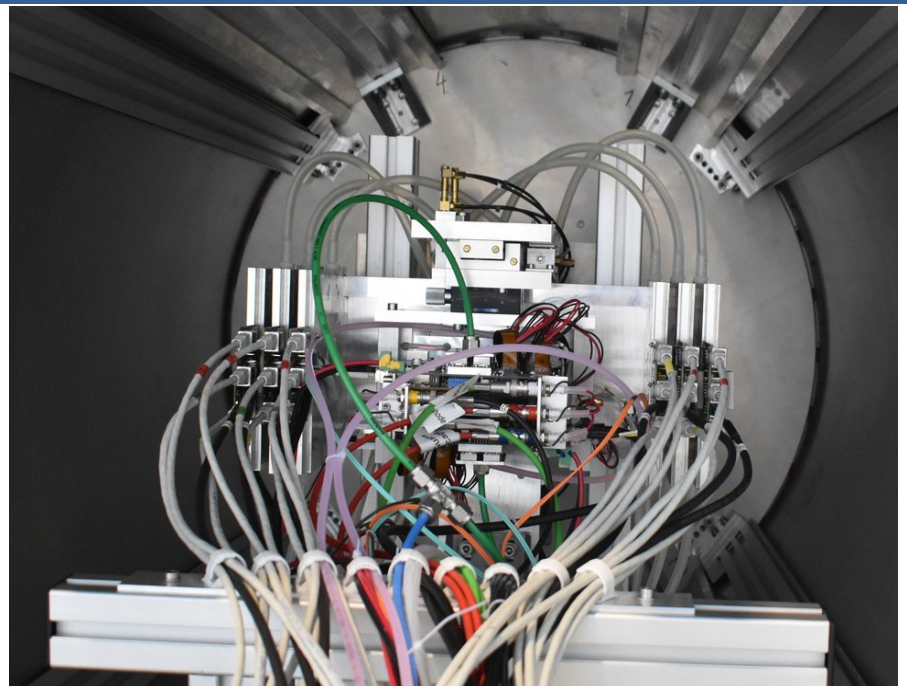


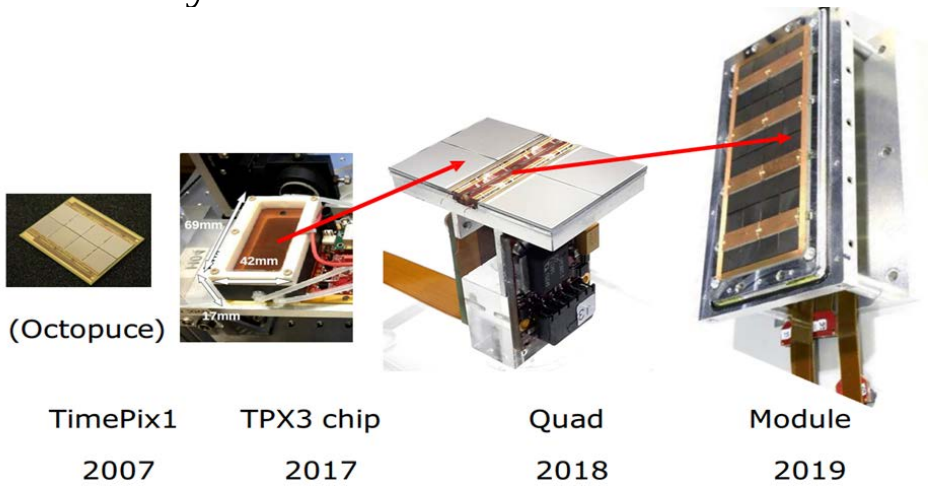
Reconstruction events and ^{55}Fe X-ray spectrum profile(middle) and cosmic ray spectrum(Right)

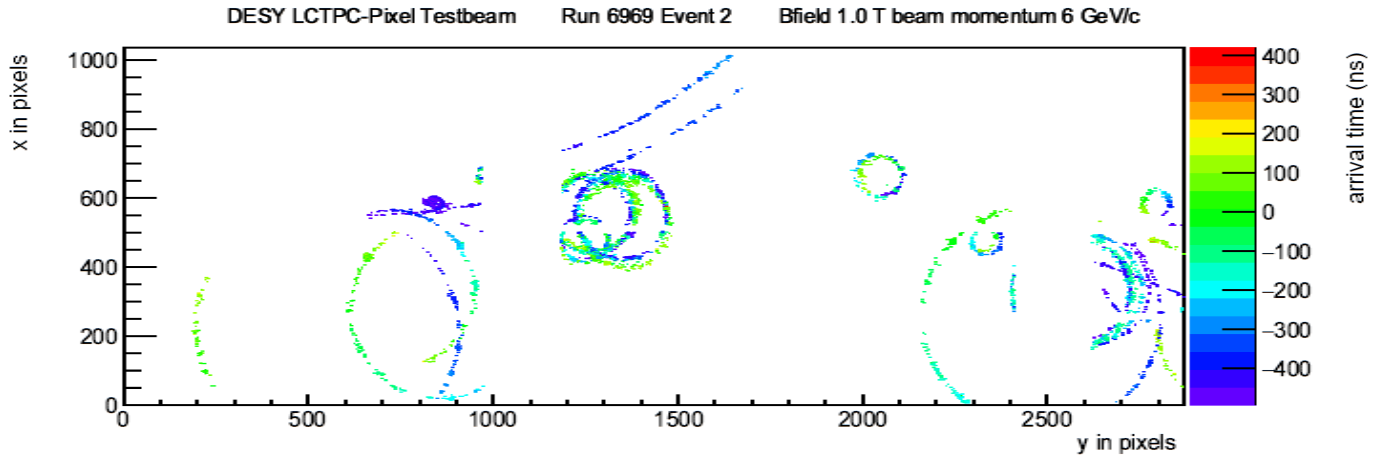
- Pixelated TPC technology

Pixelated TPC technology – Large scale readout

- TPC prototype with GridPixes:
  - A module **with 32 GridPixes has been constructed** and was in a test beam in B=1.0T at DESY in June 2021.
  - Very high detection efficiency results in **excellent tracking and dE/dx performance.** Timepix4 development is ongoing.
- During the test beam ~10^6 events were successfully collected, all results showed that **a pixel TPC is realistic.**
- Ion back flow of the module has been measured and the analysis regular meeting were set up every month with IHEP and Bonn University.







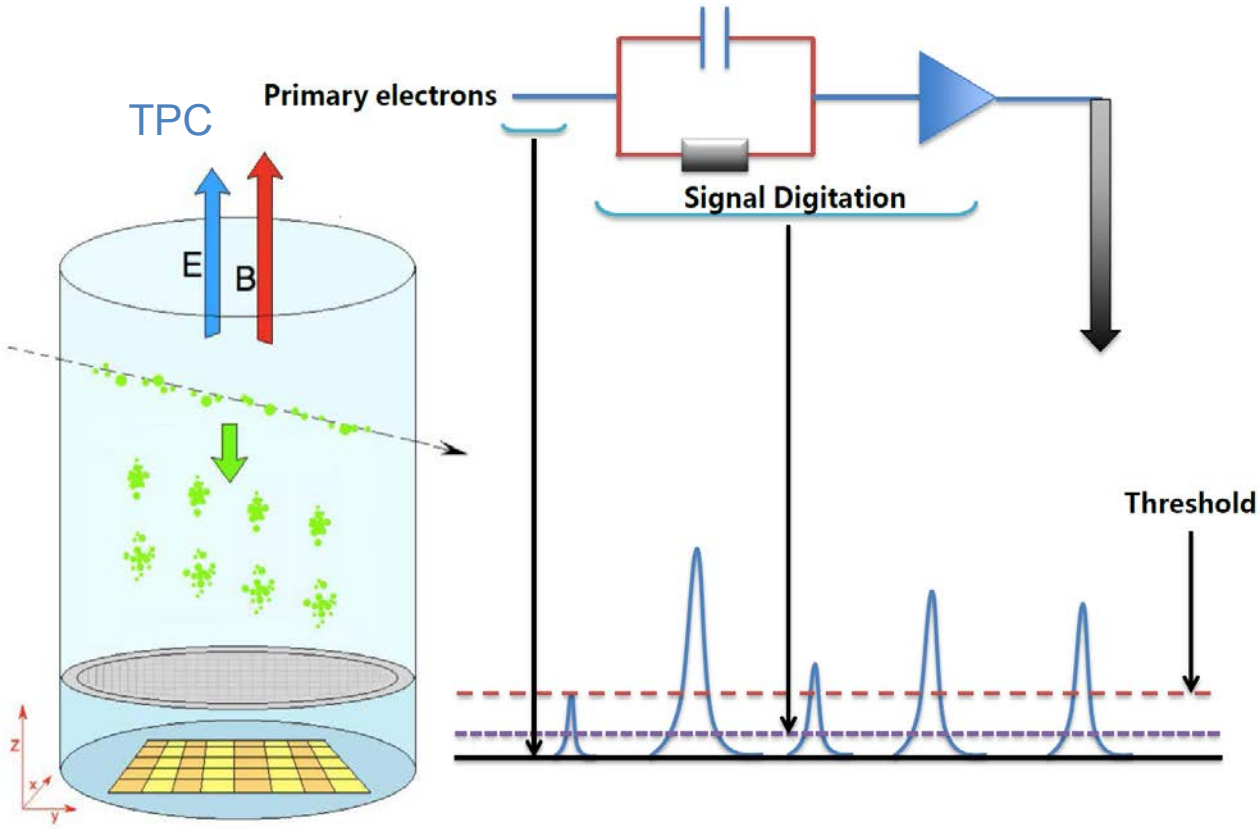
DESY testbeam in June 2021

https://arxiv.org/abs/1902.01987

Identify the clusters to achieve dN/dx and Occupancy

dN/dx cluster counting

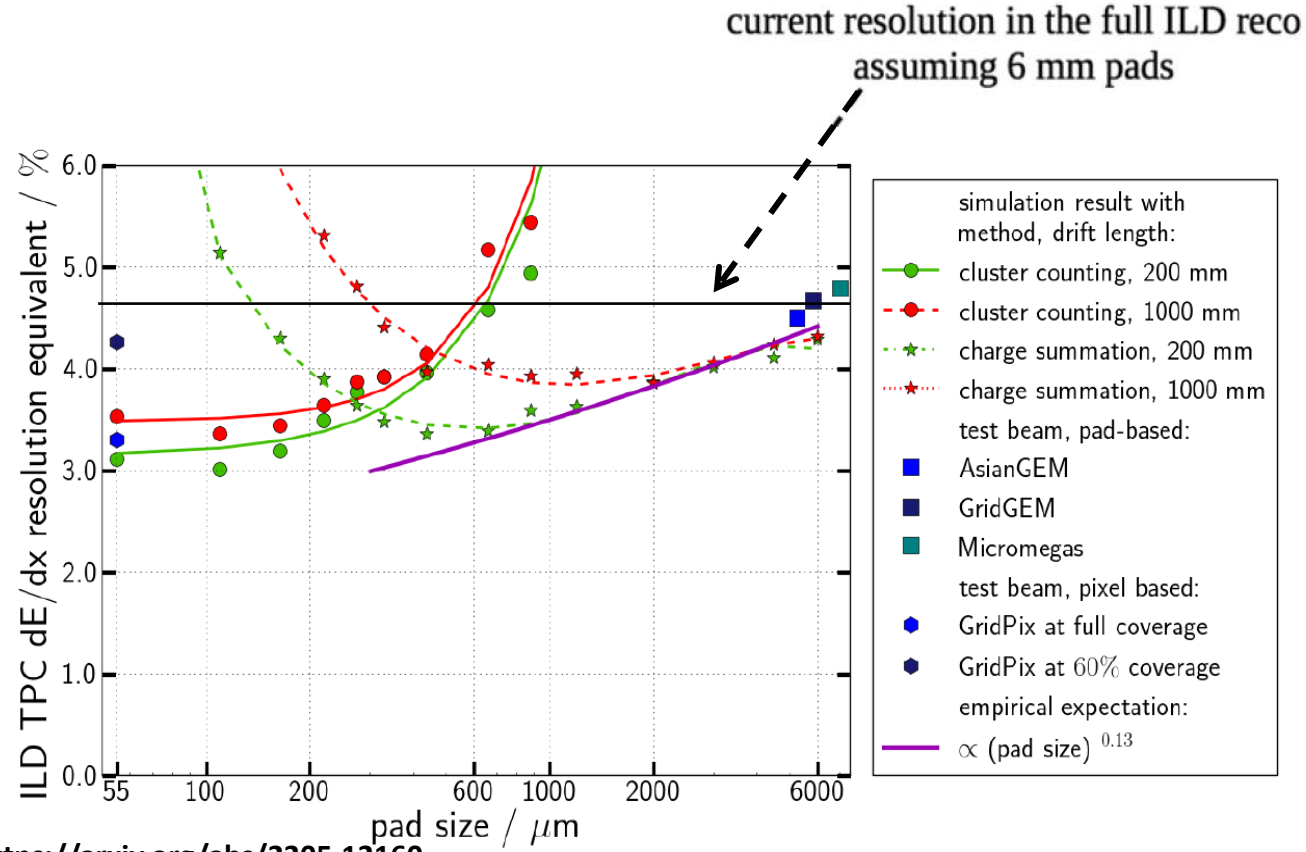
- Challenging for the **low power consumption** electronics (>40mV/fC needed at 2000 of gas gain)
- Pixelated readout
  - → **high granularity readout in endplate**
  - → the reasonable pixilation reveals the underlying cluster structure in 3D chamber
- Occupancy of the pixelated TPC
  - Occupancy is very **key issue** at the high rate or high luminosity
  - Smaller pad/pixel size
    → **smaller occupancy**
  - To be addressed by R&D
    → A detailed simulation would be necessary to determine the scaling factor
    → Simulation ongoing at IHEP

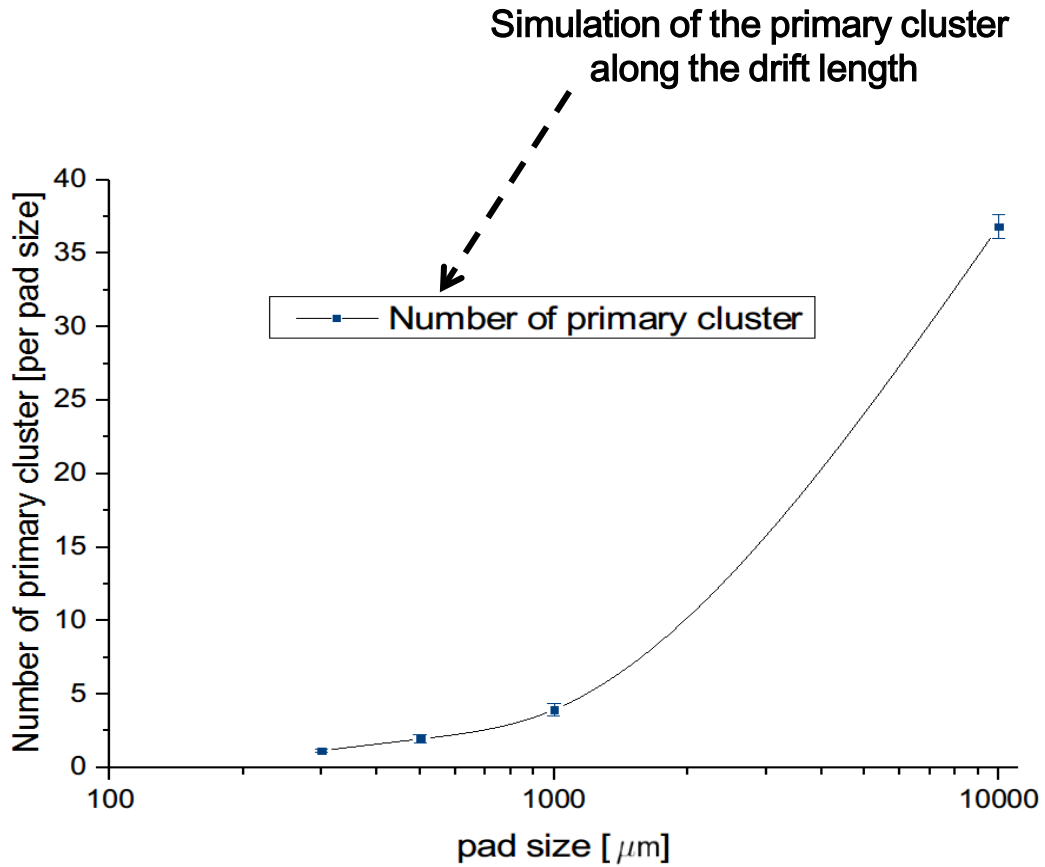


High granularity for improved PID in TPC

- Current full ILD reconstruction: 6mm pads → **~4.8% dE/dx resolution**
- 6mm → 1mm: 15% improved resolution via the charge summation (dE/dx)
- 6mm → 0.1mm: 30% improved resolution via the cluster counting (dN/dx)
  - Pad size of about 300μm can record **~1 primary cluster along track length** at T2K gas
  - High **readout granularity** VS the primary cluster size optimization

All studies ongoing

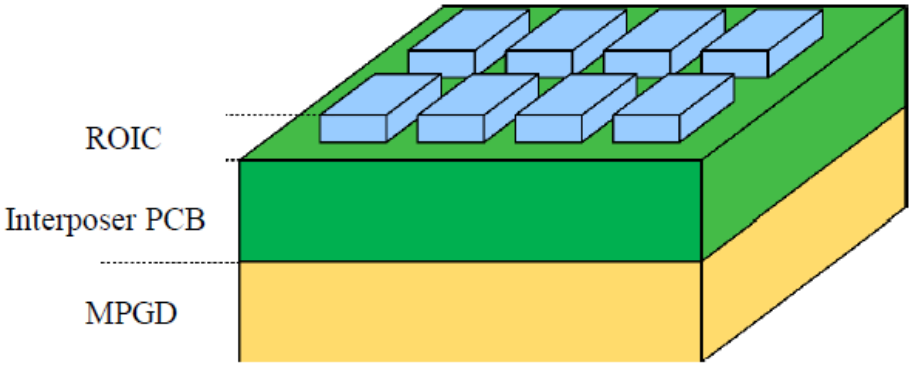




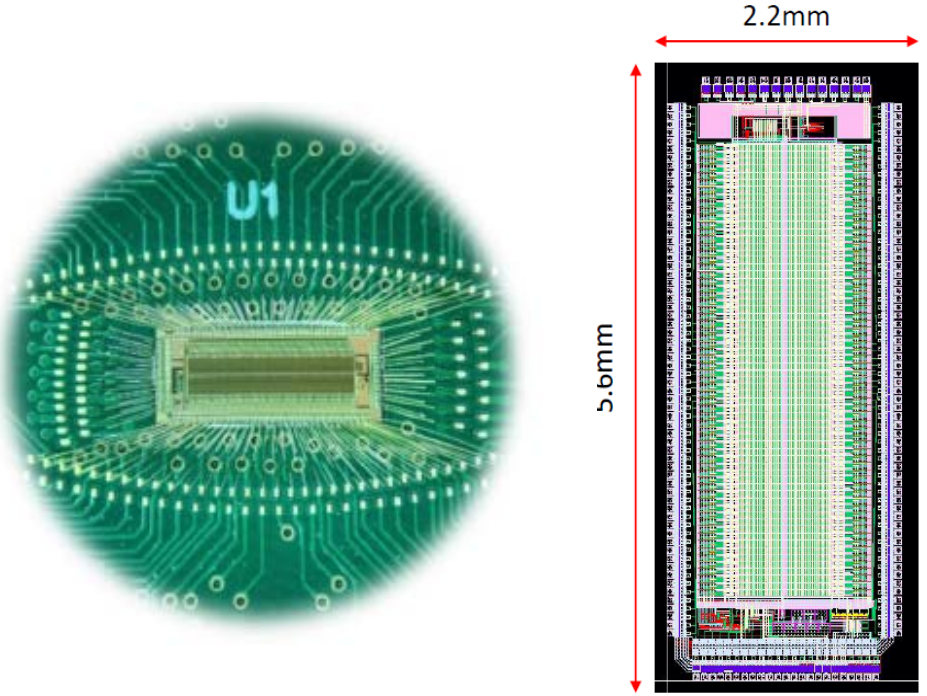
https://arxiv.org/abs/2205.12160

Updated of the pixelated TPC R&D for CEPC at IHEP/Tsinghua

- **R&D on Macro-Pixel TPC readout for CEPC**
  - Macro-Pixel TPC ASIC chip was started to developed in this year and **1st prototype wafer has done in December**.
  - The first version ROIC has been received and under testing.
  - The **TOA and TOT** can be selected as the initiation function in the ASIC chip.
    - 1mm×6mm → 500μm×500μm pixel readout
    - Higher precision and higher rate (MHz/cm^2)
    - Gain of the amplification: >40mV/fC
    - Channels: 128
    - Time resolution: 14bit (5ns bin)
    - Time discriminator: TOA (Time of Arrival)
    - Power consumption: <1mW/pixel (1st prototype)
      - ~400mW/cm^2
      - 100mW/cm^2 (Goal and final design)
    - Technology: 180nm CMOS
    - High metal coverage: 4-side buttable



Principle of Macro-Pixel TPC readout



1st readout PCB board and the ASIC layout

Summary

- TPC tracking using GEM, Micromegas and GridPix pad and pixelated readouts have been developed for the future e+e- colliders.
- Analysis of test beam data with similar set of GEM, Micromegas and Gridpix modules demonstrated the proof-of-concept and validated these technologies.
- The TPC prototype integrated 266nm UV laser tracks has successfully developed at IHEP in the last few years, the results promised the spatial resolution and dE/dx. Macro-Pixel TPC ASIC chip was started to developed in this year and the tests will be starting.
- Synergies with CEPC/FCCee/EIC/T2K/ALICE allow us to continue R&D and ongoing, we learn from their experiences and R&D.

Many thanks!