

TaichuPix3 testbeam at DESY

Zhijun Liang

on behalf of CEPC vertex detector group

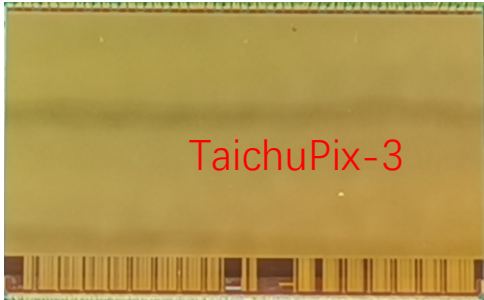
2023/01/18



Overview of MOST2 vertex detector R&D

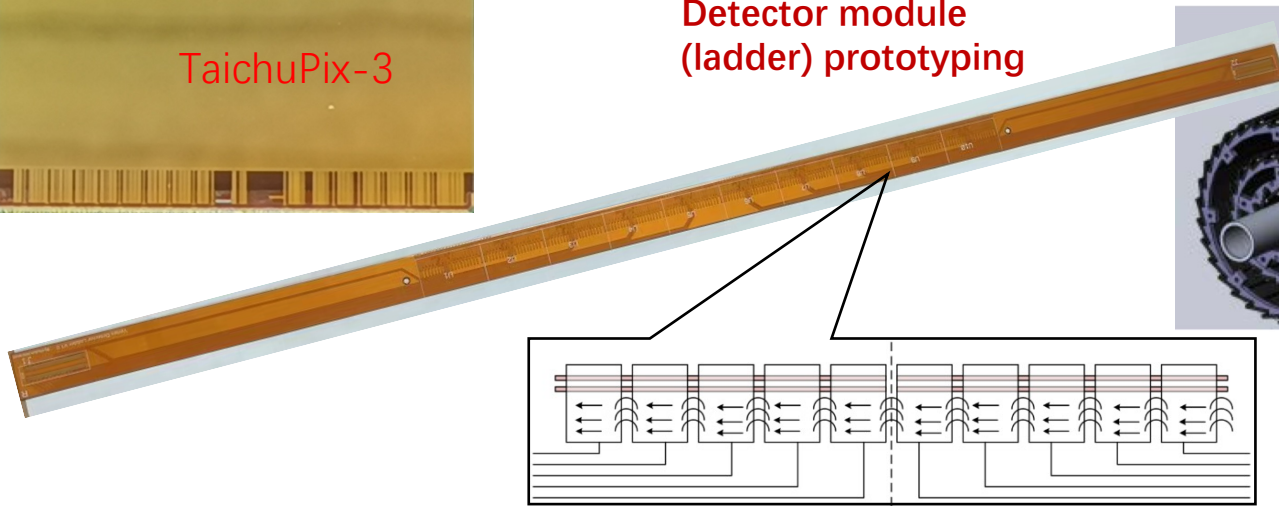
- **Can break down into sub-tasks**
 - CMOS Pixel Sensor chip R&D
 - Detector layout optimization, ladder and vertex detector support structure R&D
 - Detector assembly
 - Data acquisition system R&D

CMOS pixel sensor
prototyping



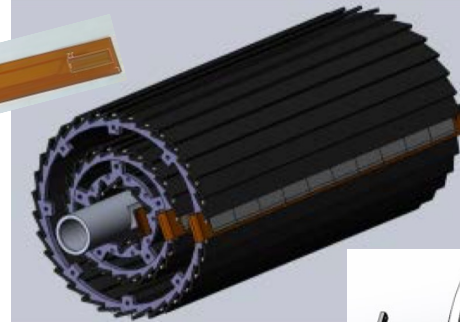
TaichuPix-3

Detector module
(ladder) prototyping

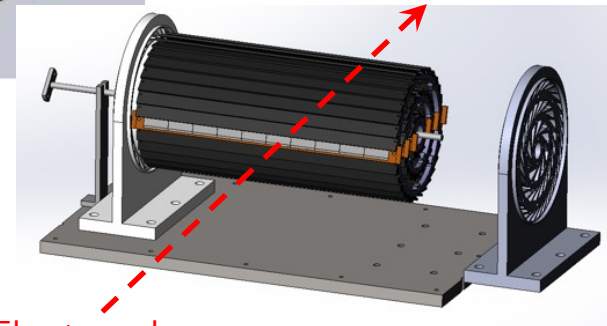


Double sided ladder
10 sensors/ladder side, read out from both ends

Full size vertex detector prototype



Beam test to verify its
spatial resolution



Electron beam





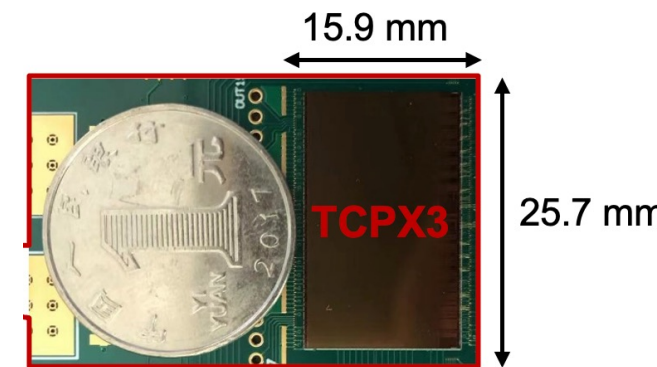
Large-scale sensor TaichuPix-3

➤ TaichuPix3 and Challenges for the CMOS sensor

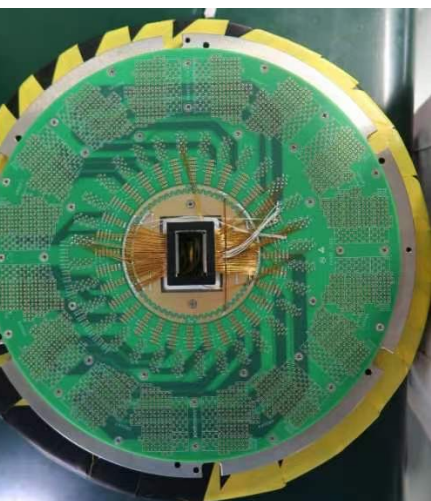
- Small pixel size -> high resolution (3-5 μm)
- High readout speed (<500ns deadtime @40MHz at Z pole) -> for CEPC Z pole high lumi
- Radiation tolerance (per year): 1 MRad

Chip size : 26 × 16 mm
Pixel size : 25 μm × 25 μm

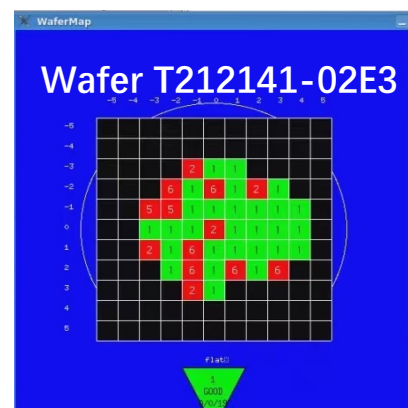
	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓



TaichuPix-3 chip vs. coin



Probe card for wafer test



An example of wafer test result

5 wafers tested

- 2 wafer based on standard process
 - Reasonable yield achieved
- 3 wafer based on modified process
 - lower yield than the std. process

Wei Wei, Ying Zhang
Tianya Wu





Testbeam on DESY

• On Site team (DESY)

- Joao (IHEP) Project leader
- Zhijun Liang (IHEP) test beam coordinator
- Tianya Wu (IHEP) Shift leader , ASIC expert
- Ming Qi (NJU) Shift leader
- Lei Zhang (NJU) Shift leader
- Xiaomin Wei (NWPU) ASIC experts
- Jia Zhou (IHEP) DAQ
- Xinhui Huang (IHEP) Assembly
- Shuqi Li (IHEP) Offline
- Hao Zeng (IHEP) Offline
- XueWei Jia (IHEP) Offline



Romate support

WeiWei, Ying Zhang (IHEP) ASIC

Jun Hu, Ziyue Yan (IHEP) firmware

Hongyu Zhang (IHEP) DAQ

Jinyu Fu, Mingyi Dong (IHEP) Assembly

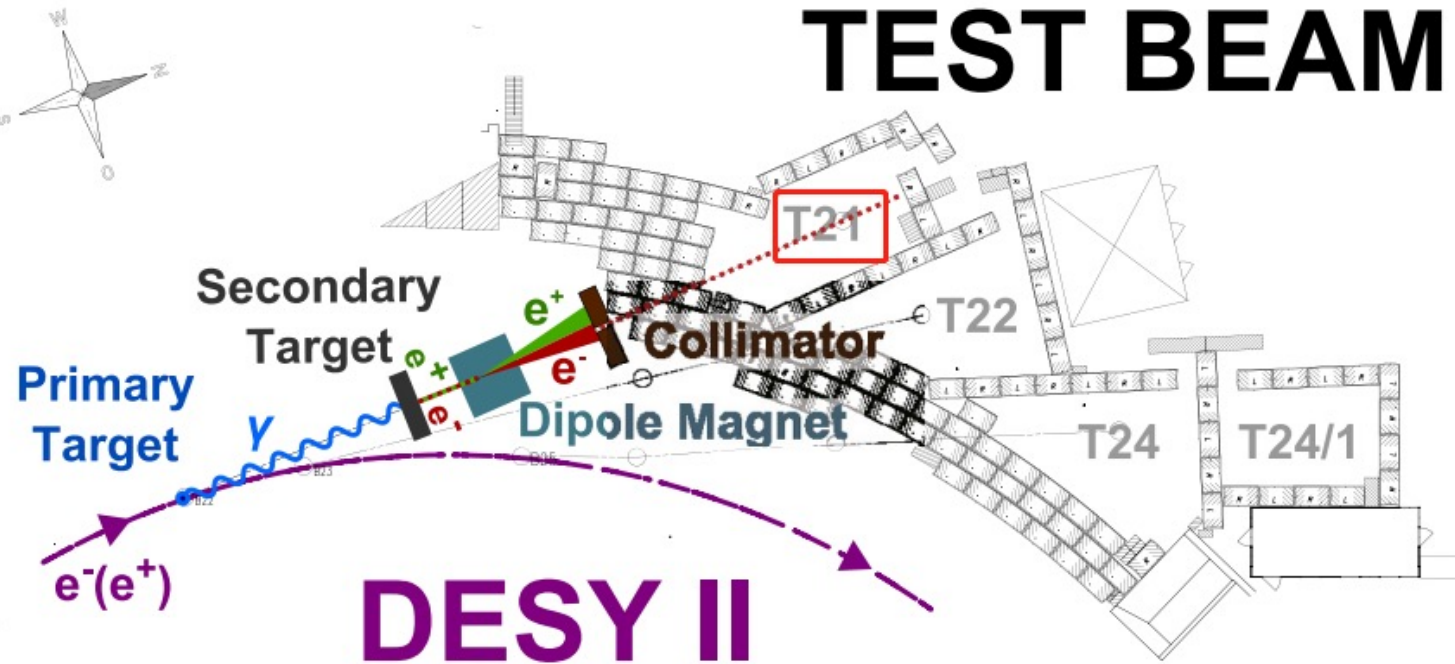
Wei Wang, Gang Li, Linhui Wu (IHEP) Offline

Yiming Hu, Xiaoxu Zhang (NJU)...



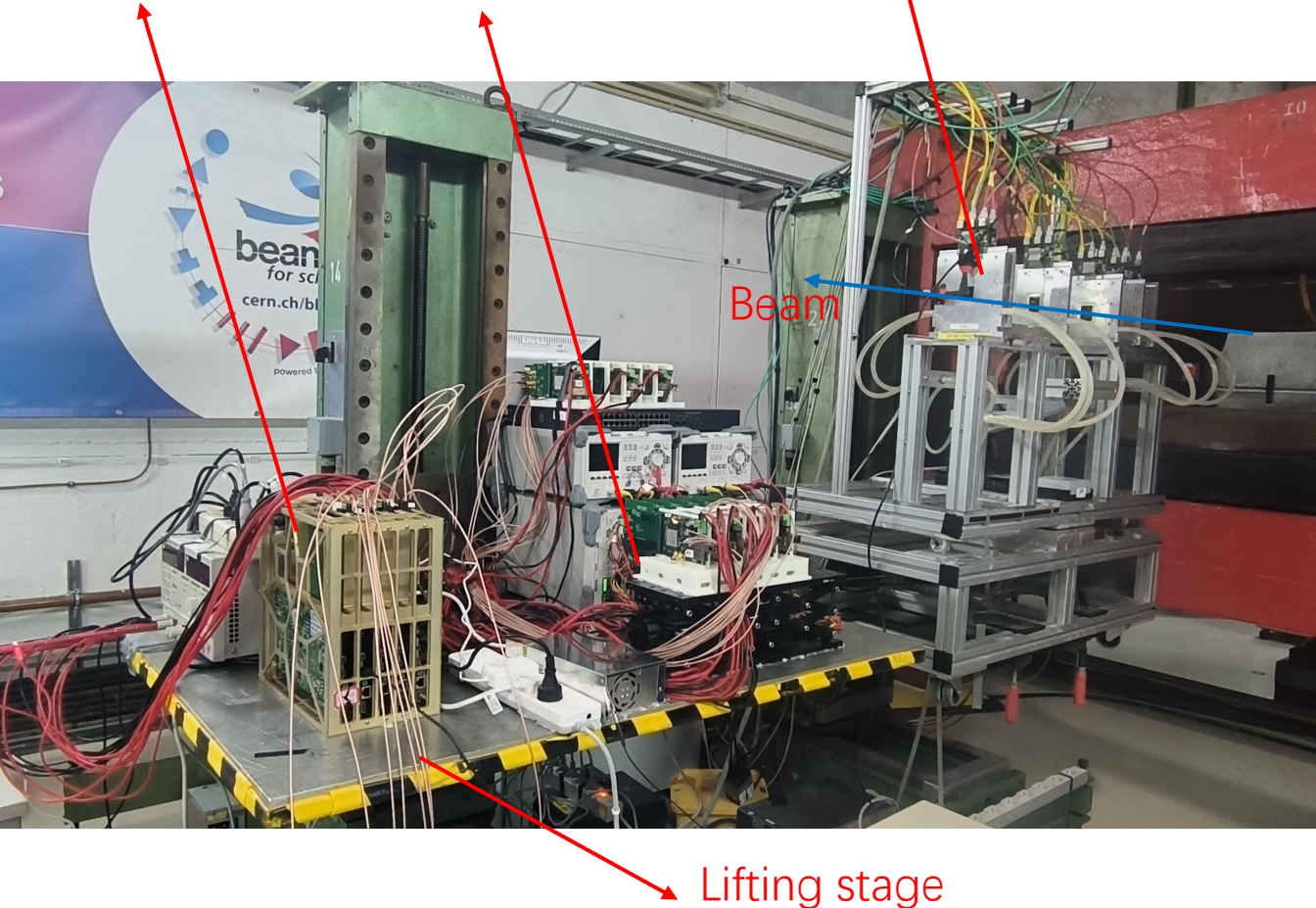


Introduction of DESY TB21



The electron or positron beams are converted bremsstrahlung beams from carbon fibre targets in the electron-positron synchrotron DESY II with up to 1000 particles per cm^2 and energies from 1 to 6 GeV, an energy spread of $\sim 5\%$ and a divergence of $\sim 1\text{mrad}$.

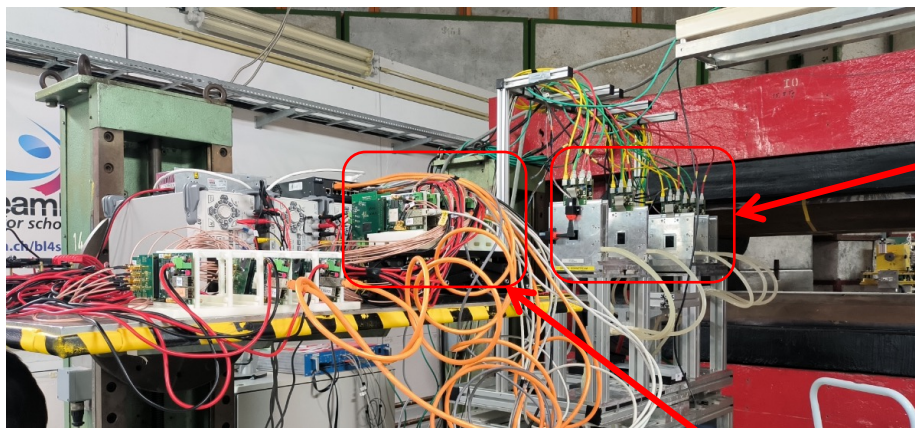
DESY Testbeam Setup



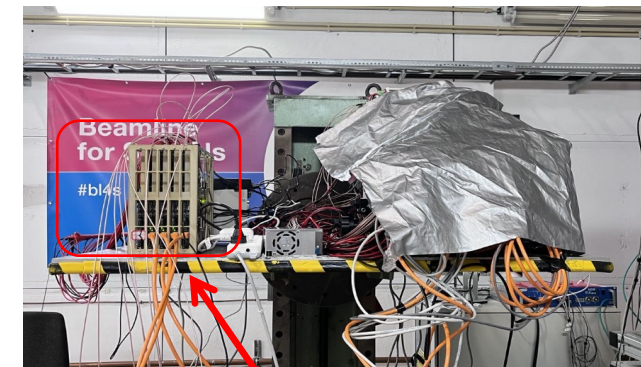
- The 6-layer of TaichuPix3 telescope was in the middle of the 5-layer MIMOSA and 4-layer JadePix telescope.
- MIMOSA is fixed there and cannot move. But it can be used to calibrate the position of the TaichuPix3 telescope



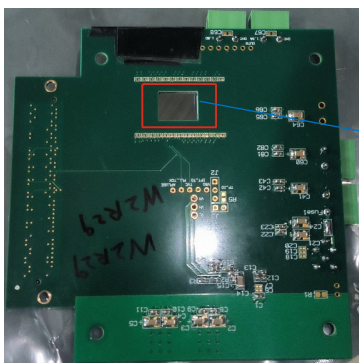
Setup of TaichuPix3



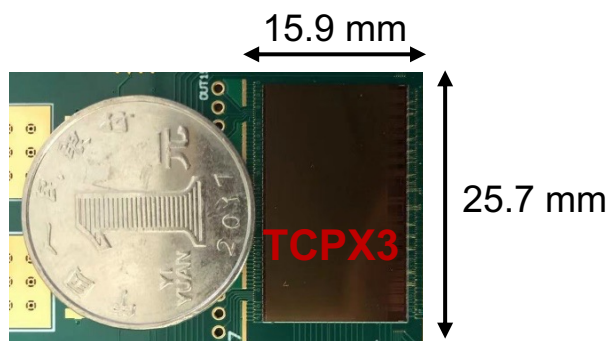
MIMOSA Telescope



• Jadepix telescope



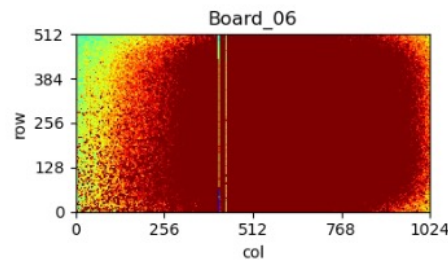
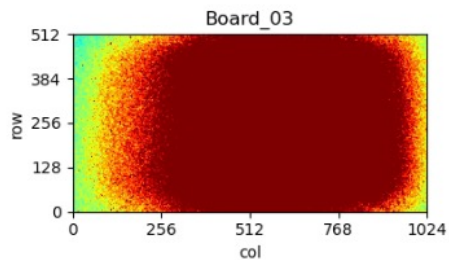
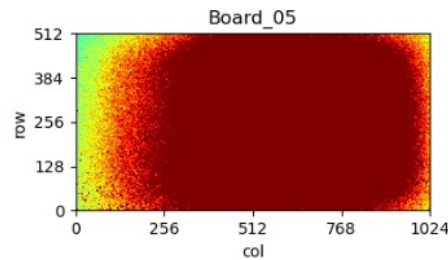
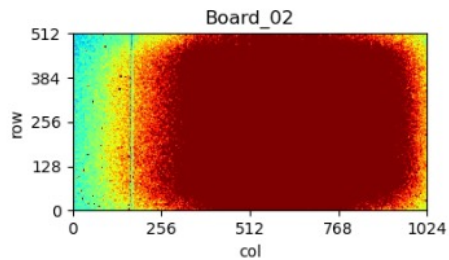
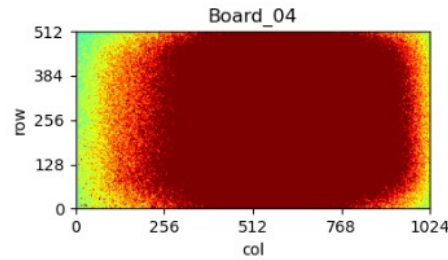
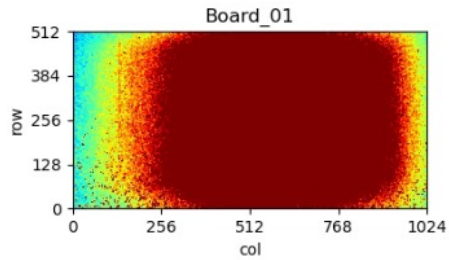
An open window in
backside of PCB with a
size of 12mm x 9mm



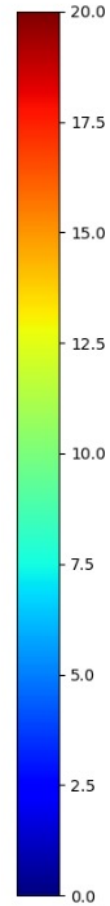


Hitmap of 3 GeV beam

Hitmap



6 layers of hit map are fine .



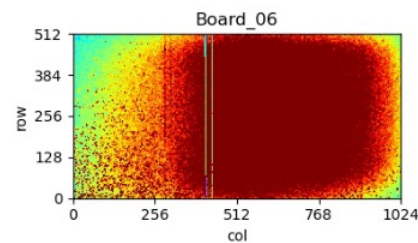
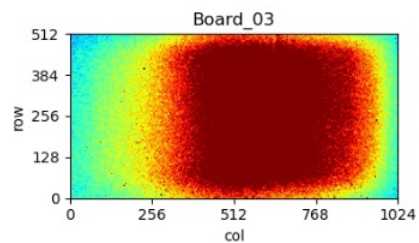
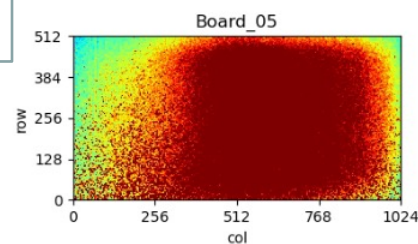
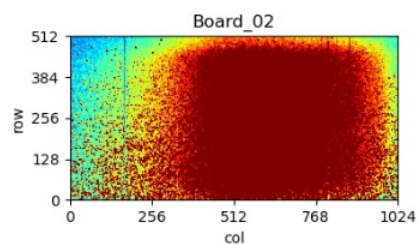
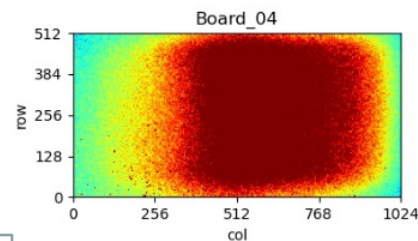
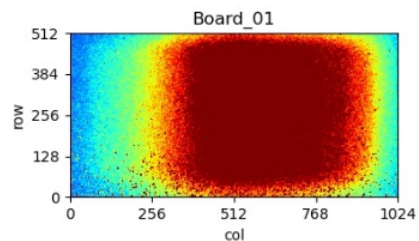
Jia Zhou
Tianya Wu
Hongyu Zhang



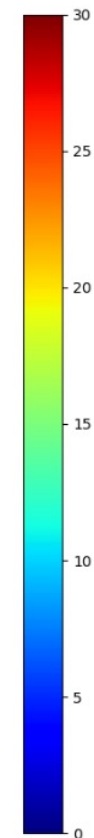


Hitmap of 4 GeV beam

Hitmap



6 layers of hit map are fine .



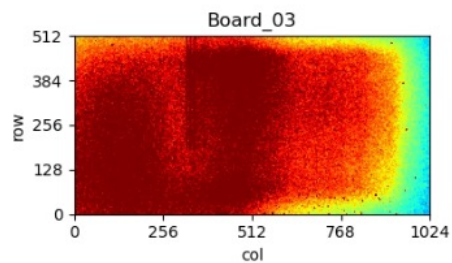
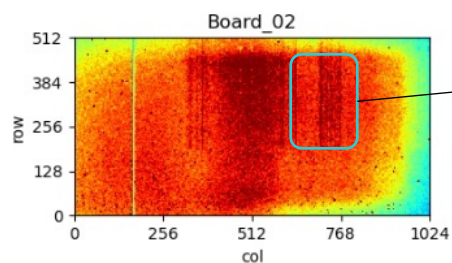
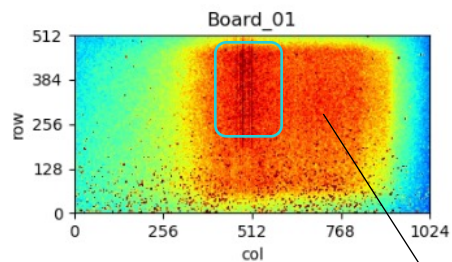
Jia Zhou
Tianya Wu
Hongyu Zhang



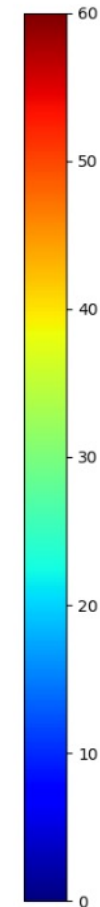
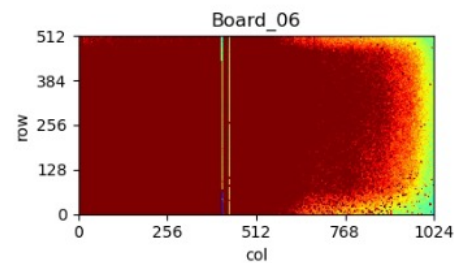
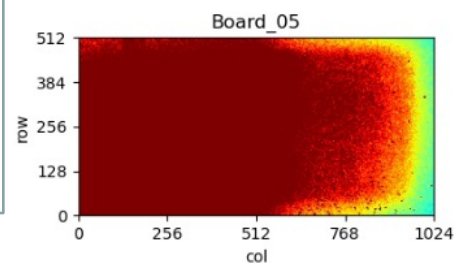
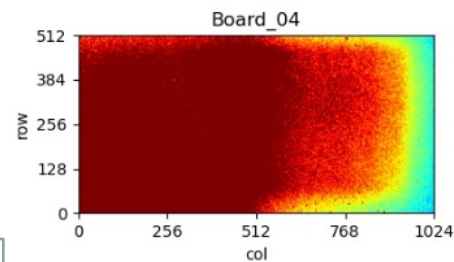


Hitmap of 5 GeV beam

Hitmap



The hitmap
are quite
different, and
with wired
strips



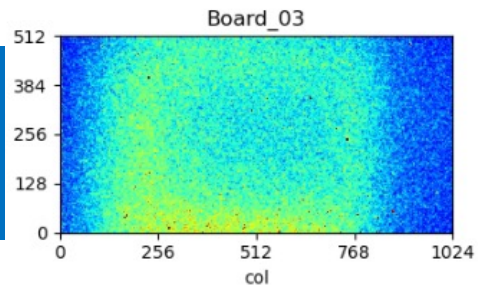
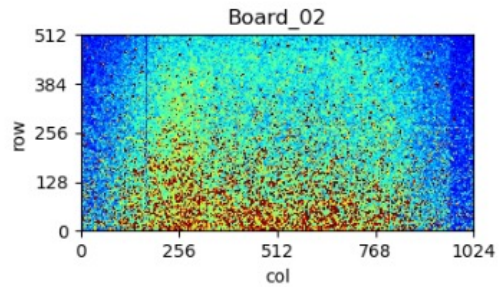
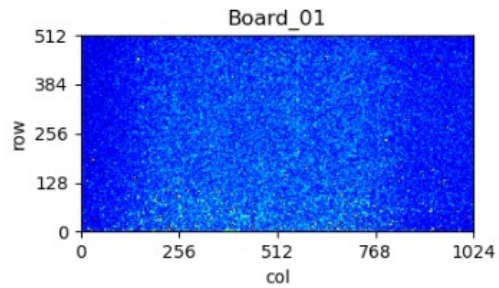
Jia Zhou
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Hongyu Zhang



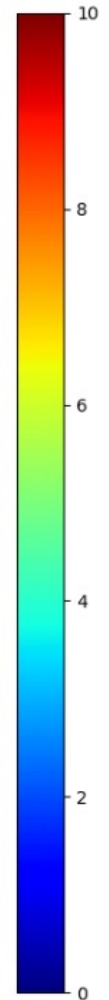
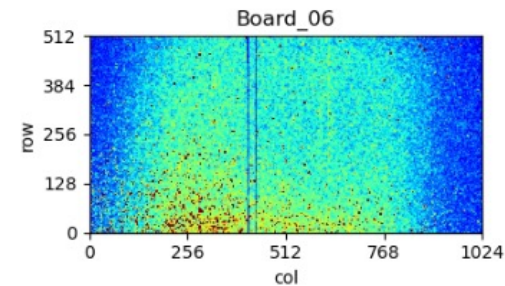
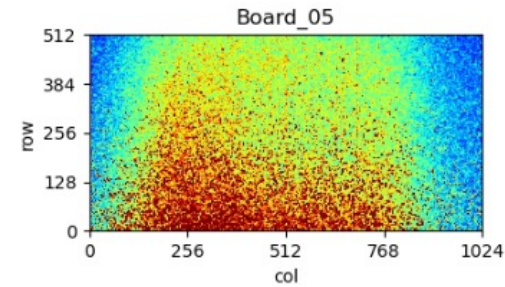
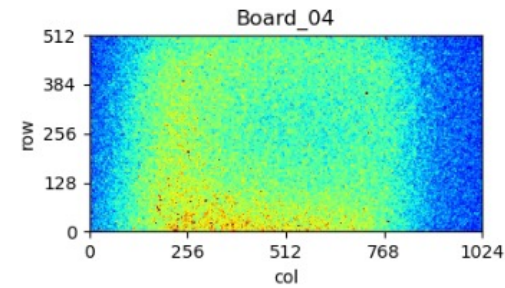


Hitmap of 6 GeV beam

Hitmap



From the hitmap, the position of beam spot is off to the initial one. west-east direction moves from 1.8 to -4.3.



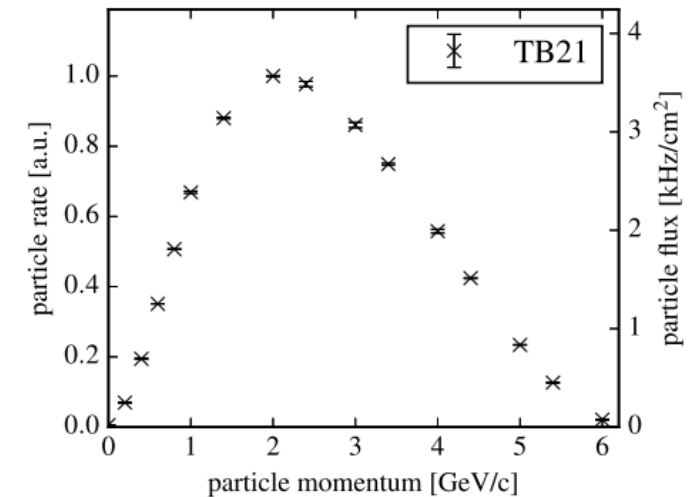
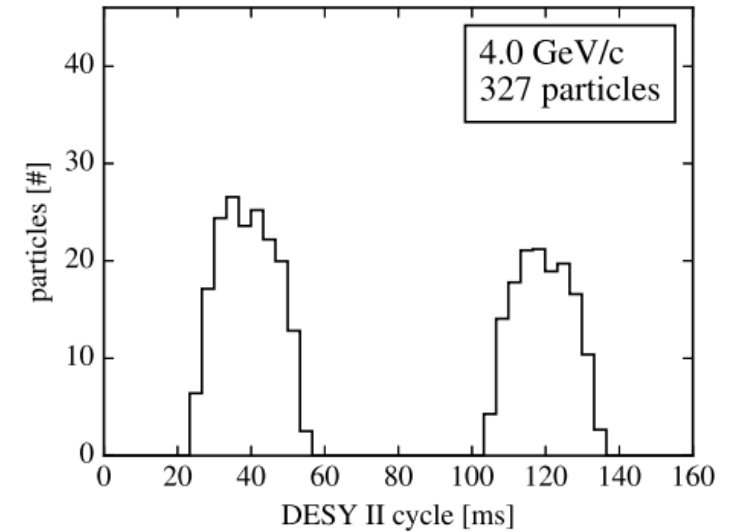
Jia Zhou
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Hongyu Zhang





DESY testbeam Energy Opti

- From hit map, 4GeV is a moderate option.
→ Enough data and higher energy
- 4 GeV is used for Threshold scan, the data rate is around 10K B/s for a standard CMOS chip and 67.4K B/s for modified process.
- The valid coincidence tracks are around 41 tracks/ s when $\chi^2 < 2$
- The sensors are working for the full beam time except for the chip replacement. Totally about 100GB valid data were recorded



(a) at TB21

Refer from: *The DESY II test beam facility*

<https://doi.org/10.1016/j.nima.2018.11.133>

NIMA, Volume 922, 1 April 2019, Pages 265-286





MOST2 offline reconstruction and alignment

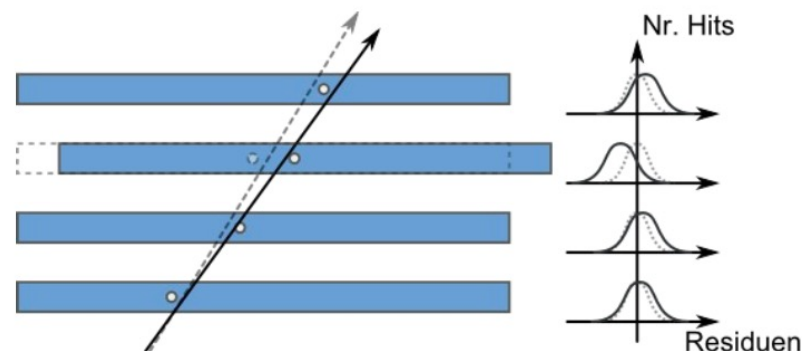
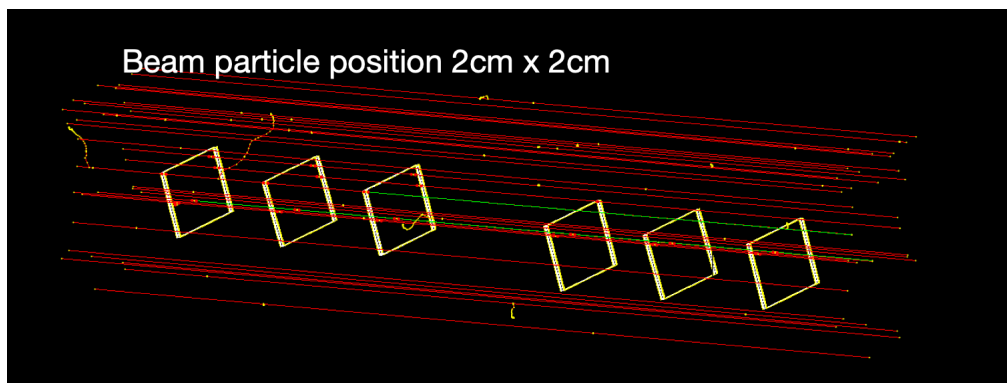
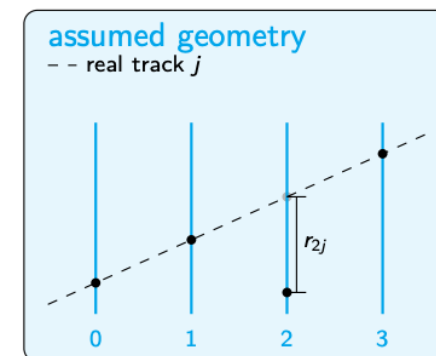
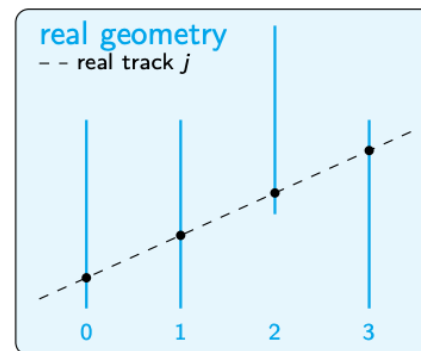
Shuqi Li
Linghui Wu
Gang Li

Track Reconstruction

- No magnetic field
- Least squares fitting (Straight line fit)
- No considering multi-scattering now

Alignment

- Using Millepede (c++ version) matrix method
- Correct for the misalignment chip position
- Evaluate the influence of different alignment parameters on spatial resolution





Alignment

- Method - millepede matrix method

p: alignment parameters, q: track parameters

- minimize: $\chi^2 = \sum_{i \in \text{tracks}} \vec{r}_i^T V_i^{-1} \vec{r}_i$ r is residual $\vec{r}_i(\vec{p}, \vec{q}_i)$, V is the covariance matrix

$$\frac{d\chi^2(\vec{p})}{d\vec{p}} = 0 \longrightarrow \chi^2(\vec{p}) = \chi^2(\vec{p}_0) + \left. \frac{d\chi^2(\vec{p})}{d\vec{p}} \right|_{\vec{p}=\vec{p}_0} (\vec{p} - \vec{p}_0) \longrightarrow \underbrace{\frac{(J^T V_i^{-1} J)}{C}}_C \Delta \vec{p} = \underbrace{J^T V_i^{-1} \vec{r}_i(\vec{p}_0)}_b$$

$$C \Delta \vec{p} = \vec{b}$$

- invert the Matrix C to find alignment correction Δp
- reduce matrix C for alignment only

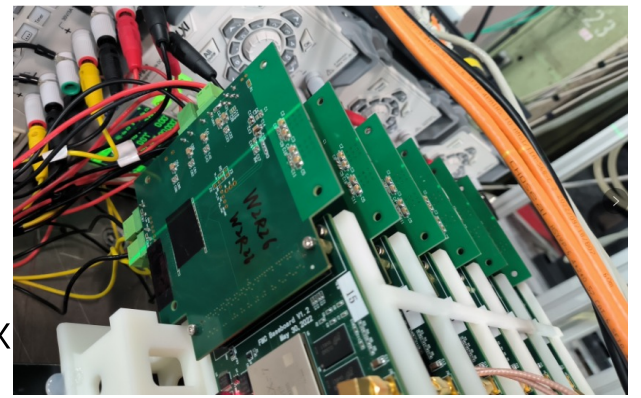
$$S = C_{11} - C_{12} C_{22}^{-1} C_{21}$$

$$\begin{pmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{pmatrix} \begin{pmatrix} \Delta \vec{p}_1 \\ \Delta \vec{p}_2 \end{pmatrix} = \begin{pmatrix} \vec{b}_1 \\ \vec{b}_2 \end{pmatrix} \longrightarrow \begin{pmatrix} \Delta \vec{p}_1 \\ \Delta \vec{p}_2 \end{pmatrix} = \begin{pmatrix} S^{-1} & -S^{-1} C_{21}^T C_{22}^{-1} \\ -C_{22}^{-1} C_{21} S^{-1} & C_{22}^{-1} - C_{22}^{-1} C_{21} S^{-1} C_{21}^T C_{22}^{-1} \end{pmatrix} \begin{pmatrix} \vec{b}_1 \\ \vec{b}_2 \end{pmatrix} \longrightarrow \Delta \vec{p}_1 = S^{-1} (\vec{b}_1 - C_{21}^T C_{22}^{-1} \vec{b}_2)$$

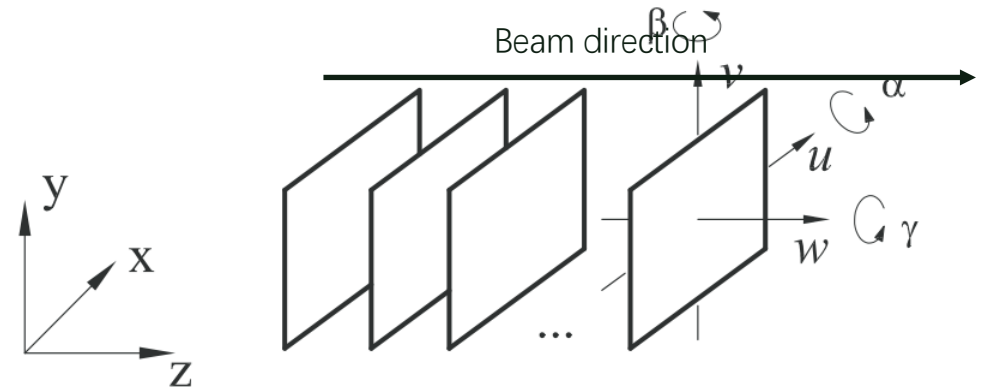
- Matrix S with smaller size than C, and C_{22} is easy to invert

- Six alignment parameters considered

- Translation along X, Y, Z direction
- Rotation around X, Y, Z axis



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Linghui Wu
Gang Li





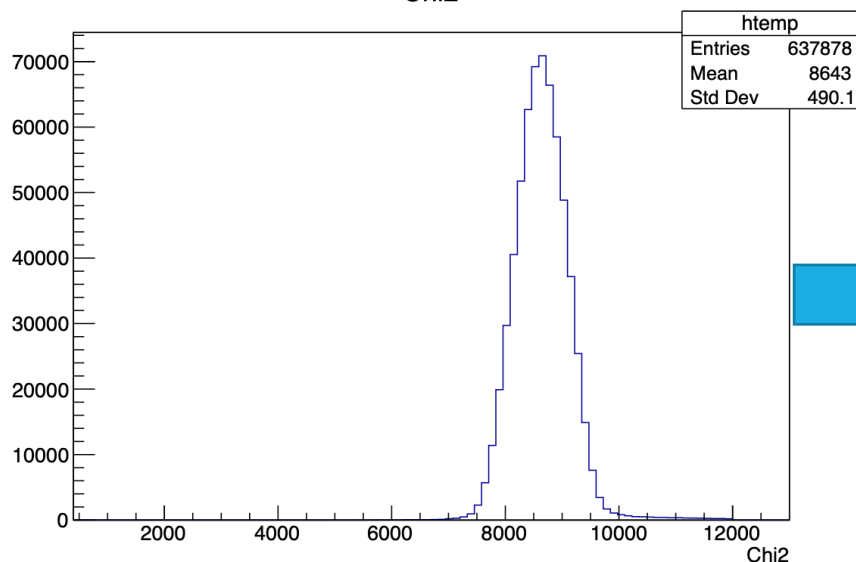
Chi2 of the track before and after Alignment

- Chi2 (no dividing ndf) distribution before and after alignment
- Chi2 of the track reduced significantly after alignment

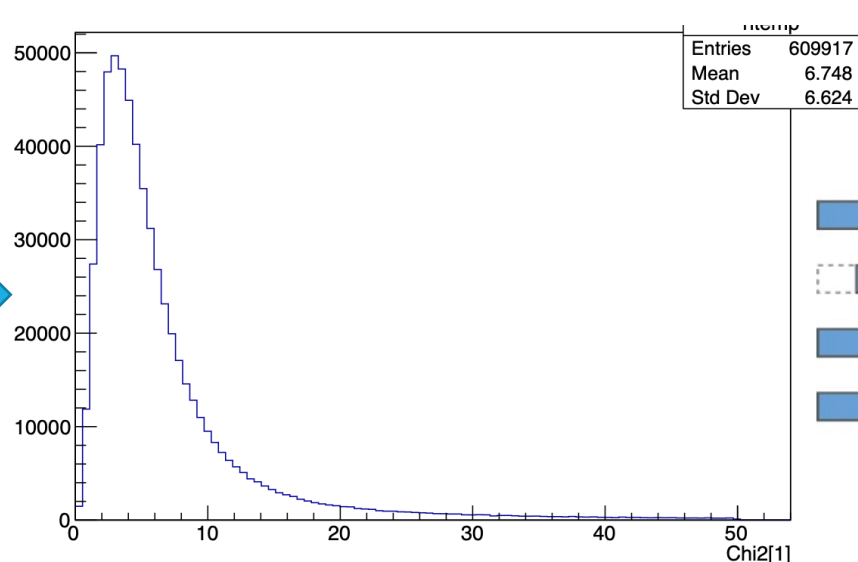
$$\chi^2(\alpha) = \sum_{i=1}^n \frac{f(x_i, \alpha) - e_i)^2}{\sigma_i^2}$$

Before alignment

Chi2



after alignment

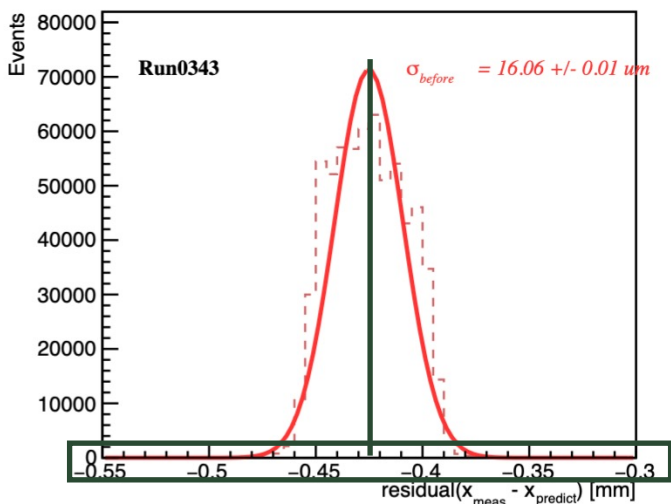


► unbiased Residual plots before and after alignment (4GeV)

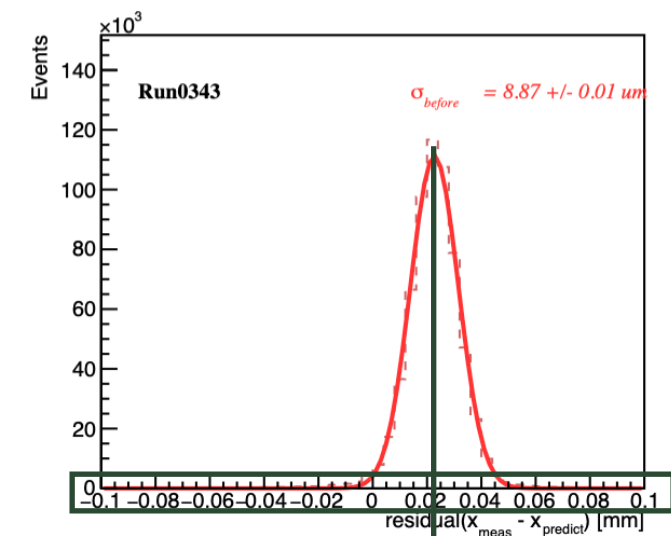
$$\chi^2(\alpha) = \sum_{i=1}^n \frac{f(x_i, \alpha) - e_i)^2}{\sigma_i^2}$$

xdirection, ChipID = 1

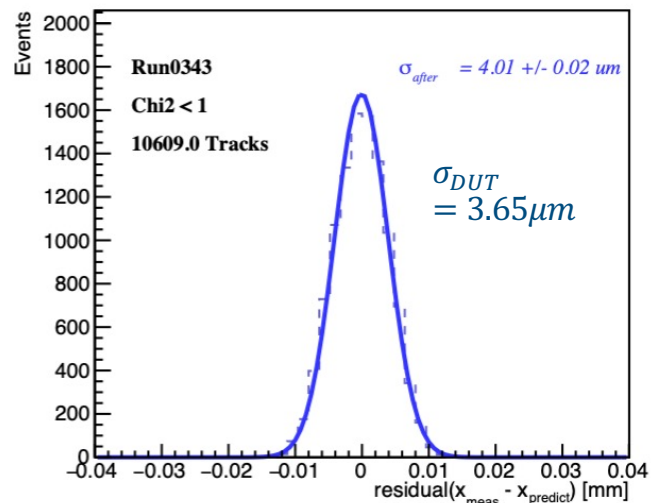
Before alignment



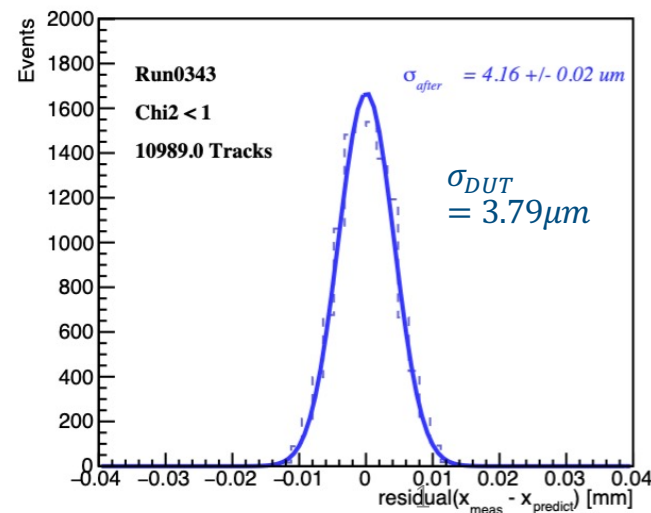
xdirection, ChipID = 4



xdirection, ChipID = 1



xdirection, ChipID = 4



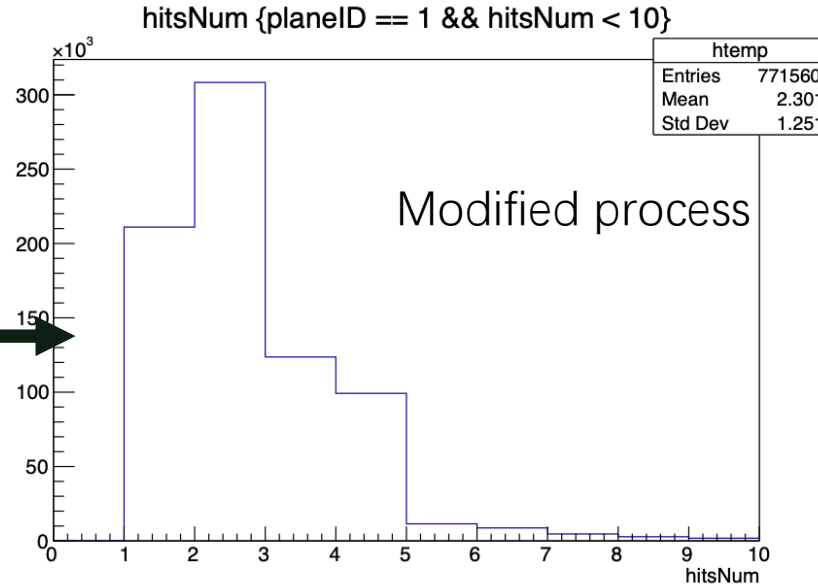
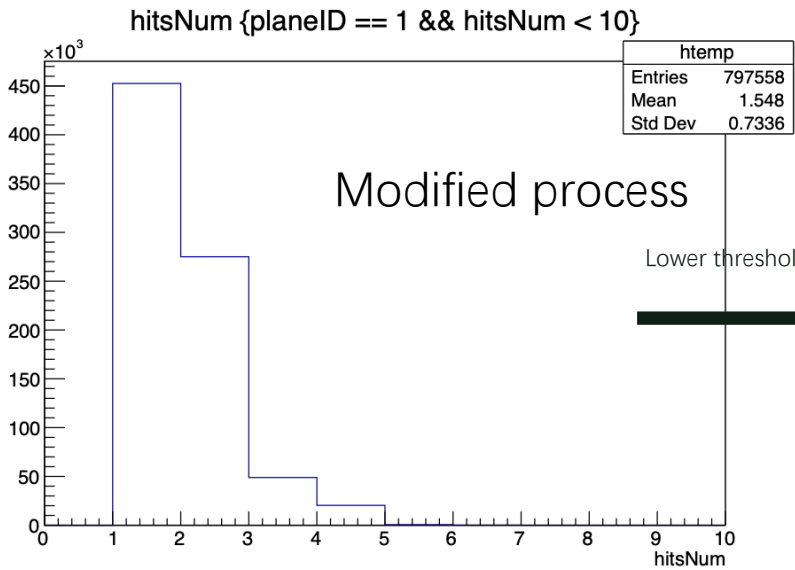
- The misalignment can be well corrected.
- The spatial resolution can reach $< 5\mu m$

- $\sigma_{meas}^2 = \sigma_{DUT}^2 + \sigma_{tel}^2$
- $\sigma_{DUT} \approx 0.91\sigma_{meas}$

Shuqi Li
Linghui Wu
Gang Li
Zhijun Liang
Xuewei Jia
Joao



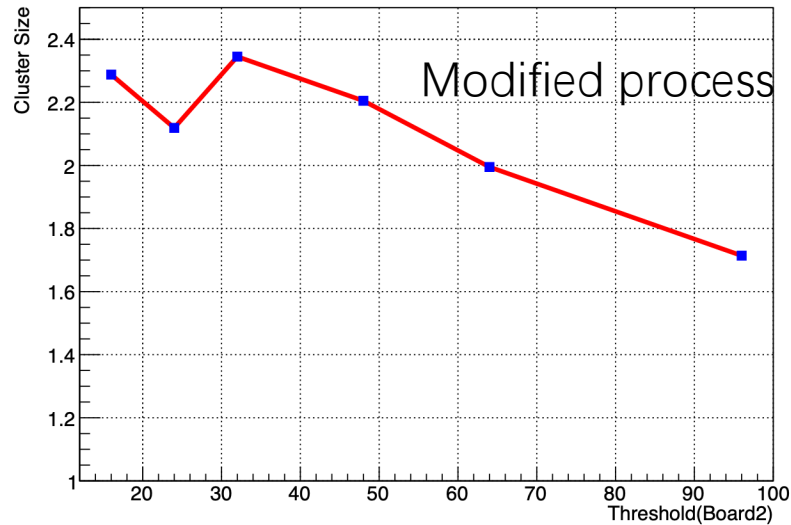
Cluster size vs. chip threshold (4GeV)



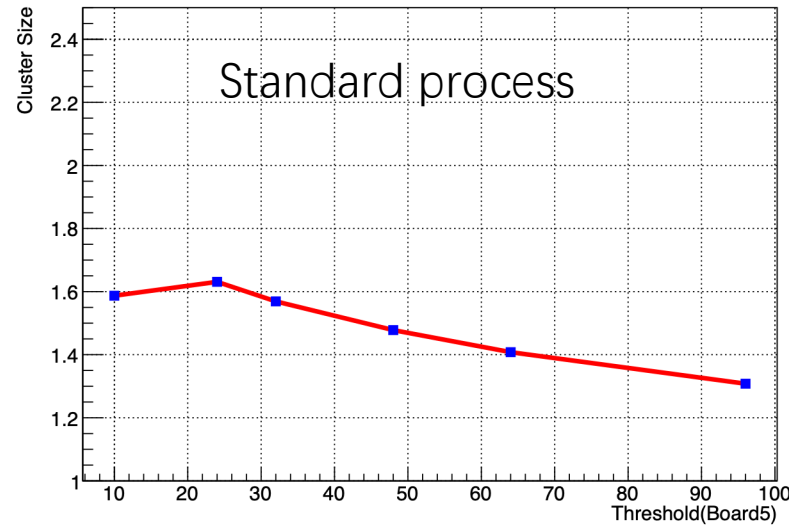
Lower threshold



Board2, Threshold(Board2) 16->24->32->48->64->96

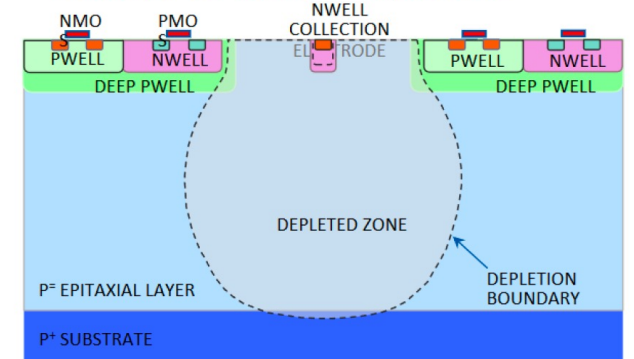


Board5, Threshold(Board5) 10->24->32->48->64->96

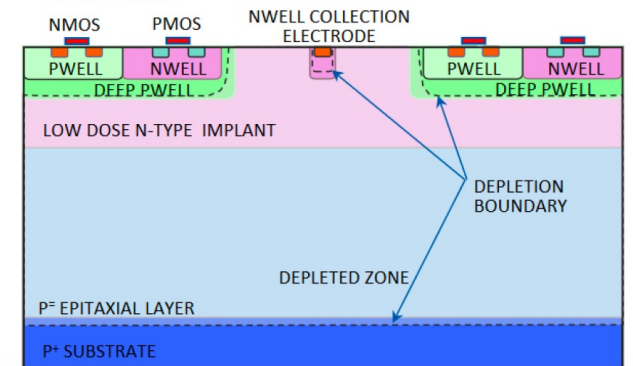


- If lowering the threshold, cluster size will be dominated by cluster with 2 hit
- In general, the higher the threshold, the smaller the cluster size

Standard : no full depletion



Modified : full depletion, faster charge collection



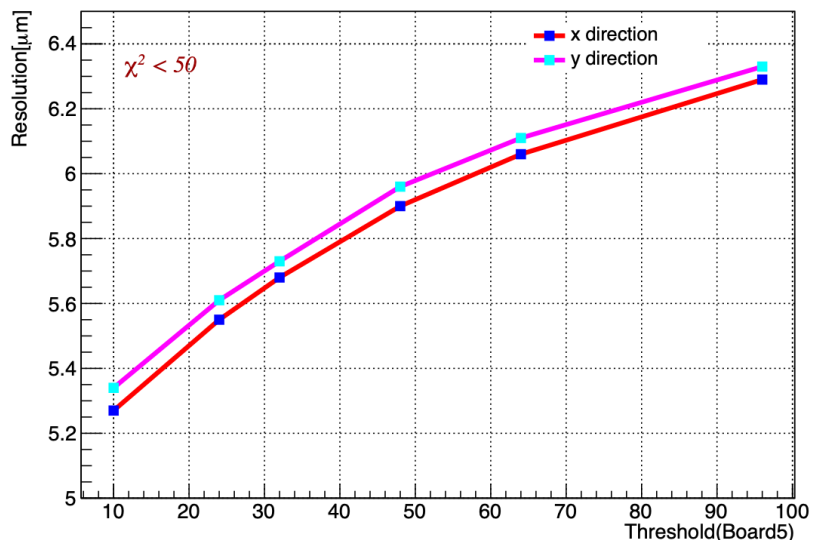


Resolution vs. chip threshold (4GeV) : Standard process

- The spatial resolution of standard chip improved with lowering the threshold
 - Can reach around **5μm resolution**
 - without Kalman filter (without correction for multiple scattering)
- The spatial resolution can reach about **3.5μm** with chi2 cut
 - Suppress the multiple scattering effect with Chi2 cut

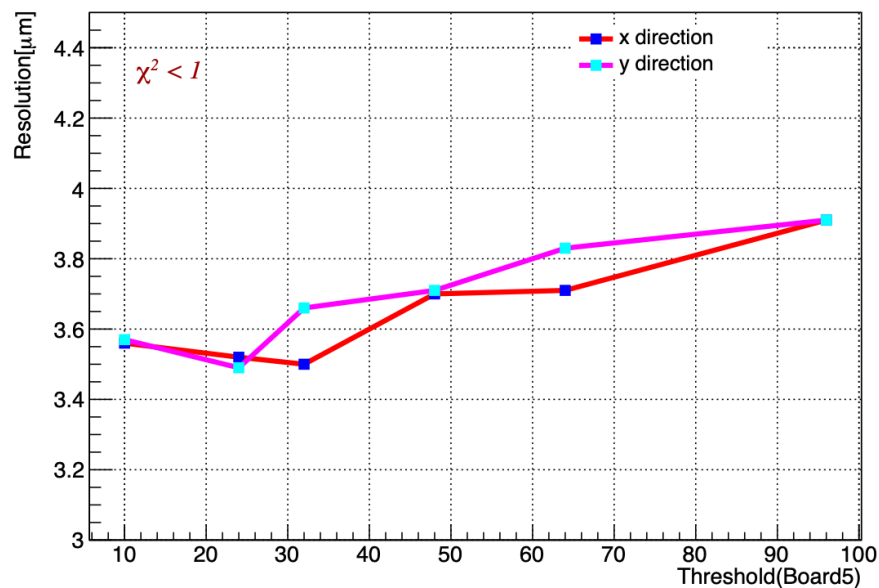
All tracks

Board5, Threshold(Board5) 10->24->32->48->64->96

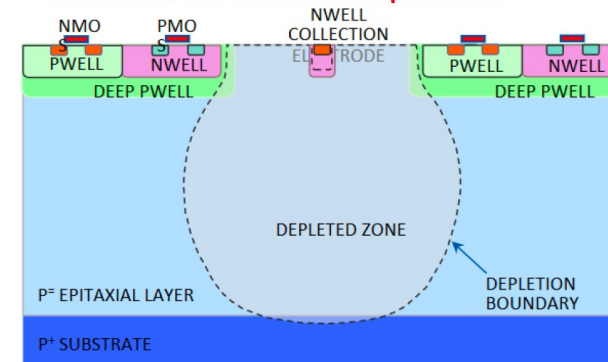


Tracks with small Chi2
Suppressing multiple scattering

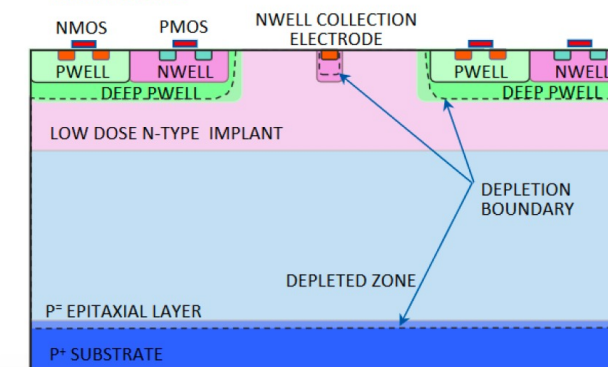
Board5, Threshold(Board5) 10->24->32->48->64->96



Standard : no full depletion



Modified : full depletion, faster charge collection



Shuqi Li
Linghui Wu
Gang Li
Zhijun Liang
Xuewei Jia
Joao

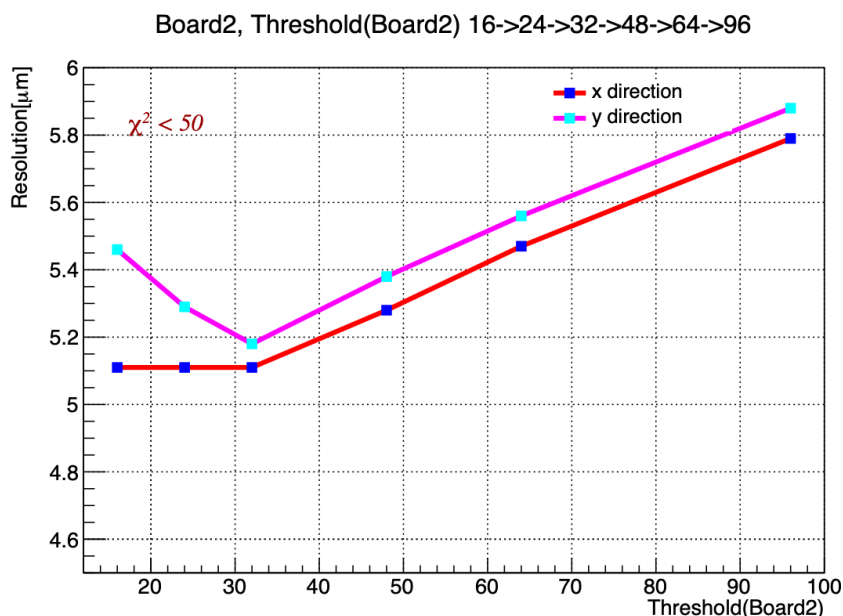




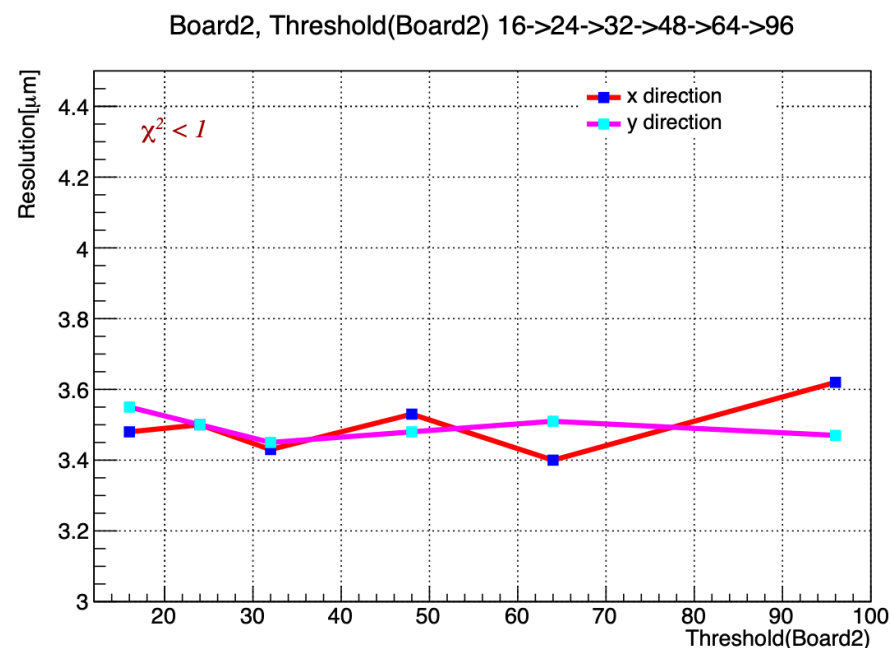
Resolution vs. chip threshold (4GeV) : modified process

- Modified process chip has effectively low threshold
- Resolution is similar to the resolution with standard process

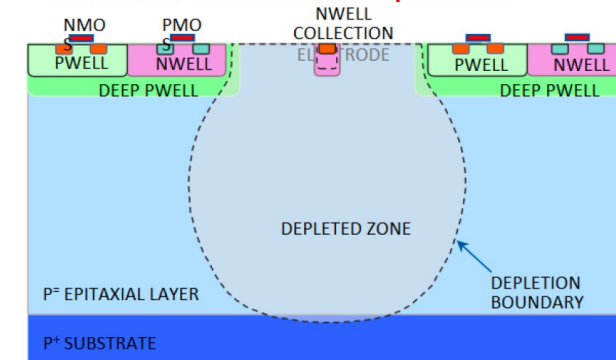
All tracks



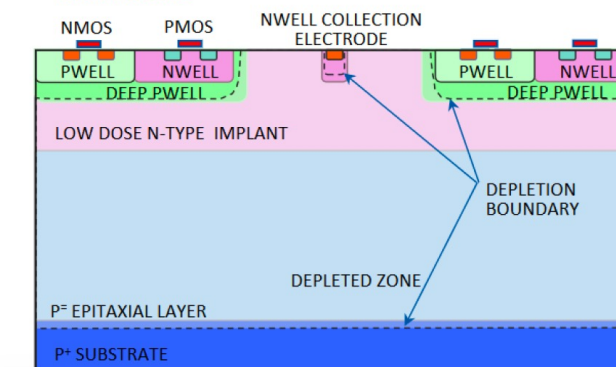
Tracks with small Chi2
Suppressing multiple scattering



Standard : no full depletion



Modified : full depletion, faster charge collection



Shuqi Li
Linghui Wu
Gang Li
Zhijun Liang
Xuewei Jia
Joao



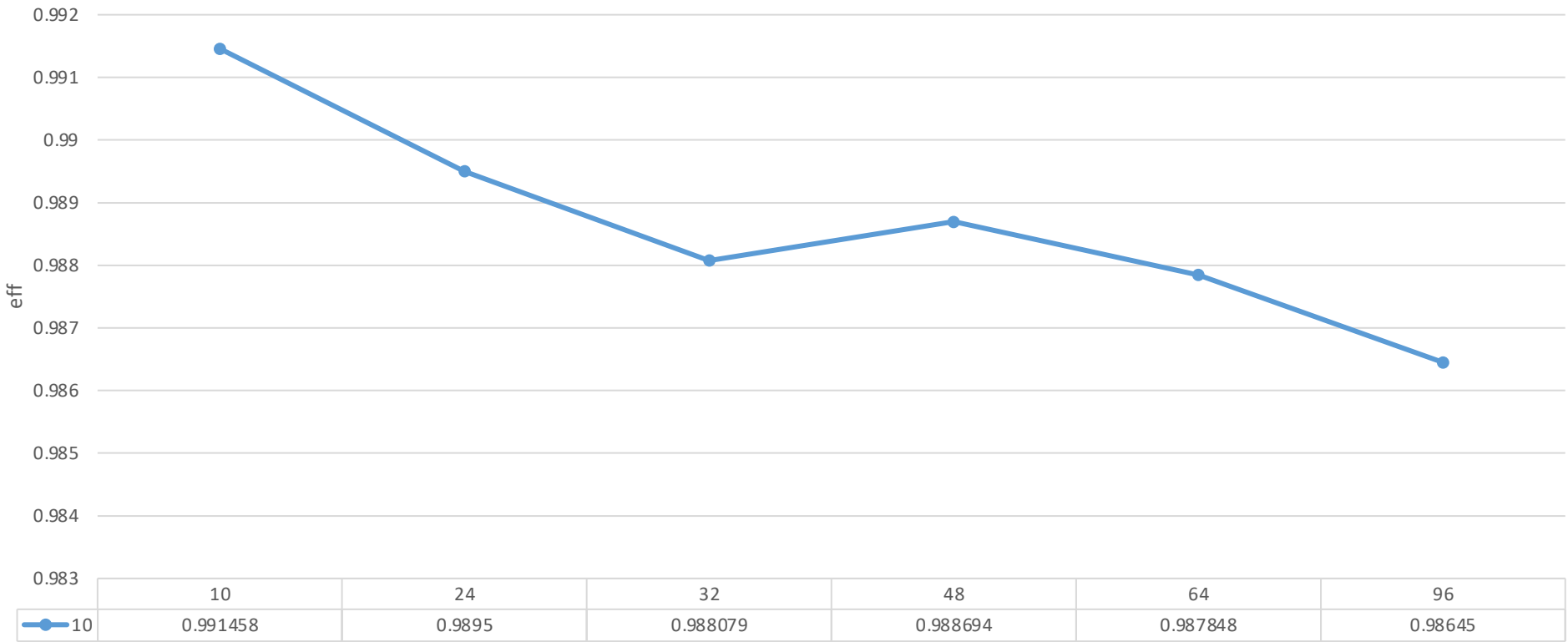


efficiency vs. chip threshold (4GeV) : standard process

- Hit Efficiency increased slightly as reducing the threshold
- Overall efficiency is about ~99% in study



Efficiency



LiYiMing Hu(NJU)
Shuqi Li



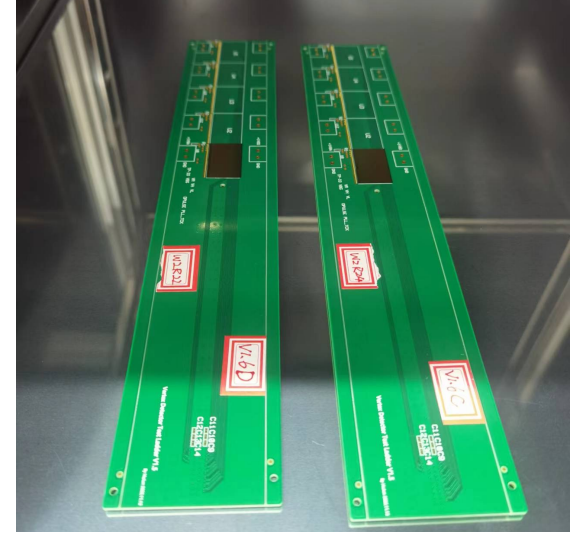
Threshold

Progress for flex board

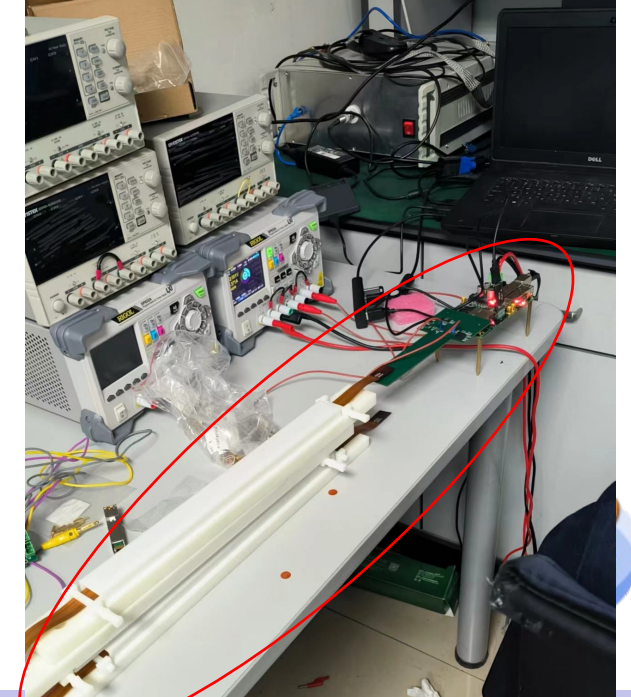
- Testbench setup: 2~3 chips wire bonded on one flex
 - Can communicate with TaichuPix in OCT mode (self-checking mode)
 - **Issue:** Readout lots noise in charge injection mode
 - **Challenge:**
 - Long flex cable (~70cm) → some issue with power distribution and delay
 - Missing test point to debug the communication issue
 - **News :**
 - Made a hard PCB with test point, try to understand the issue,
 - The hard PCB is working correctly and a 4 layer flex board is under testing.

Jun Hu
Ying Zhang
Wei Wei
Ziyue Yan
Wei Wang

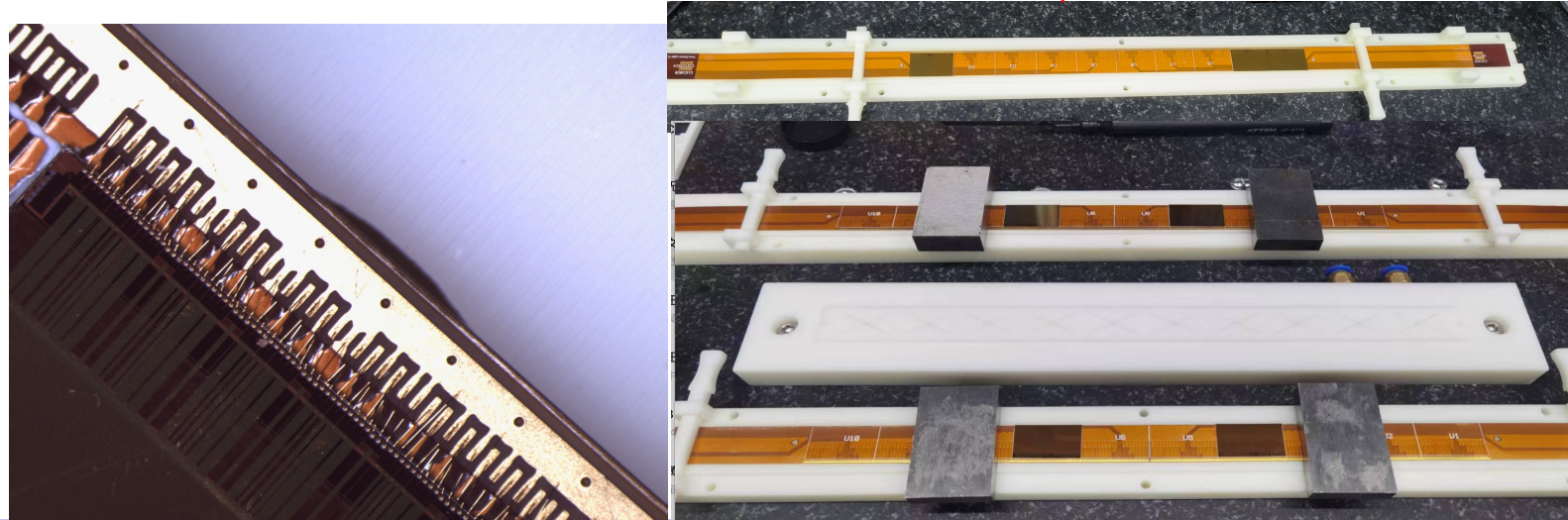
Hard PCB with test points



Electronics test bench



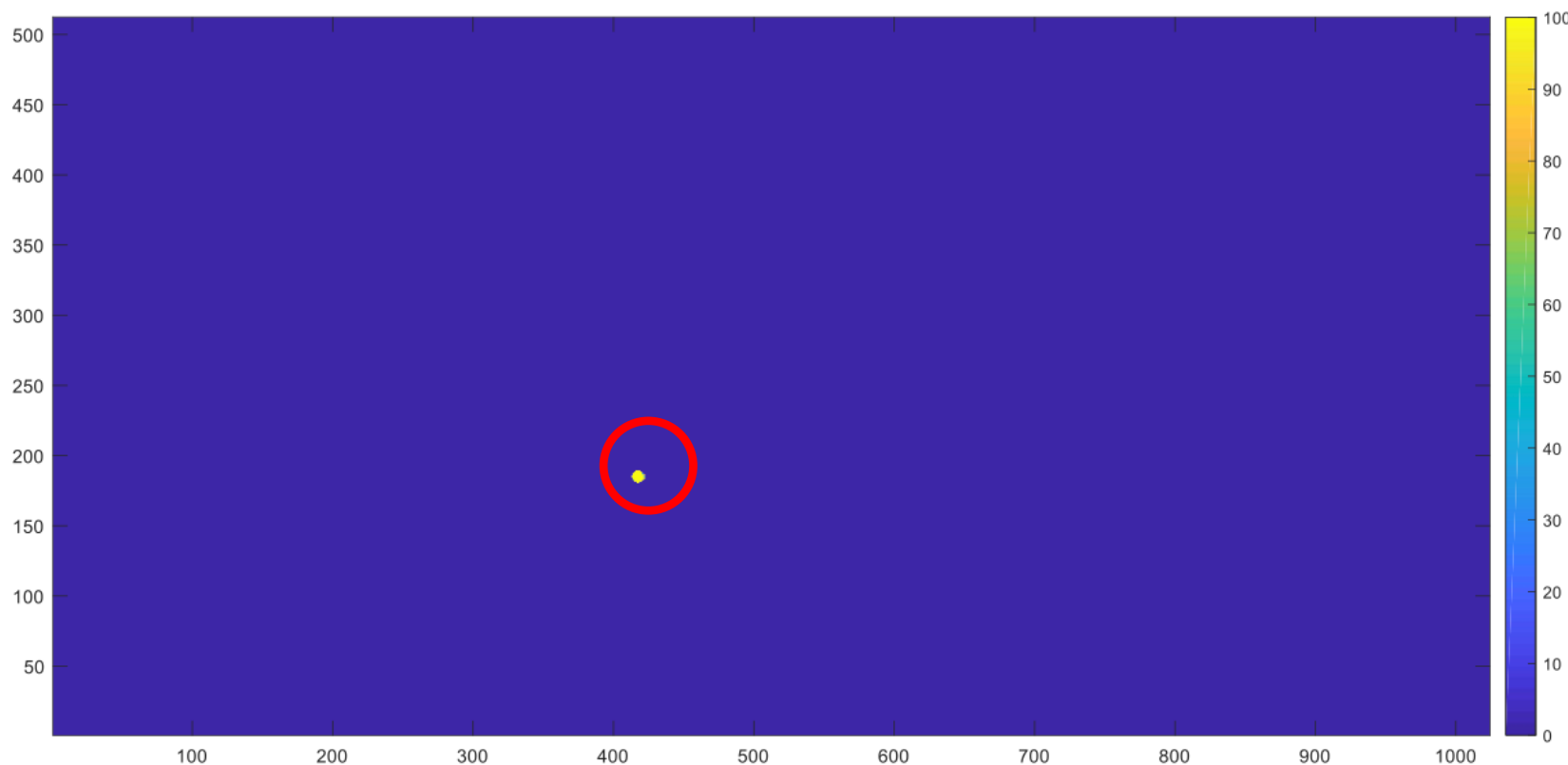
2~3 TaichuPix3 chips wire bonded on one flex





Progress for flex board

- Ladder readout is working now in laser test, after fixing a floating pad in digital injection.
- Noise level is a bit higher in 2-layer flex than in 4-layer flex



Ying Zhang
Wei Wang

Exposure 1s with a 100 Hz laser source @ITHR=96

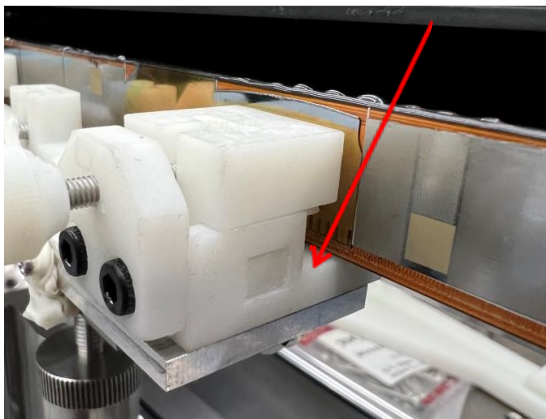




Ladder loading

- Loading procedure of ladder on vertex detector has been tested
- Ladder with one TaichuPix3 chip with wirebonds and 9 dummy silicon chip
- Wire-bonding was protected during loading

Wire-bonding



Ladder support tools

Jinyu Fu
Xinhui Huang
Wei Wang



Ladder loaded on vertex detector





Summary

- DESY testbeam achieved the expected goal
 - TaichuPix3 telescope basically works well
 - The preliminary offline results shows a spatial resolution less than 5 μm , more analysis is going on.
 - the vertex detector prototype is supposed to DESY again for testbeam in April 2023.
- MOST2 project final review
 - Project execution time up to end of April
 - Final reports need to be ready to submit before July 21st

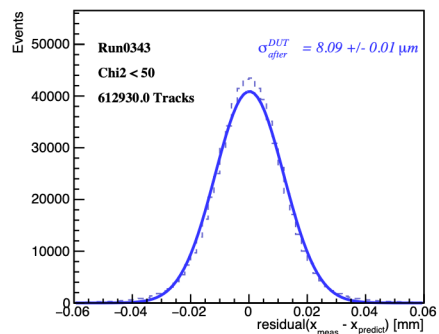
	Week	TB21		TB22		TB24/1		TB24		Announced	
			bottom		bottom	PC-MAG	Detector & ECAL		bottom		
2-Jan-23	1	Shutdown									
9-Jan-23	2										
16-Jan-23	3										
23-Jan-23	4										
30-Jan-23	5										
6-Feb-23	6	Reserve/Energy Conservation									
13-Feb-23	7										
20-Feb-23	8										
27-Feb-23	9	STARTUP									
6-Mar-23	10			CMS-HGCAL	X			SHIP-ECAL	X		
13-Mar-23	11	DSIPM	X	ATLAS-ITk-Strips	X			Telescope-Dev	X		
20-Mar-23	12	DSIPM	X	ATLAS-ITk-Strips	X			PSI-MAPS	X		
27-Mar-23	13	MONOPIX2	X								
3-Apr-23	14										
10-Apr-23	15										
17-Apr-23	16										
24-Apr-23	17	CMS-InnerTracker	X	TelePix	X						
1-May-23	18	CMS-InnerTracker	X	TelePix	X						
8-May-23	19	Belle-II CMOS	X	Tangerine	X			LHCb-ECAL	X		
15-May-23	20	CMS-HGCAL	X	Tangerine	X			LHCb-ECAL	X		
22-May-23	21										
29-May-23	22										
5-Jun-23	23										
12-Jun-23	24	CMS-InnerTracker	X	ATLAS-ITk-Strips	X			LHCb-MightyPix	X		
19-Jun-23	25	CMS-InnerTracker	X	ATLAS-ITk-Strips	X						
26-Jun-23	26	MONOPIX2	X	Telescope-Dev	X						
3-Jul-23	27	CMS-OuterTracker	X					MIMOSIS			
10-Jul-23	28	CMS-OuterTracker	X	RD50-CMOS	X						
17-Jul-23	29	Summer Shutdown									
24-Jul-23	30										
31-Jul-23	31										

关于开展国家重点研发计划“大科学装置前沿研究”重点专项“高能环形正负电子对撞机关键技术研发和验证”项目综合绩效评价工作的通知

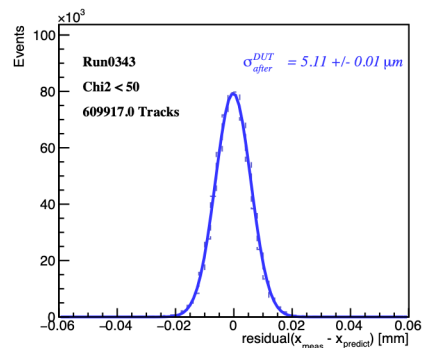


Thanks for your attention!

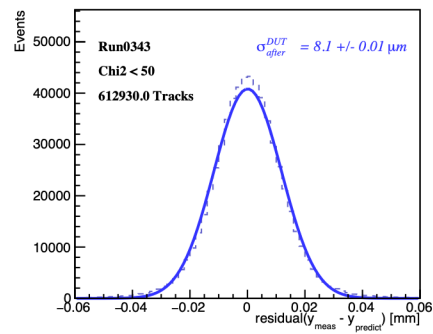
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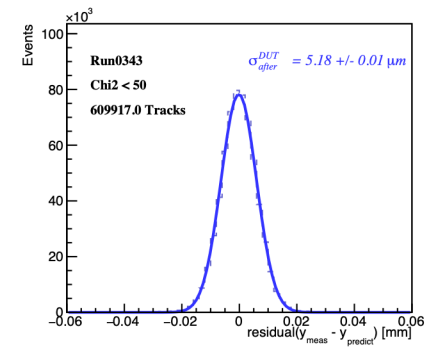
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ydirection, ChipID = 0

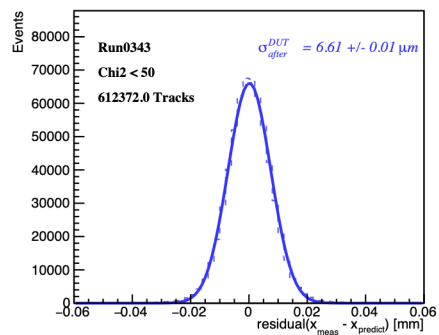


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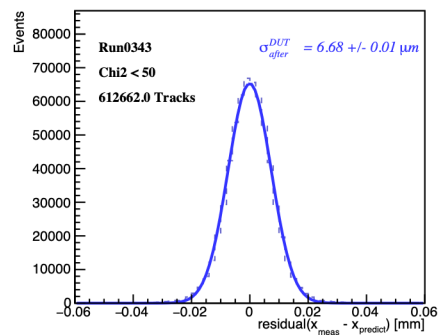


Update: Run343 DUT resolution after alignment
Chi2 < 50

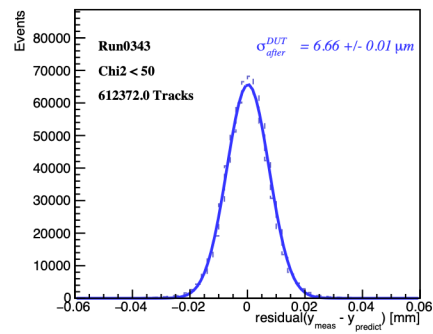
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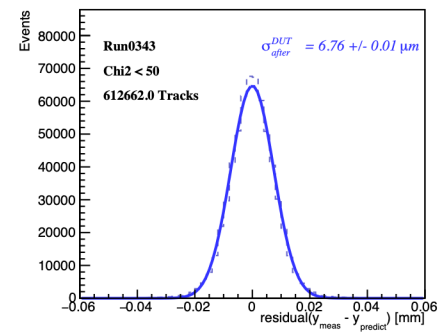
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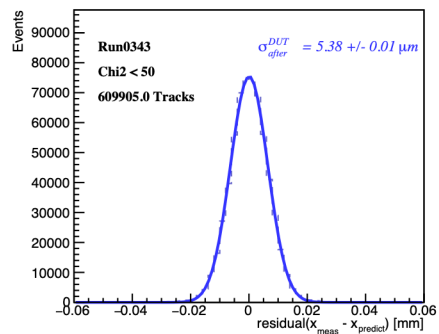
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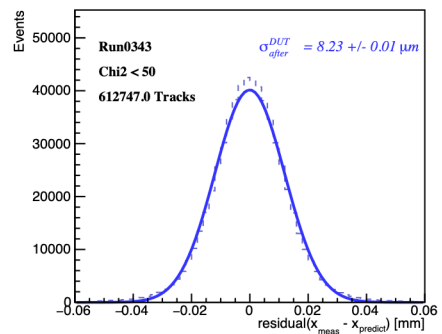
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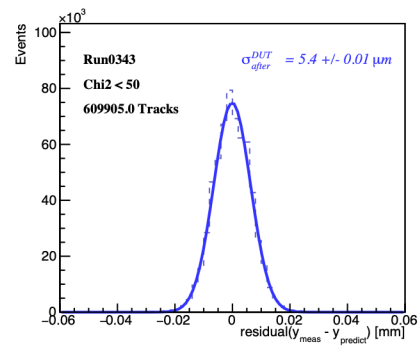
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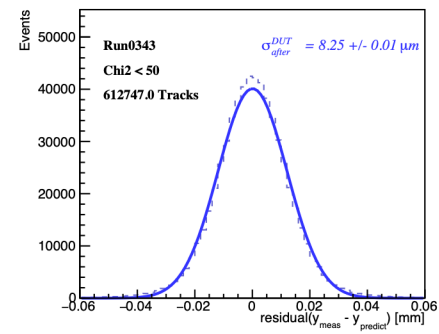
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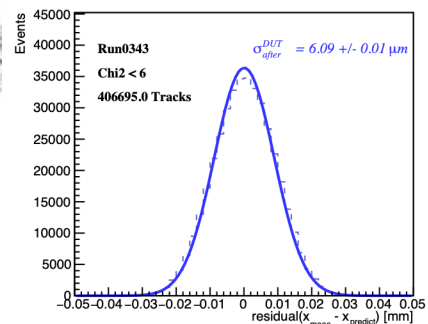
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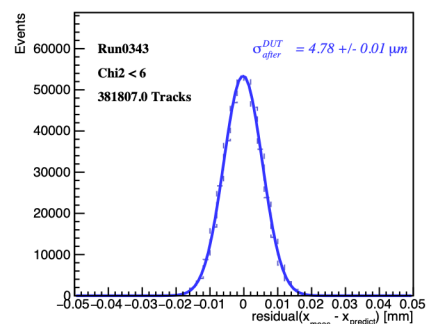
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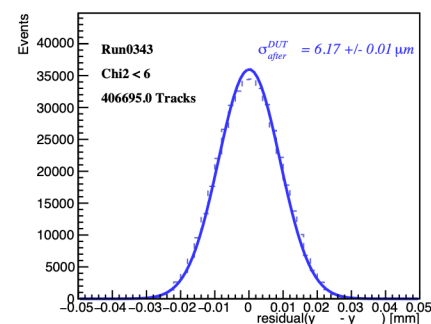
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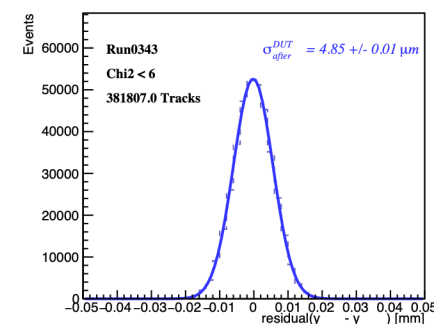
xdirection, ChipID = 1



ydirection, ChipID = 0

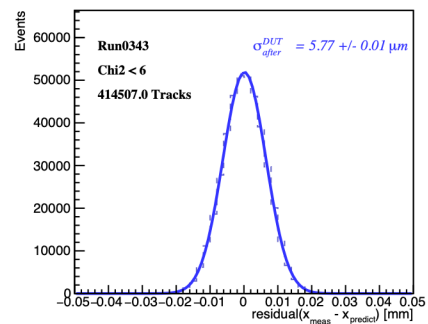


ydirection, ChipID = 1

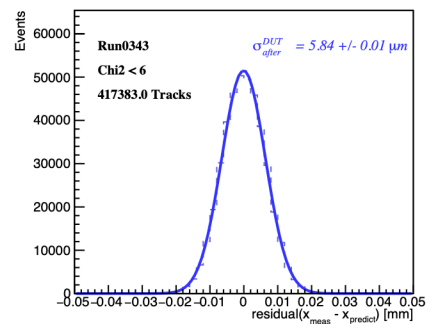


Update: Run343 DUT resolution after alignment
Chi2 < 6

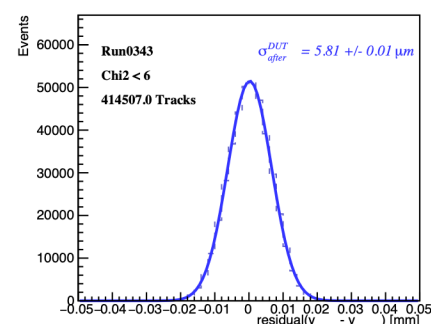
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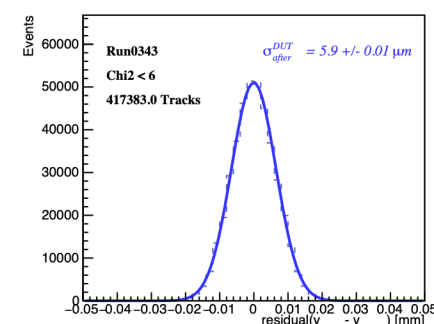
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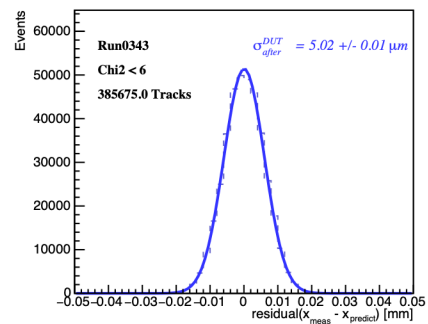
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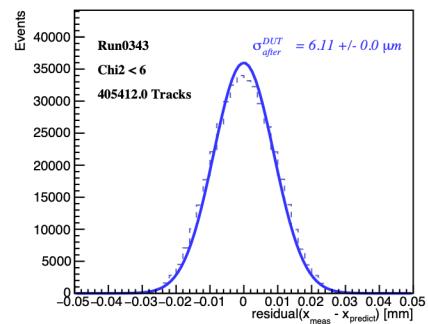
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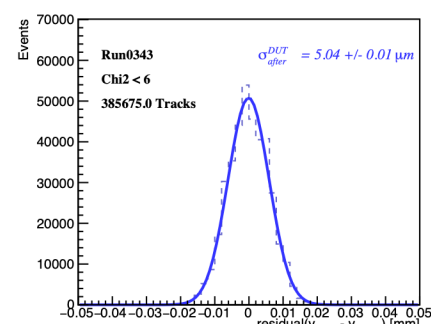
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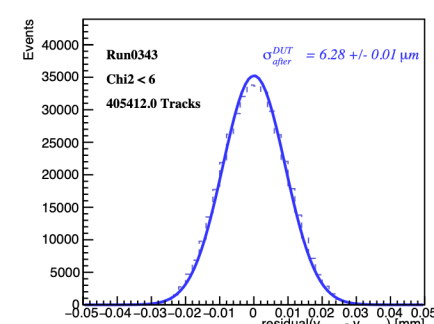
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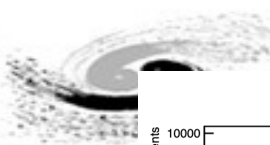


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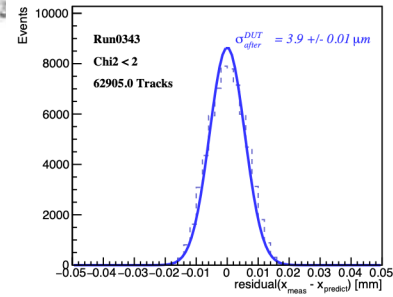


ydirection, ChipID = 5

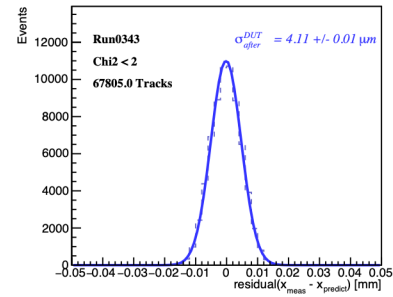




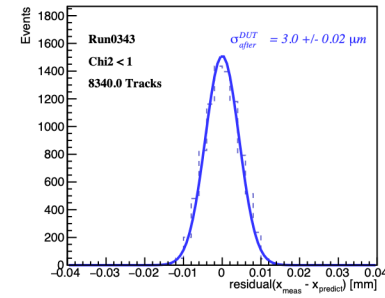
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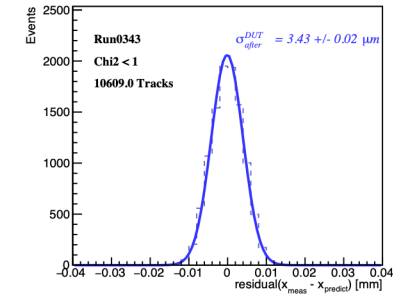
xdirection, ChipID = 1



xdirection, ChipID = 0

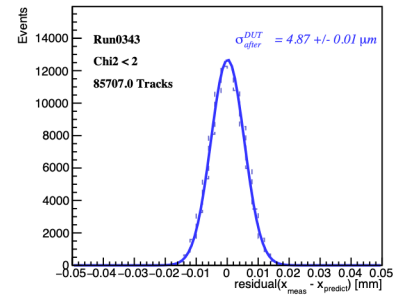


xdirection, ChipID = 1

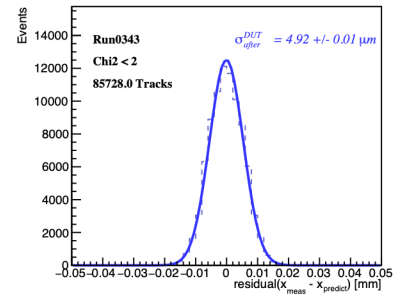


Update: Run343 DUT resolution after alignment
Chi2 < 2

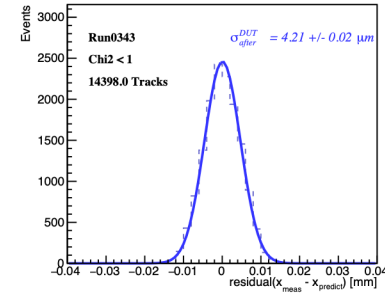
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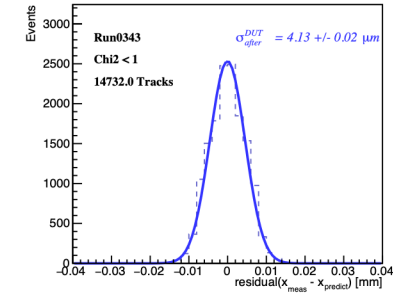
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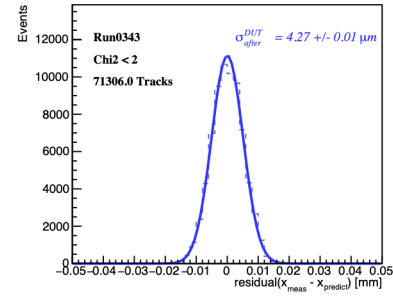
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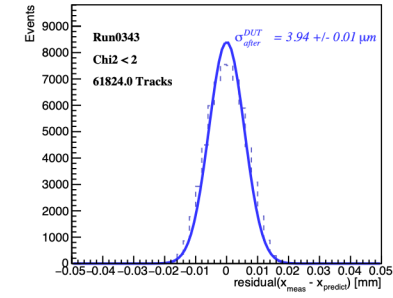
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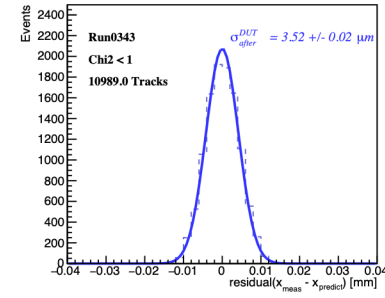
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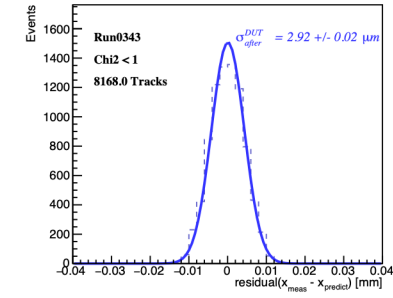
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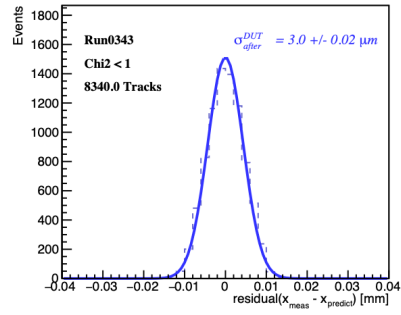
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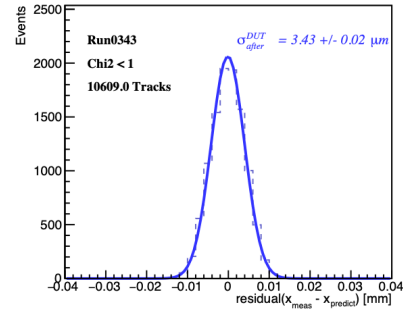
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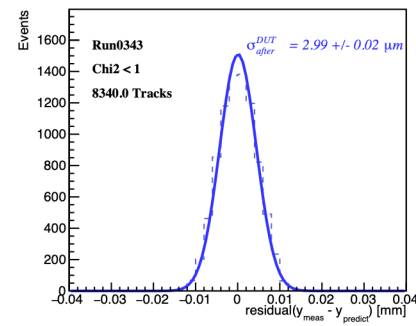
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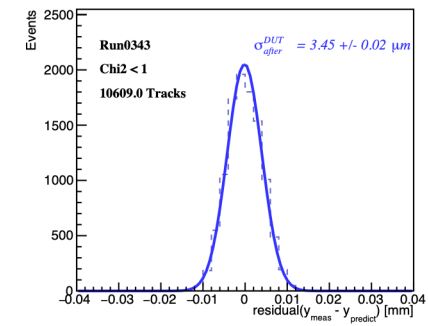
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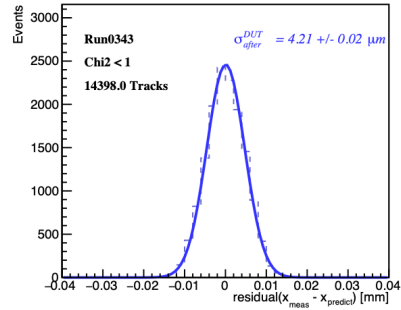
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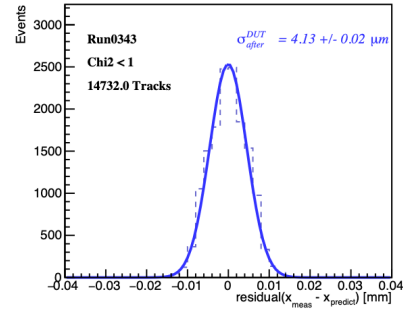
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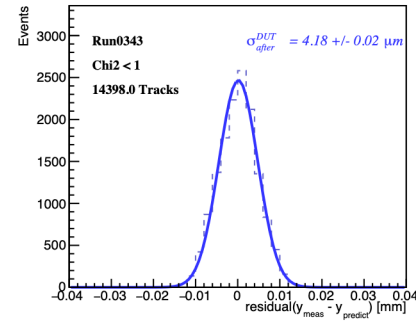
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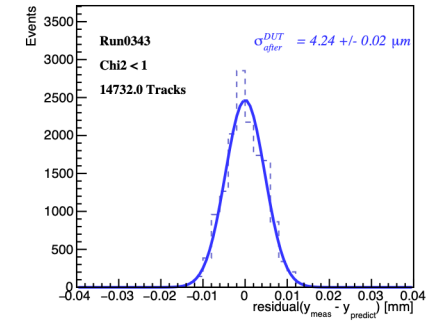
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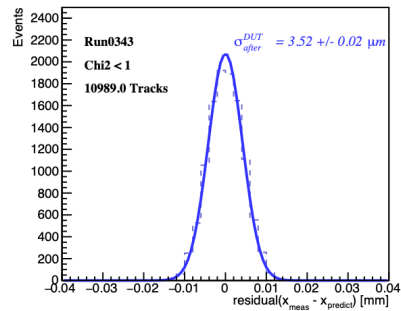
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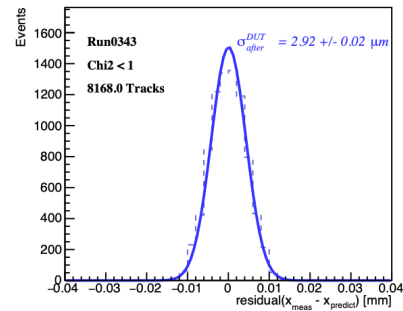
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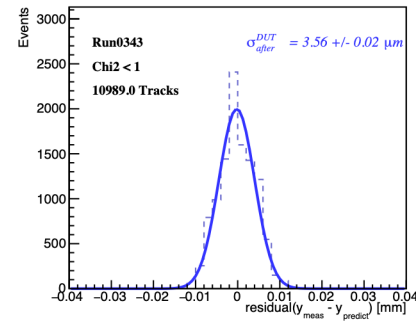
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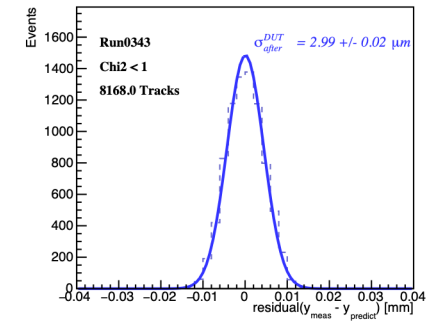
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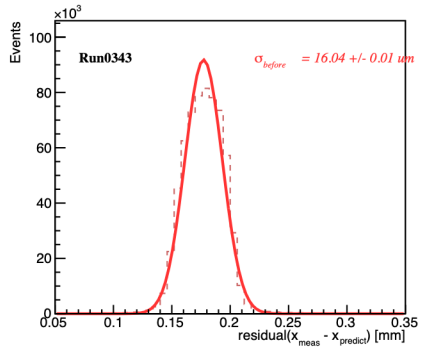
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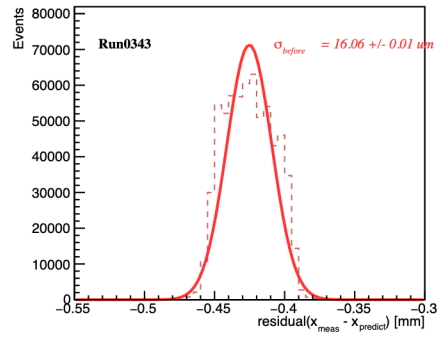
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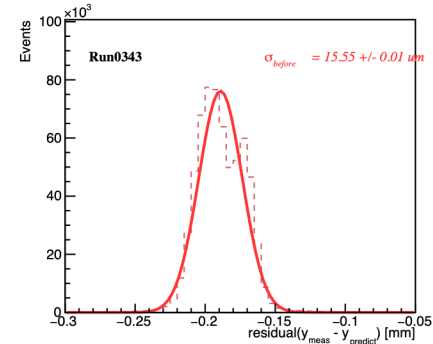
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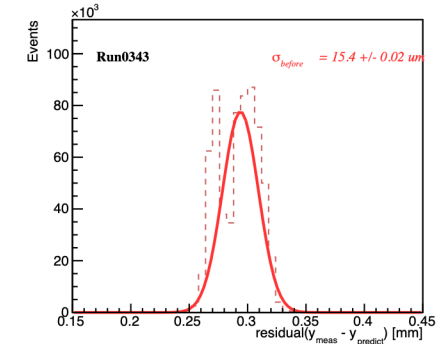
xdirection, ChipID = 1



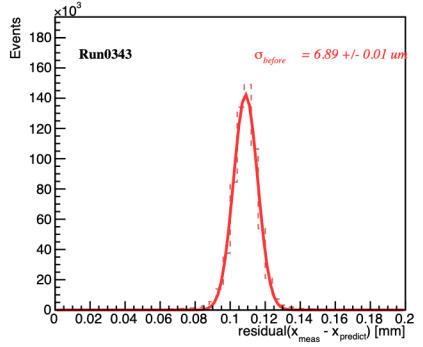
Run343 before alignment
ydirection, ChipID = 0



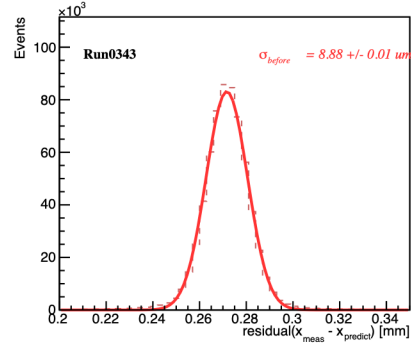
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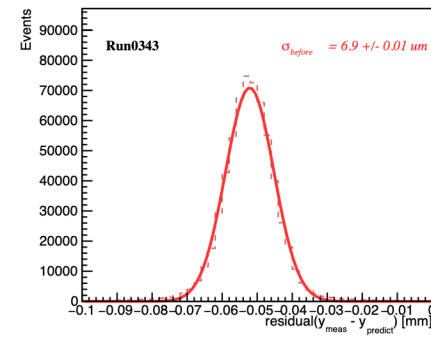
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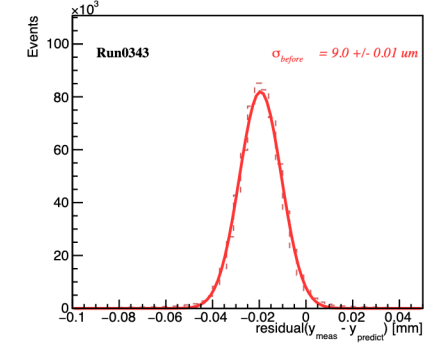
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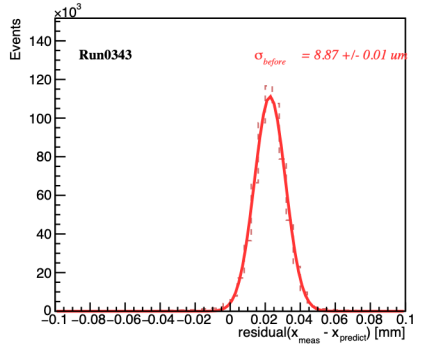
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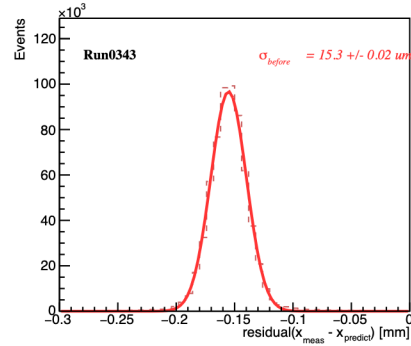
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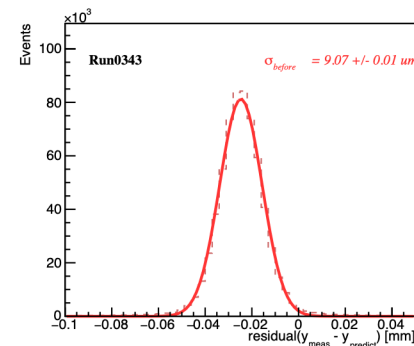
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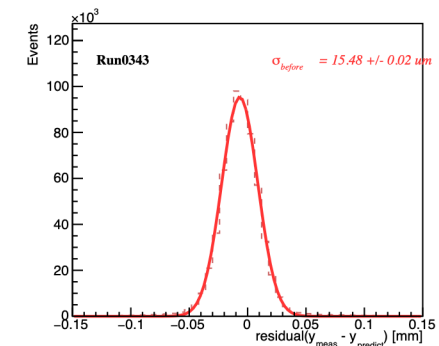
xdirection, ChipID = 5



ydirection, ChipID = 4



ydirection, ChipID = 5





Overview of testbeam

Dec.12-Dec. 17:(SETUP 1)

- 1-6: W2R3, W2R11, W2R12, W2R10, W2R29, W2R26

Dec. 17:(SETUP 2)

- 1-6: W2R3, W9R3, W9R4, W9R6, W2R29, W2R12

Dec. 18-Dec.19(SETUP 3)

- 1-6: W2R3, W9R5, **W9R4**, W9R6, W2R29, W2R12

Dec. 20- Dec.22(SETUP 4)

- 1-6: W2R3, W9R5, **W2R11**, W9R6, W2R29, W2R12

Note : **W2** : No.2 Wafer by standard CMOS process ;

R3 : chip position on wafer is 3 ;

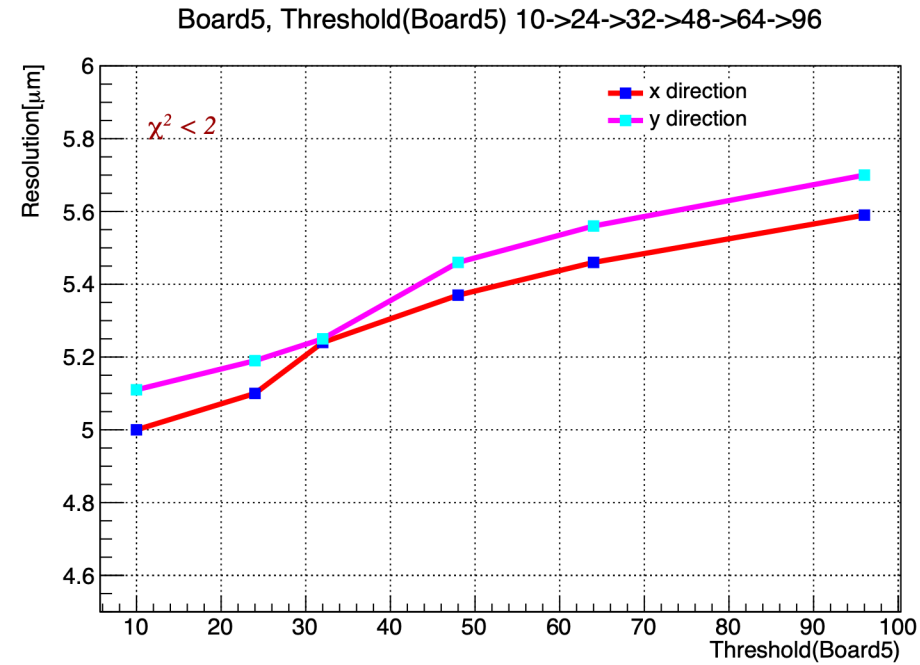
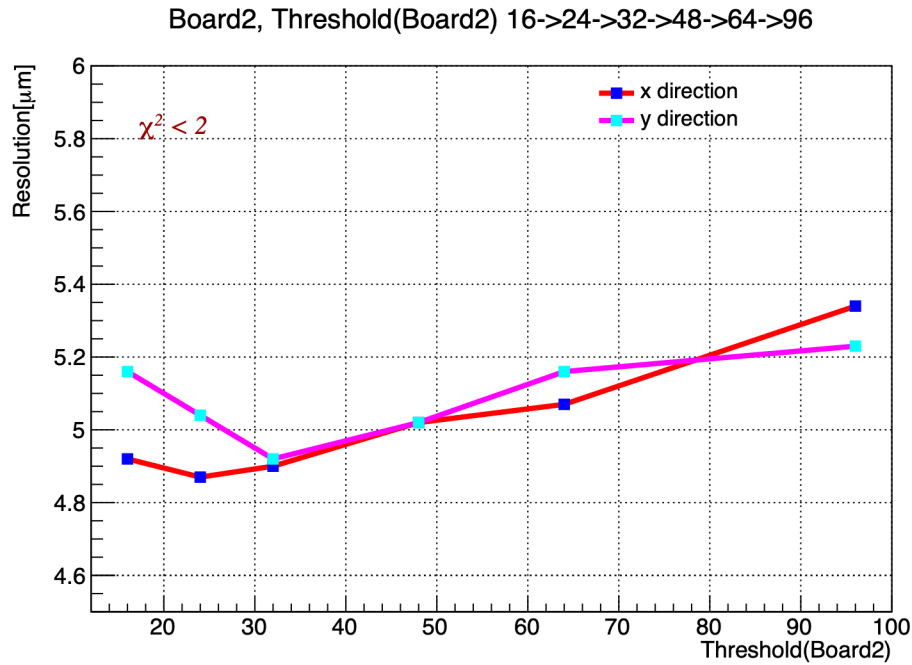
W9 : No.9 Wafer by modified CMOS process ;

The beam energy was tested from 3GeV 4GeV 5GeV 5.4GeV 6GeV

- W9R3 had a higher noisy pixels and replaced with W9R5
- W9R4 was easy to lose analog current and replaced with W2R11



Spatial resolution vs. chip threshold (4GeV)

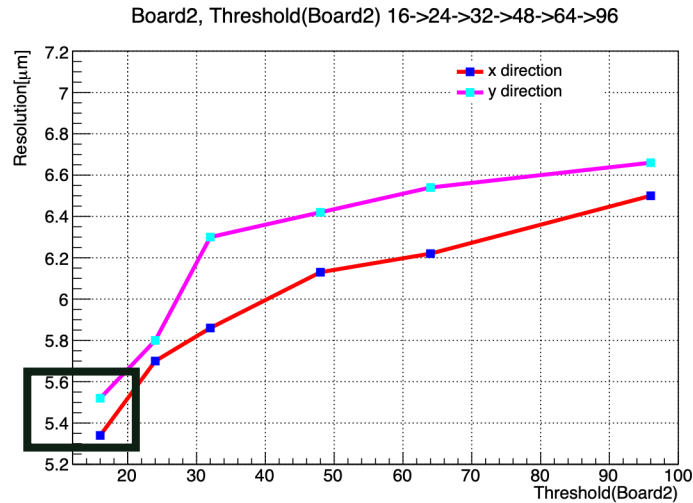


- Board2 with modified technology has a larger depletion layer than Board5 with standard technology
- In general, the higher the threshold, the worse the resolution

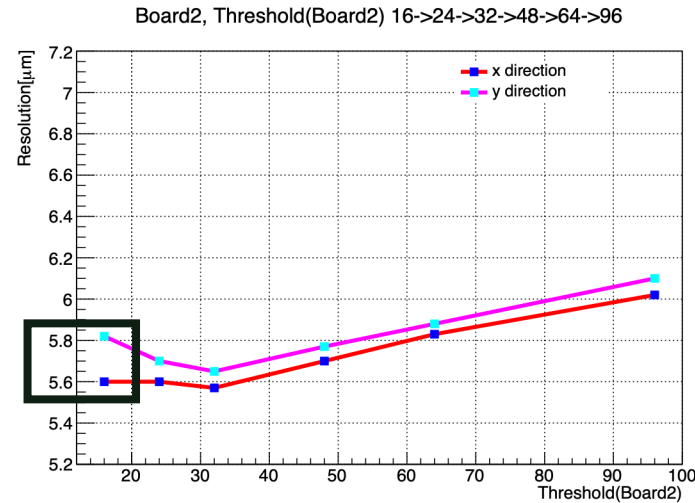
Spatial resolution vs. chip threshold (4GeV) [Comparison of ClusterSize = 1 and ClusterSize >= 1]

1]

Board2(modified) ClusterSize == 1

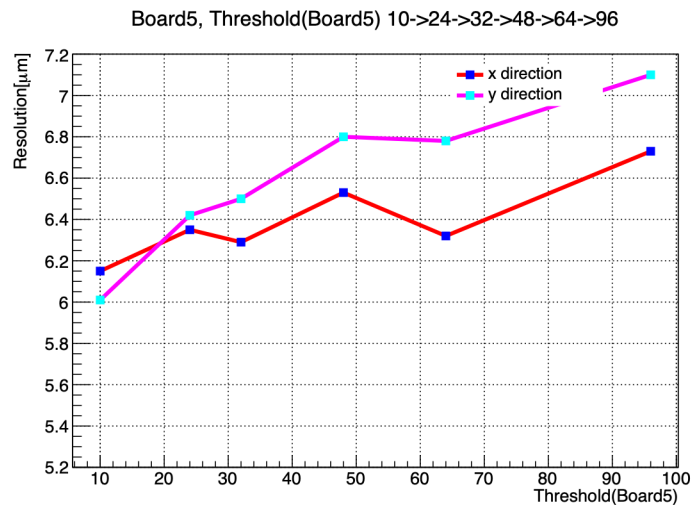


ClusterSize >= 1

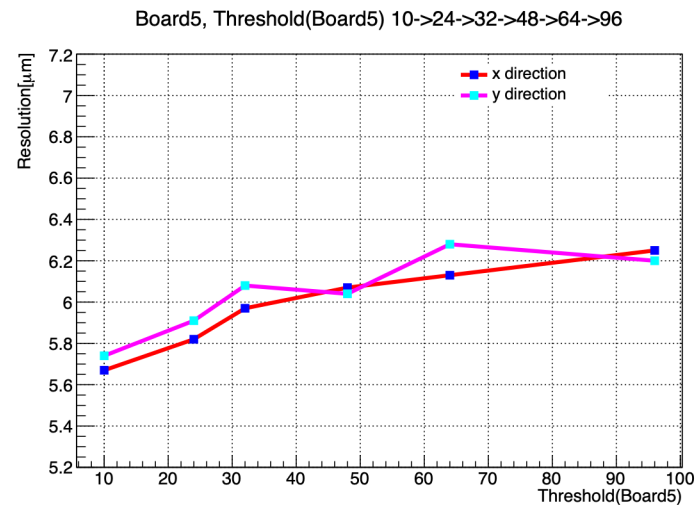


- Board2 with modified technology has a larger depletion layer than Board5 with standard technology
- ClusterSize = 1, only one hit in every cluster of every track (small statistics)
- ClusterSize >= 1, no cut on cluster size
- $\chi^2 < 8$
- Only when the modified chip2 threshold is equal to 16 (minimum threshold), the resolution of single hit is better than the resolution of multi-hit

Board5(standard) ClusterSize == 1



ClusterSize >= 1





Threshold scan

- With SETUP 4. (W2R3, W9R5, W2R11, W9R6, W2R29, W2R12)
 - Scan ITHR of board 5 (W2R29) with 10 16 24 32 48 64 96; 4GeV ;30min for each run; keep the rest of boards unchanged
 - Scan ITHR of board 2 (W9R5) with 16 24 32 48 64 96; 4GeV ;30min for each run; keep the rest of boards unchanged
- W9R5: the spatial resolution is 4.9 at ITHR16 when $\chi^2 < 2$
- W2R29: the resolution goes to 5.09 at ITHR10 when $\chi^2 < 2$

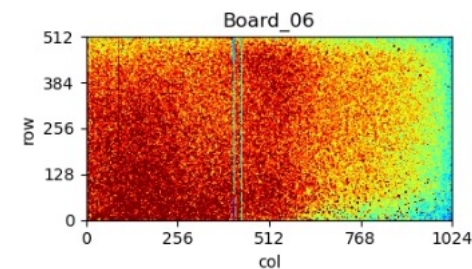
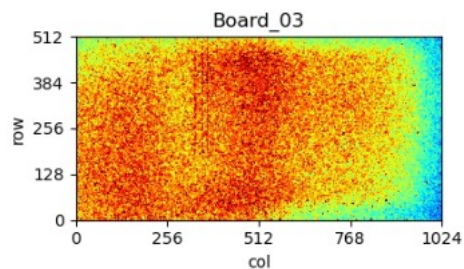
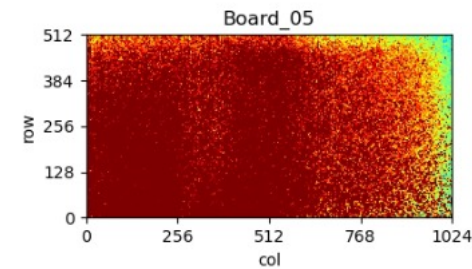
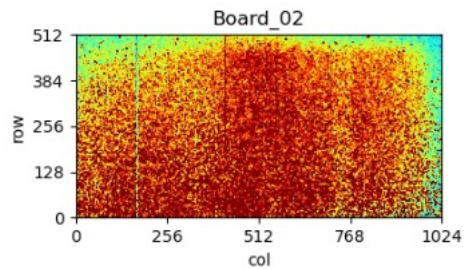
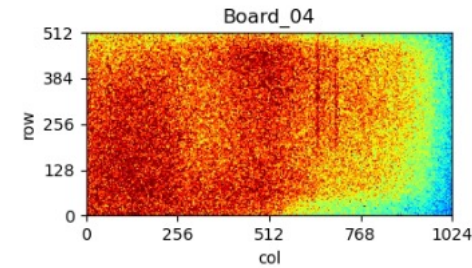
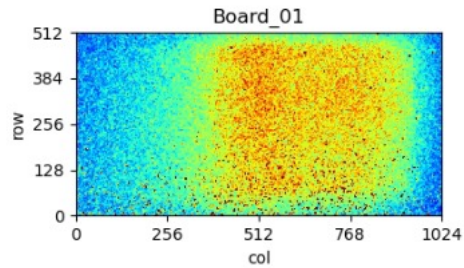
Chip	VBG[V]	ITHR16 Threshold[V]	ITHR32 Threshold[V]	ITHR64 Threshold[V]	ITHR96 Threshold[V]	ITHR16 mask pixels	ITHR32 mask pixels
W2R29	0.740	0.2654	0.3345	0.4468	0.5452	82	1
W9R5	0.737	0.1596	0.1983	0.2683	0.3113	26	4



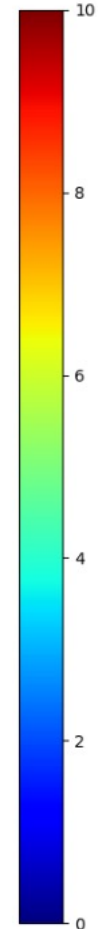


Hitmap of 5.4 GeV beam

Hitmap



The hitmap are the same as 5GeV, the backside boards records more hits.(Boards 2 & 5 are set with lower threshold than the rest)



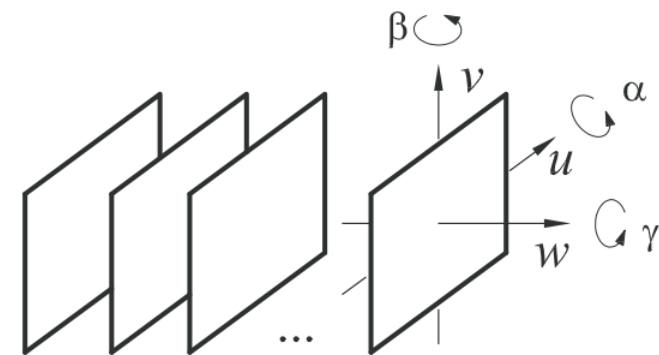
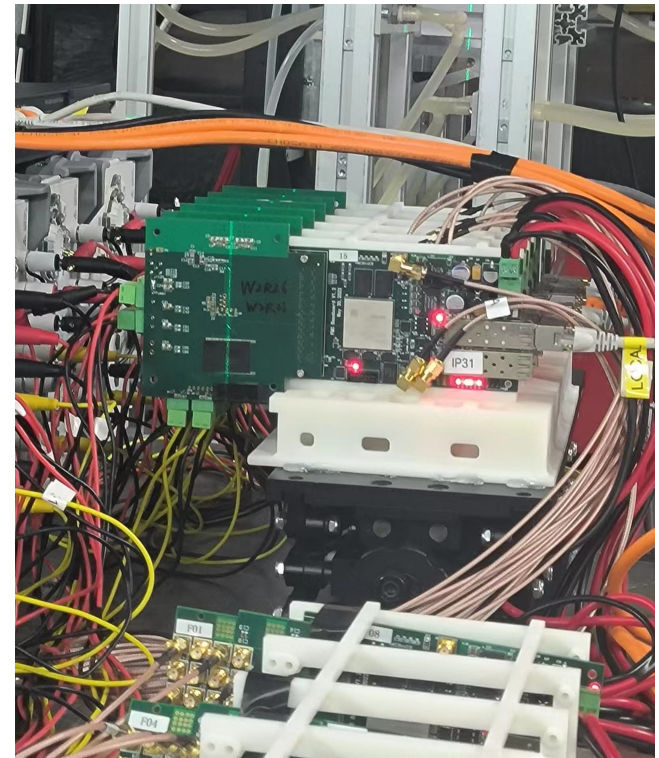
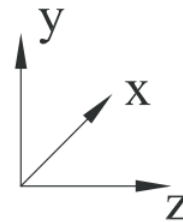
Track reconstruction

- ▶ Setup
 - 6 layer chips
 - 4cm between each other
 - electron beam energy 3-6 GeV
 - One of the chips is the detector under test (dut), the others are the telescope
- ▶ Steps for track finding and reconstruction
 - Finding hits in every chip with same time stamp of FPGA (+/- 1)
 - Forming adjacent hits into a cluster
 - No considering multiple clusters on one chip for one track currently
- ▶ Track fitting
 - least squares line fitting

$$x = a_1 z + b_1;$$

$$y = a_2 z + b_2;$$

Chi2 definition: $\chi^2(\alpha) = \sum_{i=1}^n \frac{f(x_i, \alpha) - e_i}{\sigma_i^2}$, sigmax = sigmay = 25um/sqrt(12)



The first step in the characterization of the telescope as a tracking device was the measurement of the intrinsic resolution of the reference planes and the ultimate spatial resolution achievable combining all the hits into a track. The single plane resolution (σ_{DUT}) can be obtained from the measured residual width (σ_{meas}) and the telescope resolution (σ_{tel}) using Eq. (1)

$$\sigma_{\text{meas}}^2 = \sigma_{\text{DUT}}^2 + \sigma_{\text{tel}}^2 \quad (1)$$

The telescope resolution can be determined assuming that the reference planes all have the same intrinsic resolution using Eq. (2)

$$\sigma_{\text{tel}}^2 = k \sigma_{\text{plane}}^2 \quad (2a)$$

and

$$k = \frac{\sum_i^N z_i^2}{N \sum_i^N z_i^2 - (\sum_i^N z_i)^2} \quad (2b)$$

The formula for the geometrical scaling factor k defined in (2b) is based on the assumption that the DUT is positioned at $z=0$ and it reduces to $1/N$ if the reference planes are symmetrically distributed around the DUT and the beam and telescope axes are parallel.

$$\sigma_0^{\text{DUT}} = \sigma_5^{\text{DUT}} = 0.688 \sigma_{\text{meas}}$$

$$\sigma_0^{\text{Tel}} = \sigma_5^{\text{Tel}} = 0.72547 \sigma_{\text{meas}}$$

$$\sigma_1^{\text{DUT}} = \sigma_4^{\text{DUT}} = 0.8395 \sigma_{\text{meas}}$$

$$\sigma_1^{\text{Tel}} = \sigma_5^{\text{Tel}} = 0.5438 \sigma_{\text{meas}}$$

$$\sigma_2^{\text{DUT}} = \sigma_3^{\text{DUT}} = 0.9050 \sigma_{\text{meas}}$$

$$\sigma_2^{\text{Tel}} = \sigma_3^{\text{Tel}} = 0.425 \sigma_{\text{meas}}$$
